Error Analysis and Inter-Cell Interference Mitigation in Multi-Level Cell Flash Memories

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Outline

- Multi-Level Cell (MLC) flash memory structure
- Error analysis in 1x-nm MLC NAND flash memories due to program/erase cycling and ICI
- ICI mitigation using constrained codes
- Summary

Multi-Level Cell (MLC) flash memory structure

MLC Flash Memory Structure

- **Floating gate transistor (Cell)** – Fundamental data storing unit
- Program a cell to different charge levels to represent the data bits.

Lower Page (blue)
Upper Page (red)

High Voltage

Cell Level	Bits
3	01
2	00
1	10
0	11

Low Voltage

Cell Level to Bit Mapping

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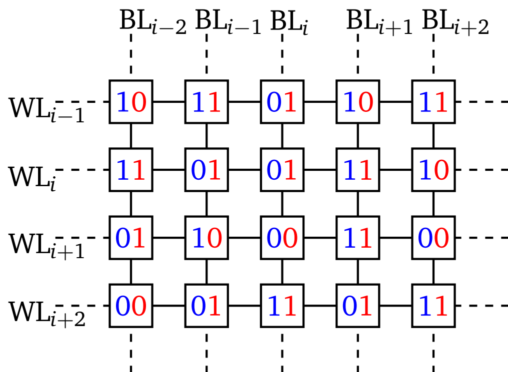
Cell Level to Bit Mapping



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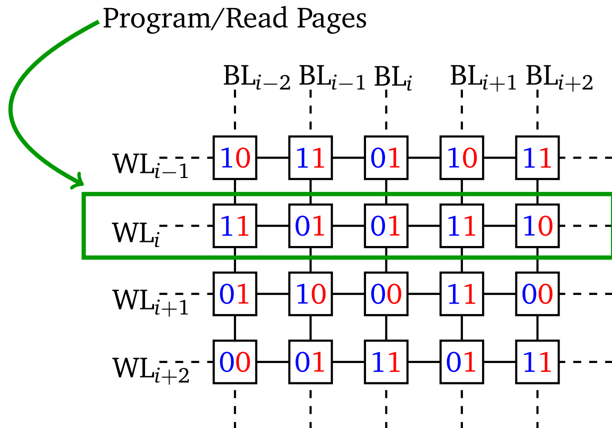

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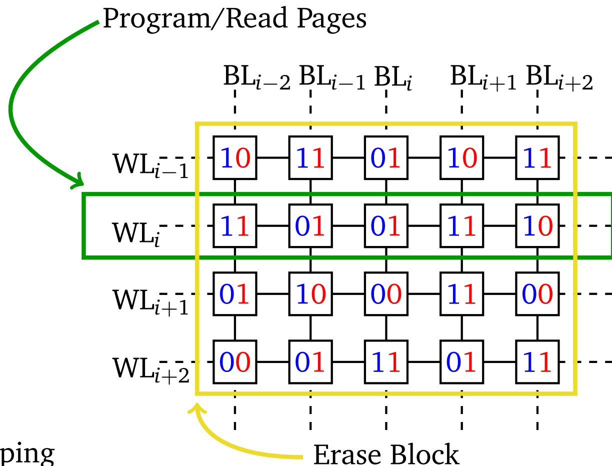


Error analysis in 1x-nm MLC NAND flash memories due to program/erase cycling and ICI

Error Mechanisms in Flash Memories

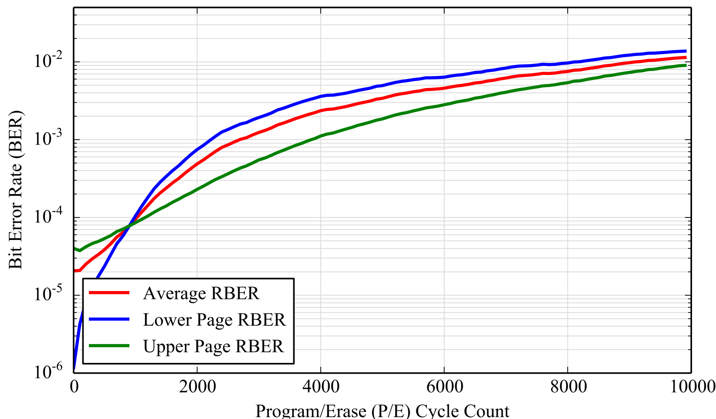
- Program/Erase (P/E) cycling
  - Charge trapped in the dielectric.
  - Cells are worn/damaged, shift in the threshold voltage.
  - Determines endurance/lifetime of a flash memory cell.
- Inter-Cell Interference (ICI)
  - Data dependent errors caused randomly after cells are programmed.
  - Parasitic capacitance coupling among neighbor cells.
  - Dominant in small feature size flash memory technology.

J. Cooke, “The inconvenient truths about NAND flash memory.”
Micron MEMCON 7, 2007.

P/E Cycling Experiment Procedure

- Program/Erase (P/E) Cycling
  - Choose a few (4 - 16) blocks of MLC Flash.
  - Erase $\longrightarrow$ Program $\longrightarrow$ Erase $\longrightarrow$ ... upto 10,000 P/E cycles
  - Read back programmed data at regular intervals (100 cycles) and record error data.
  - Use pseudo-random (PR) data for the P/E cycling.
- No extra wait (dwell) time between erase/program/read operations.

Program all pages with pseudo-random data

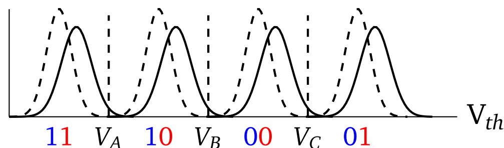


Measured average raw bit error rate over 16 blocks of MLC flash memory for when all pages are programmed with pseudo-random data in every P/E cycle.

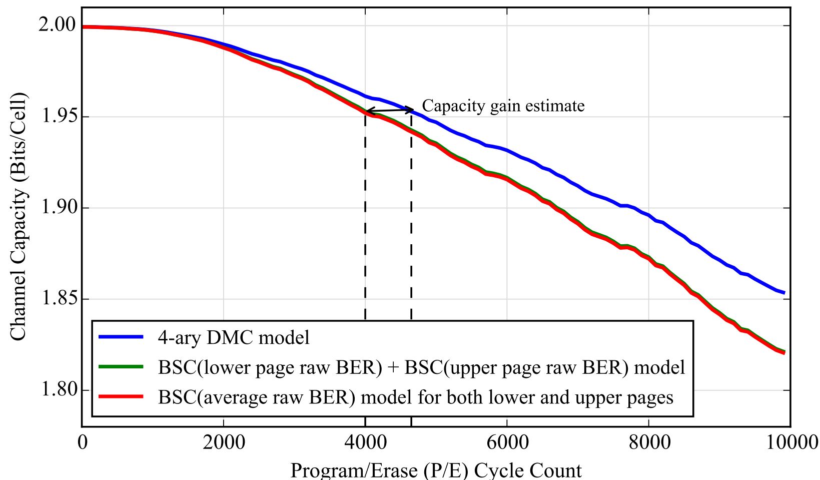
Dominant Cell Errors

Frequency of cell errors measured as a percentage of total number of cell errors.

Write Cell Values	Read Cell Values			
	11 (0)	10 (1)	00 (2)	01 (3)
11 (0)	0.00%	17.37%	0.42%	2.32%
10 (1)	0.02%	0.00%	63.64%	0.61%
00 (2)	0.00%	0.03%	0.00%	15.47%
01 (3)	0.00%	0.01%	0.11%	0.00%

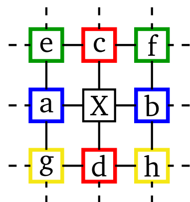


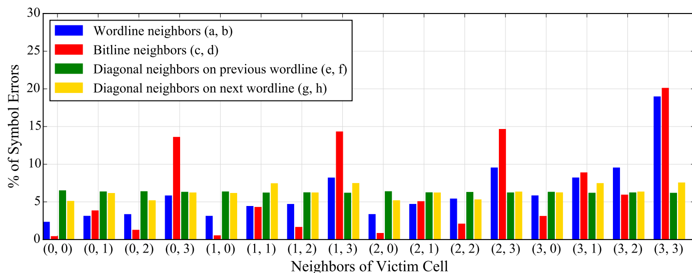
MLC Flash Channel Capacity



Comparison of evolution of the flash memory channel capacity with P/E cycles with 4-ary DMC and BSC channel models.

Correlation of Errors with Cell Neighborhood





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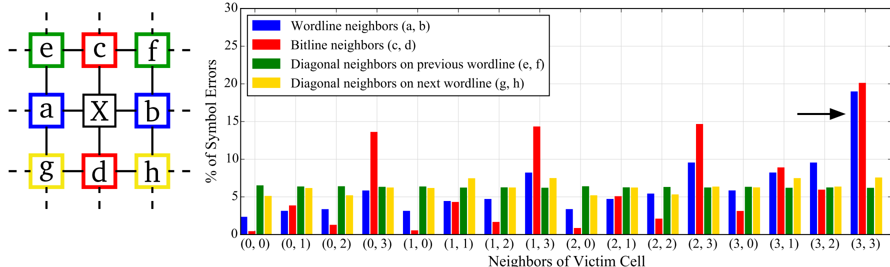

- Worst ICI effect from (3, 3) wordline and bitline neighbor patterns.

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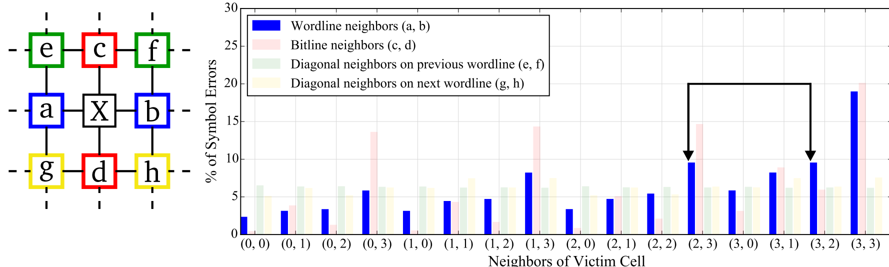

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- Symmetry in the wordline ICI effect.

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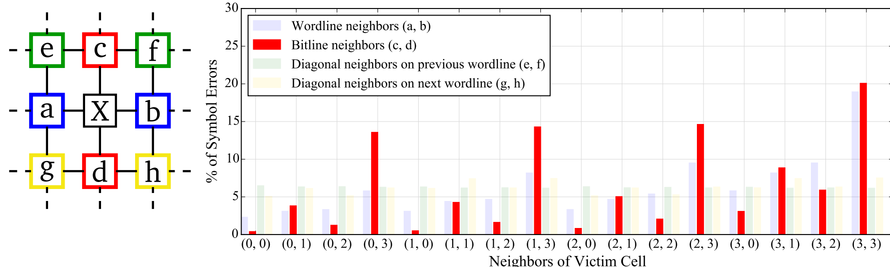

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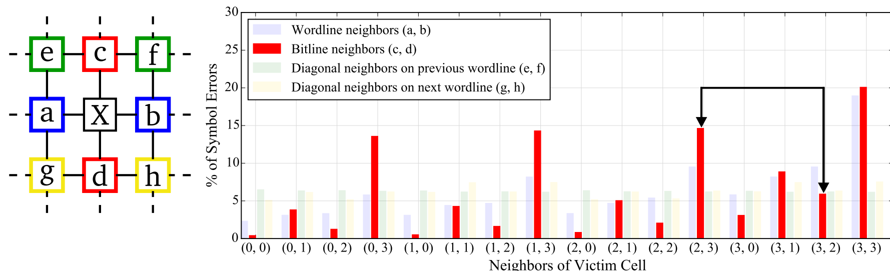

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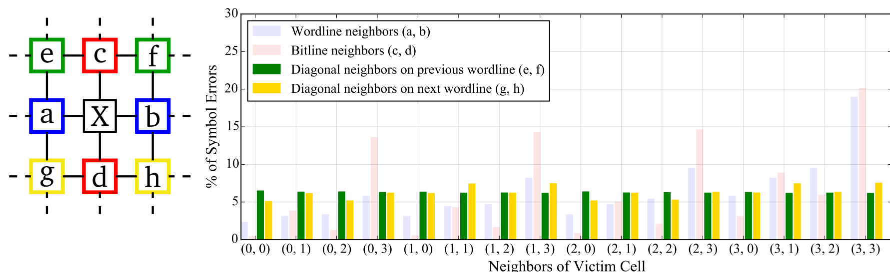

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- No ICI error correlation with diagonal neighbor data patterns.

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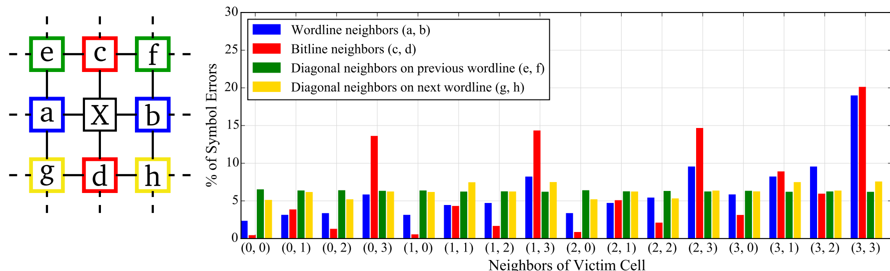


- Worst ICI effect from (3, 3) wordline and bitline neighbor patterns.
- Symmetry in the wordline ICI effect.
- Bitline ICI worse than wordline ICI.
- Asymmetry in the bitline ICI effect.
- No ICI error correlation with diagonal neighbor data patterns.
- 3-0-3, 3-1-3 and 3-2-3 are the most ICI-susceptible patterns.

ICI mitigation using constrained codes

ICI Mitigation using Constrained Codes

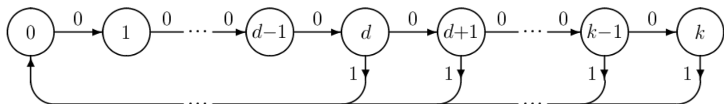
- From ICI error characterization results, 3-0-3, 3-1-3 and 3-2-3 data patterns are most susceptible to ICI.

- Don't write these patterns to the flash memory
  $\Longrightarrow$ Reduced number of cell errors due to ICI

- In **[Y. Kim, et al., 2013]**, the authors observed that
  - 3-0-3 $\rightarrow$ 01-11-01 $\rightarrow$ 1-1-1 (upper page)
  - Forbid 1-1-1 in the upper page to forbid 3-0-3.

Y. Kim, B. Kumar, K. L. Cho, H. Son, J. Kim, J. J. Kong, and J. Lee, "Modulation coding for flash memories," in *Proc. ICNC*, Jan. 2013, pp. 961-967.

(d, k) - Runlength Limited (RLL) Constrained Codes



Graph representation of (d, k)-RLL constraint

- Lengths of consecutive runs of zeros are at least d and at most k.
- Codewords of a (d, k)-RLL code are a subset of binary sequences that satisfy the (d, k)-RLL constraint.
- The Shannon capacity of a (d, k)-RLL constraint can be easily computed and represents the highest possible encoding rate for the (d, k)-RLL code.

Forbidding 3-0-3 pattern using $(1,7)$-RLL code

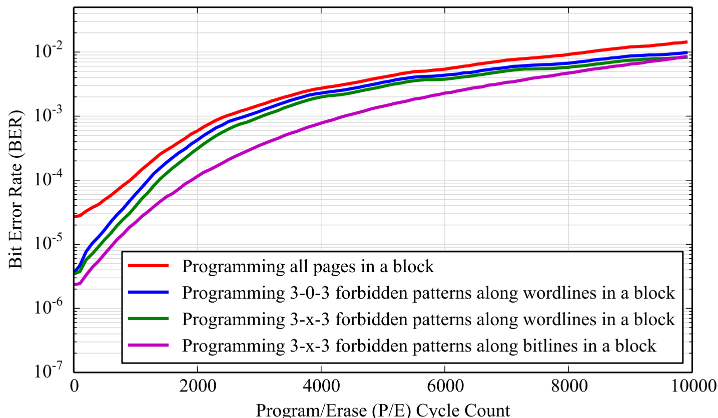
- $d = 1 \implies$ at least one zero between two ones
  $\implies$ 1-1-1 (upper page) pattern is forbidden.
- Capacity of the $(1,7)$-RLL constraint is $\sim$0.6793.
- Efficient rate-2/3 finite state encoder and decoder are available for the $(1,7)$-RLL code.
- Overall rate of the coded system is $(1 + 2/3)/2 \approx 0.83$.
- Maximum Transition Run (MTR) constrained codes with capacity approaching rates can also be used to forbid the 1-1-1 pattern. The capacity of the MTR constraint is $\sim$0.8791.

Y. Kim, B. Kumar, K. L. Cho, H. Son, J. Kim, J. J. Kong, and J. Lee, "Modulation coding for flash memories," in *Proc. ICNC*, Jan. 2013, pp. 961-967.

Forbidding 3-1-3 and 3-2-3 patterns along with 3-0-3

- 3-1-3 $\rightarrow$ 01-10-01 $\rightarrow$ 1-0-1 (upper page)
- 3-2-3 $\rightarrow$ 01-00-01 $\rightarrow$ 1-0-1 (upper page)
- $d = 2$ constraint will work, e.g., $(2, 7)$-RLL constraint.
- Capacity of the $(2, 7)$-RLL constraint is $\sim$0.5174.
- We use a rate-1/2 $(2, 7)$-RLL code with efficient finite state encoder and decoder implementations.
- Overall rate of the coded system is $(1 + 1/2)/2 \approx 0.75$.
- The capacity of the constraint that forbids both 1-1-1 and 1-0-1 is $\sim$0.6942. An interleaved pair of rate-2/3 $(1, 7)$-RLL encoders can be used.

ICI Mitigation using Constrained Codes - Results



Measured average raw bit error rate comparison when all pages are programmed with pseudo-random data and when $(1,7)$-RLL and $(2,7)$-RLL coded data are programmed to forbid '3-x-3' patterns along wordlines or bitlines.

Summary

- Characterized cell level and page level errors using P/E cycling experiments for 1x-nm MLC NAND flash memories.
- Studied the potential gain from cell level ECC based on a 4-ary DMC model using information theoretic analysis.
- Studied the data dependence of ICI errors and identified ICI susceptible data patterns along the wordline and bitline directions.
- Experimentally evaluated the performance of ICI mitigating constrained codes.
- Extension of this work: ‘Row-by-Row’ constrained coding scheme for bitline ICI mitigation [S. Buzaglo et al., ISIT 2015].

Acknowledgment

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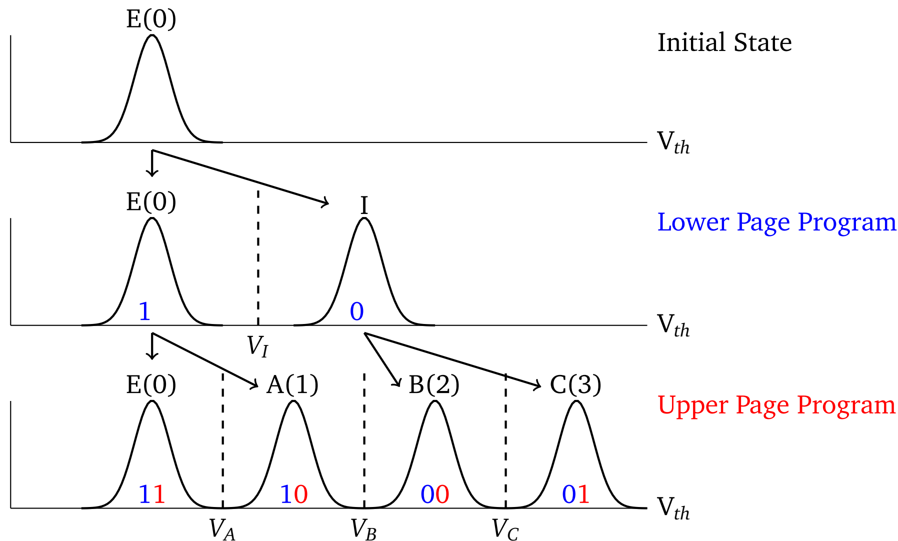
- Ray Descoteaux at CMRR, UCSD.
- Financial support from
  - Toshiba Corporation, Japan
  - NSF grants CCF-1116739, CCF-1405119

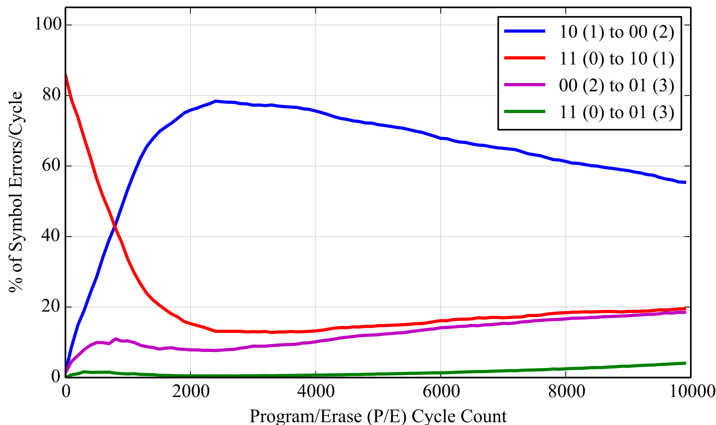
Thank You!

Q & A Slides

Programming MLC Flash Cells

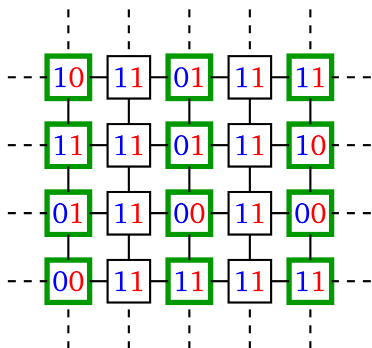


Evolution of Dominant Cell Errors

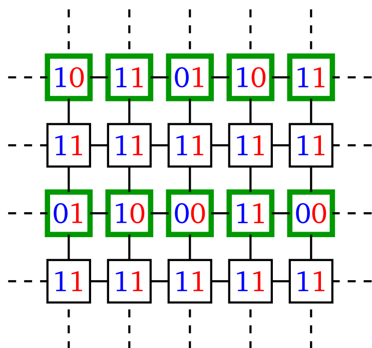


Evolution of dominant cell (symbol) errors across P/E cycles measured as a percentage of cell (symbol) errors occurring in each P/E cycle.

Isolated Wordline and Bitline ICI

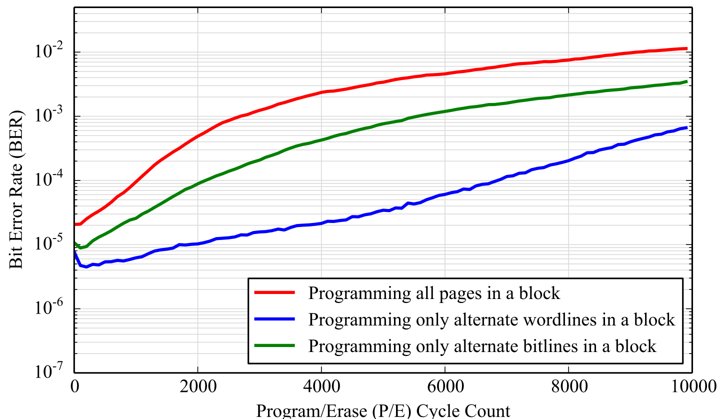


Program alternate bitlines only
$\Longrightarrow$ Isolated bitline (vertical) ICI



Program alternate wordlines only
$\Longrightarrow$ Isolated wordline (horizontal) ICI

Isolated Wordline and Bitline ICI



Measured average raw bit error rate over 16 blocks of flash memory by programming all pages in a block, only alternate wordlines in a block and only alternate bitlines in a block with pseudo-random data in every P/E cycle.