Power Electronics

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Content

Introduction

Electrical Energy flow control and type change (AC ↔ DC) is an important scientific and engineering task – starting from the installation of electrical supply systems to wide usage of electricity in industries, transport and households – for more than 100 years. Due to semiconductor revolution, nowadays electromechanical and electromagnetic transformers are being replaced with advanced Power Electronic Converters with a very high efficiency. We can find Power Electronic Equipment with power amplitude starting from some watts to many megawatts in any urbanized and industrialized area of the World.

What is Power Electronics? An adequate definition [1] is provided by Prof. R. W. De Doncker, (RWTH Aachen):

"*Power Electronics deals with the control and the low-loss conversion of electrical energy using electrical switches, nowadays – power semiconductors.*"

Basically we have two types of electrical energy: Direct Current (DC) and Alternating Current (AC). Both have different possible electrical potential (with a volume of some volts to gigavolts). Load supply with necessary electrical energy type, voltage and frequency (in case of AC supply) is the responsibility of Power Electronic Converters.

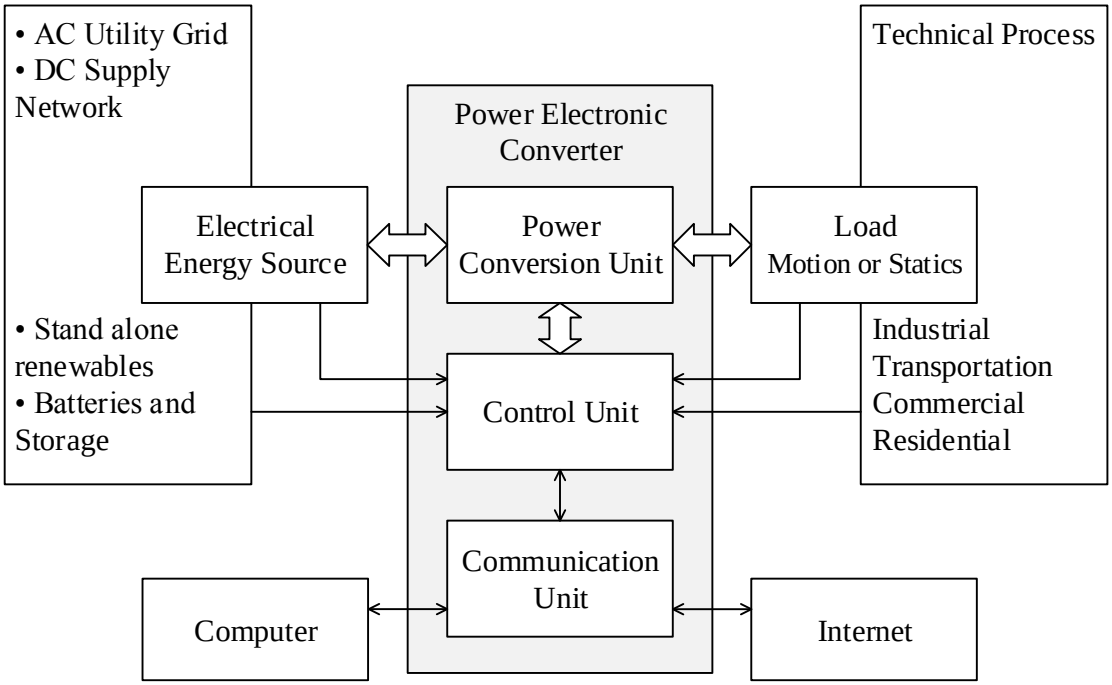

Fig.1. Power Electronic System

As it can be seen in Fig.1., Power Electronic System is complicated. The main Power Electronic Converter unit provides power flow conversion (AC to DC or DC to AC) and adjustment (for voltage and frequency regulation). The Control Unit is organizing an appropriate signal distribution to semiconductor power switches and implements control algorithms of converter. The Control Unit also is observing energy source and load conditions on real time and, of course, is following the commands from Communication Unit. In a large

and complex process or production control system, Power Electronic Equipment is only one element.

Application possibilities of Power Electronics are everywhere around us, starting from mobile telephones, cars, ships, trains, airplanes, domestic appliances, commercial buildings to all industries and military applications.

The development of Power Electronic Converters in a broader scope started after the invention of transistor in 1957. Main topologies of AC-DC, DC-AC and DC-DC converters were invented and designed at the beginning of 60's. But today the improvement of Power Electronic Converter efficiency is carried on in many research centers and companies all over the World. Development of an efficient converter is a very multidisciplinary task.

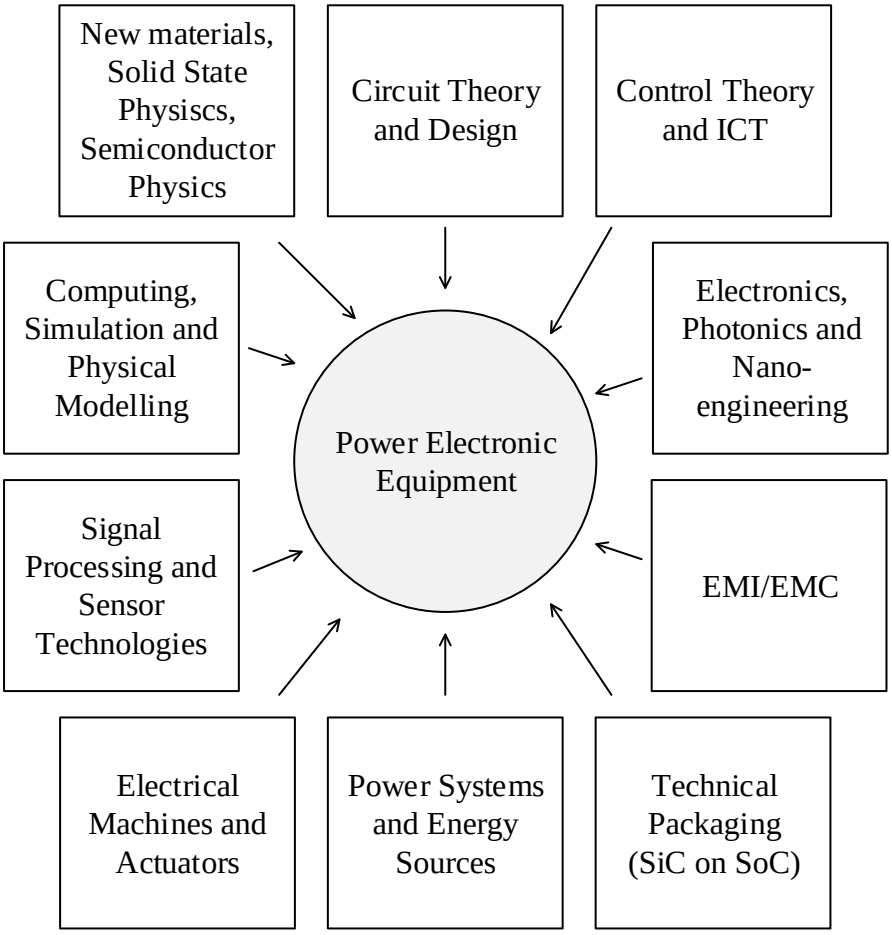

Fig.2. Multidisciplinarity of Power Electronic Technology

Fig.2. shows some research and development areas, which significantly influence Power Electronic Converter technology.

People in the World are more and more using electrical energy, fossil sources are limited, new alternative energy production technologies are being developed and it can be possible only with a wide usage of Power Electronic Converters. Therefore it is declared that Power Electronics is the main technology for the 21st century.

All contributors of this book are willing to explain the reader several topics of Power Electronic technology.

The first chapter describes basics of semiconductor devices in Power Electronics.

The second chapter more precisely explains DC-DC Converter operation at hard switching mode.

The third part of the book is devoted to rectifiers – the most applied Power Electronic Converters.

A very detailed explanation of topologies and control methods of inverters is given in the fourth chapter – Power Electronic Converters of DC to AC.

The fifth chapter is more specific and covers the basics of Matrix Converters.

In the sixth chapter snubber circuit meaning and some converter switching methods, including soft-switching, are explained.

Some application areas of Power Electronic Converters are described in chapter 7 including energy transmission and renewable energy production.

1. De Doncker R.W. Lecture Notes: Power Electronics // Koln: Hundt Druck Gmbh, 2009 – 206p.

1. Semiconductor Devices in Power Electronics

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1.1. Diodes

Diode is a semiconductor structure of two silicium layers of different conductivity: one layer (left) contains more positively charged (p) particles (Fig.1.1), the other (right) - more negatively charged (n) particles. This p-n joint is called bipolar.

The majority of the charges are obtained by means of adding to the silicium structure other active materials. Therefore both layers contain additional charges of opposite polarity - minor charges. In the neutral condition of the structure a part of p major charges move to n layer, but a part of n major charges - to the p layer.

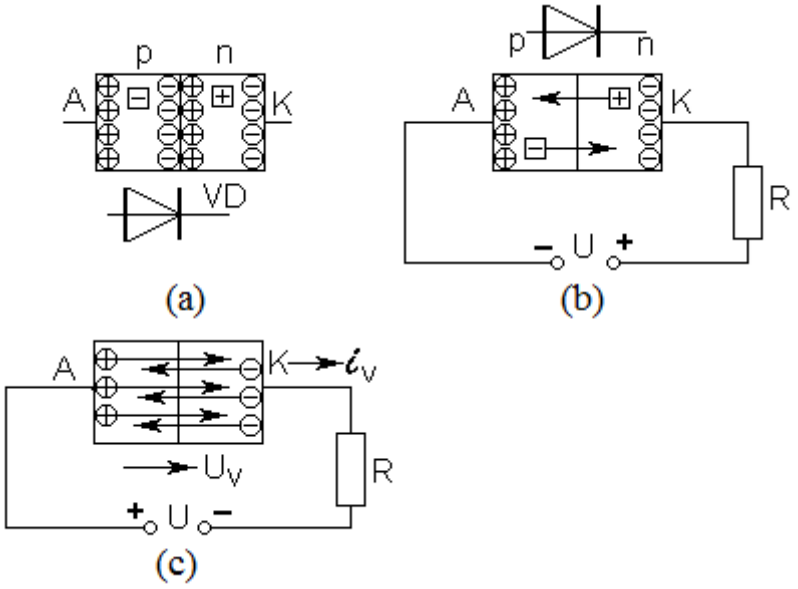


Fig.1.1. The operation of the diode structure in neutral (a), reverse (b) and direct (c) bias modes.

But crossing the barrier the further moving of p charges is slowing down because of impact of n layer negative charges crossing the barrier and getting to n layer. Similar situation takes place with n charges crossing the barrier. It produces the difference of potentials across the barrier - 0.7 V.

In the case when p layer is connected to the negative terminal of the source, n layer - to the positive one, the structure is in the mode of reverse bias, when the barrier provides very low conducting zone for the majority charges. The current is close to zero and depends on the flow of minority charges. The voltage of this polarity is reverse biasing voltage, but the current - a leakage current.

If the reverse biasing voltage is increasing the leakage current is also increasing. With some high enough voltage (hundreds of volts) the increasing of the leakage current results in high power losses and increasing of p-n structure temperature to the maximum acceptable. Exceeding of this temperature causes irreversible braking of the p-n junction - thermal breakdown.

The intensity of minority carriers' movement in the mode of reverse bias depends a lot on the heating regime of the diode, influence of light and radiation on the junction.

If p layer is connected to the positive terminal of the source, but n layer - to the negative, the majority carriers start to flow through the barrier producing the electric current.

$$I_v = \frac{U - U_v}{R} \quad , \tag{1-1}$$

where U_V is the voltage drop across the diode, higher that the difference of potentials across the barrier. The current in the circuit will exist also only if the supply voltage is higher that that of the barrier.

The arrow in the symbol of diode is directed from p to n layer and defines the possible direction of the operation current, from anode A to cathode K.

Fig.1.2 demonstrates the volt-ampere characteristics of the diode, i.e. the dependence of the current on the voltage across A and K. In the quadrant of the direct bias the grade of measurement unit of the current is usually amperes, but voltage - from zero to 2-2.5 V. In the reverse bias quadrant the current is measured in milliamperes, but the voltage - hundreds of volts. The volt-ampere characteristic of the direct bias can be linearised as

$$U_V = U_0 + I_V R_d \quad , \tag{1-2}$$

where U_0 - is so-called threshold voltage (about 0.9 V), R_d - dynamic (differential) resistance of the diode.

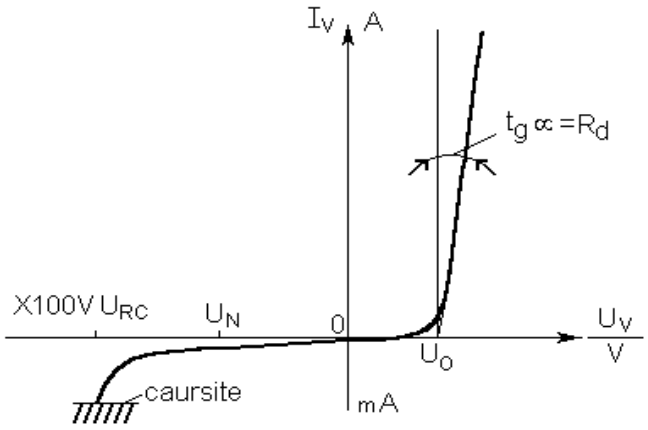


Fig. 1.2. Volt-ampere characteristics of the diode

This linearised characteristic is of top importance for the calculations of power losses of the devices. If the diode is connected into the scheme like in fig.1.3 and its instantaneous value of the current within the time interval from 0 to π is $i_v = I_m \sin \omega t$, the average power losses per period are calculated as the following

$$\Delta P_{vvid} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin\omega t.(U_0 + R_d I_m.\sin\omega t)d\omega t = \frac{I_m U_0}{\pi} + \frac{I_m^2}{4} R_d = I_{vid}.U_0 + I_{ef}^2 R_d \ . \tag{1-3}$$

This is a typical expression for these calculations. The calculated power losses define the temperature of the diode structure in the stationary regime

$$\theta_{pn} = \theta_0 + \Delta P_{V\,vid} \,.\, R_T \,, \tag{1-4}$$

where θ_0 - is an ambient temperature, R_T - thermal resistance of the structure and cooling system (^{0}C / W). To avoid the damage of the structure the temperature of it θ_{pn} should not exceed the value of about 130^{0}C.

With the known parameters R_T, R_d, U_o assuming θ_{pn} and θ_0 the acceptable current of the diode can be calculated, i.e. the average value of the current through the diode:

$$I_{dp} = \frac{-2U_0 + 2\sqrt{U_0^2 + \frac{(\Theta_{pn} - \Theta_0)\pi^2 R_d}{R_T}}}{\pi^2 R_d} \quad . \qquad (1\text{-}5)$$

The lower is resistance R_T, i.e. the cooling system is better, the higher is current I_{dp}. If rated R_T, θ_{pn}, θ_0 are assumed this expression gives an opportunity to obtain the rated current of the diode.

The rated voltage of the diode U_{RC} is assumed of about half of the diode breakdown voltage. For example, if U_{RC} = 1550 V, then U_N = 700 V, the diode is of class 7 according to the assumed voltage.

The breakdown is determined with the instant value of voltage therefore with the reverse voltage amplitude. If the circuit of the diode is connected to 220V AC source then the amplitude of this voltage higher than 300V should be taken into account. Then in this case a diode of the 4th class should be chosen.

Dynamic operation regime of the diode is also of top importance at the beginning and end of the periods of current control. At the beginning some increasing of the direct voltage drop is typical for the structure, at the end (Fig.1.3) at some time moment t_{r0} the diode conducts full current in the reverse biasing mode.

The latter regime is explained with the increased concentration of the majority carriers of opposite polarity in the correspondent layers of the diode during the period of the current conduction (n polarity in p layer and vice versa). Therefore with the changing of the current direction time t_{r0} should be known to "clear" the layers. At this time the voltage across the diode is with the polarity correspondent to the direct conductivity, but this value is gradually decreasing and equal to zero at the end of the interval. During the further period of conductivity the current is decreasing and the voltage of the diode is close to the determined reverse biasing voltage of the source.

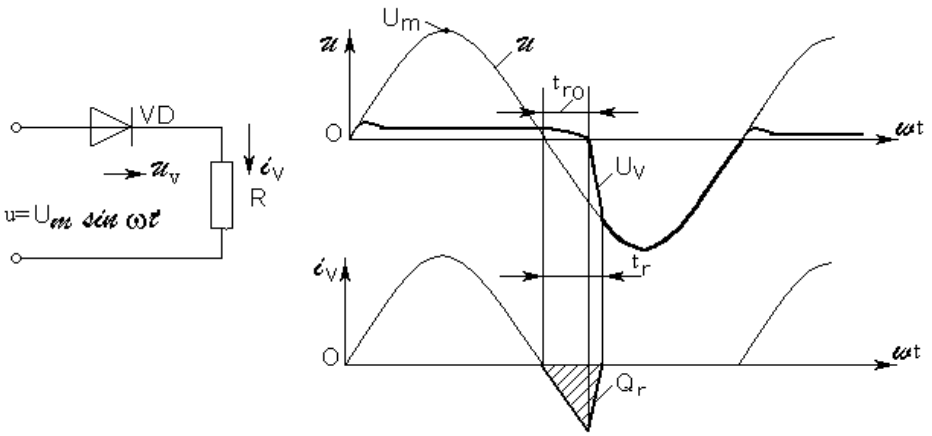


Fig. 1.3. Dynamics of the diode operation

The curve of the reverse current is characterised with such dynamic parameter as switch - off charge Q_r. The more qualitative is the diode, the lower are t_r and Q_r . t_r of a middle quality diode is about 5 μs, that of excellent quality 1 - μs. As the diode does not perform the functions of single conductivity element during the turning off process, it is obvious that with the increasing of the source voltage frequency up to some particular value the diode does not keep the function of reverse biasing more. If t_r = 5 μs, it takes place at 5 μs of the period or 10 μs of that. The acceptable frequency is

$$f_{\max} = \frac{10^6}{10} = 100 \ kHz \ . \tag{1-6}$$

As p-n junction is the base of all semiconductor devices they all have similar static and dynamic characteristics, i.e. a semiconductor element is not an ideal conductor and not absolutely high-performance.

$$t_r = \sqrt{\frac{Q \cdot 0{,}2}{500 \cdot 10^3}} = 6{,}32 \mu s \ . \tag{1-7}$$

Amplitude of the reverse current

$$I_{VRm} = \frac{500 \cdot 6{,}32 \cdot 10^3}{10^6 \cdot 0{,}1} = 31{,}6A \ . \tag{1-8}$$

Maximum available rated current of the modern produced diodes is kilo-amperes and rated voltage is higher than 10kV. For the decreasing of the power losses and the temperature of the structure more effective natural and forced cooling with air and liquid flows is provided.

1.2. Thyristors

Thyristor is a controlled semiconductor switch with the features of a diode. Thyristor is formed with the specific connection of two transistors (Fig.1.4). VT1 transistor is of p-n-p type with the current transfer factor α_1, and its collector forms the base of the second VT2 transistor that is simultaneously the control electrode (gate) G of the thyristor.

The base of the first transistor in its turn is connected with the collector of the second transistor. If the thyristor is supplied with direct voltage (positive pole to anode A, negative - to cathode K) then the four-layer p-n-p-n structure of the thyristor (Fig.1.4) consists of two diodes of direct bias and one, that in the middle, is supplied with the reverse voltage. This diode conducts leakage current I_{CO} formed from its minority charges flow.

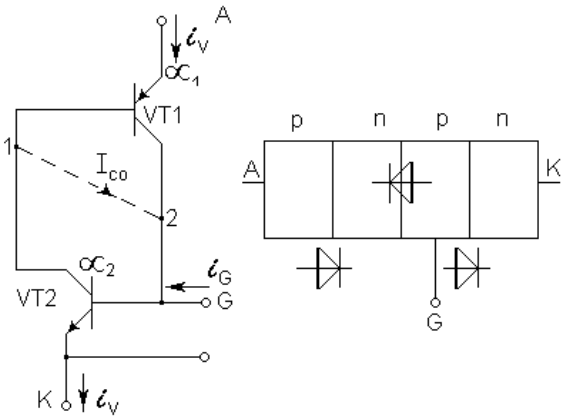


Fig. 1.4. The equivalent circuit of the thyristor and four-layers structure

First of all the case when the control current $i_G = 0$ is under the reviewing. The collector current of transistor VT2 is equal to $\alpha_2 i_V$. The base current of transistor VT1 is $i_V(1- \alpha_1)$. Therefore for junction 1 of the circuit taking into account leakage current I_{CO} the following current equation is valid

$$i_V (1- \alpha_1) = I_{C0} + \alpha_2 i_V \quad . \tag{1-9}$$

Then the thyristor current

$$i_v = \frac{I_{C0}}{1-\alpha_1-\alpha_2} \quad . \tag{1-10}$$

As it is known α is zero with low emitter current of the thyristor structure. This feature provides the stability of the thyristor structure with low leakage currents. With the leakage current achieving a particular value (for powerful thyristors 30...50 mA) α_1 and α_2 are increased causing i_V increasing and further increasing of α_1 and α_2 , etc., i.e., and avalanche-like switching-on process takes place. After this process $(\alpha_1 + \alpha_2) > 1$ and the leakage current I_{CO} changes its sign.

The leakage current can increase if

1) the voltage across anode and cathode is increasing,

2) the temperature of the structure is increasing,

3) the central junction is affected with an outside luminous flux,

4) the central junction is affected with an outside radiation flux.

The first opportunity is applied for the production of low-power diode with voltage switching or dinistor. The third opportunity to increase I_{CO} to a necessary value by means of light is applied for the production of optical controlled thyristors.

Temperature is not used for the thyristor switching on, but during the utilization the increasing of the thyristor temperature should be taken into account. Therefore during the operation the voltage, at which the leakage current achieves its critical value, is increasing. The utmost temperature until which the thyristor can stand the direct voltage without additional control is assumed of 120^0C.

The second case of the thyristor operation is when $i_G > 0$. Taking into account that the current of VT2 emitter is $(i_V + i_G)$ the equation is

$$I_{CO} + \alpha_1 i_V + i_G = (1 - \alpha_2)(i_V + i_G). \quad (1\text{-}11)$$

Therefore

$$i_v = \frac{I_{C0} + \alpha_2 i_G}{1 - \alpha_1 - \alpha_2} \quad . \quad (1\text{-}12)$$

As it is obvious the increasing of the current factor and thyristor switching on can be achieved increasing the base current of transistor VT2 above its critical value. The control signal is short-time (30...100 μs). The ratings of thyristor contain necessary control current and voltage. Typically the control current does not exceed 1 A, and the voltage - 4 V.

The volt-ampere characteristic of thyristor in on condition is similar to that of the diode (fig.1.5). But the threshold voltage can achieve U_0 = 1,2 ... 1.3 V. It should be taken into account that the VAC of on condition of the direct bias does not go from zero, but starts from comparatively low hold current I_{NO}. If the resistance of the circuit does not provide the current higher than I_{NO} the thyristor in this case will not be switched on.

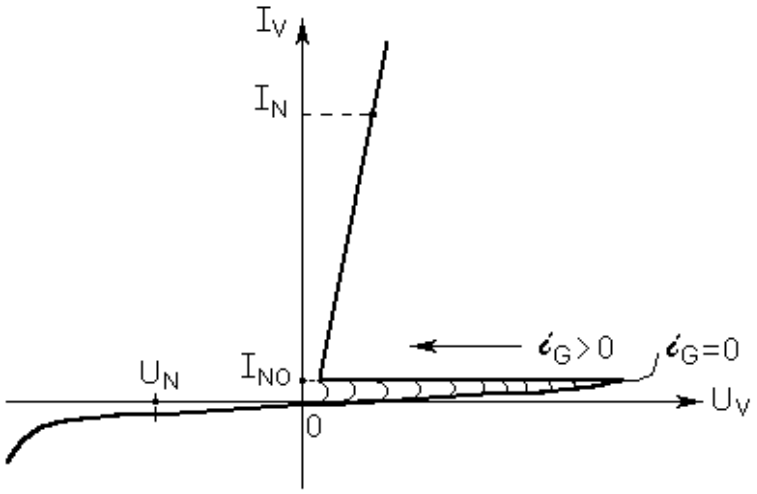


Fig. 1.5. Volt-ampere characteristic of thyristor

While $i_G = 0$ the characteristic of the direct bias is symmetrical to that of the reverse bias, i.e. $i_V (U_V) = - i_V (-U_V)$. When the level of threshold voltage is achieved in the direct bias the thyristor is on and VS characteristic stepwise transforms to the characteristic of the on-state with low direct voltage level.

In the 80th fully controlled thyristors were produced - so called Gate Turn Off thyristors. As in on-state $(\alpha_1 + \alpha_2) > 1$ then for the conducting of basic current i_V (assuming that the leakage current I_{CO} is already decreased till zero) the following control current should be supplied

$$i_G = \frac{(1-\alpha_1-\alpha_2)i_V}{\alpha_2} < 0 \quad , \tag{1-13}$$

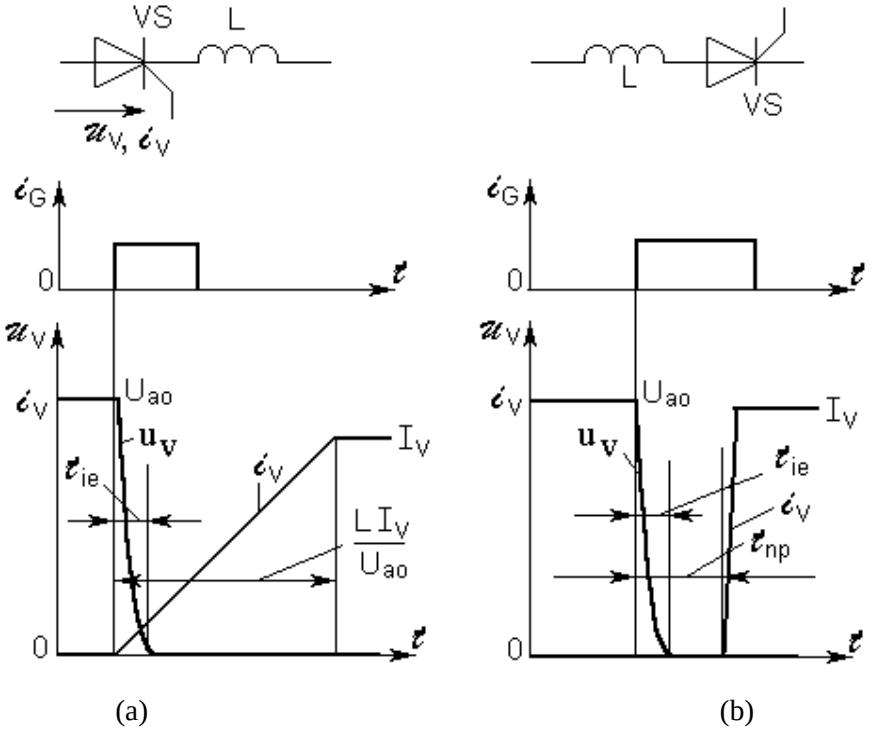
that can be about 30...70 % of basic current i_V. If in on-state i_V =200A, $\alpha_1 = \alpha_2 = 0.7$ then current of $i_G = \frac{-0{,}4.200}{0{,}7} = -114$ A is necessary for switching on.

Although the time necessary for the flow of control current is small (about 5 μs) the strength of the control electrode circuit should be increased as well as the circuit of high control current is necessary. Usually the capacitor discharge is applied.

The dynamic regimes are of great importance for all the thyristor types semiconductor elements: the processes of switching on, off, stability to fast changes of voltage.

The process of switching on is characterised with the gradual conductance of the structure in the direction from control electrode with speed 0.5 mm/μs. If the current of the basic circuit instantly flows through the initially small switching zone then high current density is produced there causing high losses and increased temperature. The temperature exceeding an acceptable one causes an irreversible damage of the structure.

Therefore regular thermal regime of the initial switching zone requires the limitation of fast increasing of the current during the time of full switching on of the structure, for the modern thyristors this time is about 5...7 μs. There are two approaches to realise these requirements: by means of linear reactor and saturation reactor.



(a) (b)

Fig. 1.6. The process of the thyristor switching with linear reactor (a) and saturation reactor (b)

The first variant applies the ratings of acceptable speed of current increasing [di / dt], and the inductance of the reactor connected in series with the thyristor (Fig.1.6.(a)) is calculated taking into account the level of the voltage just before switching on of the element U_{a0} :

$$L \geq \frac{U_{a0}}{[di/dt]} \tag{1-14}$$

Then the maximum losses of power during the switching on process t_{ie} are

$$\Delta P_{mie} \approx 0{,}25 U_{a0}^2 \frac{t_{ie}}{L} \quad , \tag{1-15}$$

but those average within the period T = 1 / f

$$\Delta P_{ievid} \approx 0{,}16 f \frac{U_{a0}^2 t_{ie}}{L} \quad . \tag{1-16}$$

As it is obvious from the expressions the power losses existing during the switching process are sharply increasing with the increasing of the throttle inductance. However this inductance is high enough and causes the voltage drop when the current of the basic circuit is changed in the quasi-steady process. Therefore instead of that linear the saturation reactor with square-form magnetizing characteristics of its core is often.

Until the core is not saturated the inductive resistance of the coil is almost infinite and there is no current in the circuit. The parameters of the throttle should be selected in terms of the fact that the time of operation in a non-saturated regime after supplying the thyristor with control signal should not be lower than t_{ie} :

$$t_{np} = \frac{(B_p - B_0) sw}{U_{a0}} \geq t_{ie} \quad , \tag{1-17}$$

where B_p, B_0 are the saturation and residual inductances (T) of the magnetic material, s, w - are the cross-section area (m^2) and number of turns of the coil. As soon as the core is saturated and its inductive resistance is close to zero the structure of the thyristor is on and the increasing of the current does not cause the switching losses.

The other dynamic process is thyristor's switching off (Fig.1.7). Similar to the diode (Fig.1.3) after reaching zero level the current of the thyristor continues to flow in the reverse direction for some time and then in t_{r0} time the structure is recovered. At the end of this stage the reverse biasing value of the thyristor voltage is increasing. At this moment the changing of its polarity to the direct polarity (Fig.1.7) can cause the problem of the repeating thyristor switching on, i.e. an emergency situation. This is related to the fact that during the recovery process not all the majority charges of the thyristor structure return to the positions necessary for the direct bias voltage maintaining. That is why the reverse biasing voltage should correspond to the known time given in the thyristor ratings - off time t_{iz} .

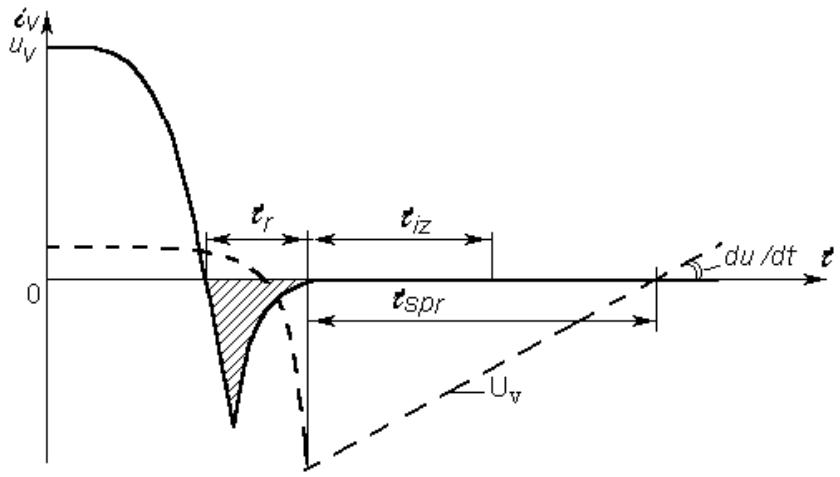


Fig. 1.7. The diagram of the regular switching off process of thyristor

The process of switching off demonstrated in the diagram is successful as the duration time of the reverse biasing voltage is $t_{spr} > t_{iz}$. In the case of AC circuit t_{iz} limits the maximum thyristor operation frequency. Thus the half-period of the voltage should be longer than t_{iz} and

$$f_{\max} < \frac{1}{2t_{iz}} \quad . \tag{1-18}$$

If t_{iz} = 100 μs (weak thyristor), therefore f_{max} < 5 kHz. The qualitative thyristors have t_{iz} = 20...30 μs, and can operate with frequency 15...25 kHz.

The off time of the thyristors has a special importance for the commutated DC circuits where the thyristor switching off is realised with the help of forced commutation with in advance charged capacitor. The higher is t_{iz} , the higher is the capacity necessary for the similar conditions. For the decreasing of the sizes of the commutation circuit the thyristors with low t_{iz} are applied.

The third dynamic process - increasing of the direct voltage - is connected with the thyristor direct voltage recovery speed after the off process. The middle junction (fig.1.4) with its direct bias has a particular capacity C_{np}. With fast recovered voltage the leakage current through this junction-capacitor is increased:

$$i_{C0} = i_{Cnp} = C_{np} \frac{du}{dt} \quad . \tag{1-19}$$

If du / dt is high current i_{C0} can exceed a critical value when transfer factors α_1 and α_2 of the thyristor equivalent transistors start increasing from the initial zero values. In this case the thyristor can be spontaneously switched on and cause an emergency situation. If critical current I_{C0} = 30 mA, the junction capacity $C_{np} = 100. 10^{-12}$ F, then the critical value du / dt is 300 V/ μs. For the safe switching of the thyristor the direct voltage should be supplied at time moment t_{spr} when the off processes of the thyristor are fully completed, i.e. $t_{spr} > t_{iz}$ (Fig.1.7).

Basically the thyristors are produced for high enough powerful devices. Nowadays the thyristors are with rated currents up to some kA, rated voltage above 10kV, admissible [di / dt]> 1000A/μs, [du / dt] > 1000 V / μs and off time lower than 20 μs.

1.3. Transistors

Bipolar transistor consists of 3 semiconductor layers: two p and one n, forming p-n-p transistor (Fig.1.8) and two n and one p forming n-p-n. One border layer and its electrode are called emitter (E) and signed with an array defining the direction of the current conducting (the current flows from the source positive pole to the negative). The layer in the middle together with emitter forms controlling bipolar junction or diode in the direction of the array and is called a base (B). The third layer with the help of outside voltage source carries a part of the emitter major charges getting the base layer because of the control voltage to the operation circuit. This layer is called a collector (C) (Fig.1.8).

The direction of the transistor array defines the necessary polarity of the control and operation voltage source: E of p-n-p transistor is connected to the positive pole directly or through resistor, B and C - to the negative pole of the control and operation voltage sources correspondingly (Fig.1.8.a); the electrodes of n-p-n transistor are connected to the sources in the opposite way (Fig.1.8.b).

To provide the transistor effect - carrying a part of the emitter major charges from base layer to the operation circuit - the voltage of the basic operation circuit should be higher than that of the control circuit U_{EB} or U_{BE}. The displayed circuits respond to so called common emitter circuit widely applied in the power converters.

In accordance with the Kirhhoff's Law the currents in the transistor circuit are

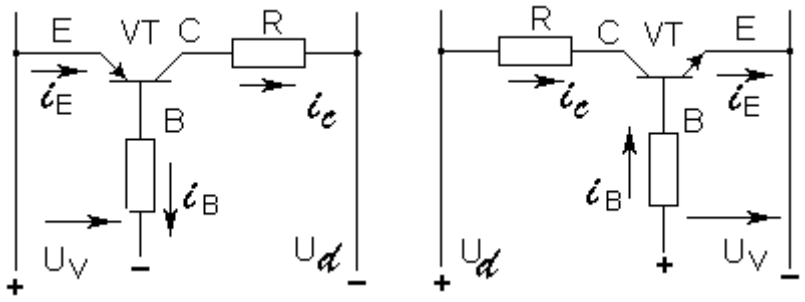
$$i_C = i_E - i_B \quad , \tag{1-20}$$

where all the currents can be with positive signs only.

The correlation of collector and emitter currents is called the factor of current conducting

$$\alpha = \frac{i_C}{i_E} < 1 \quad , \tag{1-21}$$

defining how effectively the major charges of the emitter are carried to the collector circuit. Relation $\alpha = f(i_E)$ is of top importance for the forming of a complex p-n structure (Fig.1.9). Silicium has some dead zone at low emitter currents but then α is increasing achieving its maximum at about a half of the rated current.



(a) (b)

Fig. 1.8. p-n-p (a) and n-p-n (b) transistors connection

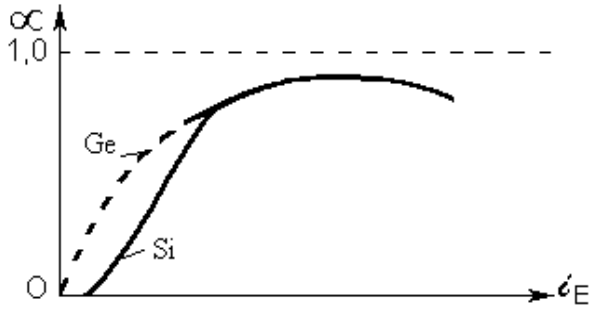


Fig. 1.9. Dependence of the Silicium and Germanium (Ge) transistors currents transfer factors on the emitter current

The relation of collector and base currents is a static factor of the current amplification β:

$$\beta = \frac{i_C}{i_B} = \frac{\alpha}{1-\alpha} \quad . \tag{1-22}$$

As α is a function of i_E, then β depends on i_E. The amplification of the current reaches its maximum value at α_{max}. For example, if α_{max} = 0,95, then β_{max} = 19. For the qualitative bipolar transistors β reaches 100 and more. However the regulation of high collector currents requires a high base current that complicates the application of BT.

The operation of BT can be characterised with the help of collector current I_C dependence on the voltage collector-emitter U_{CE} (for n-p-n transistor) changing values of the base current (Fig.1.10). With a constant base current and increasing collector voltage the current of the collector sharply increases at the beginning, but later is almost constant. If the base current is zero the collector voltage is about 85% of the operation circuit voltage, and a low collector current is flowing (point A). Even if the current is low the voltage can be high enough with appreciable power losses. For example, is I_{CO} = 10 mA, but U_{CEO} = 400 V, then ΔP_0 = 4 W, that is high enough for the transistor. For better BT switching off the polarity of the control voltage is changed allowing decreasing of power losses to minimum.

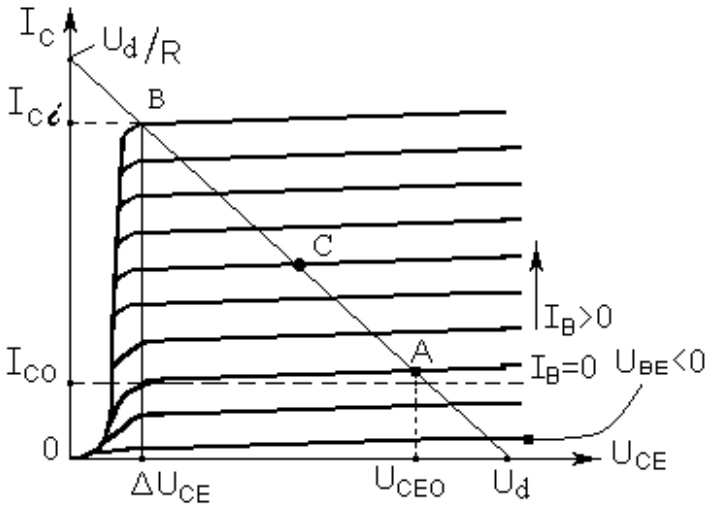


Fig. 1.10. Collector current of n-p-n BT depending on collector voltage

The increasing of base current maintaining U_d unchangeable the collector voltage is decreasing and with high enough I_B the transistor is fully on, and the collector current is a bit lower than short circuit current U_d / R. It is called "saturation" of the transistor in operation regime, point B. The direct voltage ΔU_{CE} in this regime can be lower than that of base-emitter, pointing that the collector-base diode is in the direct bias, i.e. the collector layer contains a lot of negative emitter charge carriers, but the base has a lot of positive and the diode conducts in the direction from base to collector (n-p-n transistor).

The power losses of the transistor in the saturated regime are not high. If U_d = 100 V, ΔU_{CE} = 2 V, R = 10 Ω, the collector current is 9,8 A, but the losses in the transistor ΔP_i = 19,6 W. If the transistor is operating at point C (Fig.1.10.) with U_{CE} =0,5 U_d , then the current is 5 A, but the losses - 250 W.

Taking into account low values of the losses in two regimes - saturated and off-state - the regulating effect in the power electronic systems is achieved with the application of these two regimes only: the transistor is operating in so called "switch" mode (Fig.1.11.). The losses within the operation period consist of those in the border regimes ΔP_0 and ΔP_i and losses ΔP_k of the transient periods from one state to other. If the transistor operates with a resistive load and both switching periods are the same then

$$\Delta P = \Delta P_0 + \Delta P_i + 2\Delta P_k = I_{C0}.U_d \frac{t_a}{T} + I_{Ci}.\Delta U_{CE} \frac{t_i}{T} + 2\frac{I_{Ci}.U_d.t_k}{6T} \quad . \qquad (1\text{-}23)$$

I_{C0} and I_{Ci} are the collector currents in on and off states; t_k - switching time (typically 1...2 μs); t_a , t_i , T - the duration of the control signal in the on and off part of the switching period T (Fig.1.11.).

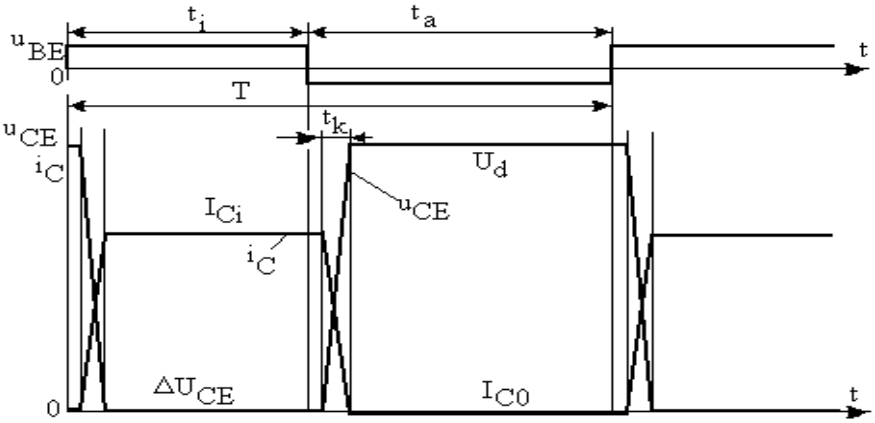


Fig. 1.11. Voltage and current diagrams of the transistor in "switch" mode with active load

With the increasing of frequency the specific switching time during the shortened period T is increasing, and the third component of losses is also growing - the specific commutation losses ΔP_k. When the frequency is tens of kilohertz the commutation losses can achieve 50...70% of the admissible power losses of the transistors ΔP_{TR}. For the calculation of the heating process expression (1-4) can be applied.

The ratings of transistors contain maximum admissible collector voltage in off state, maximum admissible current in on state, amplification factor as a function of I_C, voltage ΔU_{CE} at I_{Cmax} , switching time and others.

The most important disadvantage of bipolar transistors is a low amplification factor as well as dependence of power losses on the base current. In order to improve the static amplification factor the complicated transistor schemes are applied. In the case of two transistors connection it is called Darlington scheme (Fig.1.12).

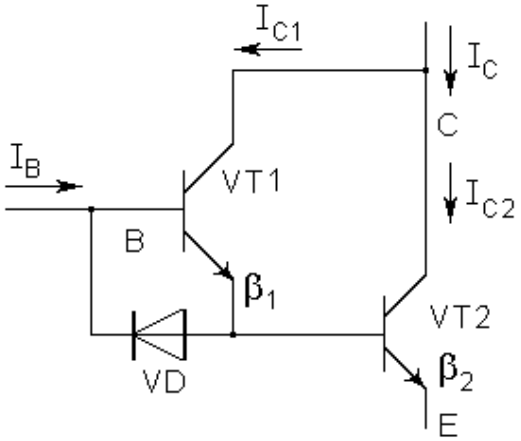


Fig. 1.12. Darlington scheme

In this scheme the emitter current of the first transistor VT1 is the base current of the second one VT2:

$$II_{B2} = I_B + I_{C1} = I_B\,(1 + \beta_1)\,. \qquad (1\text{-}24)$$

The common collector current

$$I_C = I_{C1} + I_{C2} = \beta_1\, I_B + \beta_2\, I_{B2} \quad . \qquad (1\text{-}25)$$

Taking into account (1-21) the static amplification factor of the scheme

$$\beta = \frac{I_C}{I_B} = \beta_1 + \beta_2 + \beta_1\beta_2 \quad . \tag{1-26}$$

As it is obvious the common β is higher than the multiplication of amplification factors of the both transistors.

The second disadvantage of the transistors is their limited overload durability. If with constant base current in on state the collector current is increasing above some calculated value, i.e. in Fig.1.10. the line is turned clock wise, the collector current and power losses are growing. It can result in overheating of the structure and damage of the junctions. An operative control with the switching base signal can provide an avoidance of this situation. While the collector voltage is increasing the control signal should be switched off.

Modern bipolar transistors are produced for hundreds amperes of collector current and hundreds volts of collector voltage.

1.3.1. Powerful Field Effect Transistors

The other version of the transistors realisation is connected with the forming of current conducting channel by an outside electric field influence. Thus the MOSFET version has been realised. A channel can be formed by n carriers as well as p carriers forming correspondingly n channel or p channel field transistors.

Field transistors are formed on the basis of n or p layer adding at its edges contact areas of opposite conductivity. The sizes of this area define the thickness of conducting channel.

An insulating oxide layer is placed over this base but over this layer in its turn - a metal electrode G - a gate that is supplied with one pole of the control voltage. The other pole of the control voltage is supplied to the base, that in its turn is connected to one of the contact areas of the semiconductor - source (S). The second area is called a drain (D).

If the base is of n-conductivity type then the electrical field between G and S fills in the channel with p base minority carriers forming p channel. With this aim the gate should be supplied with voltage potential more negative than that of the base. As the base is connected to the positive contact area S then for the switching p channel transistor on gate G should be supplied from the negative electrode of the control voltage. The array of the base defines the polarity of the control electric field necessary for the switching on. As the gate is insulated from the base the control current is zero. If the base is of p-conductivity type, contact areas - of n-conductivity, then the control electrical field between G and S can fill in the channel with n base minority charge carriers forming n channel. With this aim G should be connected to the positive potential but the base - to the negative contact area S. The scheme in Fig.1.13 demonstrates field effect transistor the gate G of which is connected to the positive control voltage electrode.

This transistor without control voltage normally is off, but with a necessary control voltage (typically less than 20 V) the channel is filled being called an enhancement mode MOSFET. The transistors are usually produced with an integrated fast-acting diode protecting from breakdown voltages. The switching on of the MOSFET requires about 4...7 V across G and S

(the threshold voltage is about 2...4 V). In fully on state the voltage across the transistor depends on the relation of the channel resistance and general load and channel resistance multiplied with the supply voltage. If the supply voltage is increasing then U_V across the switched on field transistor is also increasing. Together with it the transistor losses are also increasing. This is the most important disadvantage of the MOSFET elements.

In the informative materials the resistance of the channel $R_{DS(on)}$ is defined, for example, for a 10 A MOSFET with rated voltage 100 V of about 0,1 Ω, with 200 V - 0,2 Ω, with 400 V - 0,6 Ω, with 1000 V - 1,2 Ω. Approximately

$$R_{DS(on)} = k \cdot U_{N^{1,5}}. \tag{1-27}$$

If the admissible power losses in the element are 300 W (close to the typical parameters of powerful MOSFET) with voltage 1000 V the rated current can not exceed 15 A. It should be noted that MOSFET transistors can operate with the temperature of the structure up to 150^0C.

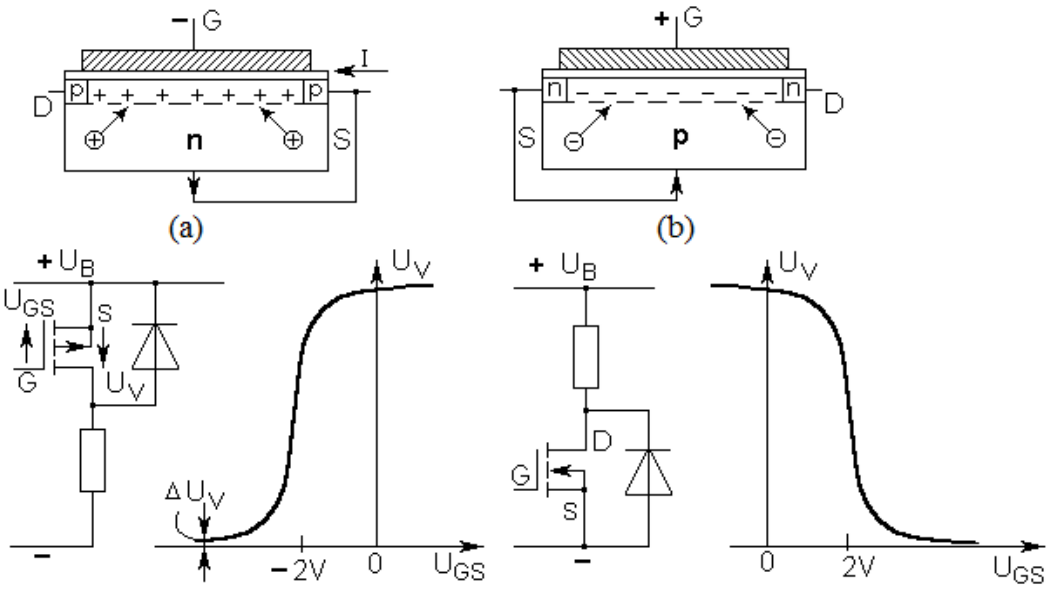


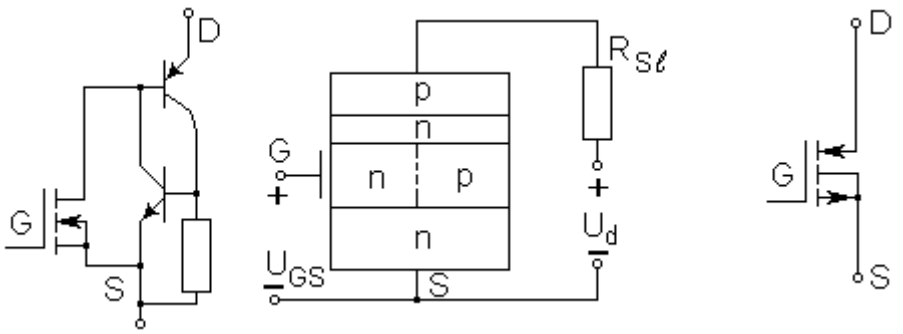
Fig. 1.13. MOSFET with p channel conductivity (a) and n channel conductivity (b)

MOSFET transistors are very fast-operating, and their switching time is measured in nanoseconds. Typically on time is 20...50 ns, but off time - 200...250 ns. The switching time does not depend on the temperature. MOSFET can operate with the frequency up to several millions hertz.

MOSFET can operate in parallel connection, as its particular resistances of the channel provide the smoothing of the currents between the transistors. This is a very important feature allowing a comparative easy way to improve the power of the installation.

The MOSFET transistors under consideration are so called transistors of logic level L^2FET. A new field effect transistor version is so called conductively modulated FET.

(COMFET). COMFET with n channel conductivity is in Fig.1.14 providing its equivalent scheme and structure.



(a) (b) (c)

Fig. 1.14. COMFET equivalent scheme (a), structure (b) and principal schematic symbol (c)

It is obvious that COMFET is a thyristor controlled with a field effect transistor. Therefore in on-state it is described with the volt-ampere characteristic with the direct voltage 2.5 V not depending on current. But the switching time is much higher than that of MOSFET. Typically their on time is 200 ns, but off time - 700...900 ns.

Taking into account that the voltage of COMFET in on-state does not depend on the operation voltage the rated voltages of COMFET with high enough currents (50...100A) can be increased to 1 kV and above.

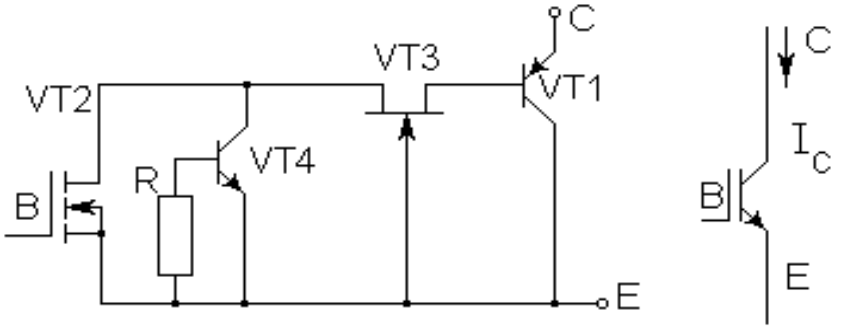
1.3.2. Bipolar transistors with insulated base (IGBT)

The integration of MOSFET transistor, bipolar transistor and at some rate thyristor in one element forms a switch called a bipolar transistor with insulated base with zero static control current, high rated voltage and current and small switching time (IGBT).

The equivalent scheme of IGBT is given in Fig.1.15 and resembles a pseudo-Darlington connection from p-n-p bipolar transistor VT1 and n-channel control field effect transistor VT2. A traditional field transistor VT3 connected between VT2 drain and VT1 base takes a part of direct voltage across the p-n-p transistor emitter (IGBT collector) and collector allowing to VT2 form some $R_{DS(ON)}$ with a low voltage.

If the potential of the base is more positive than that of the emitter then with direct voltage VT2 and VT1 are on. In on-state the direct voltage can never be lower than that across p-n-p transistor diodes between emitter and base. The typical IGBT volt-ampere characteristics are in Fig.1.16.

The admissible temperature of this element is about $+150^0$C. As it is obvious the current in the circuit depends on the control voltage. For full switching on with low voltage drop (below 2V) a comparatively high control voltage should be supplied - close to maximum admissible 20V. The control voltage for switching off is minus 20 V.



(a) (b)

Fig. 1.15. IGBT equivalent scheme (a) and schematic symbol (b)

When p-n-p transistor is switching on it is not in fully saturated condition as it disturbs VT1 base current flow. Therefore IGBT switching off is fast enough - from 100 to 3000 ns. If the off time is fast the switching losses are comparatively low that results in the opportunity to operate with high frequency.

IGBT are divided into 3 groups:

S - IGBT of standard operation speed with full on-time about 25 ns, full off-time 1600 ns, switching process power losses within the period 7.0 mJ (at rated current 10 A), that can operate with switching frequency till 1 kHz;

F - fast IGBT with full on-time about 13 ns, full off-time 600 ns, switching process power losses within the period 1.8 mJ (at rated current 10 A), that can operate with switching frequency till 10 kHz;

U - very fast IGBT with full off-time 190 ns, switching process power losses within the period 1 mJ, that can operate with switching frequency up to some tens kilohertz.

The switching power losses are reflected in the scheme in Fig.1.17 where once for short moment VT1, VT2 are on taking current I_C in throttle L that after the transistor switching on is conducted through diode V1 and stabiliser V2 forming initial and final collector voltage across the transistor under investigation.

When transistor VT3 is on its switching process takes place with the voltage of stabiliser UC when its current is growing from 0 to I_C, but then with full I_C the voltage is decreasing from U_C to zero. For some period while switching off the collector current is equal to I_C, the collector voltage is growing, but after the stabiliser is on U_C is constant and the current is decreasing. The periods of time presented in the figure are related to TGBTs of F group. If within the considered experiment U_C = 450 V, I_C = 10 A, then the common power losses are

$$\Delta E_k = (450.\ 5 + 225.\ 10)\ (15 + 600)\ .\ 10^{-9} = 2{,}77\ \text{mJ}.$$

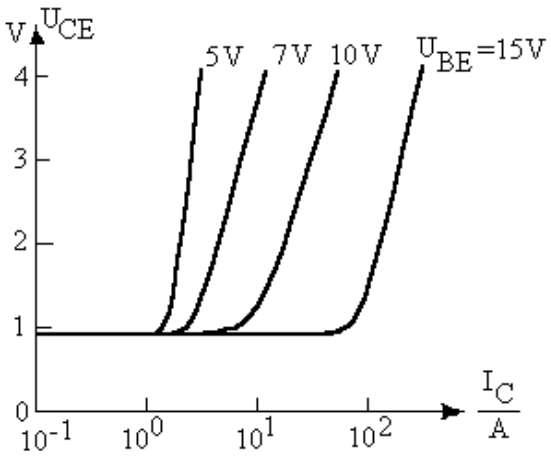
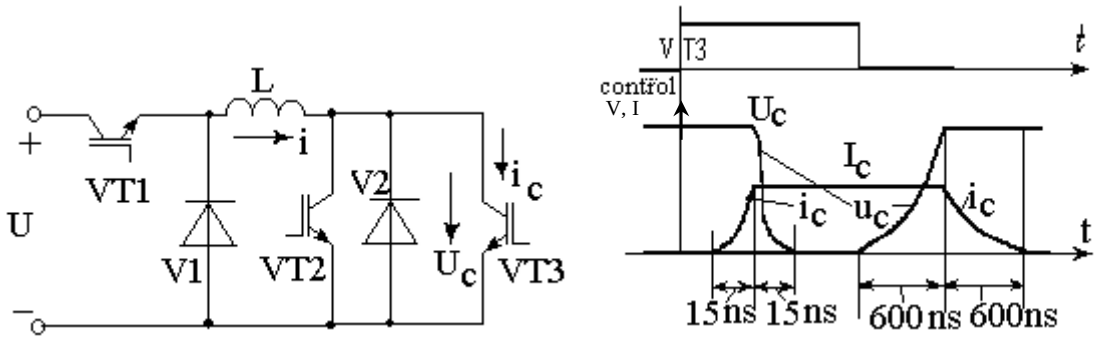


Fig. 1.16. Characteristics of an IGBT transistor at different U_{BE} values

IGBT structure is p-n-p-n junction therefore it is similar to that of thyristor. If the sum of the transfer factors of the VT1 and VT2 currents is equal to 1 then the structure spontaneously switches on. That can take place at the sharp direct voltage increasing speed du/dt.



(a) (b)

Fig. 1.17. Investigation of IGBT switching: scheme (a), diagrams of the current and voltage during the process of switching (b)

IGBT long operating currents achieve some hundreds amperes, but admissible direct voltages - up to 2-3 kV.

1.4. Power losses

The temperature of a semiconductor element determines its power losses and the parameters of its cooling system. In steady-state regime the steady temperature is

$$\Theta_p = \Theta_0 + \Delta P_p . R_T \quad , \tag{1-28}$$

where Θ_0 is the temperature of the environment, ΔP_p is the power losses in semiconductor (W), R_T - stationary thermal resistance of the cooling system (^{0}C/W).

Power losses for the diodes and thyristors can be calculated in accordance with expression (1-3), but for the transistors operating in the mode of switching - in accordance with -

$$\Delta P_p = U_v . I_v . \gamma + \Delta E_k . f \quad , \tag{1-29}$$

where U_v , I_v are the voltage and current of the element in on-state, ΔE_k - power losses within the switching process (J), f - switching frequency (Hz), γ - relative time of switching on within the switching period T=1/f.

If all the parameters and the admissible temperature of the structure are known [Θ_p], then maximum admissible switching frequency can be defined f_{max}. For example, if IGBT transistor temperature is [Θ_p]=130^{0}C, environment temperature is 30^{0}C , R_T=3 ^{0}C/W , γ=0,5 , I_v=10 A , U_v=2 V, ΔE_k = 2,77 mJ , then the maximum admissible switching frequency is f_{max}=8 kHz.

This methodology of calculations of the heating regime can be applied also for the other semiconductor elements. The stationary thermal resistance depends on the construction of radiator as well as on the method of cooling (Fig.1.18). The best construction of a semiconductor is a pill form with double side radiator. If the semiconductor construction is cooled with an air flow with the speed of 12 m/s, then the stationary thermal resistance is two times lower if to compare it with the cooling under natural condition. In many cases the rated current of the semiconductors is given for the forced ventilation regime with speed 12 m/s.

An improved cooling can be realised also with a liquid flowing through the radiator. Usually in the case of rated cooling regime the speed of the liquid flow is 3 l/min.

In many cases it is necessary to calculate the heating of p-n structure for the short-time pulse-type current. If the duration of a current pulse flowing through the element is lower than that for the steady-state (usually for some hundreds seconds) then the values of transient thermal resistance r_T dependent on time is applied (Fig.1.18).

The calculation is made with the help of superposition principle according to the changes of the temperature during the time of each pulse and the following infinitely long pause: starting with each next pulse the value of positive power losses is acting; starting with each pause the value of positive and negative power losses is acting infinitely long, the values calculated during the pulse and pause are summed up.

Then after 1 pulse the temperature of the structure is

$$\Theta_1 = \Theta_0 + \Delta P.r_{T10} \quad , \tag{1-30}$$

after a pause -

$$\Theta_2 = \Theta_0 + \Delta P.r_{T20} - \Delta P.r_{T21} \quad , \tag{1-31}$$

after the second pulse -

$$\Theta_3 = \Theta_0 + \Delta P(r_{T30} + r_{T32} - r_{T21}) \quad , \tag{1-32}$$

after the second pause –

$$\Theta_4 = \Theta_0 + \Delta P(r_{T40} + r_{T42} - r_{T41} - r_{T43}) \tag{1-33}$$

etc., where r_{Tab} is a transient thermal resistance for the time interval $t_a - t_b$; ΔP – power losses within the current pulse.

If the number of the pulses is high the heating process is close to a stationary.

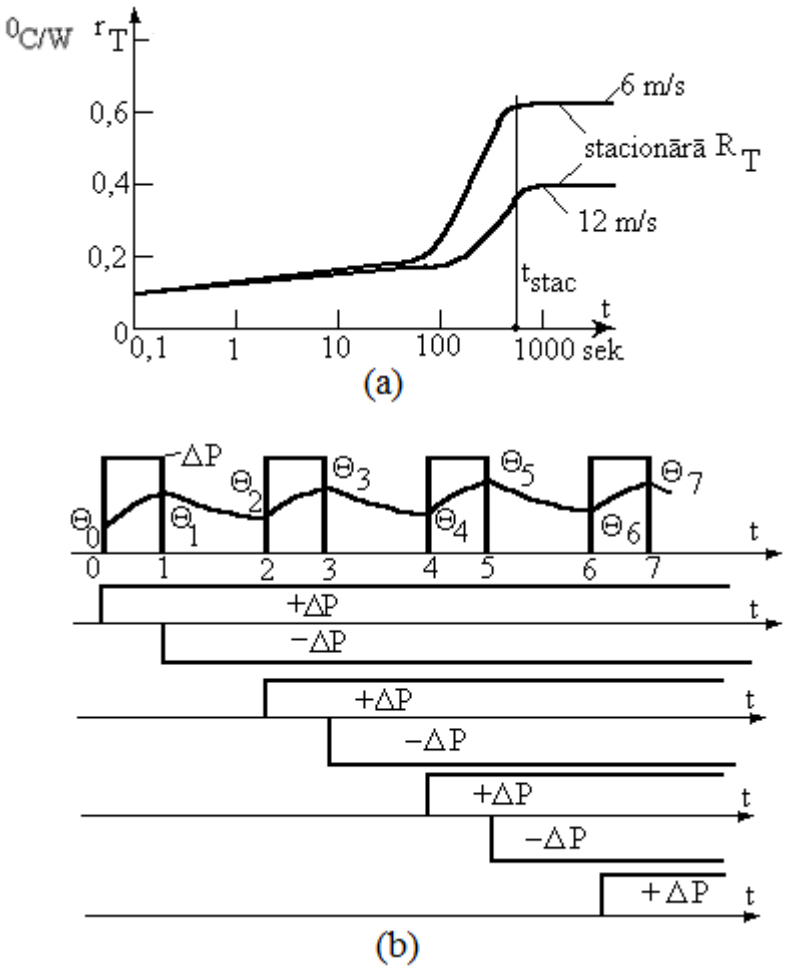


Fig. 1.18. Changes of the transient thermal resistance in time (a) and influence of the pulse type power losses onto the heating of the structure (b)

1.5. Comparison of Semiconductor Devices

Only a few definite statements can be made comparing all these semiconductor devices since a number of properties should be considered simultaneously and the devices are all the time evolving at a rapid pace [1]. The basic comparative parameters of semiconductor devices are given in Table 1-1, where U_{op} – is an operation voltage, I_{op} – current of operation, operation frequency - f_{op}.

Table 1-1. The basic comparative parameters of semiconductor devices

	diodes	thyristors	BT	MOSFET	IGBT
U_{op}	200V-12kV	12kV	1700V	4000V	6500V
I_{op}	300A-10kA	1000A-6kA	120A	2000A	2400A
f_{op}	400Hz-xMHz	400Hz-xkHz	x10kHz	100kHz-xMHz	x1…100kHz
Control	-		With current, high control power	With voltage, low control power	With voltage, low control power

Unlike BT the reverse voltage of MOSFET supplied to the gate of the transistor can achieve 30 V that significantly fasten the process of discharging of the number of minor charge carriers. MOSFETs as well as IGBTs have a high capacitance of the gate, recharging of which requires significant control currents. If to compare with BT the advantage of MOSFET is increased operation speed. Switching on time does not depend on the operation regime and is about 20…25ns with the delay not higher than 50ns. The time of switching off depends on relation of drain and source currents.

For decreasing of losses in the on-state the MOSFET is introduced into saturated regime with the supply of gate current. Therefore like in BT at the stage of switching on the process of minor charge carriers takes place. It results in the switching of delay and can be in the range from 20ns to 5μs.

Besides the high characteristics of MOSFET, IGBTs are much more qualitative in their operation speed and control power. Their most important advantage is low resistance of p-n-barrier in on-state that is 0,1…0,025Ω.

The comparison of semiconductor devices demonstrates fast development of those during the last 20-25 years with a significant increasing of power – from some Watts to MW. The frequency range is very wide – from Hz to MHz. The similar increasing takes place with the maximum currents and voltages.

References:

[1] Mohan N., Undeland T., Robbins W. Power Electronics: Converters, Application, Design. – NY: John Wiley and sons, 1989, 667 pp.

2. Hard-Switching DC-DC Converters

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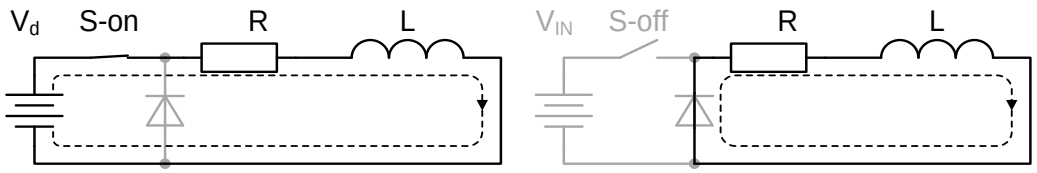
2.1. Fundamentals of Hard-Switching DC/DC Converters

2.1.1. Quasi-Stationary Mode

As it is follows from their name, the hard-switching DC/DC converters transform constant voltage of their input into another constant voltage of their output (or transform constant current into constant current). Such converters, in fact, continuously operate in one or another transient mode defined by particular combination of switches. In the same switching period there are several converter states and several transients (at least two). The exact analysis of these transients is too complicated and bulky. However, it is possible to split these transients into two large groups, irregular and regular, which are analyzed in more systematical way.

(a)



(b)

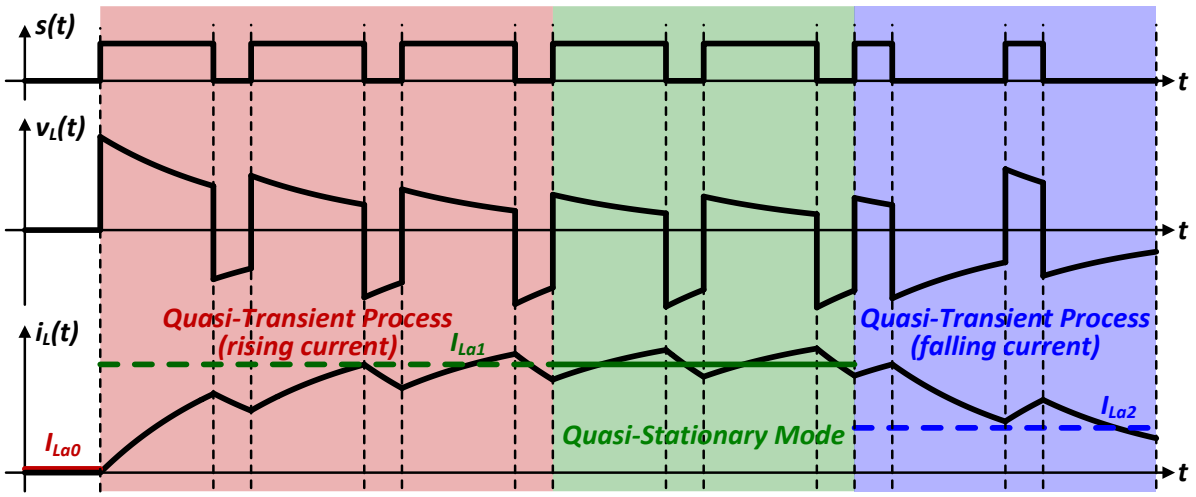


Fig. 2.1. Operation modes of switching converters: states of switching circuit (a) and operation diagrams (b)

The irregular transients are always different and form different values of system variables at the end of the new switching period. So while the irregular transients occur it is not possible to speak about repetitive processes – then the converter operates in the quasi-transient mode. In contrast, the regular transients repeat in each switching period and their fragments form periodical signals, i.e. then all variables are piece-wise periodical functions described by the following general equation:

$$x(t) = x(t + n \cdot T_{sw}), \tag{2-1}$$

where: ***x(t)*** – is a variable (instantaneous voltage, current, power etc.), but ***n*** – integer number. The corresponding mode is called quasi-stationary or static or steady state. The quasi-stationary mode is the main subject of analysis of power electronic converter.

An example of the quasi-transient and quasi-stationary modes of operation of an electronic converter is shown in Fig. 2.1. In this example switching period consists of two stages: when the switch is on, Fig. 2.1.(a), and off, Fig. 2.1.(b). When the switch is on the load current is rising, when it is off – falling. In the quasi-stationary mode of operation this increase is equal to the following drop, so that the output current is the same at the beginning and at the end of the period (green area). Note that although the current is the same at the ends it is changing in the middle.

In the transient mode the increase and drop are different. If the difference is positive then the resulting process is uprising (red area), but if negative – the process is descending (blue area).

2.1.2. Operation of Semiconductor Elements in Hard-Switching Converters

Semiconductor elements in the discussed converters operate in switching mode – i.e. are either completely "on" (conducting full operating current at low voltage drop) or completely "off" (endure full operation voltage at negligible leakage current) or toggling between one of the above two states (Fig. 2.2.). This operation is characterized with significant on-state and switching power losses ΔP which, however, are much lower than the controlled power and are ignored in this chapter (see Chapter 1 for more details of switch operation). Therefore, the input power P_d of switching converters is approximately equal to their output power P_o:

$$P_d = P_o + \Delta P \approx P_o \tag{2-2}$$

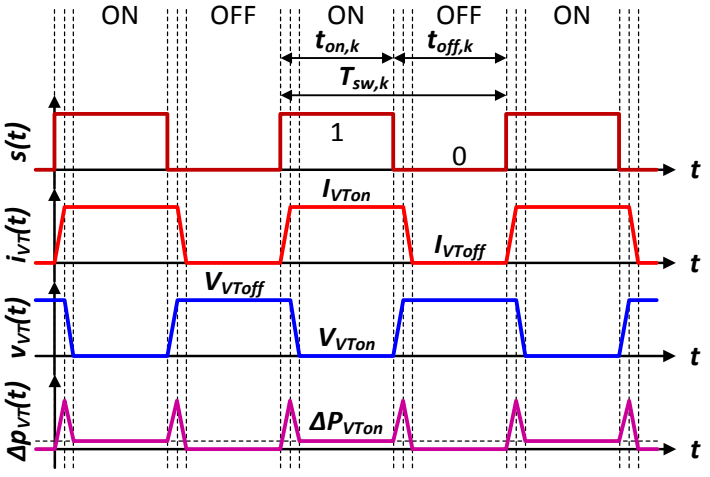


Fig. 2.2. Operation of semiconductor elements in hard-switching converters

The switching times are typically negligible compared with switching period T_{sw}, so it is possible to say that switches are "on" or "off". Then for each switch it is possible to compose its switching function s(t), which values are either 1 (if the corresponding switch is "on") or 0 (if it is "off"). The definite integral of the switching function of a switch within its k-th operation cycle (switching period) produces the value, known as "duty cycle" D_k:

$$D_k = \frac{1}{T_{sw,k}} \int_{kT_{sw}-T_{sw}}^{kT_{sw}} s(t)dt = \frac{t_{on,k}}{T_{sw,k}}, \tag{2-3}$$

where k is index – number of the switching cycle in their sequence since the beginning of the operation. Note that the D_k is rather function of this index, but not a time function (it is constant within the same switching cycle). Also it must be noted that the switching periods $T_{sw,k}$ are usually constant – the corresponding control mean is called Pulse-Width Modulation (PWM).

The duty cycle D_k is defined by the control system and its dynamic (real-time) calculation is not a subject of this course. However, the static definition of this parameter is directly related to the operation of corresponding converters and is discussed below.

2.1.3. Operation of Inductors and Capacitors in Quasi-Stationary Mode

The capacitors and inductors play two roles in the hard-switching converters – they serve either as filtering elements or as energy transferring elements. These elements may also have the third function – sometimes they serve as an energy sources: the capacitors – as voltage sources, but the inductors – as current sources.

The voltage across filtering capacitors and the current in the filtering chokes is almost constant with exception of low ripples (defined as an input parameter of the design). Therefore the energy of filtering elements is also almost constant.

In contrast, the voltage across energy transferring capacitors and current in the energy transferring inductors may vary significantly within a switching cycle. Operation of many switching converters is based on energy transfer through such elements.

In spite of their function there are certain rules of capacitors and inductor operation in the quasi-stationary mode. Understanding of these rules helps to develop the equations of static operation of electronic converters.

The main operation rule for capacitors (C) follows from the voltage equilibrium at the ends of the switching period $v(t)=v(t+T_{sw})$ then it is possible to compose the equation

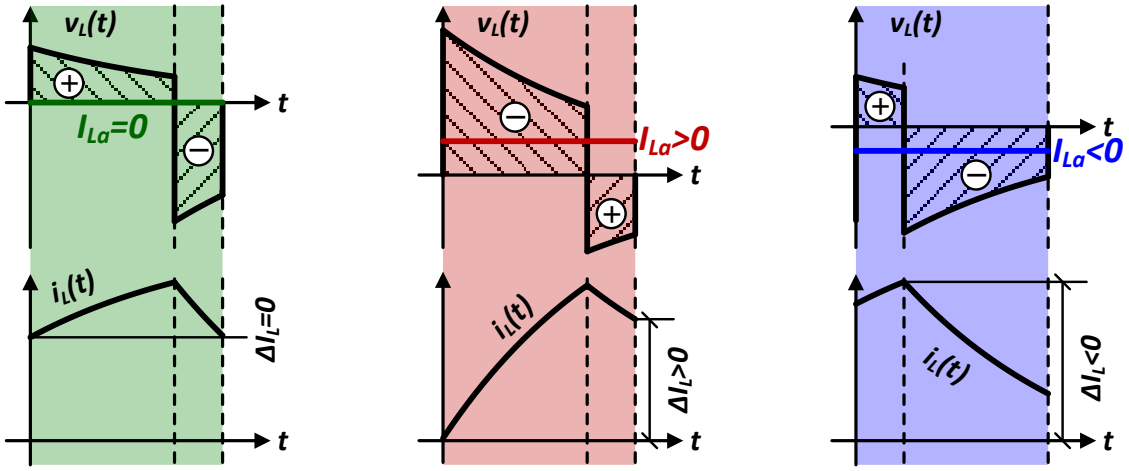
$$\Delta v_C = v_C(t+T_{sw}) - v_C(t) = \frac{1}{C}\int_0^{T_{sw}} i_C(t)dt = \frac{T_{sw}}{C}\cdot\frac{1}{T_{sw}}\int_0^{T_{sw}} i_C(t)dt = \frac{T_{sw}}{C}\cdot I_{Ca} = 0, \tag{2-4}$$

from which the main rule of capacitor follows – capacitor's average current in quasi-stationary mode is 0. In the similar way it is possible to prove that the average inductor's voltage in the quasi-stationary mode has also to be 0. Analytically it is written as

$$I_{Ca} = \frac{1}{T_{sw}}\int_0^{T_{sw}} i_C(t)dt = 0 \text{ and} \tag{2-5}$$

$$V_{La} = \frac{1}{T_{sw}}\int_0^{T_{sw}} v_L(t)dt = 0. \tag{2-6}$$

(2-5) and (2-6) themselves or (2-5) in conjunction with Kirchhoff's current law or (2-6) in conjunction with Kirchhoff's voltage law significantly simplify the calculation of other averaged parameters.



(a) (b) (c)

Fig. 2.3. Voltage balance across inductor: zero – final current is the same (a), positive – final current is higher (b), negative – final current is lower (c)

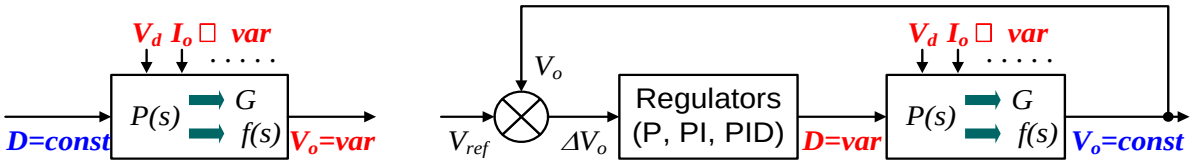
Fig. 2.3. reveals the details of the voltage balance across the inductor. Fig. 2.3.(a) presents the balanced inductor operation. In this case the square of the positive voltage pulse is equal to the square of negative. Therefore, the average value of the voltage is 0. In this case the current increase corresponding to the positive pulse is fully compensated by the current decrease caused by the negative. So, the inductor current at the beginning of the period is the same like at the end.

In contrast, in Fig. 2.3.(b) and Fig. 2.3.(c) unbalanced occasions are given. Fig. 2.3.(b) shows the occasion when the positive pulse is more valuable. Then the average voltage is positive, current increasing is more intensive and inductor's current at the end is higher. Fig. 2.3.(c) presents the case when the negative pulse is larger. It corresponds to the negative average voltage, weaker current increase and lower inductor's current at the end.

2.1.4. Open and Closed Loop Operation

The logic and order of analysis of power converters depend a lot on the system configuration. If it is an open loop system – a system without feedbacks - shown in Fig. 2.4.(a), then the aim of the analysis is to find the reaction of the system on the parameter changes when the main regulation variable – duty cycle remains constant. In this case the output characteristic $V_o=f(D)$ and load characteristic $V_o=f(I_o)$ are constructed and investigated.

Another occasion – is a closed-loop system with a voltage feedback, Fig. 2.4.(b). The output voltage in such systems is kept constant by means of the wise real-time modification of the duty cycle. Then the regulation characteristic $D=f(V_d)$ and stabilization characteristic $D=f(I_o)$ are analyzed.



(a) (b)

Fig. 2.4. Open (a) and closed (b) loop configuration of DC/DC converters

2.1.5. Types of DC/DC Converters

It is possible to split the hard-switching DC/DC voltage converters in two groups: converters with energy transferring inductor (transformer) and converters = switching circuits + filters. The first group consists of such converters as classic buck (step-down), boost (step-up), buck/boost (step-up/step-down), Chuk, SEPIC and Zeta. The second group includes, for example, bridge and half-bridge circuits, as well as, again, buck converter. The following section of this chapter reveals the detail of operation of these converters.

2.2. DC/DC converters with energy transferring magnetic element

2.2.1. Genesis of basic DC/DC converters with energy transferring inductor

As it was shown in the previous section the average voltage across inductors in the quasi-stationary mode is 0. At the same time their current may vary in a wide range. If within some time period an inductor is connected to a positive voltage (direct current path) like in Fig. 2.3..(a), its current will rise from I_{Lmin} to I_{Lmax} , but its energy – as:

$$E_{L\min} = \frac{L \cdot I_{L\min}^2}{2} \Rightarrow E_{L\max} = \frac{L \cdot I_{L\max}^2}{2}. \qquad (2\text{-}7)$$

Then it is possible to say that the inductor is charged from the positive voltage source. Then if the inductor is attached to a negative voltage (freewiling current path often provided by diodes), like in Fig. 2.3..(b), its current will drop from I_{Lmax} to I_{Lmin} and energy will decrease as

$$E_{L\max} = \frac{L \cdot I_{L\max}^2}{2} \Rightarrow E_{L\min} = \frac{L \cdot I_{L\min}^2}{2}. \qquad (2\text{-}8)$$

It means that the inductor is being discharged to the second voltage source. The difference of energy

$$\Delta E = E_{L\max} - E_{L\min} \qquad (2\text{-}9)$$

is transferred from the first source (input) to the inductor during the first stage and from the inductor to the second source (output) during the second stage. This process is regarded here as energy transmission through the energy transferring inductor. Here the voltage across the inductor consists of positive and negative pulses of the same square, Fig. 2.3.(c), but the

current – is triangular, Fig. 2.3.(d). The converter power (P_{conv}) depends on the commutation frequency and can be expressed as:

$$P_d = P_{conv} = \left(E_{L\max} - E_{L\min}\right) \cdot f_{sw} = \left(E_{L\max} - E_{L\min}\right) / T_{sw} = P_o \ . \qquad (2\text{-}10)$$

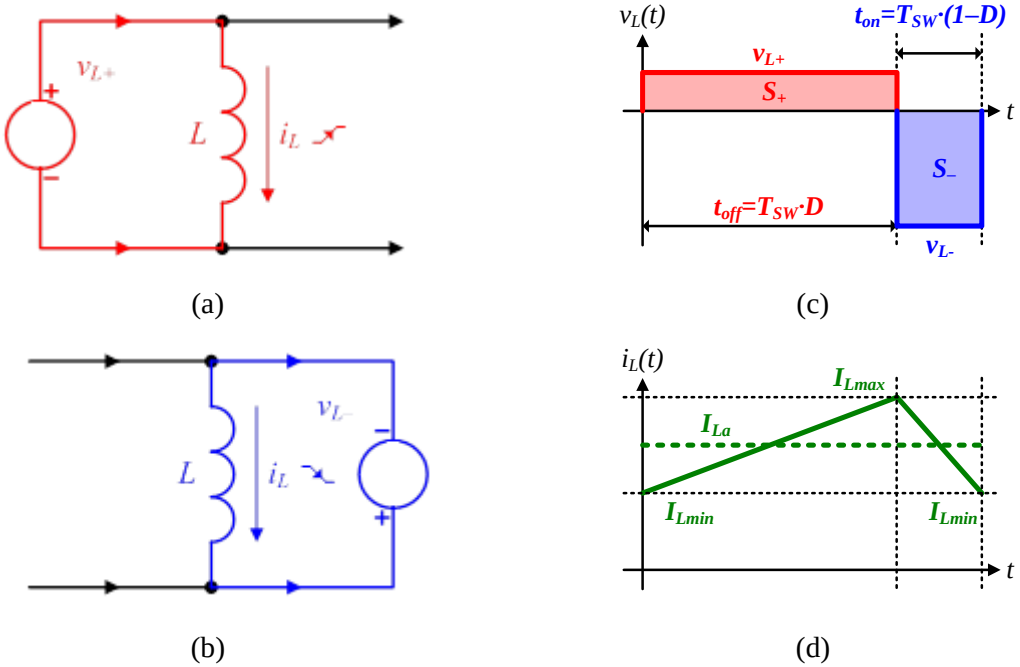
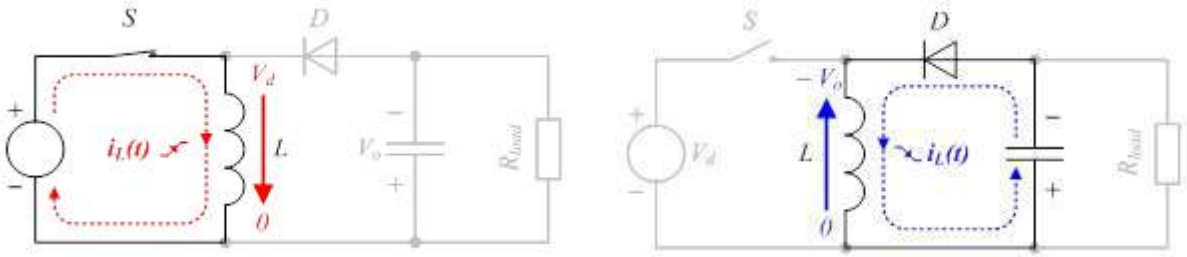


Fig. 2.5. Typical operation cycle of converter with energy transferring choke: positive voltage is applied (a), negative voltage is applied (b), operation voltage (c), operation current (d)

Applying input and output voltages directly

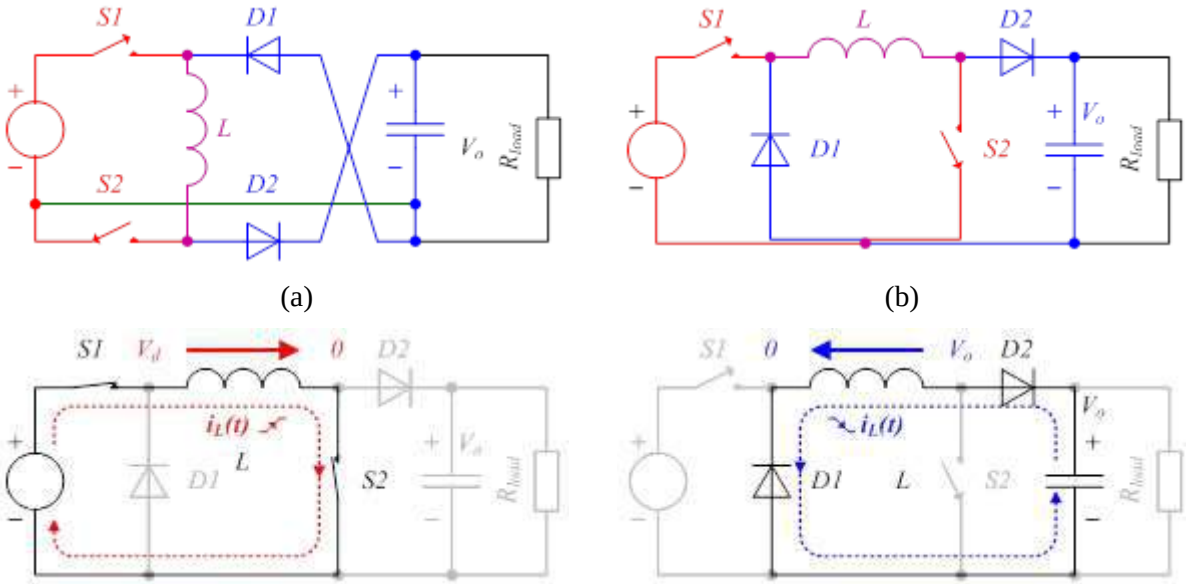
The direct implementation of the above described principle forms a switch mode converter known as inverting buck/boost (step-up/step-down). Since in this circuit the input voltage and output voltages are applied to the inductor one by one directly there is no theoretical limitation on their values – they may be equal or one of them may be higher – zero voltage balance can be achieved by means of the correct choice of pulse lengths (duty cycle). On the other hand the output voltage has to be negative.

This approach may be implemented also with positive output voltage. The positive input voltage can be applied as previously, red path in Fig. 2.7.(a). Then, since the second pulse across the inductor has to be negative, the positive output voltage has to be applied in reverse direction – blue path in Fig. 2.7.(a). Finally, grounds of two sources are connected - green wire in Fig. 2.7.(a). The obtained converter, known as non-inverting buck/boost, is given in Fig. 2.7.(b). Note that it has 2 switches in each current path. The forming of the direct current path is explained in Fig. 2.7.(c), but the configuration of the free wiling path is shown in Fig. 2.7.(d).



(a) (b)

Fig. 2.6. Direct commutation of the input and output voltages – synthesis of inverting buck/boost converter: positive input voltage is directly applied (a), negative output voltage is directly applied (b)



(c) (d)

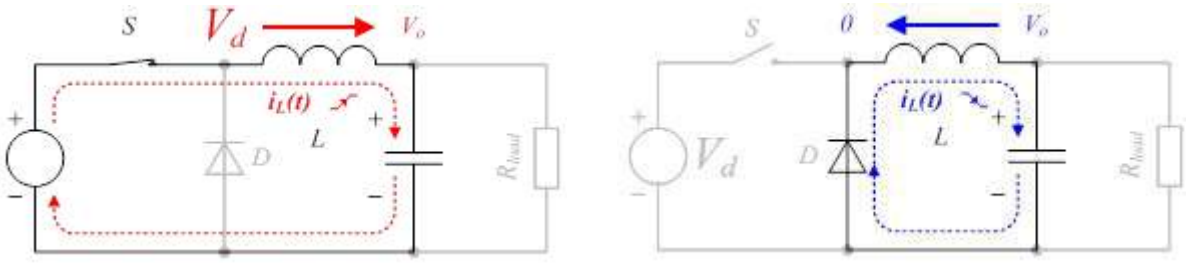
Fig. 2.7. Direct commutation in non-inverting buck/boost converter: the input is applied directly (red) (a), the output – reversely (blue), grounds are connected (green), common view (the same colours) (b), positive input is directly applied (c), positive output is reversely applied (d)

Applying voltage differences

It is possible to form the voltage pulses across the inductor not only applying input/output voltages directly, but also utilizing voltage differences. This opportunity, however, is available only if the fact which of the voltages is higher is known. It is also important to provide (in average) the flowing-out current of the input source, as well as flowing-in current of the output source (otherwise the power is not transferred from the input to the output). If these conditions are fulfilled a circuit which applies the difference in correct direction can be synthesized utilizing a set of formal rules: 1) positive charging voltage pulse is applied through a couple of controllable switches; 2) negative discharging voltage pulse is applied through a couple of diodes; 3) parallel switches can be substituted with a short-circuit.

If the value of the input voltage is higher than those of the output, the difference of input and output voltages is positive, but of output and input – negative. One opportunity assumes obtaining the positive voltage pulse across the inductor (charging pulse) as a difference of input and lower output voltages – Fig. 2.8.(a). The current in such loop flows from the input source through the inductor to the output. The negative (discharging) voltage pulse can be

obtained as the output voltage applied in the reverse direction – Fig. 2.8. (b). Then it is possible to connect one terminal of the inductor to the lower output voltage, but the second – toggle between the input voltage and ground. The corresponding switching circuit is known as buck (step-down) converter due to its natural feature to decrease voltage. There are other combinations of such voltages (**Table 2-1**), but most of them are either the circuits already known or those that have reverse biased electronic switches on their input that makes the forward current flow impossible.

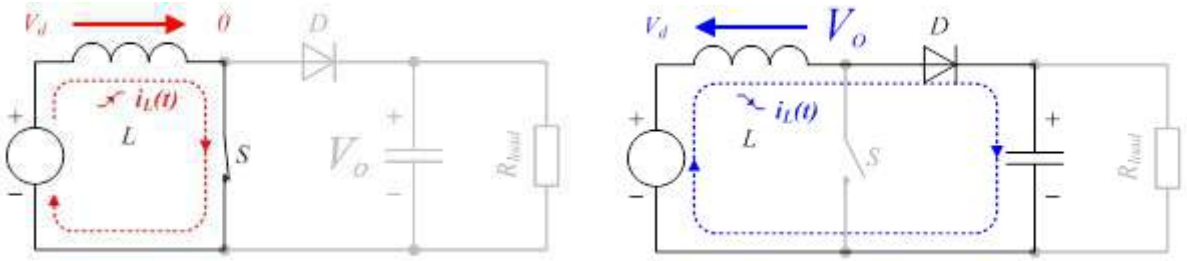


(a) (b)

Fig. 2.8. Synthesis of buck converter: positive difference of higher input and lower output voltage is directly applied (a), positive output voltage is reversely applied (b)

Table 2-1. Possible voltages across inductor if input voltage is higher

v_{L+}	v_{L-}	**Remarks**
V_d	$-(V_d - V_o)$	Circuit with limited functionality
V_d	$-V_o$	Non-inverting buck/boost converter
$V_d - V_o$	$-V_d$	Circuit with limited functionality
$V_d - V_o$	$-V_o$	Buck converter (Fig. 2.8)
V_o	$-V_d$	Reversed non-inverting b/b converter – no forward current flow possible
V_o	$-(V_d - V_o)$	Reversed boost converter – no forward current flow possible



(a) (b)

Fig. 2.9. Synthesis of boost converter: positive output voltage is directly applied (a), positive difference of higher output and lower input voltage is reversely applied (b)

Another occasion – the output voltage is higher than the input. Then the difference of input and output voltages is negative, but that of output and input – positive. One of the circuits with flowing-out input current is based on forming the positive voltage pulse across the inductor (charging pulse) applying the input voltage directly – Fig. 2.9.(a), but the negative pulse (discharging) – applying the difference of lower input and higher output voltages – Fig. 2.9.(b). Then the first terminal of the inductor can be connected to the input source, but the second – toggled between the output and ground. The obtained switch-mode converter given in Fig. 2.9 is known as boost or step-up, due to its feature to increase the voltage. Again, most

of the other combinations of voltages (**Table 2-2**) produce either known schematics or the converters that cannot operate.

Table 2-2. Possible voltages across inductor if input voltage is lower

v_{L+}	v_{L-}	**Remarks**
V_d	$-(V_o - V_d)$	Boost converter (Fig. 2.9.)
V_d	$-V_o$	Non-inverting buck/boost converter
$V_o - V_d$	$-V_d$	Reversed buck converter – no forward current flow possible
$V_o - V_d$	$-V_o$	No forward current flow possible
V_o	$-V_d$	Reversed non-inverting b/b converter – no forward current flow possible
V_o	$-(V_o - V_d)$	Circuit with limited functionality

2.2.2. Static operation of DC/DC converters with energy transferring inductor

Static operation of DC/DC converters is their operation in quasi-stationary mode. In this mode the instantaneous functions of converter's variables are periodical. This makes their description possible with the corresponding average values as well. At the same time, the most important element of these converters is their energy transferring inductor. That is why the average voltage and current equations for this inductor in fact describes the operation of the converter and are the most important during the analysis.

The main target during this analysis is the output voltage as a function of the duty cycle and output current. The other significant parameters of the discussed converters are output voltage, input current, voltages and currents of electronic switches, as well as those of the output capacitor.

There are two basic modes of operation of the DC/DC converters with energy transferring inductor identified by the current pattern in the time domain: continuous conduction mode and discontinuous mode of the inductor current.

In both modes the positive voltage is applied to the inductor when the switch of the converter is on (time interval t_{on}), but negative – when the diode is on (switch is off - time interval t_{off}). Then the voltage balance across the inductor can be defined as:

$$V_{La} = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_L(t)dt = \frac{S_+ + S_-}{T_{sw}} = 0 \quad \Rightarrow \quad S_+ + S_- = v_{L+} \cdot t_{on} + v_{L-} \cdot t_{off} = 0. \qquad (2\text{-}11)$$

This balance remains the same for both modes, but the definition of positive ($S_+ = v_{L+} \cdot t_{on}$) and negative ($S_- = v_{L-} \cdot t_{off}$) components of the definite integral in (2-11) is different.

Output voltage in continuous conduction mode

In the Continuous Conduction Mode (CCM) the current of energy transferring inductor is always higher than 0 (Fig. 2.5.). That is why $t_{on} + t_{off} = T_{sw}$ that, with $t_{on} = D \cdot T_{sw}$, forms $t_{off} = (1 - D) \cdot T_{sw}$. The voltages in ($S_+ = v_{L+} \cdot t_{on}$) and negative ($S_- = v_{L-} \cdot t_{off}$) are defined by switch state in the particular converter for the given phase of operation. These voltages are summarized in

Table **2-3**.

Table 2-3. Voltages across inductor in voltage converters

Converter	v_{L+}	v_{L-}
Buck	$V_d - V_o$	$-V_o$
Boost	V_d	$-(V_o - V_d)$
Inverting Buck/Boost	V_d	V_o
Non-inverting Buck/Boost	V_d	$-V_o$

The values from

Table **2-3** placed in (2-11) for the buck converter gives the balance equation

$$S_+ + S_- = (V_d - V_o) \cdot T_{sw} \cdot D + (-V_o) \cdot T_{sw} \cdot (1-D) = 0$$

which after simplification can be transformed to

$$V_o = V_d \cdot D. \tag{2-12}$$

The same procedure for the boost converter gives

$$S_+ + S_- = V_d \cdot T_{sw} \cdot D + (-(V_o - V_d)) \cdot T_{sw} \cdot (1-D) = 0$$

or

$$V_o = \frac{V_d}{1-D}. \tag{2-13}$$

In turn, for inverting buck/boost converter the voltage balance looks as

$$S_+ + S_- = V_d \cdot T_{sw} \cdot D + V_o \cdot T_{sw} \cdot (1-D) = 0$$

or

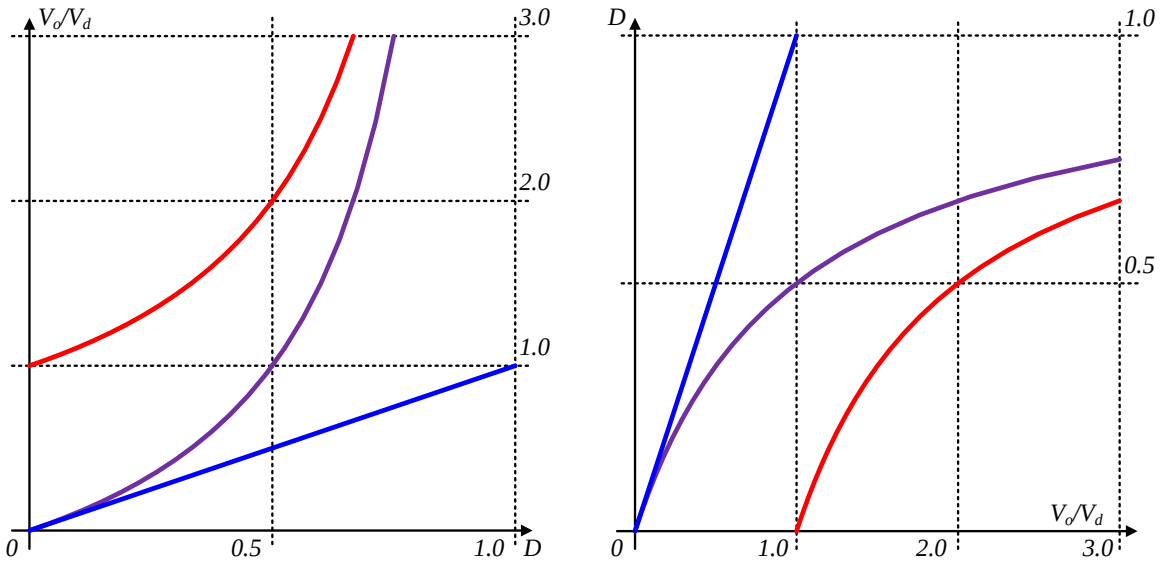
$$V_o = -\frac{V_d \cdot D}{1-D}. \tag{2-14}$$

The equation of non-inverting buck/boost converter differs only in sign and looks as

$$V_o = \frac{V_d \cdot D}{1-D}. \tag{2-15}$$

The equations (2-13)…(2-15) show that in the discontinuous conduction mode the output voltages of the converters do not depend on their output currents. This conclusion, of course, is valid only if internal resistances of switches, inductor and capacitor are ignored – only then the equations (2-5), (2-6), (2-10) and (2-11) can be used.

Therefore the output curve [functional dependence of the output voltage on the duty cycle $V_o=f(D)$, Fig. 2.10.(a)] and regulation curve [functional dependence of the duty cycle on the output voltage $D=f(V_o)$, Fig. 2.10.(b)] of the converters can be drawn utilizing equations (2-13)…(2-15). At the same time the load curves [output voltage vs. output current $V_o=f(I_o)$] and stabilization curves [duty cycle necessary for a constant output voltage vs. output current $D=f(I_o)$] are horizontal lines.



(a) (b)

Fig. 2.10. Output (a) and regulation (b) curves of buck (blue), boost (red) and buck/boost (magenta) voltage converters

Input, output and internal currents

The key element of the basic DC/DC converters is their inductor. On one hand its voltage balance allows to define the output voltage, but on the other – its current helps to determine other currents of the converter.

Since it is assumed that there are no internal resistances in the inductor and switches the current of inductor can be described as triangular – Fig. 2.11.(a). Its rising part is conducted by the controllable switch of the converter – Fig. 2.11.(b), but its falling part – flows through converter's diode – Fig. 2.11.(c). These current ripples in CM can be expressed as

$$\Delta I_{La} = \frac{1}{L}\int_0^{t_{on}} v_{L+}dt = -\frac{1}{L}\int_0^{t_{off}} v_{L-}dt = \frac{v_{L+}\cdot D\cdot T_{sw}}{L} = -\frac{v_{L-}\cdot(1-D)\cdot T_{sw}}{L}, \tag{2-16}$$

which, taking into account (2-12), gives for buck converter

$$\Delta I_{La\_buck} = \frac{(V_d - V_o)\cdot D\cdot T_{sw}}{L} = \frac{V_d\cdot(1-D)\cdot D\cdot T_{sw}}{L} = \frac{V_o\cdot(1-D)\cdot T_{sw}}{L}, \tag{2-17}$$

applying (2-13) for boost gives

$$\Delta I_{La\_boost} = \frac{V_d\cdot D\cdot T_{sw}}{L} = \frac{(V_o - V_d)\cdot T_{sw}}{L} = \frac{V_o\cdot D\cdot(1-D)\cdot T_{sw}}{L}, \tag{2-18}$$

but utilizing (2-15) for buck/boost converter produces

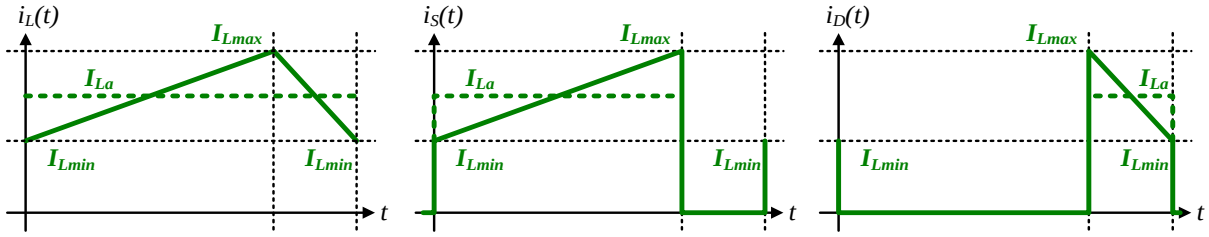
$$\Delta I_{La\_bb} = \frac{V_d\cdot D\cdot T_{sw}}{L} = \frac{V_o\cdot(1-D)\cdot T_{sw}}{L}. \tag{2-19}$$

In turn, the average value of inductor current depends on the load current: in the buck converter it is of the same value, in boost converter – it can be expressed from the power balance (2-2) and static voltage expression (2-13), but in the buck/boost converters – it is a

sum of input and output currents which can be found based on (2-2) and (2-14)/(2-15) – see Table 2-4.

Table 2-4. Input and output currents of basic DC/DC converters

Converter	I_{La}	I_d	I_o
Buck	I_o	I_{VT}	I_L
Boost	$I_o/(1-D)$	I_L	I_{VD}
Inverting Buck/Boost	$I_o/(1-D)$	I_{VT}	I_{VD}
Non-inverting Buck/Boost	$I_o/(1-D)$	I_{VT}	I_{VD}



(a) (b) (c)

Fig. 2.11. Currents of basic DC/DC converters: inductor current (a), transistor current (b), diode current (c)

Fig. 2.11 shows that the current of inductor is distributed between the switch and diode of the converter. Its average value, which can be found as

$$I_{La} = \frac{1}{T_{SW}}\left[\int_0^{t_{on}}\left(I_{\min} + \frac{\Delta I}{t_{on}}\cdot t\right)dt + \int_{t_{on}}^{t_{on}+t_{off}}\left(I_{\max} - \frac{\Delta I}{t_{off}}\cdot(t-t_{on})\right)dt\right] = \frac{I_{\max}+I_{\min}}{2} \qquad (2\text{-}20)$$

can also be "distributed" between controllable switch

$$I_{Sa} = \frac{1}{T_{SW}}\int_0^{t_{on}}\left(I_{\min} + \frac{\Delta I}{t_{on}}\cdot t\right)dt = \frac{I_{\max}+I_{\min}}{2}\cdot D = I_{La}\cdot D \qquad (2\text{-}21)$$

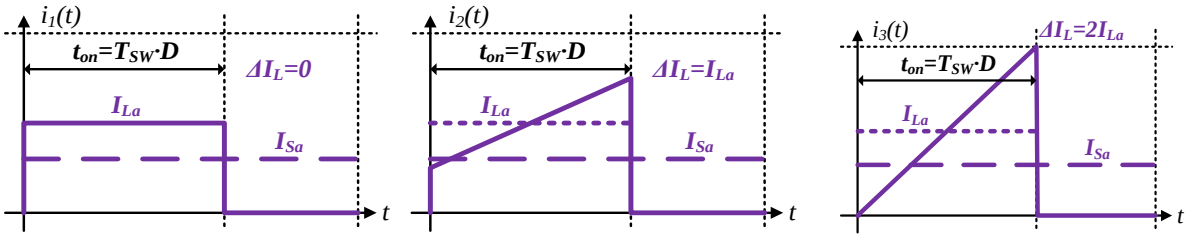
and diode

$$I_{Da} = \frac{1}{T_{SW}}\int_{t_{on}}^{t_{on}+t_{off}}\left(I_{\max} - \frac{\Delta I}{t_{off}}\cdot(t-t_{off})\right)dt\,.$$

The last equation in CCM produces

$$I_{Da} = \frac{I_{\max}+I_{\min}}{2}\cdot(1-D) = I_{La}\cdot(1-D)\,. \qquad (2\text{-}22)$$

One more significant parameter is root-mean square (rms) value of converter's currents. In particular, this parameter is useful for power loss calculation and it is required for the choice of power semiconductor switches. This parameter depends a lot on the ripples of the analyzed current (or voltage). Fig. 2.12. shows three different shapes of the transistor current.



(a) (b) (c)

Fig. 2.12. Currents of the same average value: pulse (a), trapezoidal (b), triangular (c)

The last one, saw-tooth shown in Fig. 2.12.(c), obviously has higher value of the ripples. It is also possible to prove that this shape has the maximal rms value, which can be expressed as

$$I_{Srms\_\max} = \sqrt{\frac{1}{T_{SW}}\int_0^{t_{on}}\left(\frac{\Delta I}{t_{on}}t\right)^2 dt} = \sqrt{\frac{1}{T_{SW}}\int_0^{D\cdot T_{SW}}\left(\frac{2\cdot I_{La}}{D\cdot T_{SW}}t\right)^2 dt} = \sqrt{\frac{3}{4}}\cdot I_{La}\sqrt{D} = 1.15\cdot I_{La}\sqrt{D}. \quad (2\text{-}23)$$

In the same way it can be shown that

$$I_{Drms\_\max} = \sqrt{\frac{3}{4}}\cdot I_{La}\sqrt{1-D} = 1.15\cdot I_{La}\sqrt{1-D}. \quad (2\text{-}24)$$

Note that (2-23) and (2-24) produces the result, which is not exact rms value of any current shape, but reflects the "worst case", which is useful for the choice of semiconductor elements.

Open-circuit and short-circuit

Before discussing DCM it is worth to take a look at short-circuit and at open-circuit (no-load) operation of the discussed converters. The first configuration is important for understanding of safety of the converter, but the second one – is the most explicit occasion of DCM.

Analysis of the converters shows two types of short-circuits. In buck (Fig. 2.13.) and buck/boost (Fig. 2.15.) converters global short-circuit occurs only if the controllable switch is turned on. Moreover, in the buck/boost converter it is rated operation. If inductor's current in these converters can be measured quite quickly, but the switch – turned off, it is possible to avoid damage of the converter due to catastrophic over-current.

In contrast short-circuit of the boost converter Fig. 2.14.(a) occurs as soon as its output terminals are connected. If there are no extra protection elements on its input, the converter will be damaged.

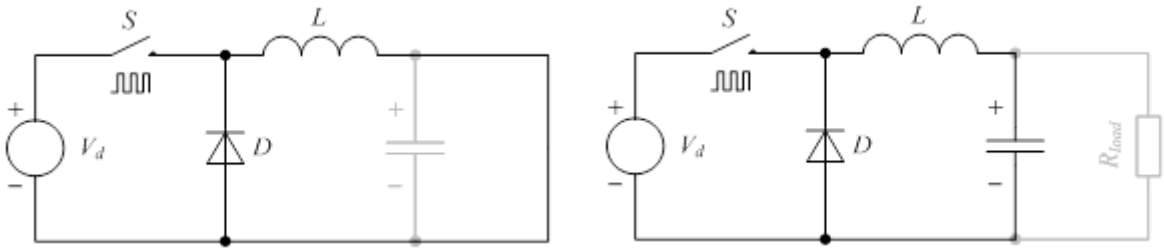
No-load operation of basic DC/DC converters also occurs in two ways. No-load operation of the buck converter – Fig. 2.13.(b) – can be described by differential equations

$$V_d = L\cdot\frac{di(t)}{dt} + v_C(t) \text{ and } i(t) = C\cdot\frac{v_C(t)}{dt}, \quad (2\text{-}25)$$

which, at zero initial conditions has solution

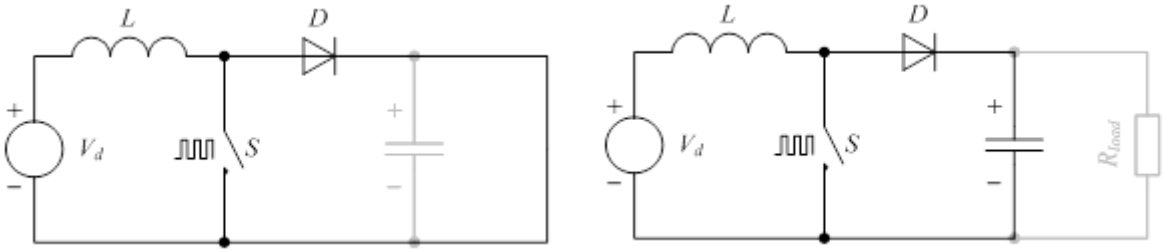
$$v_C(t) = V_d - V_d\cdot\cos(\omega t), \quad (2\text{-}26)$$

where $\omega = 1/\sqrt{LC}$. If the time is sufficient (when the switch is continuously on) the voltage across capacitor achieves the value $2V_d$.



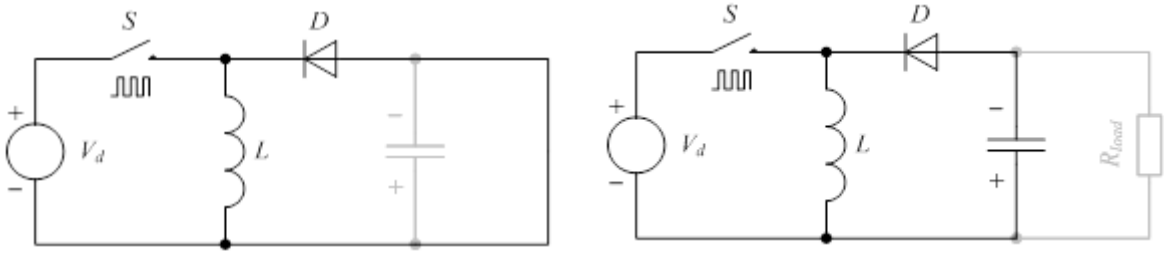
(a) (b)

Fig. 2.13. Short-circuit (a) and no-load [(b) diagrams of buck converter



(a) (b)

Fig. 2.14. Short-circuit (a) and no-load (b) diagrams of boost converter



(a) (b)

Fig. 2.15. Short-circuit (a) and no-load (b) diagrams of buck/boost converter

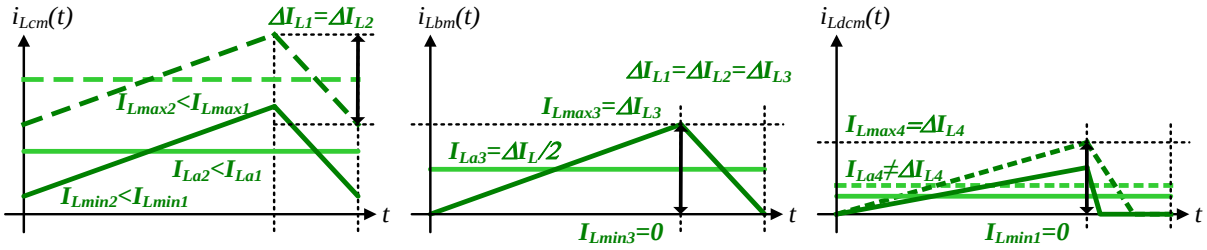
It can be said that charge process of the inductor in the buck converter is limited with the difference of input and output voltages and cannot be infinite. Then, if the switch is not continuously on, but turned on and off at commutation frequency, the voltage across capacitor in steady state mode just slightly exceeds value V_d.

In contrast in the boost – Fig. 2.14.(b) – and buck/boost –Fig. 2.15.(b) converters the inductor is charged directly from the input. This may occur at any output voltage which can rise infinitely at no load. Therefore in these converters the output voltage has to be measured and switch operation has to be disabled at the critical value of this voltage.

Operation in boundary mode

The previously obtained equations of static operation (2-13)…(2-15) were composed for the occasion, when the inductor current never drop to zero value. However, the key points of this current (its maximum, minimum and average value) are moving down at lower load currents (moreover – in the buck converter load current is equal to the average value of

inductor current). In Fig. 2.16.(a) two occasions are presented – the dashed one corresponds to a higher load current than the solid one. Further load current decrease will lead to a working point, where inductor's current achieves zero value once (in one time instant) per period. This mode is called Boundary Conduction Mode (BCM), Fig. 2.16.(b).



(a) (b) (c)

Fig. 2.16. Inductor current in different operation modes: continuous (a), boundary (b) and discontinuous (c)

In the boundary mode the average value of current through the inductor is exactly half of its ripples

$$I_{La\_b} = \Delta I_L / 2,$$

which in conjunction with (2-17) and taking into account that for buck converter $I_{La}=I_o$ (Table 2-4) produces (for V_d=const)

$$I_{ob\_buck} = \frac{\Delta I_{La\_boost}}{2} = \frac{V_d \cdot T_{sw} \cdot (1-D) \cdot D}{2 \cdot L}, \tag{2-27}$$

which has maximum $I_{obm\_buck}=V_d \cdot T_{sw}/8 \cdot L$ at D=0.5 or (for V_o=const)

$$I_{ob\_buck} = \frac{V_o \cdot T_{sw} \cdot (1-D)}{2 \cdot L} \tag{2-28}$$

with maximum $I_{obm\_buck}=V_o \cdot T_{sw}/2 \cdot L$ at D=0.

For boost converter the similar equation is obtained from (2-18) and $I_o = I_{La} \cdot (1-D)$ (Table 2-4). For V_d=const it gives

$$I_{ob\_boost} = \frac{\Delta I_{La\_boost}}{2} \cdot (1-D) = \frac{V_d \cdot T_{sw} \cdot D \cdot (1-D)}{2 \cdot L} \tag{2-29}$$

with maximum $I_{obm\_buck}=V_d \cdot T_{sw}/8 \cdot L$ at D=0.5, but for V_o=const –

$$I_{ob\_boost} = \frac{V_o \cdot T_{sw} \cdot D \cdot (1-D)^2}{2 \cdot L} \tag{2-30}$$

with maximum $I_{obm\_buck}= 2 \cdot V_o \cdot T_{sw}/27 \cdot L$ at D=1/3.

In turn, for buck/boost the corresponding equations of boundary current follows from (2-19). For V_d=const this equation is the following

$$I_{ob\_bb} = \frac{\Delta I_{La\_bb}}{2} \cdot (1-D) = \frac{V_d \cdot T_{sw} \cdot D \cdot (1-D)}{2 \cdot L} \tag{2-31}$$

and has maximum $I_{obm\_buck}=V_d \cdot T_{sw}/8 \cdot L$ at D=0.5, but for V_o=const –

$$I_{ob\_bb} = \frac{V_o \cdot (1-D)^2 \cdot T_{sw}}{2 \cdot L} \tag{2-32}$$

with maximum $I_{obm\_buck}= V_o \cdot T_{sw}/2 \cdot L$ at D=0.

Output voltage in discontinuous conduction mode

Further (compared with BCM) reduction of the load current leads to a mode in which inductor's current achieves zero value and remains at zero level for some time. This mode is entitled Discontinuous Conduction Mode (DCM). In DCM, due to the zero current interval $t_{on}+t_{off}<T_{sw}$ at equations (2-12)…(2-15) are not valid. At the same time the rule of voltage balance across the inductor remains valid and produces an equation where $t_{off}=\delta \cdot T_{sw}$ (δ is diode on-time expressed in relative units) is unknown. Since the voltage balance equation contains two unknown variables another equation has to be composed in order to achieve a solvable system. This equation can be formed basing on the current balance of the output capacitor which says that the load current is equal to inductor's current (buck) or diode current (boost and buck/boost). Let us apply these rules to the basic converter schemes.

For the buck converter inductor's voltage balance looks as

$$S_+ = (V_d - V_o) \cdot D \cdot T_{sw} = S_- = V_o \cdot \delta \cdot T_{sw},$$

but capacitor's current balance – as

$$I_o = I_{La} = \frac{\Delta I_L}{2} \cdot (D+\delta) = \frac{(V_d - V_o) \cdot T_{SW} \cdot D}{L} \cdot \frac{1}{2} \cdot (D+\delta).$$

Excluding δ from these equations produces

$$I_o = \frac{(V_d - V_o) \cdot T_{SW} \cdot D}{L} \cdot \frac{1}{2} \cdot \left(D + \frac{(V_d - V_0) \cdot D}{V_0} \right),$$

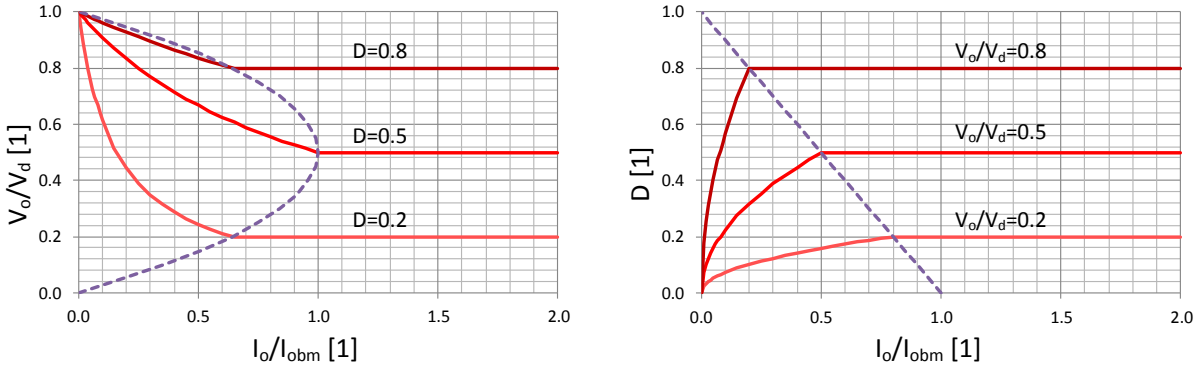
which can be rearranged extracting the output voltage

$$\frac{V_o}{V_d} = \frac{4 \cdot D^2}{I_o / [V_d \cdot T_{sw} / 8L] + 4 \cdot D^2} \tag{2-33}$$

or extracting the duty cycle

$$D = \sqrt{\frac{(I_o / [V_o \cdot T_{sw} / 2L]) \cdot (V_o / V_d)^2}{1 - V_o / V_d}}. \tag{2-34}$$

The corresponding load and stabilization characteristics of the buck converter constructed based on **(2-33)** and (2-34) are shown in Fig. 2.17.



(a) (b)

Fig. 2.17. Load (a) and stabilization (b) characteristics of buck converter in CCM and DCM

Similarly in the boost converter inductor's voltage balance

$$S_+ = V_d \cdot D \cdot T_{sw} = S_- = (V_o - V_d) \cdot \delta \cdot T_{sw}$$

and capacitor's current balance

$$I_o = \frac{V_d \cdot T_{SW} \cdot D}{L} \cdot \frac{1}{2} \cdot \delta$$

forms

$$V_d^2 \cdot D^2 \cdot T_{SW} + V_d \cdot I_o \cdot 2L - V_o \cdot I_o \cdot 2L = 0$$

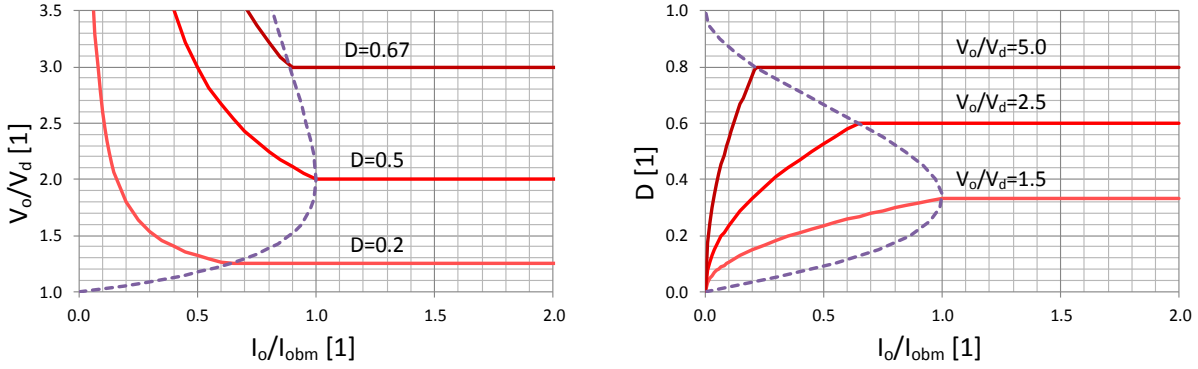
which can be represented as

$$\frac{V_o}{V_d} = 1 + \frac{4 \cdot D^2}{I_o / [V_d \cdot T_{sw} / 8L]} \tag{2-35}$$

or

$$D = \sqrt{\frac{4}{27} \cdot \frac{I_o}{[2V_o \cdot T_{sw} / 27L]} \cdot \left(\left(\frac{V_o}{V_d} \right)^2 - \frac{V_o}{V_d} \right)}. \tag{2-36}$$

(2-35) and (2-36) forms the following load and stabilization curves (Fig. 2.18.).



(a) (b)

Fig. 2.18. Load (a) and stabilization (b) characteristics of buck converter in CCM and DCM

Finally inductor's balance of the buck/boost (non-inverting) converter is even simpler than those of the boost

$$S_+ = V_d \cdot D \cdot T_{sw} = S_- = V_o \cdot \delta \cdot T_{sw}.$$

In turn, capacitor's current balance is the same as for the boost

$$I_o = \frac{V_d \cdot T_{SW} \cdot D}{L} \cdot \frac{1}{2} \cdot \delta.$$

Excluding δ gives

$$V_d^2 \cdot D^2 \cdot T_{SW} - V_o \cdot I_o \cdot 2L = 0$$

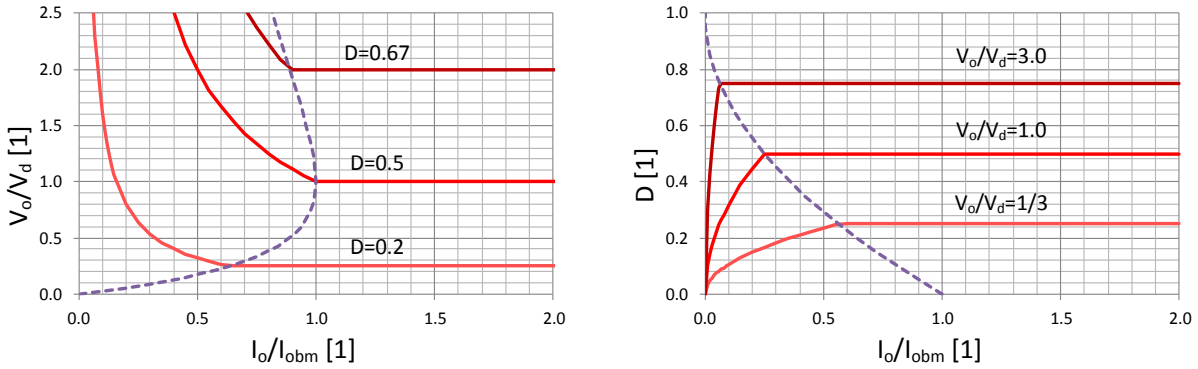
that can be rearranged as

$$\frac{V_o}{V_d} = \frac{4 \cdot D^2}{I_o / [V_d \cdot T_{sw} / 8L]} \tag{2-37}$$

or

$$D = \sqrt{\frac{I_o}{[V_o \cdot T_{sw} / 2L]} \cdot \left(\frac{V_o}{V_d}\right)^2}. \tag{2-38}$$

(2-37) and (2-38) forms the characteristics of the buck/boost converter presented in Fig. 2.19. It is seen that the out characteristics are the same just shifted by 1 that can be explained by the similarity of the input parts of the boost and buck/boost converters.



(a) (b)

Fig. 2.19. Load (a) and stabilization (b) characteristics of buck converter in CCM and DCM

The analysis of the equations **(2-33)** ... (2-38) and Fig. 2.17...Fig. 2.19 shows that in DCM operation point moves closer to those the open-circuit, which is described by the infinitely high output voltage in the boost and buck/boost converters and output-equal-to-input voltage in the buck converter. The corresponding desired value of the duty cycle in the closed loop system is 0.

It must be noted that the equations of the static operation of the converters in DCM could be extracted also from the power balance (2-10). Taking into account that in DCM $I_{Lmin}=0$ (2-10) can be recomposed as

$$E_{L\max} \cdot f_{sw} = \frac{L \cdot I_{L\max}^2}{2} \cdot \frac{1}{T_{sw}} = \frac{L \cdot \Delta I_L^2}{2} \cdot \frac{1}{T_{sw}} = P_o = V_o \cdot I_o.$$

Then applying of the particular voltages gives for the buck converter

$$\frac{L\cdot\left(\frac{(V_d - V_o)\cdot D\cdot T_{sw}}{L}\right)^2}{2}\cdot\frac{1}{T_{sw}} = V_o \cdot I_o{}'$$

but for the boost and buck/boost

$$\frac{L\cdot\left(\frac{V_d \cdot D\cdot T_{sw}}{L}\right)^2}{2}\cdot\frac{1}{T_{sw}} = V_o \cdot I_o{}'$$

which after some transformations gives equations **(2-33)**, (2-35) and (2-37).

Internal voltages and voltages across switches

Classical buck, boost and inverting buck-boost converters have one internal voltage in the mid-point of T-connection of the switch diode and inductor. In continuous conduction mode this point is tied either by the controllable switch or by diode to a voltage potential. The values of these voltage potentials depend on the converter and operation stage (Table 2-5). Applying these particular values produces the diagrams of the internal voltage shown in Fig. 2.20.

Table 2-5. Input and output currents of basic DC/DC converters

Converter	V_S	V_D	V_L
Buck	V_d	0	V_o
Boost	0	V_o	V_d
Inverting Buck/Boost	V_d	V_{o-}	0

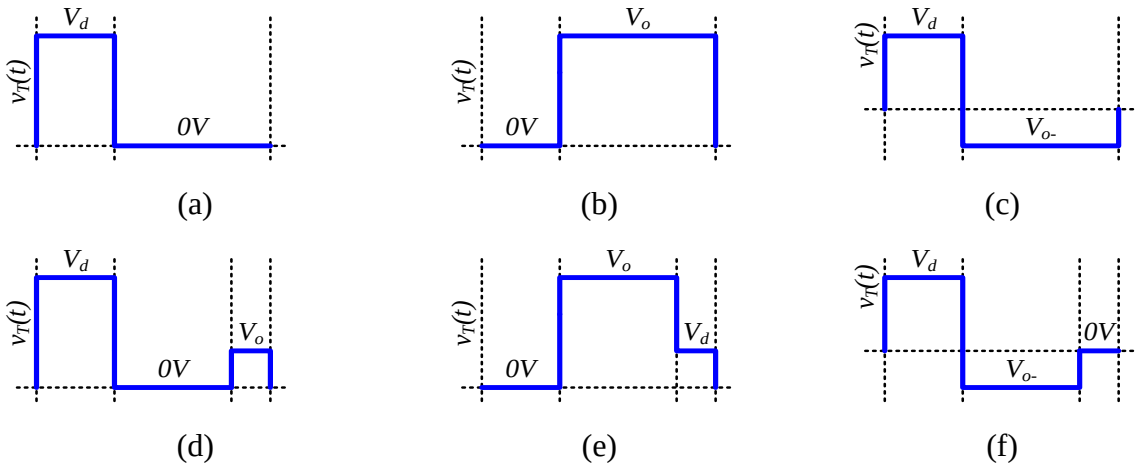


Fig. 2.20. Internal voltage (voltage of mid-point of T-connection) of DC/DC converters: buck (a) and (d), boost (b) and (e), buck/boost (c) and (f), discontinuous conduction mode (a, b, c), discontinuous conduction mode (d, e, f)

As soon as T-voltage is known the voltage across the switches can be found as a difference (Table 2-6) of the T-voltage and voltage of the second terminal of the switch which is either input voltage V_d, output voltage V_o or zero ground voltage. The time diagrams of instantaneous voltages are given in Fig. 2.21 and Fig. 2.22.

The maximal value of these voltages is of special importance because it allows choosing the transistor and switch (Table 2-6). Note that in the case of buck and bust converter this voltage is maximum from the input and output voltages, but in the case of buck/boost – their sum. Therefore, the buck/boost converter requires switches with higher operation voltage.

Table 2-6. Voltages across controllable switch and diode

Converter	V_S	V_{Smax}	V_D	V_{Dmax}
Buck	$V_d - v_T(t)$	$\boldsymbol{V_d}$	$0 - v_T(t)$	$\boldsymbol{-V_d}$
Boost	$v_T(t) - 0$	$\boldsymbol{V_o}$	$v_T(t) - V_o$	$\boldsymbol{-V_o}$
Inverting Buck/Boost	$V_d - v_T(t)$	$\boldsymbol{V_d - V_{o-}}$	$V_{o-} - v_T(t)$	$\boldsymbol{-(V_d - V_{o-})}$

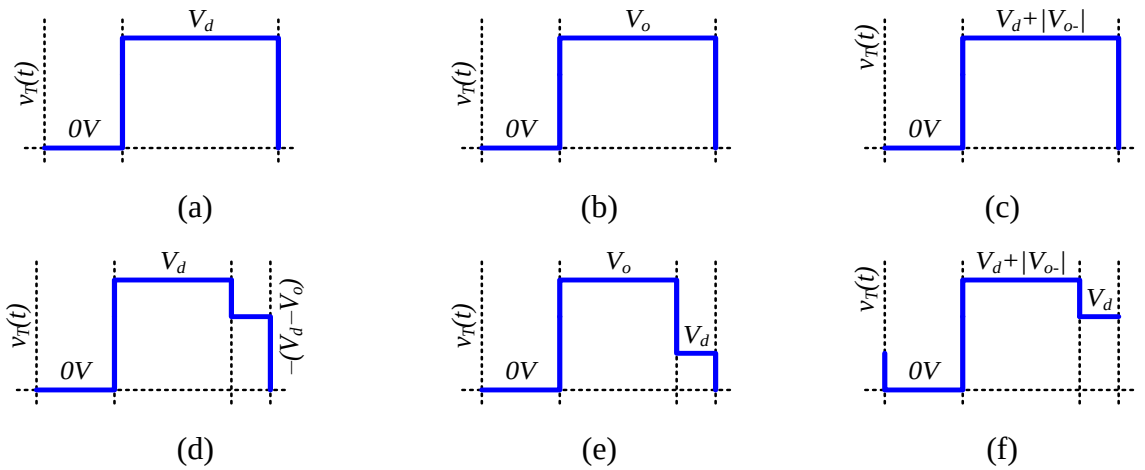


Fig. 2.21. Switch voltage of DC/DC converters: buck (a) and (d), boost (b) and (e), buck/boost (c) and (f), discontinuous conduction mode (a, b, c), discontinuous conduction mode (d, e, f)

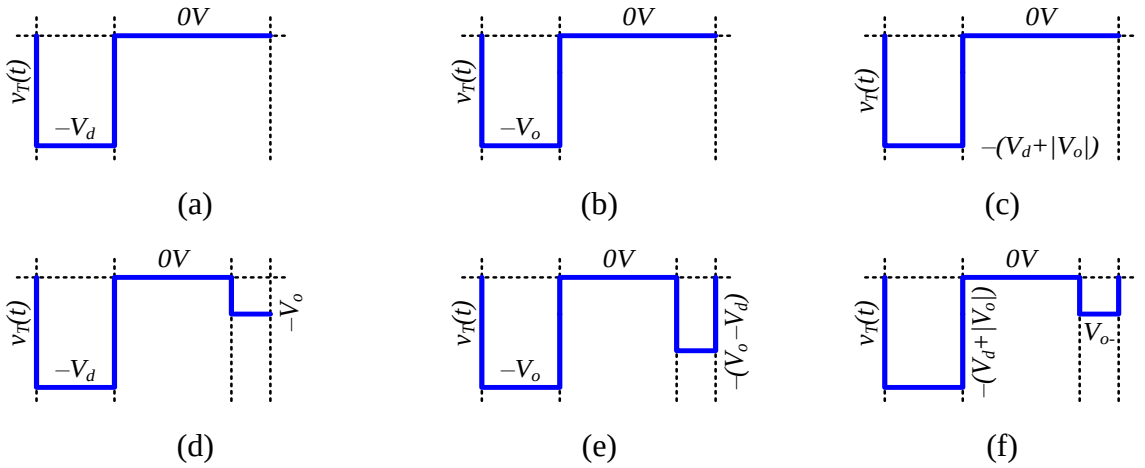


Fig. 2.22. Diode voltage of DC/DC converters: buck (a) and (d), boost (b) and (e), buck/boost (c) and (f), discontinuous conduction mode (a, b, c), discontinuous conduction mode (d, e, f)

Output voltage

In the previous section it is assumed that the output voltage is constant. This, however, is not entirely truth. The output voltage has little ripples the value of which directly depends on the output capacitor and topology of converter. There are two basic occasions. The output capacitor of the buck converter is charged/discharged by the difference of the triangular inductor current and constant output current, Fig. 2.23.(a) – green curve:

$$i_C(t) = i_L(t) - I_o .$$

When taking into account that I_{Ca}=0 it is possible to conclude that the time-current square between these two currents in the quasi-stationary mode must be zero or the positive part of this square is equal to the negative one. On the other hand, this square is a charge that, if transferred into the output capacitor, leads to its voltage increase, but if taken from the capacitor – leads to voltage decrease, Fig. 2.23.(a) – blue curve. This charge can be found based on geometrical considerations of the current, i.e. as

$$\Delta Q = \frac{1}{2} \cdot \frac{T_{sw}}{2} \cdot \frac{\Delta I_L}{2} = \frac{V_o \cdot (1-D) \cdot T_{sw}^2}{8L},$$

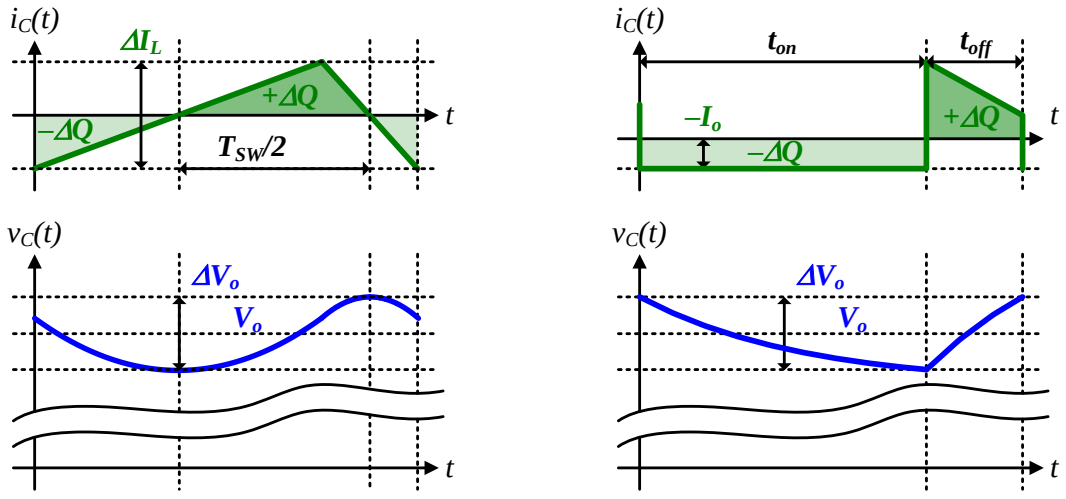
but the corresponding voltage changes as

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{V_o \cdot (1-D) \cdot T_{sw}^2}{8L} \cdot \frac{1}{C}.$$

If the combination of inductor and output capacitor is interpreted as a low-pass filter with cut-off frequency $f_C = 1/(2\pi \cdot \sqrt{LC})$, as well as taking into account that $f_{sw}=1/T_{sw}$ then it is possible to form the rule for the choice of the inductor and capacitor

$$\frac{\Delta V_{o\_max}}{V_o} \le \frac{(1-D) \cdot T_{sw}^2}{8LC} = \frac{\pi^2 \cdot (1-D)}{2} \cdot \frac{f_c^2}{f_{sw}^2}, \qquad (2\text{-}39)$$

where ΔV_{o_max} is maximal allowed value of the output voltage ripples.



(a) (b)

Fig. 2.23. Current (a) – positive output voltage is directly applied,
(b) positive difference of higher output and lower input voltage is reversely applied

Another occasion is charging/discharging of the output capacitor by the difference of the trapezoidal inductor current and constant output current (boost and buck/boost converter, Fig. 2.23.(b) – green curve)

$$i_C(t) = i_D(t) - I_o .$$

The principles of analysis in this case are the same. The charge is found based on geometrical consideration (as a rectangular square):

$$\Delta Q = t_{on} \cdot I_o = D \cdot T_{sw} \cdot I_o .$$

Then the voltage ripples can be found as

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{D \cdot T_{SW} \cdot I_o}{C} = D \cdot T_{SW} \cdot \frac{V_o}{R_{LOAD} \cdot C}.$$

Where from the rule of capacitor choice is

$$\frac{\Delta V_{o\_\max}}{V_o} \le D \cdot \frac{T_{SW}}{\tau}, \tag{2-40}$$

where $\tau = RC$ – time constant of the load.

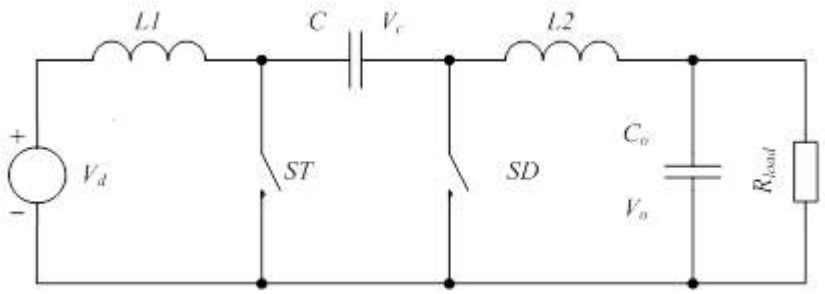
Equations (2-39) and (2-40) produces quite accurate result, but a "worst case analysis" also exists there. It assumes that the output capacitor is charged within infinitely short time, while its discharge occurs almost all switching period. Then, if the load current all the time is I_o the output voltage ripples can be found as

$$\Delta V_o = \frac{I_o \cdot T_{sw}}{C} \text{ where from } C \ge \frac{I_o \cdot T_{sw}}{\Delta V_{o\_\max}}. \tag{2-41}$$

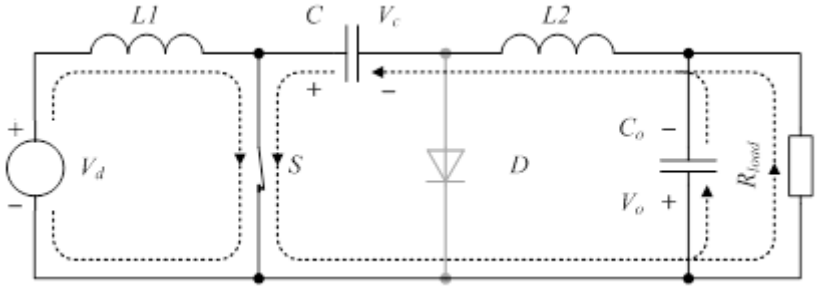
2.2.3. Chuk converter

There are three more converters with buck-boost functionality. Their operation is initially derived from the operation of the buck-boost of converter, but, at the same time, is characterized by certain attractive features. In addition, the analysis of these converters is interesting from the point of view how inductor's zero voltage low can be applied.

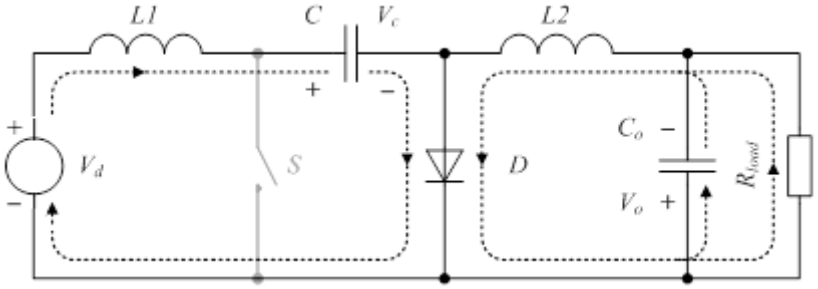
The first converter, named for its inventor, Slobodan Chuk, consists of a series of inductor, capacitor and one more inductor located between the input of the converter and its output (Fig. 2.244.). Either one or another internal connection of these elements is tied to the ground by means of electronic switches (the second one is typically a diode). This converter can be analyzed exactly as it was done previously, based on the zero voltage law of the inductors. Since there are two inductors in the circuit, two voltage equilibriums have to be written.



(a)



(b)



(c)

Fig. 2.24. Chuk converter: generalized schematic (a); switch is on (b); switch is off (c)

The first inductor is either tied to the positive voltage of input source, when the switch is on, or supplied with the negative difference of the input and internal capacitor's voltage, when the switch is off. Then the voltage equilibrium is the following

$$V_d \cdot D \cdot T_{SW} + (V_d - V_c) \cdot (1 - D) \cdot T_{SW} = 0$$

and, with respect to the voltage of internal capacitor, produces the static equation of boost converter

$$V_c = \frac{1}{1-D} \cdot V_d \qquad (2\text{-}42)$$

Similarly, the second inductor can be tied to the output voltage through the diode. For the possible polarities of the output voltage and current of the second inductor this is a discharging stage and indictor's current falls during this time interval. In turn, when the switch is on, the second inductor is placed between the output and internal capacitor. The corresponding voltage difference is then positive and charges the inductor. The correspondent voltage balance

$$(V_c + V_o) \cdot D \cdot T_{SW} + (V_o) \cdot (1 - D) \cdot T_{SW} = 0$$

produces a formula of buck converter with regard to the internal capacitor's and output voltage

$$V_o = -D \cdot V_c \ . \qquad (2\text{-}43)$$

Combining (2-42) and (2-43) express the output voltage as a function of the duty cycle and input voltage exactly as for classical buck/boost converter.

The polarity of the output voltage of Chuk converter is also negative, but both the input and the output currents are formed in inductors reducing the value of the output capacitor and facilitating the use of Chuk converter with current sensitive sources like photovoltaic and fuel

cells. Also Chuk converter is output short-circuit proof because the input is connected to the output through a series capacitor.

2.2.4. SEPIC converter

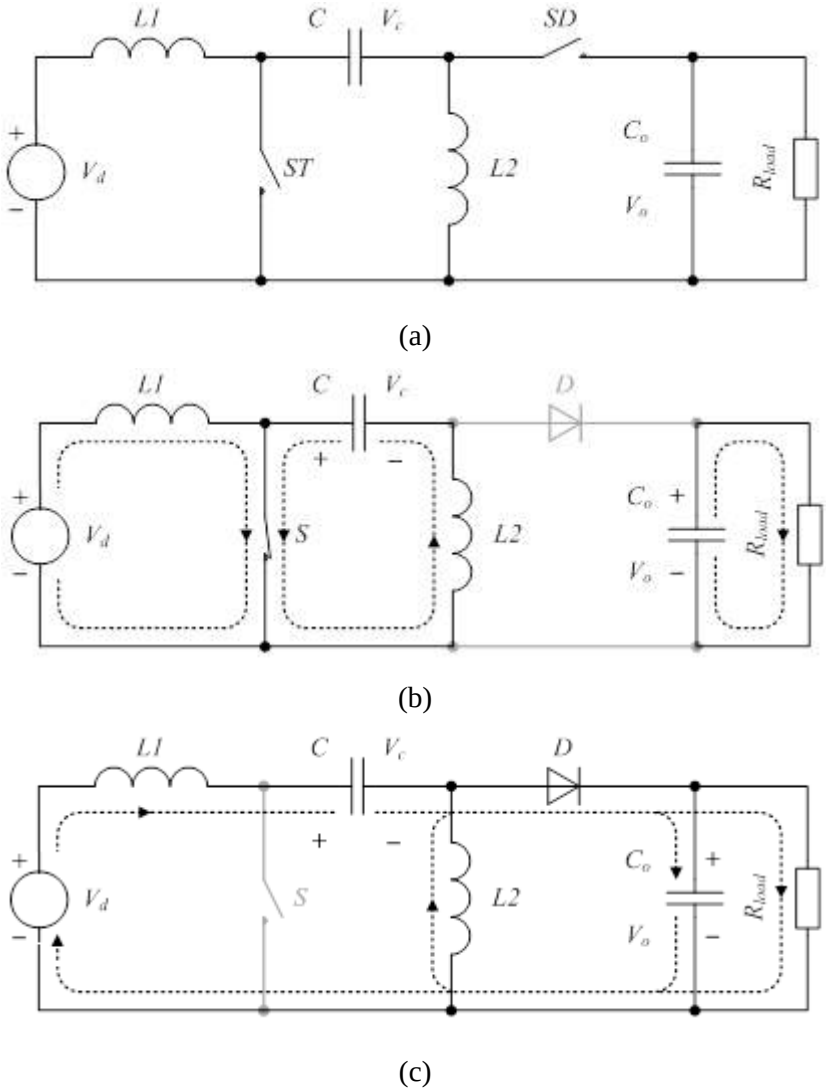


Fig. 2.25. SEPIC converter: generalized schematic (a); switch is on (b); switch is off (c)

Single-Ended Primary Inductor Converter (SEPIC) can be derived from Chuk converter where output diode and inductor are toggled (Fig. 2.25.). For this converter, voltage equilibrium can be easy written only for the output inductor L2

$$V_c \cdot D \cdot T_{SW} + (-V_o) \cdot (1-D) \cdot T_{SW} = 0, \tag{2-44}$$

while for the input one it refers to all three voltages. This is why it is more reasonable to compose the second necessary equation based on Kirchhoff's voltage law for average values of input voltage source, inductor L1, internal capacitor C and inductor L2:

$$V_d = V_{L1} + V_c - V_{L2}.$$

Taking into account that inductor's average voltages are 0 it gives

$$V_d = V_c$$

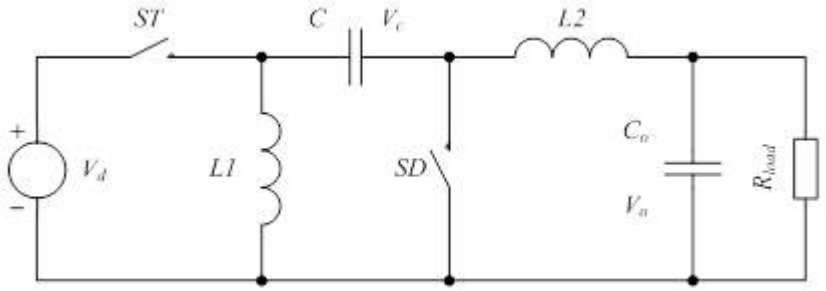
At the same time (2-44) produces

$$V_o = \frac{D}{1-D} \cdot V_c$$

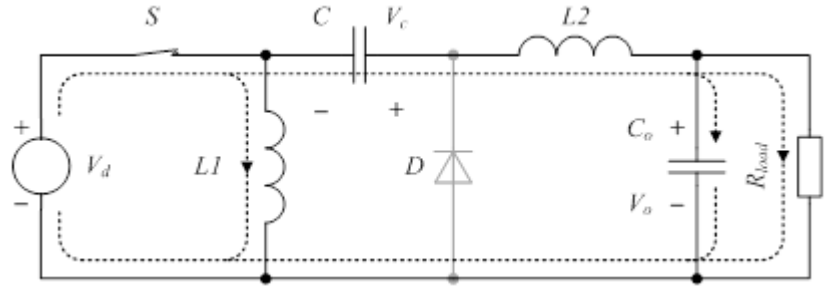
which together again gives buck/boost conversion formula.

SEPIC produces positive output voltage with smooth input current. At the same time the output current of SEPIC is formed in a diode which requires bigger output capacitor. Like Chuk converter SEPIC is output short-circuit proof.

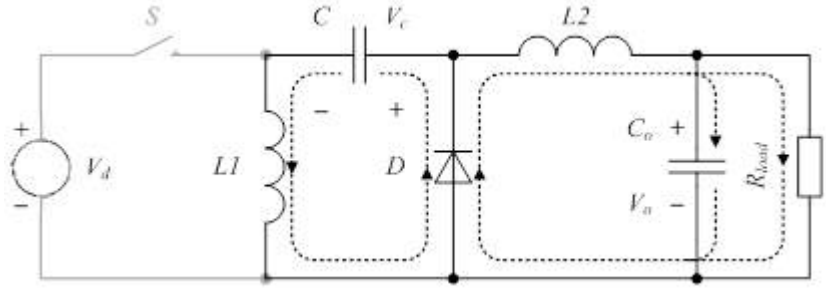
2.2.5. ZETA converter



(a)



(b)



(c)

Fig. 2.26. ZETA converter: generalized schematic (a); switch is on (b); switch is off (c)

Like SEPIC, ZETA converter is obtained from Chuk converter, but here the input inductor and controllable switch are toggled (Fig. 2.266.). For this converter it is more convenient to compose the voltage equilibrium for the input inductor L1:

$$V_d \cdot D \cdot T_{SW} - V_c \cdot (1-D) \cdot T_{SW} = 0, \quad (2\text{-}45)$$

but Kirchhoff's voltage equation for L1, C, L2 and Co

$$-V_{L1} + V_c + V_{L2} - V_o = 0. \quad (2\text{-}46)$$

(2-45) produces

$$V_c = \frac{D}{1-D} \cdot V_d ,$$

but (2-46) can be rewritten as

$$V_c = V_o .$$

Together these expressions again give the buck/boost regulation law.

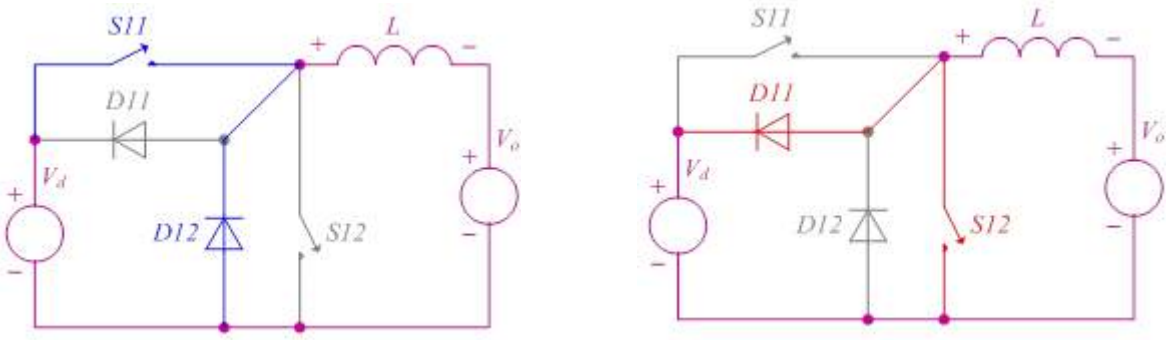
ZETA converter has pulse mode input current, smaller output capacitor and is output short-circuit proof.

2.3. Multi-quadrant DC/DC converters

Sometimes the energy flow between source and load is bidirectional. For example, a battery charger must be capable of supplying positive (charging) current into the battery and taking negative (discharging) current back from the battery. Also negative voltage may be necessary for the same direction of the output current (for example, drive). Below, two occasions of such converters are discussed.

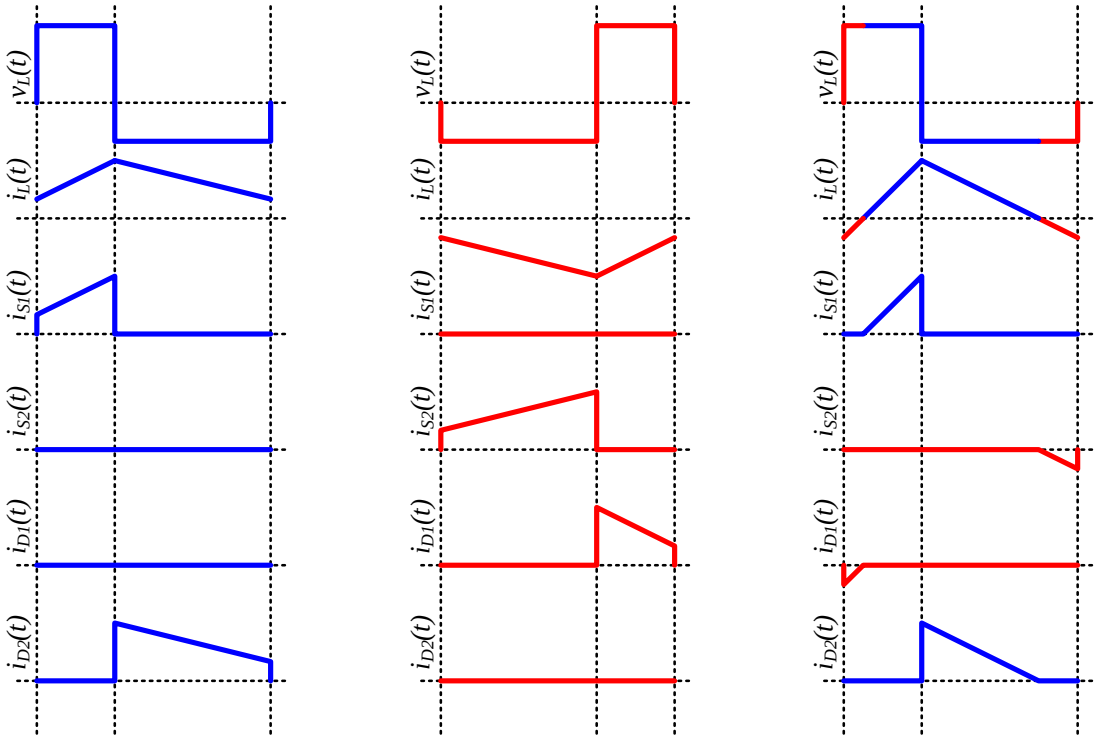
2.3.1. Synchronous buck converter – bidirectional output current

Let us compose a buck converter. It consists of the input source V_d, switch S11, diode D12, inductor L and output source V_o – blue and magenta elements in Figure 2.27.(a). The converter provides energy transfer from V_d to V_o in the case if $V_d \geq V_o$. The same elements V_d, L and V_o may form a basis for a boost converter where V_d is the input source, but V_o – the output source. This, however, requires two more switches – controllable switch S12 and diode D11 – red and magenta elements in Figure 2.27.(b). Together all the above mentioned components form a bidirectional converter which may have both positive and negative current for positive input and output. Besides the distinct forward buck mode shown in Fig. 2.28.(a) and operated by S11 and D12, as well as reverse boost mode presented in Fig. 2.28.(b) and operated by S12 and D11, the converter may operate in the mixed mode, in which inductor's instantaneous current may be positive or negative and both couples of the switches synchronously provide these positive and negative pieces of inductor's current, Fig. 2.28.(c). Therefore the converter has no discontinuous conduction mode, but requires careful control of the switches.



(a) (b)

Fig. 2.27. Synchronous buck converter: forward buck (a), reverse boost (b)



(c) (b) (c)

Fig. 2.28. Operation of synchronous buck converter: forward buck mode (iL – positive) (a), reverse boost mode (iL – negative) (b), mixed mode (iL – positive and negative) (c)

2.3.2. Diode and transistor half-bridge converter – bidirectional output voltage

In contrast to synchronous buck converter (Fig. 2.29.) the half bridge converter operates with one polarity of the output current and both polarities of the output voltage. When there is a passive load at the output of the converter, one of the switches S11 or S22 is on, but the other is switching then the circuit operates as ordinary buck converter.

If the switches S11 and S22 operate synchronously with the same duty cycle, then the inductor charge phase is similar to that of the buck converter (it is charged by the difference of input and output voltages), but inductor's discharge occurs through series connected input and output. Then the fall time of inductor current is shorter than its rise time and discontinuous operation with a passive load is possible only at duty cycle values D>0.5.

However, operation at D<0.5 is possible if there is an active voltage source at the output and its polarity is negative. Then the inductor is charged by the sum of input and output voltage, but its current fall time is longer. Taking into account the same polarity of output currents this mode assumes that energy is transferred from the output to the input of the converter.

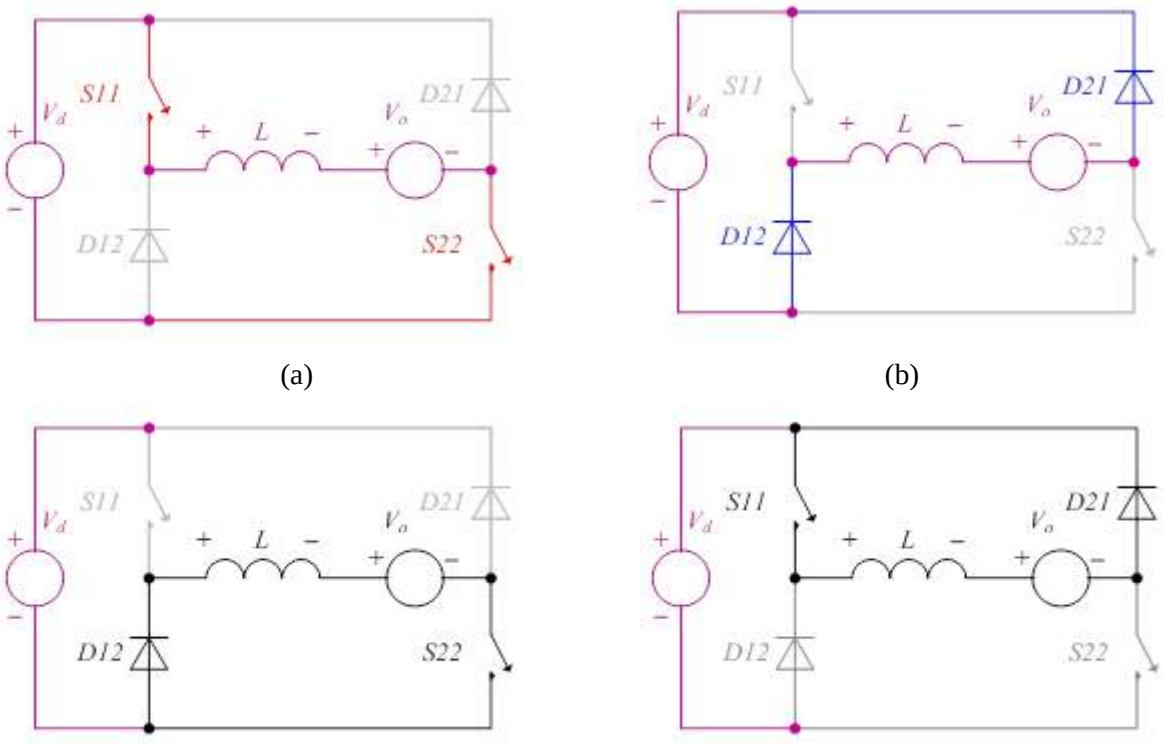


Fig. 2.29. Diode and transistor half-bridge: positive output (a), negative output (b), – zero output (c) and (d)

2.3.3. Full-Bridge and Capacitor Half-Bridge Converters – Bidirectional Output Voltage and Current

Genesis of multi-quadrant converters

Consideration of Fig. 2.28. and Fig. 2.29. together shows that the use of bidirectional (transistor + diode) switches provides opportunity for bidirectional output current, but the use of H-topology – opportunity for bidirectional output voltage. Therefore, the combination of the bidirectional switches and H-topology could provide both the bidirectional output current and voltage. Such a converter, known as full-bridge or transistor H-bridge, is presented in Fig. 2.30. The schematic in Fig. 2.30.(a) shows how this converter can be configured for the synchronous buck mode, Fig. 2.30.(b) – for transistor and diode half-bridge, but Fig. 2.30.(c) – represents its complete four-quadrant configuration. The operation of the switches in this converter is explained in Table **2-7**. It is seen from this table that the input voltage can be applied in both directions to the output. Also the output current can flow in both directions. It can be found that the full-bridge converter forms a buck converter for both possible polarities of the output voltage. For the positive output voltage charge state with switched on S11 and S22 is described as

$$\Delta i_{o+}(t) = \frac{1}{L} \cdot \left(V_d - V_o\right) \cdot T \cdot D. \tag{2-47}$$

The corresponding discharge state takes place if only one of the switches S11 and S22 is on. This stage can be described as

$$\Delta i_{o-}(t) = \frac{1}{L} \cdot \left(-V_o\right) \cdot T \cdot (1-D). \tag{2-48}$$

Combining and converting (2-47) and (2-48) gives well known conversion formula for buck converter (2-12). In the full bridge converter the state when both switches are off is possible. Then the input voltage is applied in the reversed direction:

$$\Delta i_{o-}(t) = \frac{1}{L} \cdot \left(-V_d - V_o\right) \cdot T \cdot (1-D). \tag{2-49}$$

If such stage appears then the discharge is faster and minimal duty cycle is 0.5. Similar equations can be written for negative output voltage.

One transistor leg of the full bridge converter can be substituted with a capacitor leg – Fig. 2.30.(d). The obtained topology is called capacitor half-bridge. It has two significant features. Firstly, the amplitude of the output voltage cannot be higher than one half of the input voltage. Secondly, this topology is not suitable for DC/DC operation (operation with constant output voltage), but in DC/AC operation (pulse mode AC output) the capacitor leg has to be balanced all the time.

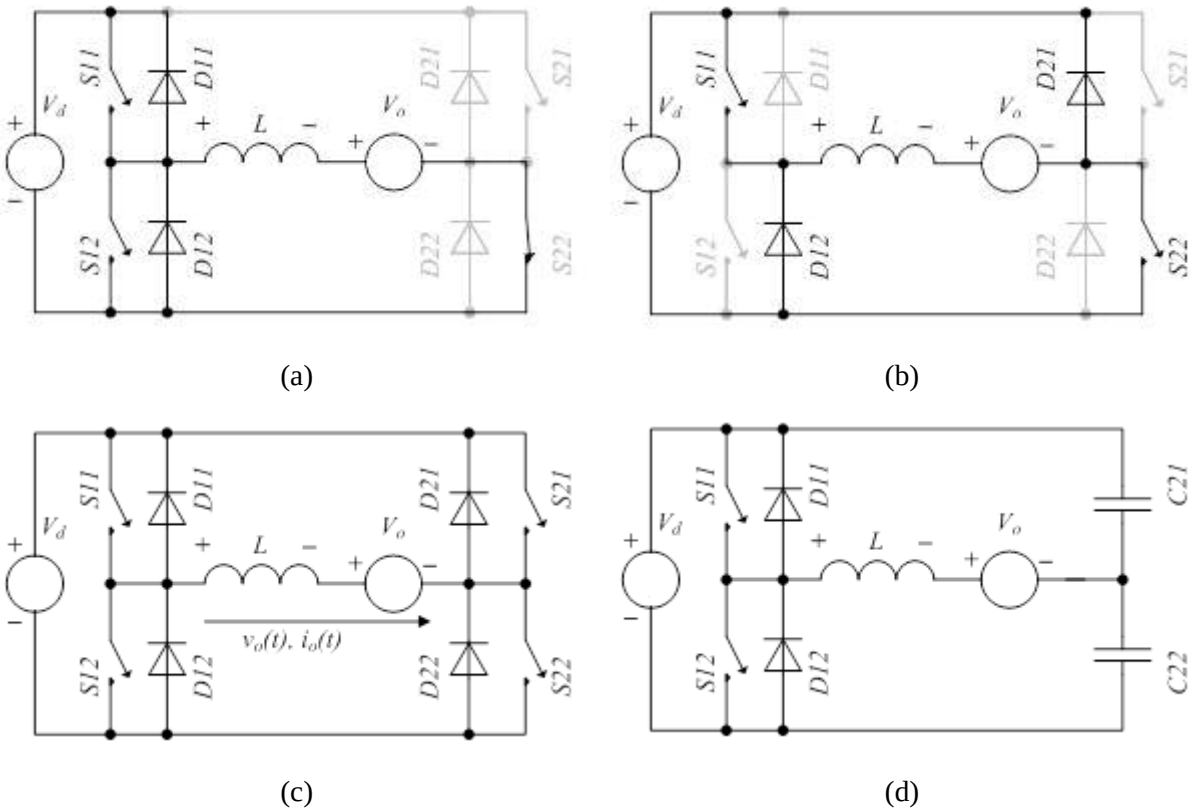


Fig. 2.30. Genesis of multi-quadrant converters: synchronous buck converter positive output (a), diode and transistor half-bridge (b), full-bridge (c) and capacitor half-bridge (d)

Table 2-7. Voltages and currents in full bridge converter

Conducting switches	$v_o(t)$	$i_o(t)$
S11 and S22	+	+
D11 and D22	+	–
S12 and S21	–	–
D12 and D21	–	+
S11 and D21	0	+
S22 and D12	0	+
S21 and D11	0	–
S12 and D22	0	–

2.4. Current fed converters

2.4.1. Synthesis of Current Fed Converters

Current Fed (CF) regulators are most useful in applications with natural current sources, such as photovoltaic (PV) batteries and superconductive magnetic energy storages, or with current related loads like LEDs. The CF converters can be derived from the corresponding Voltage Fed (VF) circuits applying a set of rules given in simplified form in Table 2-8. Then it is possible to transform any traditional VF converter into the corresponding CF circuit (Fig. 2..). An example of such transformation of a VF buck-boost converter into the corresponding CF buck-boost converter is explained in Fig. 2.31.(a) and Fig. 2.31.(b). In these diagrams

typical combinations of elements before and after the transformation are drawn on the same background. In turn Fig. 2..(c) presents CF buck, but Fig. 2.31.(d) – CF boost converter.

Table 2-8. Rules of Transformation of VF circuits into CF circuits

VF	**CF**
Voltage source	Current source
Capacitor	Inductor
Open circuit	Short circuit
Star connection (in particular: T-stage)	Ring connection (in particular: Π-stage)
Switches ON	Switches OFF

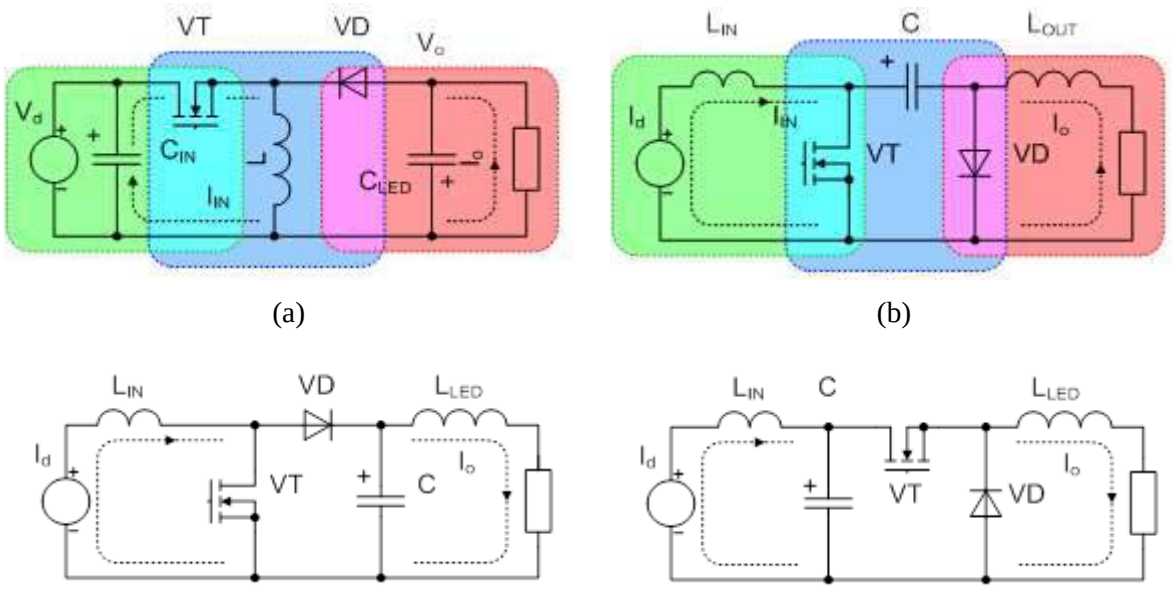


Fig. 2.31. Obtaining CF converters: initial VF buck/boost (a); final a CF buck/boost (b); CF buck (c) and CF boost (d)

2.4.2. Static Model of CF Converters

Static operation of CF buck converter is defined by the currents balance of its capacitor, like operation of VF converter is defined by the voltage balance of its inductor. When the transistor is on the current source is short-circuited. Then the capacitor is being charged by the load current (discharged). Then voltage across capacitor CCF decreases and can be expressed with the equation:

$$\Delta V_{C-} = \frac{1}{C}\int_{D\cdot T}^{T}(-I_o)dt = -\frac{I_o \cdot D \cdot T}{C} \ . \tag{2-50}$$

When the transistor is off the current is conducted by diode D1 and the capacitor of the converter is charged from the difference of the supply and load currents IIN –ILED. The corresponding voltage increasing by:

$$\Delta V_{C+} = \frac{1}{C}\int_{D\cdot T}^{T}(I_d - I_o)dt = \frac{(I_d - I_o)\cdot(1-D)\cdot T}{C} \ . \tag{2-51}$$

In (4) and (5) T is switching period, but D – the duty cycle of its switch operation. In the case of static operation of the converter the voltage across capacitor has to be the same at the borders of the switching period $\Delta V_{C-}+\Delta V_{C+}=0$. This gives the following current transformation equation:

$$I_{o\_cbuck} = I_d \cdot (1-D) \ . \tag{2-52}$$

It can be seen that the static equations for the above described CF converters can also be derived from those of VF converters, where 1–D is located instead of D. Then the current transformation expression of a CF boost converter

$$I_{o\_cfboost} = I_d \cdot \frac{1}{D}, \tag{2-53}$$

as well as for a CF buck/boost

$$I_{o\_cfbb} = I_d \cdot \frac{1-D}{D} \ . \tag{2-54}$$

Like VF converters, CF converters have discontinuous mode, which is defined by the shape of capacitor's voltage. Analyzing together the current balance of input capacitor and voltage balance of the output inductor it is possible to obtain current transformation equations also for discontinuous voltage mode. In this mode the sum of voltage rise time and fall time is shorter than the switching period and (2-52) is expressed as

$$I_o \cdot \delta = (I_d - I_o) \cdot (1-D), \tag{2-55}$$

where δ can be found based on the capacitor's voltage

$$V_o = V_C = \frac{\Delta V_{C+}}{2} \cdot (t_+ + t_-) = \frac{(I_d - I_o) \cdot T}{C} \cdot (1-D+\delta), \tag{2-56}$$

(2-55) and (2-56) together form the current transformation expression for a discontinuous voltage mode, which looks like the following

$$I_{o\_cfbuck\_dm} = \frac{I_d \cdot (1-D)^2}{(V_o \cdot 2C)/(I_d \cdot T_{sw}) + (1-D)^2}, \tag{2-57}$$

of the CF boost converter as

$$I_{o\_cfboost\_dm} = \frac{I_d^2 \cdot (1-D)^2 \cdot T_{sw}}{V_o \cdot 2C} + I_{IN}, \tag{2-58}$$

but of the CF buck/boost converter as

$$I_{o\_cfbb\_dm} = -\frac{I_d^2 \cdot (1-D)^2 \cdot T_{sw}}{V_o \cdot 2C} \ . \tag{2-59}$$

where V_o – is the output voltage of CF buck converter.

It has to be noted that in the case of some loads like LEDs, the output voltage is close to constant (and very close to the rated voltage of the LEDs, i.e. it is quite high). For this reason the discontinuous voltage mode in such CF drivers with a LED load is almost impossible and equations (2-57) to (2-59) are not of practical interest.

3. Rectifiers

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3.1. Introduction

In this chapter, different types of rectifiers will be discussed. Rectifiers are the devices transforming electrical energy form AC to DC. In this chapter, single phase and three phase rectifiers will be discussed. These rectifiers can be subdivided into controlled and uncontrolled rectifiers. After reading this chapter, the reader should:

- understand the operation principle of typical rectifier circuits,
- know which type of rectifier is needed in a specific situation,
- be able to design the chosen rectifier for the specific situation.

All circuits are explained using simulations made with Simulink [Matlab 2013], using the library Simscape. In this library, a lot of the power electronic components are predefined and ready to use in the electronic circuit.

In this chapter, all elements are assumed to be ideal.

3.2. Single-phase rectifiers

The single phase rectifiers are mainly used in household appliances since often only a single phase grid is available. In this kind of applications, the cost price is very important and in general the required power output is low. There are different kinds of divisions, one could make the division on the fact whether the output voltage is controllable or uncontrollable. Another division could be made on the fact whether the rectifier is rectifying the full AC-wave or only the half of the AC-wave. Fig. 3.1 shows the different divisions applicable for the single-phase rectifiers.

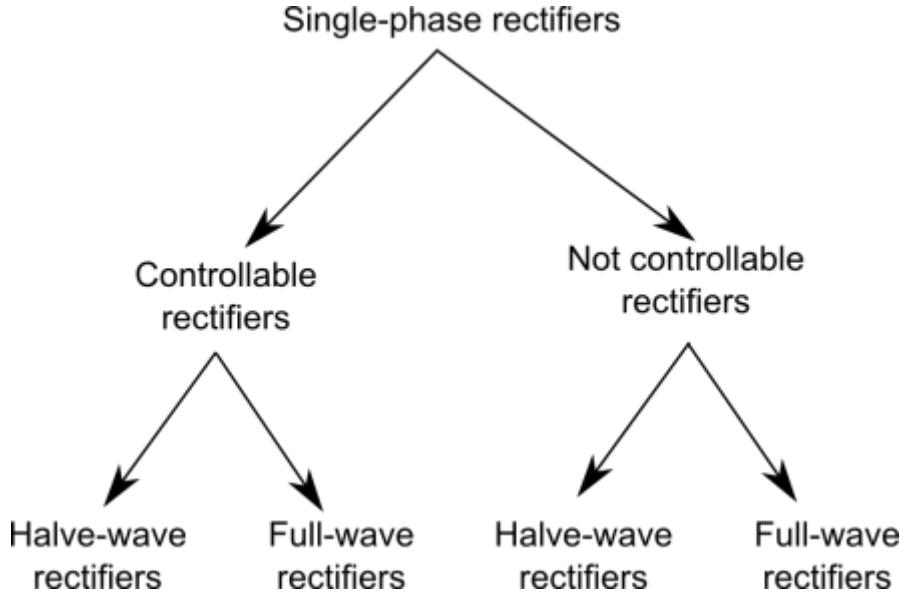


Fig. 3.1. Division of the different types of single-phase rectifiers

3.2.1. Single-phase uncontrollable rectifiers

The single-phase uncontrollable rectifiers are also known as the single-phase diode rectifiers. The ideal diode has a zero forward voltage drop and a zero reverse recovery time. When considering rectifiers which rectify the grid voltage these assumptions are valid since the voltage drop over the diode is much smaller than the amplitude of the grid voltage. Moreover, the recovery time of a real diode is small in comparison with the period of the grid voltage (20 ms in case of a 50 Hz frequency).

Single-phase uncontrollable half-wave rectifiers with resistive load

The single-phase uncontrollable half-wave rectifier is the easiest rectifier type. Fig. 3.2 shows the circuit of a single-phase uncontrollable half-wave rectifier. The single phase voltage is rectified when the forward voltage is higher than zero which is obtained when the AC voltage u_ac is positive.

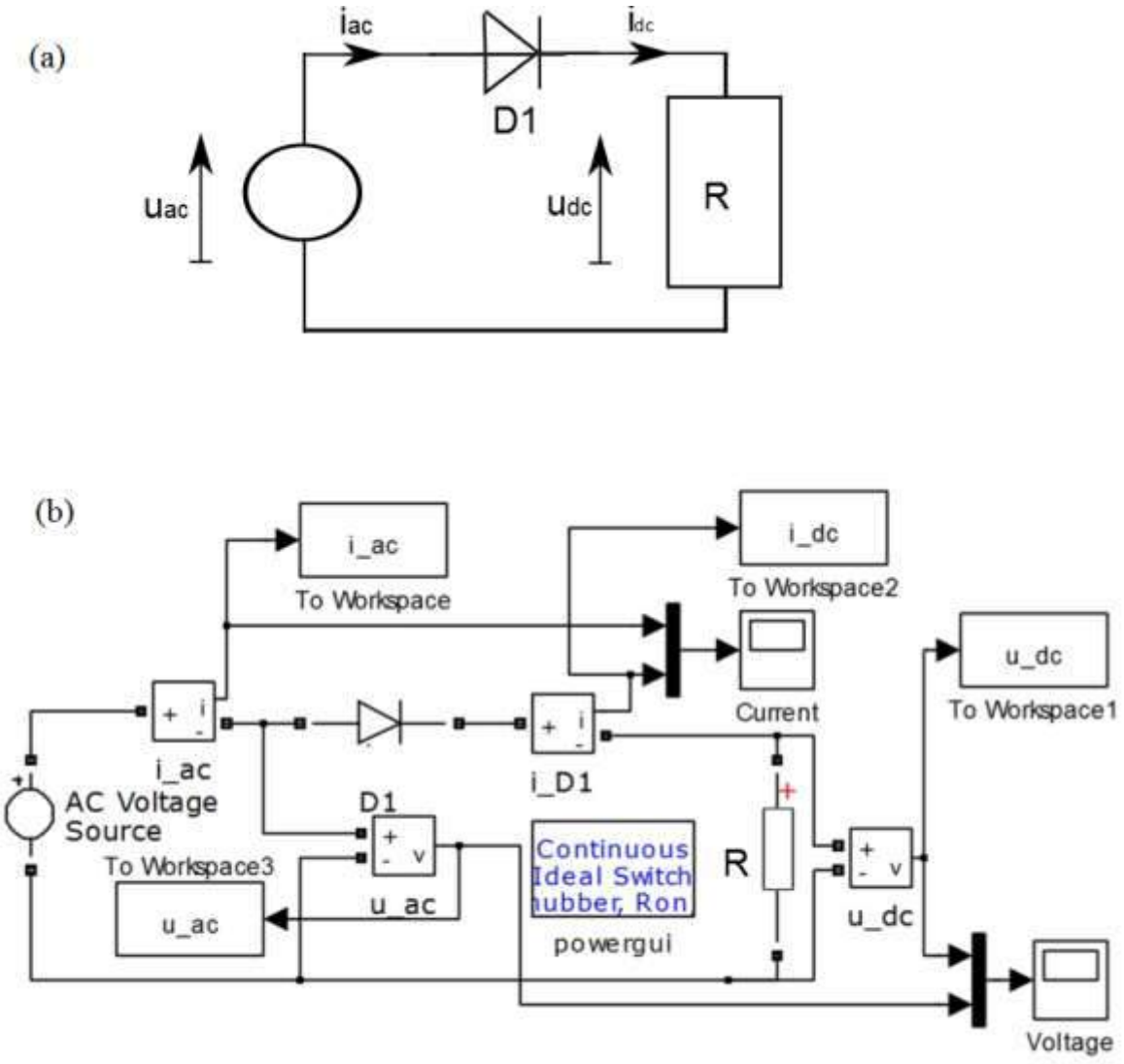


Fig. 3.2. The circuit of the single-phase uncontrollable half-wave rectifier: the electrical circuit (a) the Simulink model (b).

The obtained DC-voltage u_dc is equal to the positive alternation of the AC-voltage u_ac, as shown in Fig. 3.3. Indeed, a half-wave rectifier only passes half of the AC-voltage wave.

Although this DC-voltage (a voltage is DC when the sign of the voltage does not change) has no ideal form, it can be described with a Fourier series and we/the powered devices are interested in the average of the voltage only. The average of the voltage is obtained by taking the integral over one period of the DC-voltage and dividing it with the length of this period:

$$U_{DC} = \frac{1}{T}\int_0^T u_{dc}(t)\,dt = \frac{1}{\theta}\int_0^\theta u_{dc}(\omega t)\,d\omega t \tag{3-1}$$

Where U_{DC} is the average of the DC-voltage, T is the length of the period, $u_{dc}(t)$ is the instantaneous value of the DC-voltage. The period can be described as a function of time (e.g. T = 20 ms) or the electrical angle (ωt) giving a period which equals to $(\theta = \omega T = 2\pi$ rad).

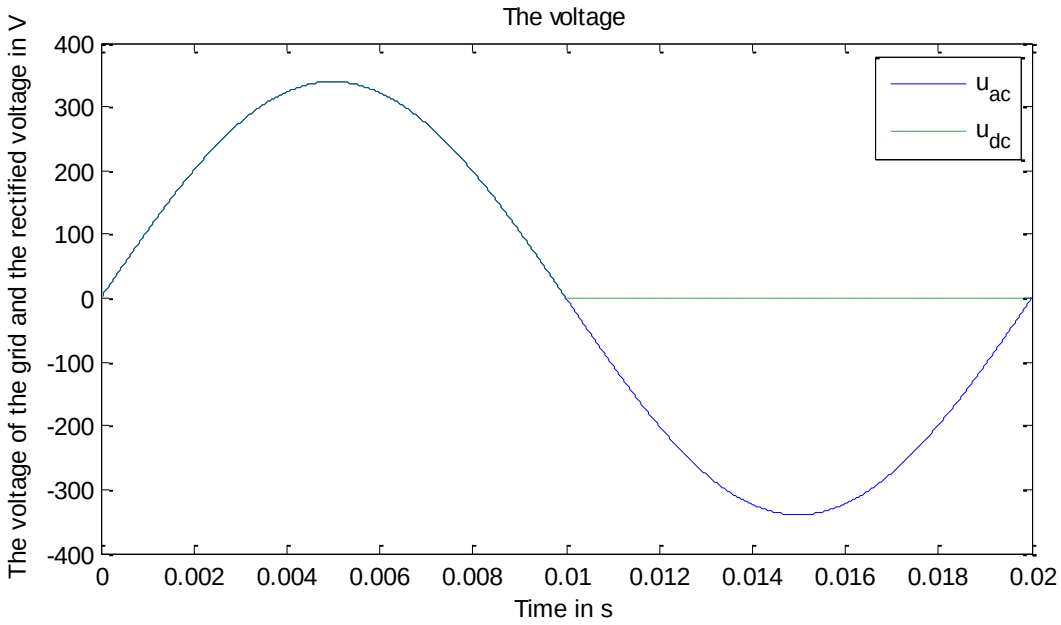


Fig. 3.3. The DC-voltage of the single-phase uncontrollable half-wave rectifier in case of an AC voltage with an rms value of 240V and a frequency of 50Hz

Studying Fig. 3.3. one notices that a period of u_{dc} can be divided in two parts, i.e. the positive alternation of u_{ac} and zero. This leads to:

$$U_{DC} = \frac{1}{\theta}\int_0^{\omega T/2} u_{ac}(\omega t)\,d\omega t = \frac{1}{2\pi}\int_0^{\pi} u_{ac}(\omega t)\,d\omega t = \frac{\sqrt{2}}{\pi}U_{ac} \tag{3-2}$$

Here, U_{ac} equals the RMS-value of u_{ac}. As visualized in Fig. 3.3., only during the positive alternation of the voltage a current is flowing as shown in Fig. 3.4. Here, the current of the grid equals to the diode D1 current. This implies the disadvantage that the current in the grid only has a positive alternation, i.e. it is a DC current. When calculating the Fourier series of the grid current i_{ac} using (notice we use a general x as variable since x can be time, angle, distance, …):

$$f(x) = \frac{a_0}{2} + \sum_{n=1}^{\infty}(a_n \cos(n\,x) + b_n \sin(n\,x)) \tag{3-3}$$

$$a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)\cos(n\,x)\,dx \quad \textit{for all positive integer values } n \textit{ (from 0 to } \infty) \tag{3-4}$$

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)\,sin(n\,x)\;dx\;\;for\;all\;positive\;integer\;values\;n\;(from\;0\;to\;\infty) \quad (3\text{-}5)$$

the frequency spectrum is obtained, as visualized in Fig. 3.5.

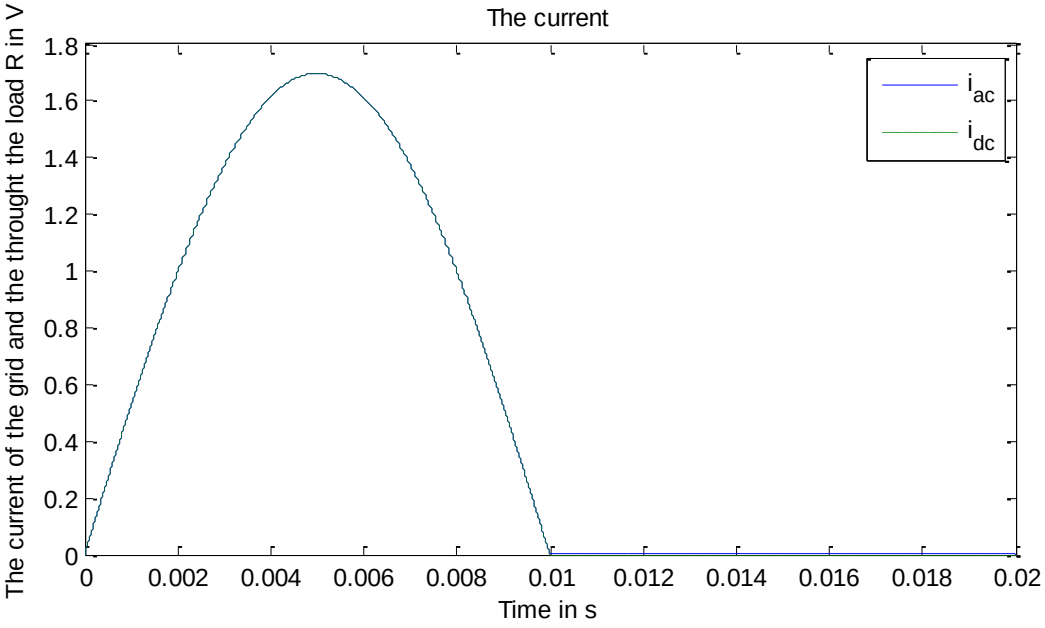


Fig. 3.4. The current of the grid (iac) and the diode D1 (idc) current for a single-phase uncontrollable half-wave rectifier

When calculating the Fourier series manually, one must be aware that for n=1 the integral is calculated separately to obtain a_1. When calculating the coefficients a_n (n > 1) divided by the peak value, one obtains:

$$a_n = \frac{1}{\pi}\int_0^{\pi} \sin(x)\cos(nx)\;dx = -\frac{\cos\big((n+1)\pi\big)}{2(n+1)} - \frac{\cos\big((1-n)\pi\big)}{2(1-n)} + \frac{\cos(0)}{2(n+1)} + \frac{\cos(0)}{2(1-n)}$$

n	$-\frac{\cos((n+1)\pi)}{2(n+1)}$	$-\frac{\cos((1-n)\pi)}{2(1-n)}$	$\frac{\cos(0)}{2(n+1)}$	$\frac{\cos(0)}{2(1-n)}$	⟨1⟩ + ⟨2⟩ + ⟨3⟩ + ⟨4⟩	$\frac{⟨5⟩}{\pi}$
1	\	\	\	\	\	0
2	1/6	-1/2	1/6	-1/2	-2/3	-2/(3 π)
3	-1/8	1/4	1/8	-1/4	0	0
4	1/10	-1/6	1/10	-1/6	-2/15	-2/(15 π)
5	-1/12	1/8	1/12	-1/8	0	0
6	1/14	-1/10	1/14	-1/10	-2/35	-2/(35 π)
7	-1/16	1/12	1/16	-1/12	0	0
8	1/18	-1/14	1/18	-1/14	-2/63	-2/(63 π)

When calculating the Fourier series manually, one must be aware that for n=1 the integral is calculated separately to obtain b_1. The obtained values for the coefficients b_n (n>1) divided by the peak value are:

$$b_n = \frac{1}{\pi}\int_0^{\pi} \sin(x)\sin(nx)\,dx = \frac{\sin\big((1-n)\pi\big)}{2(1-n)} - \frac{\sin\big((1+n)\pi\big)}{2(1+n)} - \frac{\sin(0)}{2(1-n)} + \frac{\sin(0)}{2(1+n)}$$

n	$\frac{\sin((1-n)\pi)}{2(1-n)}$	$-\frac{\sin((1+n)\pi)}{2(1+n)}$	$-\frac{\sin(0)}{2(1-n)}$	$\frac{\sin(0)}{2(1+n)}$	⟨1⟩ + ⟨2⟩ + ⟨3⟩ + ⟨4⟩	$\frac{⟨5⟩}{\pi}$
1	\	\	\	\	π/2	1/2
2	0	0	0	0	0	0
3	0	0	0	0	0	0
4	0	0	0	0	0	0
5	0	0	0	0	0	0
6	0	0	0	0	0	0
7	0	0	0	0	0	0
8	0	0	0	0	0	0

The fundamental wave, which is the harmonic component having the lowest frequency in $i_{ac}(t)$, has a frequency of 50 Hz or 60 Hz which equals to the grid frequency. In the case the grid voltage equals to $u_{ac}(t) = \sqrt{2}U_{ac}\sin(\omega t)$, the fundamental wave is obtained by the b_n coefficient while all the other harmonic components are obtained by the a_n coefficients. Here, only even higher order harmonics are obtained. The values of the harmonic components are plotted in a graph which is called the spectrum.

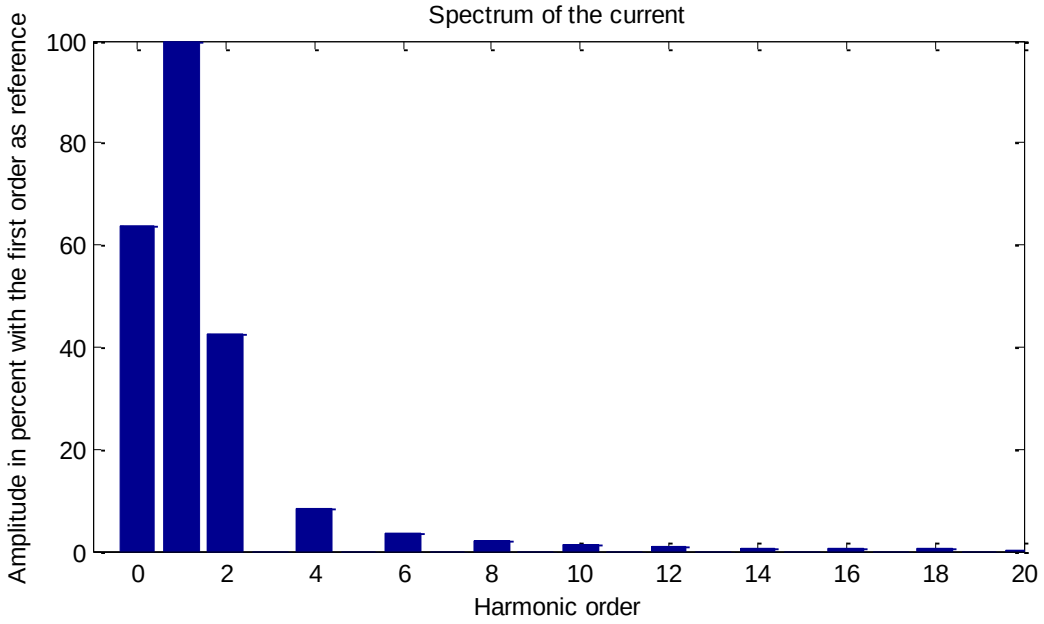


Fig. 3.5. Spectrum of the current iac for a single-phase uncontrollable half-wave rectifier

Fig. 3.5 shows the amplitude of each harmonic component relative to that of the fundamental wave. The DC component in the current has an order zero. The spectrum contains an infinite number of components, as the harmonic order increases the amplitude of the harmonic component decreases. In this chapter, only the positive frequencies are visualized although there are the definitions defining positive and negative frequencies.

Fig. 3.5 shows that the grid has to deliver a DC-component of more than 60% of the fundamental wave. There are also a lot of even order harmonics in the current i_{ac}. The grid is designed to provide a sinusoidal current implying the impact of the harmonics must be reduced. The Total Harmonic Distortion (THD) measures and quantifies the distortion of the

shape of the current. The THD compares the harmonic components with the fundamental wave. There are several different definitions in order to determine the THD, more precisely

$$THD_i = \frac{\sqrt{\sum_{i=2}^{\infty} I_i^2}}{I_1} \tag{3-6}$$

$$THD_i = \frac{\sqrt{I_{total}^2 - I_1^2}}{I_1} \tag{3-7}$$

$$THD_i = \frac{\sqrt{\sum_{i=2}^{\infty} I_i^2}}{\sqrt{\sum_{i=1}^{\infty} I_i^2}} \tag{3-8}$$

where the RMS-values of the harmonic components I_i and the total current I_{total} are used. Using equation (3-6) on this rectifier, the THD equals to 43.52%. Equation (3-7) gives a THD of 100% and equation (3-8) gives a THD of 39.91%. Although equation (3-6) is frequently used, one must always be aware which definition is used to determine the THD.

It is also useful to study the spectrum of the rectified voltage visualized in Fig. 3.6. In this case, the amplitudes of the harmonic components are compared with the DC-component (the rectifier is intended to obtain a DC-voltage). The rectifier is intended to obtain a DC-voltage which approximates a constant DC-voltage. As shown in Fig. 3.3 and Fig. 3.6, one notices there is a large ripple of this DC-voltage. In order to quantify the ripple, the ripple factor is introduced and defined by equation (3-9).

$$RF = \frac{V_{s,ac}}{U_{dc}} \tag{3-9}$$

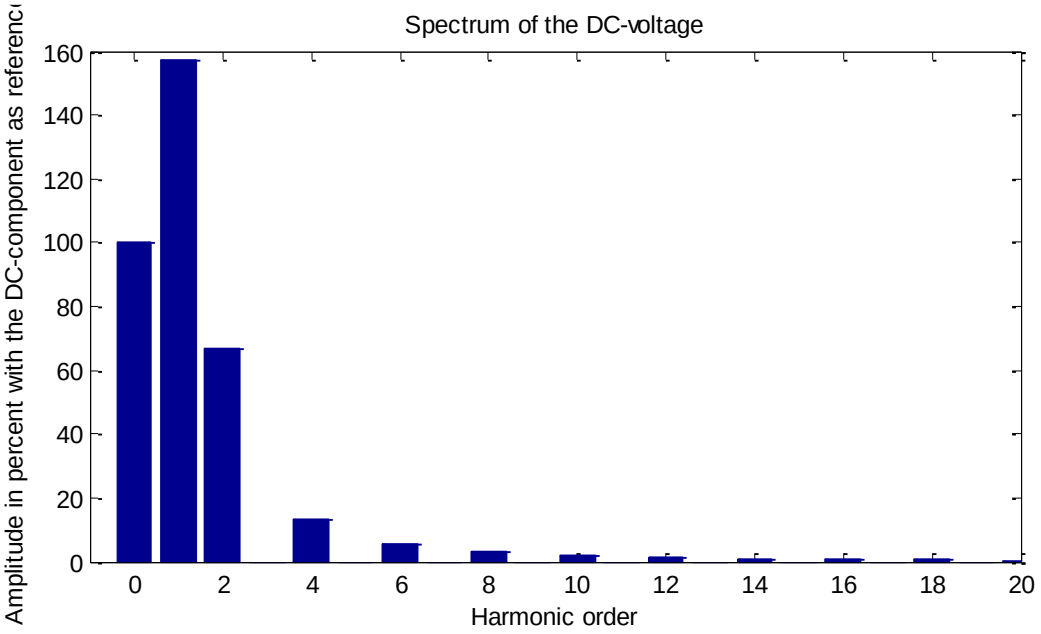


Fig. 3.6. Spectrum of the voltage udc for a single-phase uncontrollable half-wave rectifier

The parameter $V_{s,ac}$ is the RMS-value of the AC-signal added with the DC-component, which equals the square root of the quadratic sum of the RMS-values of all the harmonics

except the harmonic with order zero. U_{dc} is the mean value of the DC-voltage i.e. the harmonic with order zero. Applied in Fig. 3.6., equation (3-9) leads to:

$$RF = \frac{V_{s,ac}}{U_{dc}} = \frac{\sqrt{\sum_{i=1}^{\infty} u_{dc,fft,i}^{\ 2}}}{u_{dc,fft,1}} = 1.21$$

Single-phase uncontrollable full-wave rectifiers with resistive load

When considering the single-phase uncontrollable full-wave rectifiers, only the bridge full-wave rectifier is explained. Notice however there is a second variant of this kind of rectifiers named the center-tapped transformer full-wave rectifier. The bridge full-wave rectifier is shown in Fig. 3.7.

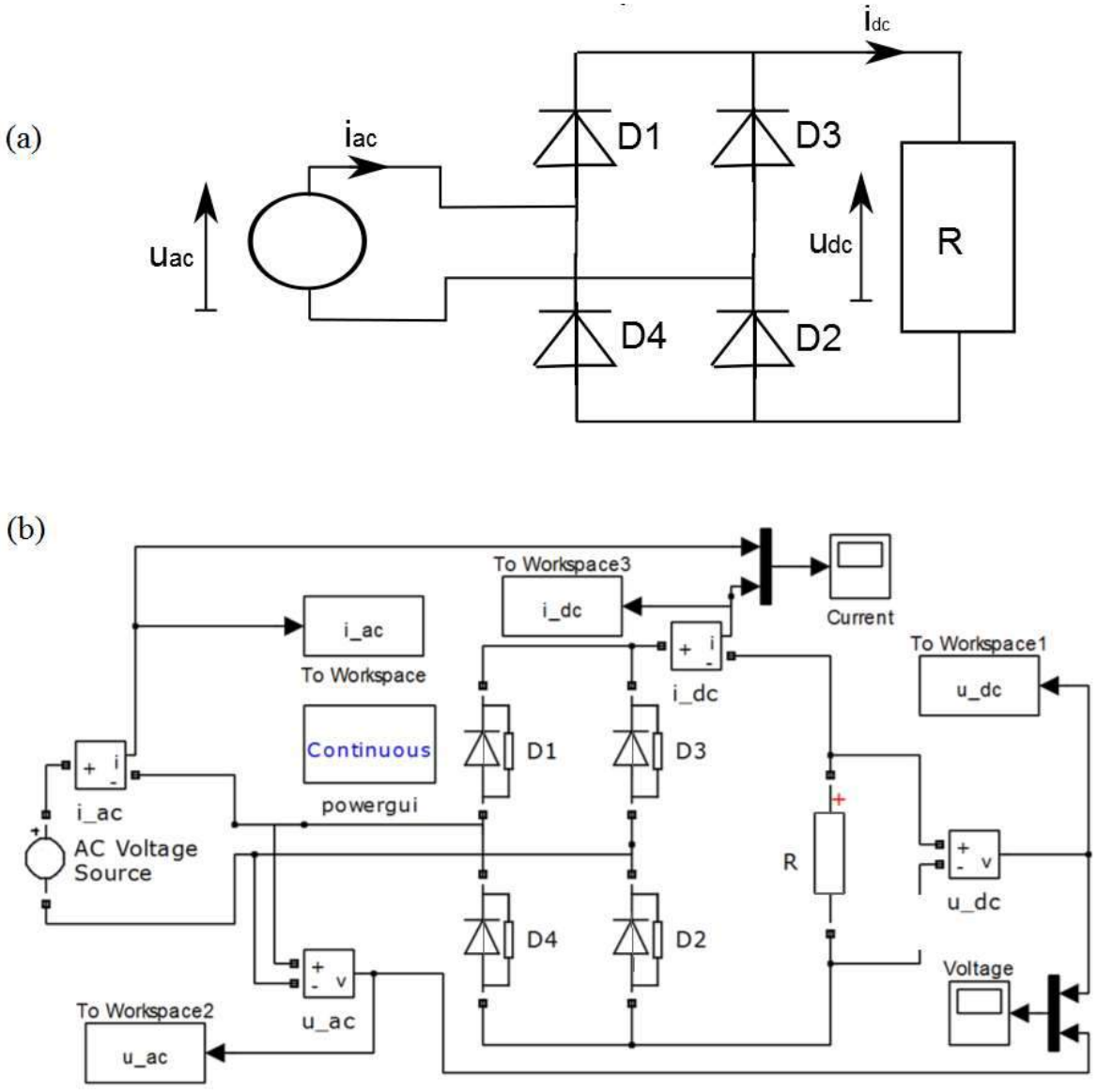


Fig. 3.7. The single-phase uncontrollable full-wave bridge rectifier: (a) electrical circuit (b) Simulink model

When the source voltage u_{ac} is positive and the instantaneous value of this voltage is larger than twice the forward voltage of a diode, the current will flow through diodes D1 and D2. When the source voltage u_{ac} is negative and the absolute value of the instantaneous value of

the voltage is larger than twice the forward voltage of a diode, the current will flow through diodes D3 and D4. This implies the whole period of the grid voltage is rectified, meaning the positive cycle and the negative cycle of the grid voltage are used. It doubles the mean value of the rectified DC-voltage, as becomes clear when comparing Fig. 3.3 and Fig. 3.8.

When applying equation (3-1) to Fig. 3.8., one obtains that the mean value equals to $\frac{2\sqrt{2}}{\pi} U_{ac}$ with U_{ac} the RMS value of the voltage source. Notice from Fig. 3.8 that the period of the rectified voltage equals to 10ms. Notice the mean value of the voltage obtained by the single-phase full-wave bridge rectifier equals to the double mean value of the voltage obtained by the single-phase half-wave rectifier. This is one of the advantages of this rectifier in comparison with the single-phase half-wave rectifier.

Another advantage of the full-wave bridge rectifier is found in the current as visualized in Fig. 3.9. Notice the grid current i_{ac} has a positive alternation and a negative alternation. Moreover, these alternations are symmetrical implying the grid current has no DC-component. This is also visualized by the spectrum of the grid current in Fig. 3.10. The spectrum shows there are no other harmonic components in the grid current than the fundamental, i.e. the grid current is a sine-wave. When calculating the THD of the grid current using equations (3-6), (3-7) and (3-8), they all give the same result of 0%.

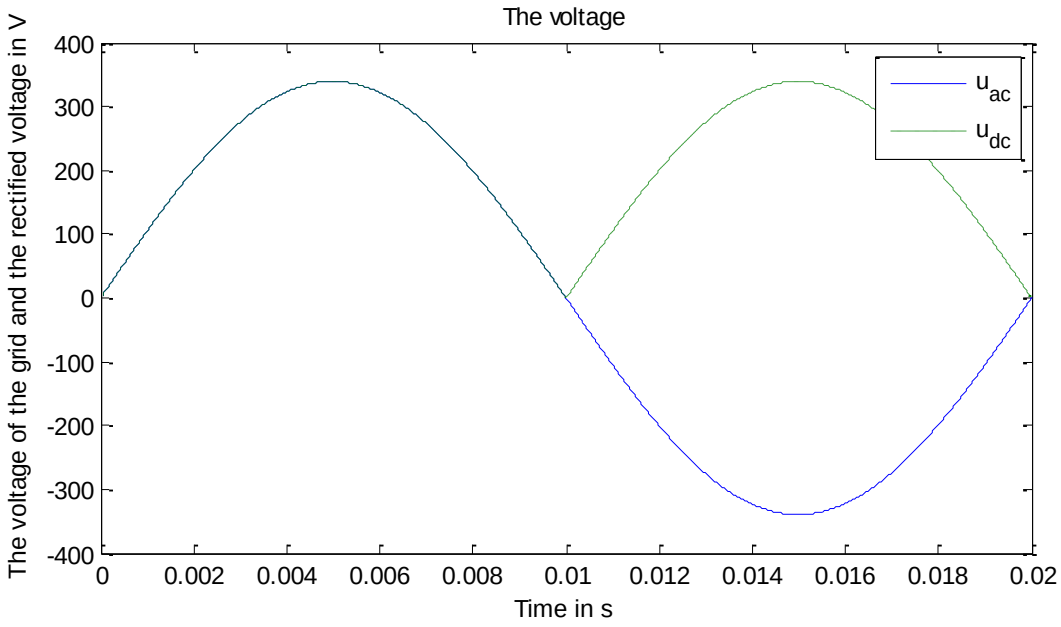


Fig. 3.8. The DC-voltage of the single-phase uncontrollable full-wave bridge rectifier in case of an AC voltage with an rms value of 240V and a frequency of 50Hz

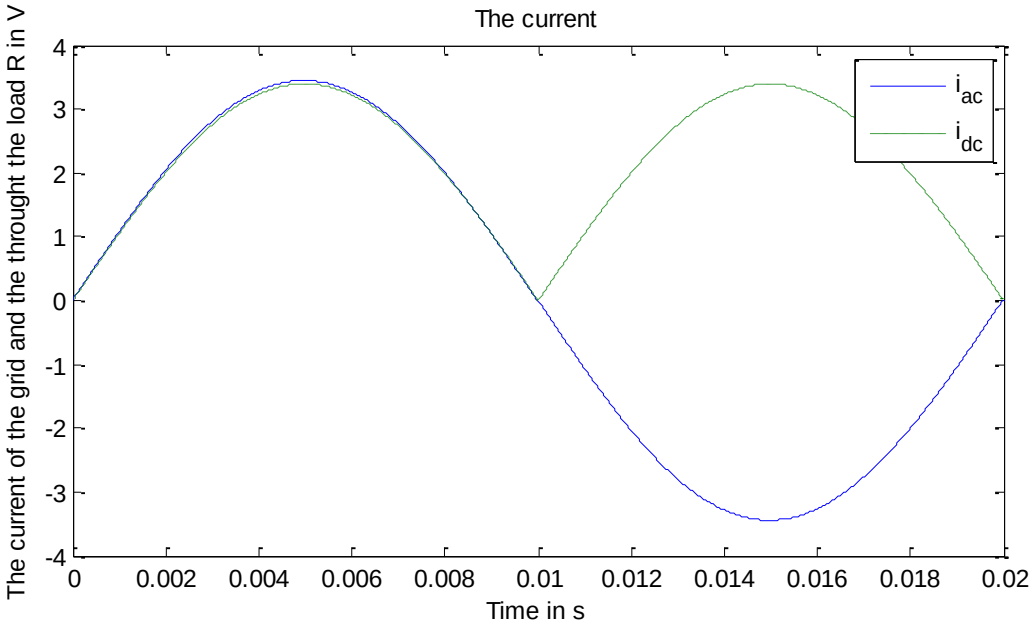


Fig. 3.9. The grid current (iac) and the load R (idc) current for a single-phase uncontrollable full-wave bridge rectifier

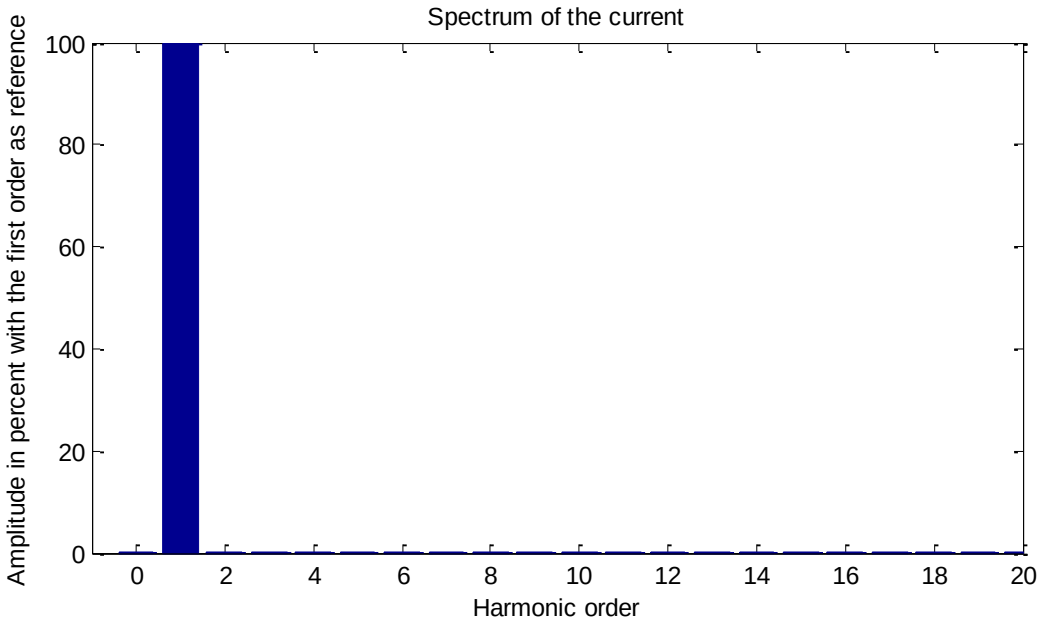


Fig. 3.10. Spectrum of the current iac for a single-phase uncontrollable full-wave bridge rectifier

As already mentioned, the single-phase uncontrollable full-wave bridge rectifier has a number of advantages over the single-phase uncontrollable halve-wave rectifier. However, there is an additional advantage in the design of this full-wave bridge rectifier. Since there are always two diodes in series, the reversed voltage or breakdown voltage of these diodes need to be only half of the maximum grid voltage. For the single-phase uncontrollable half-wave rectifier, the diode has to withstand the full maximum grid voltage. By using two diodes in series, also some disadvantages occur. The forward voltage drop across this bridge rectifier is doubled. Moreover, the cost to build this bridge rectifier is larger i.e. four diodes instead of one single diode is needed.

When studying the spectrum of the DC-voltage visualized in Fig. 3.11 and applying equation (3-9), one obtains that the RF equals to 48.34%. This lower RF value is an important improvement in comparison to the single-phase uncontrollable half-wave bridge rectifier having a RF which is equal to 121%.

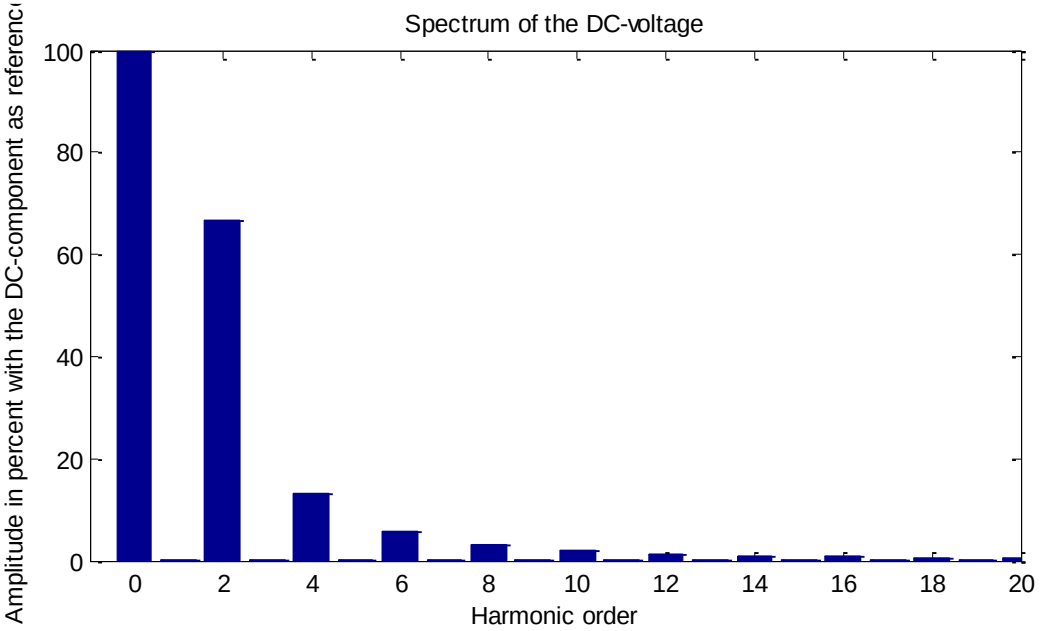


Fig. 3.11. Spectrum of the voltage udc for a single-phase uncontrollable full-wave bridge rectifier

3.2.2. Single-phase controllable rectifiers

The single-phase controllable rectifiers can be subdivided in two groups: the single-phase thyristor rectifiers also known as the line-commutated single-phase controlled rectifiers and the single phase circuits working with high switching frequency also known as Power Factor Correctors (PFC). The ideal thyristor has a zero forward voltage drop and a zero reverse recovery time. Even when using ideal thyristors, these thyristor rectifiers will generate current harmonics in the grid. The last years, a lot of efforts have been made to reduce these current harmonics and to obtain a better current waveform by using Power Factor Correctors.

Line-commutated Single-phase Controlled Rectifiers

These rectifiers resemble the rectifiers of paragraph 0 ***Single-phase uncontrollable half-wave rectifiers*** and 0 ***Single-phase uncontrollable full-wave rectifiers***, but the diodes are replaced with thyristors. In comparison with the uncontrollable diodes, thyristors can be controlled. Thyristors need a forward voltage and a trigger (a current pulse on the gate) to conduct. If one these two conditions is not satisfied, the thyristor will not conduct. It is important to notice we are not able to control when the thyristor stops conducting. This off-state occurs when the current of the thyristor is lower than the hold current. An ideal thyristor has a zero hold current implying the off-state obtained when the current through the thyristor achieves zero.

Controlling the trigger (current pulse on the gate), it is possible to control the instant of the time the thyristor starts conducting. A thyristor can start conducting at the same instant of

time a diode would start conducting implying the thyristor behaves similar with a diode. It is possible to delay the trigger which delays the conducting behavior of the thyristor. In this way the mean value of the rectified DC-voltage can be varied by varying the trigger or firing point which will be indicated by the firing angle α.

Single-phase controllable half-wave rectifier with resistive load

Fig. 3.12 shows a single-phase controllable half-wave rectifier including the gate controller for the thyristor. Similar with the conclusions in paragraph 0 ***Single-phase uncontrollable half-wave rectifiers***, this circuit can only rectify the positive alternation of the grid voltage.

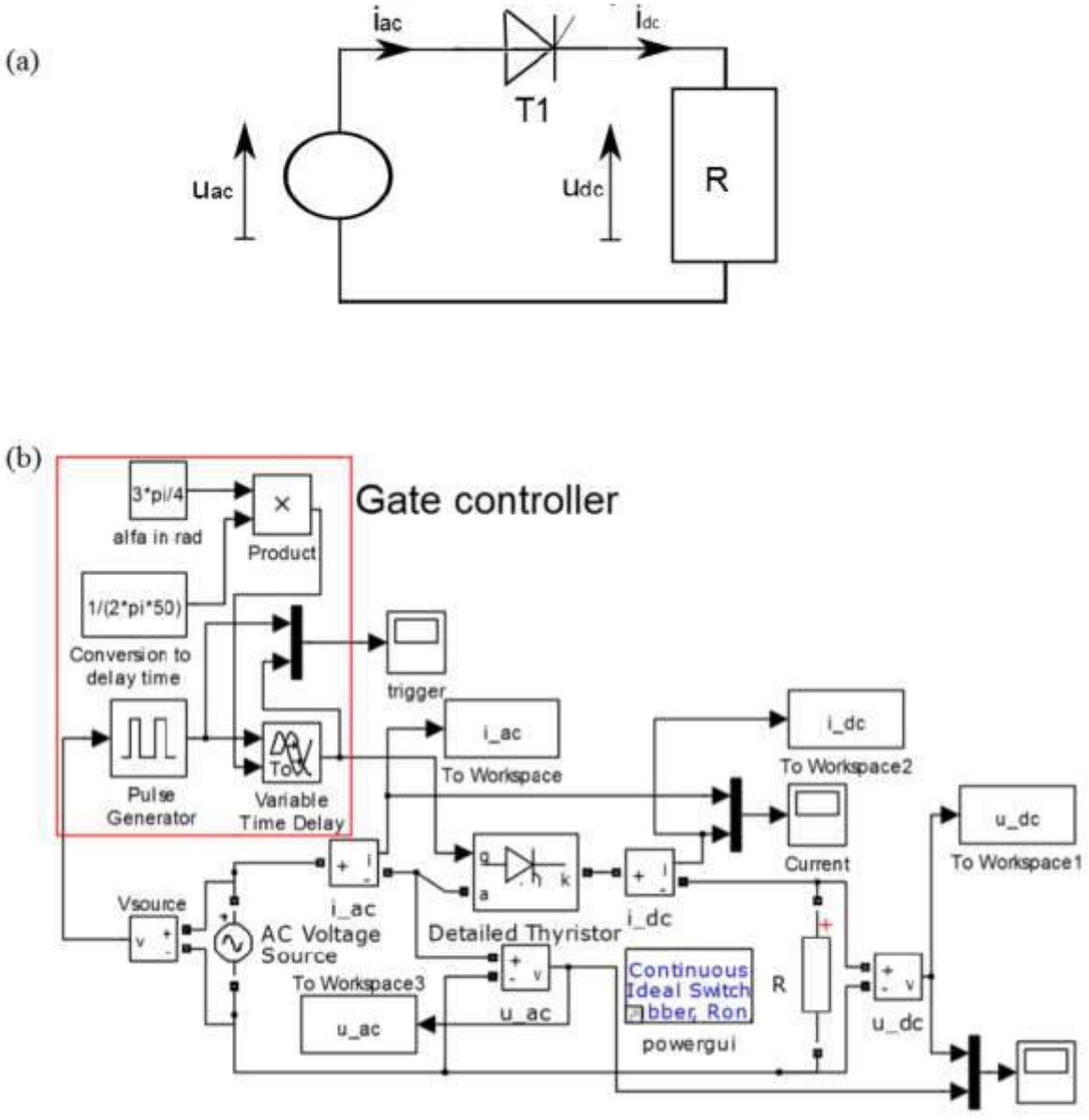


Fig. 3.12. The circuit of the single-phase controllable half-wave rectifier with gate controller: (a) electrical circuit (b) Simulink model

The main difference is the necessity to inject a current pulse to the gate of the thyristor in order to allow the thyristor to conduct. This is shown in Fig. 3.12 with the gate controller. First the earliest possible firing point must be determined (the zero crossing of the applied grid voltage). In the case of a single phase uncontrollable full-wave bridge rectifier, this point is

the start of the positive alternation of the grid voltage, i.e. the point where the diode starts to conduct. By measuring the voltage of the grid, this point can be determined. At this point, a current pulse should be sent to the thyristor in order to behave like the diode. This point is the reference point of the firing angle α. When the thyristor has to be activated an angle α later, this angle is converted to a time delay (depending on the grid frequency). This happens in the red box in Fig. 3.12(b).

When applying a firing angle $\alpha = 3\pi/4$, the waveform of the DC-voltage is shown in Fig. 3.13. When triggering the gate, the thyristor starts conducting. Since the load of the rectifier is a resistor, the thyristor switches off at the next zero crossing of the grid voltage where the current through the thyristor achieves zero. This means the switch-off point of the thyristor does not change with changing of α. This is important when calculating the mean DC-value of the rectified voltage. By applying equation (3-1) for Fig. 3.13 using the parameter α gives (with θ the period of the DC-voltage which equals 2π):

$$U_{DC,\alpha} = \frac{1}{\theta}\int_0^{\theta} u_{dc}(\omega t)\,d\omega t = \frac{1}{2\pi}\int_{\alpha}^{\pi} \sqrt{2}U_{ac}\sin(\omega t)\,d\omega t = \frac{\sqrt{2}}{2\pi}U_{ac}(1+\cos(\alpha))$$

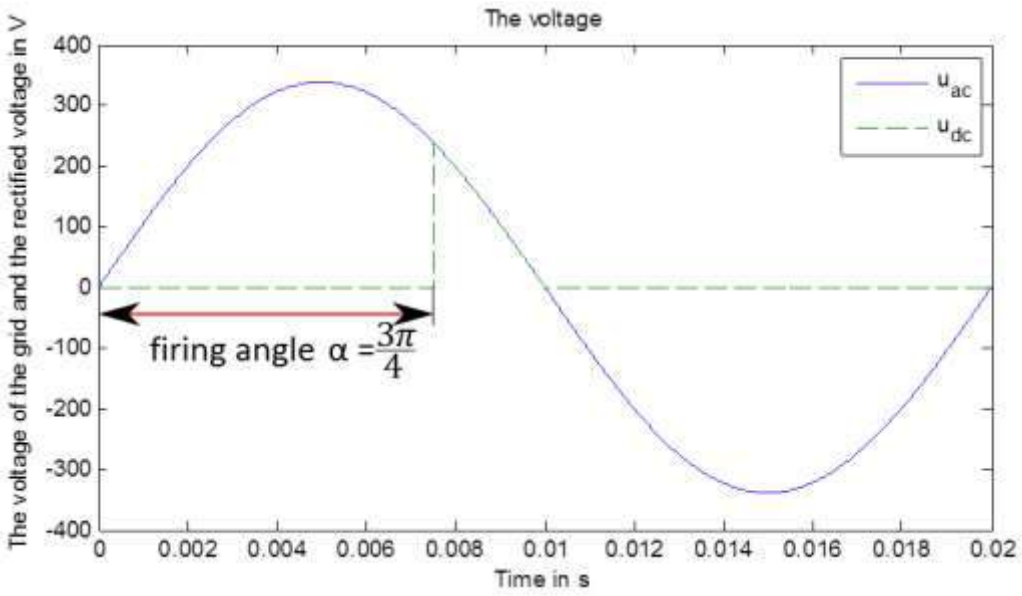


Fig. 3.13. The DC-voltage obtained by the single-phase controllable half-wave rectifier having a firing angle 3π/4, a grind voltage with an rms value of 240V and a frequency of 50Hz. The load is resistive.

The DC-voltage can be controlled by changing the firing angle α giving a mean value proportional with $(1 + cos\alpha)/2$ (the firing angle has a value between 0 and π). When the firing angle is larger than π, the grid voltage is negative when the current pulse is injected into the gate which implies the thyristor will not switch on. Due to the resistive load, the instantaneous value of the load current is proportional with the DC-voltage implying the current has the same shape and the same phase as shown in Fig. 3.14. This property is not obtained when the load is not strictly resistive as explained in paragraph ***Single-phase controllable full-wave bridge rectifier with non-resistive load***.

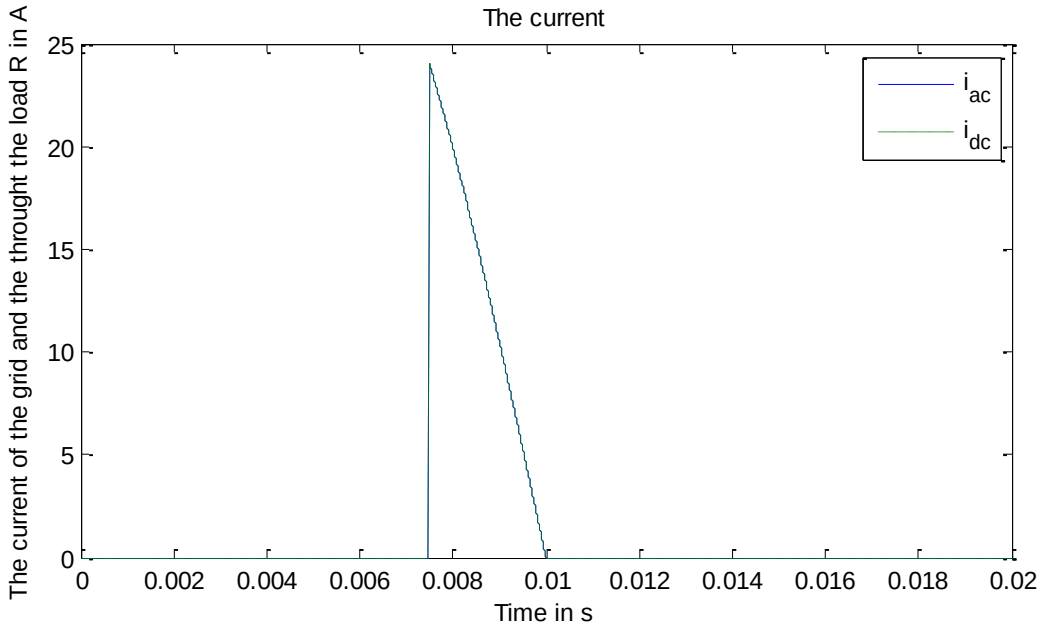


Fig. 3.14. The grid current iac and the load current idc for a single-phase controllable half-wave rectifier with a firing angle $\alpha = 3\pi/4$

The harmonic distortion of the grid current obtained by equations (3-6), (3-7) and (3-8) and the ripple factor of the DC-voltage defined by equation (3-9) both depend on the firing angle α as shown in Table 3-1.

Table 3-1. The THD and RF of the single-phase controllable half-wave rectifier for different firing angles

Firing angle α in rad	THD of i_{ac} equation (3-6) in %	THD of i_{ac} equation (3-7) in %	THD of i_{ac} equation (3-6) in %	RF of u_{dc} equation (3-9)
0	43.52	100	39.91	1.21
$\frac{\pi}{6}$	55.00	102.26	48.19	1.32
$\frac{2\pi}{6}$	79.84	113.35	62.39	1.59
$\frac{3\pi}{6}$	112.68	135.88	74.79	1.98
$\frac{4\pi}{6}$	160.45	176.25	84.87	2.59
$\frac{5\pi}{6}$	225.78	265.52	93.13	3.8544
$\frac{179\pi}{180}$	1545	1547	99.8	21.90
π	NaN	NaN	NaN	NaN

As shown in Table 3-1 the THD of the grid current and the RF of the DC-voltage increase with the increasing of firing angle. When calculating the THD, notice that equations (3-9) and (3-7) converge to each other as the firing angle increases. With the increasing of firing angle, the mean DC-voltage becomes lower while the harmonic distortion of the grid current

increases. When the firing angle equals π, the grid current as well as the DC-voltage are zero explaining why the THD and the RF is "Not a Number" (NaN).

Single-phase controllable full-wave bridge rectifier with resistive load

Fig. 3.15 shows the circuit of the single-phase controllable full-wave rectifier and the controller needed to send pulses to the gates of the thyristors. Similar with the results available in paragraph 0 ***Single-phase uncontrollable full-wave rectifiers***, this circuit rectifies the positive and the negative alternations of the grid voltage. The main difference originates from the required current pulses on the gates of the thyristors allowing these thyristors to conduct the current. This is shown in Fig. 3.12 containing the gate controller.

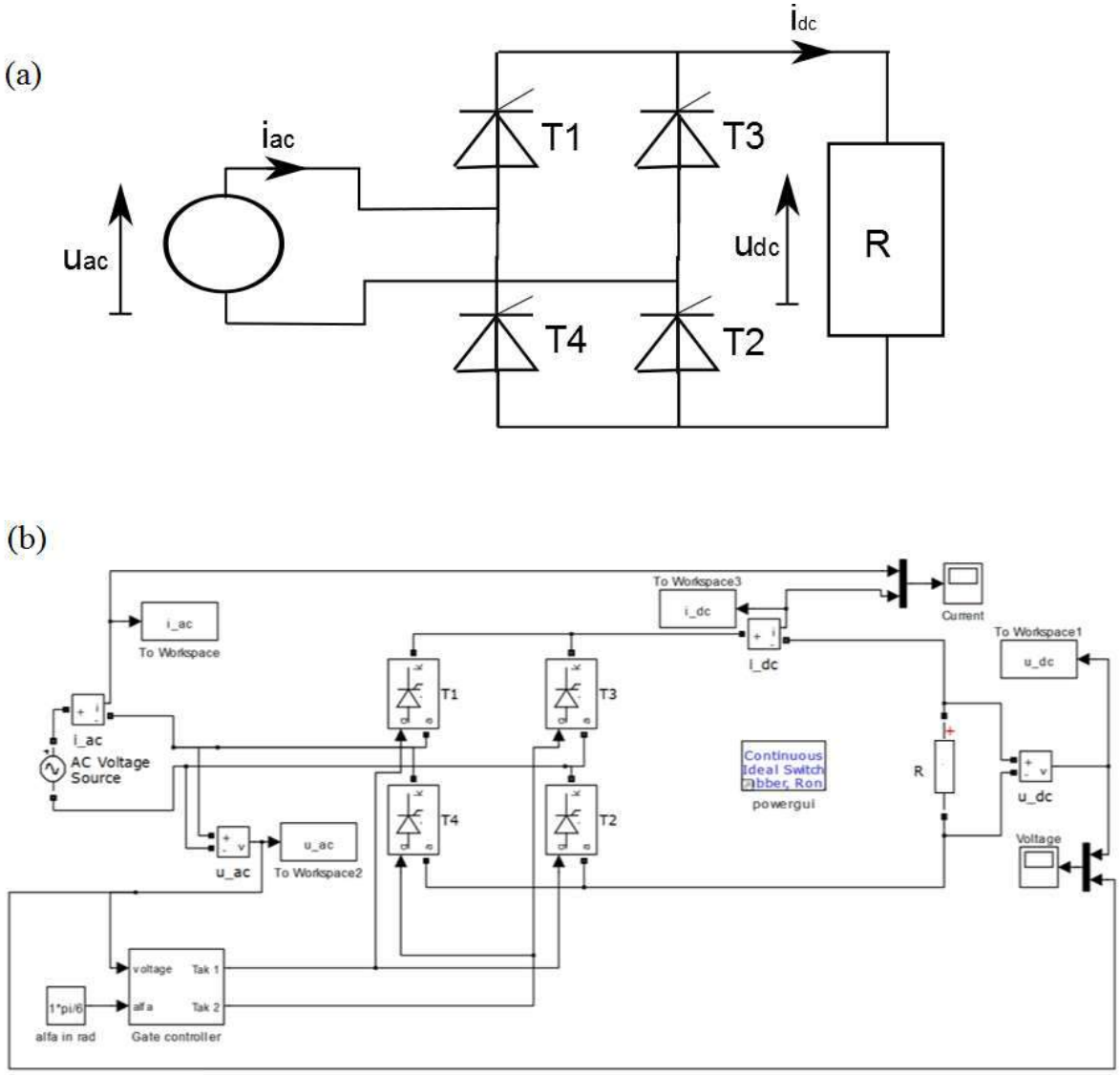


Fig. 3.15: The circuit of the single-phase controllable full-wave bridge rectifier with gate controller: electrical circuit (a) Simulink model (b)

The working principle of the controller generating the pulses to the gates first of all needs to determine the earliest possible firing points (corresponding with the zero crossings of the grid voltage). Such a point is the start of the positive alternation of the grid voltage for thyristors T1 and T2 (the point where the diodes D1 and D2 of the uncontrollable rectifier

start to conduct). Such a point is the start of the negative alternation of the grid voltage for thyristors T3 and T4 (the point where the diodes D3 and D4 of the uncontrollable rectifier start to conduct). By measuring the voltage of the grid, these starting points can be located. At such a point, a current pulse should be sent to the thyristors (T1 and T2 or T3 and T4) in order to behave like diodes.

These points are the reference points for the firing angle α. It is important the firing angle α for T1 and T2 is the same as the firing angle α for T3 and T4, since implementing twice the same firing angle is easier and the obtained THD and RF are better. When the thyristors have to be activated an angle α later, this angle is converted to a time delay (depending on the grid frequency) and the thyristors are fired after this delay by the gate controller in Fig. 3.15.

When applying a firing angle $\pi/6$, the waveform of the DC-voltage is shown in Fig. 3.16. Since the load of the rectifier is a resistor, the thyristors switch off when the grid voltage becomes zero. Indeed, at this point the current through the thyristors is zero. This means the switch-off points of the thyristors do not change as α changes. By applying equation (3-1), the mean value of the rectified DC-voltage which depends on the angle α can be calculated. Based on Fig. 3.16 (notice the period of the DC-voltage equals to π), the mean value of the DC-voltage equals to:

$$U_{DC,\alpha} = \frac{1}{\theta}\int_0^{\theta} u_{dc}(\omega t)\, d\omega t = \frac{1}{\pi}\int_{\alpha}^{\pi} \sqrt{2}U_{ac}\sin(\omega t)\, d\omega t = \frac{2\sqrt{2}}{\pi}U_{ac}\frac{(1+\cos(\alpha))}{2}$$

The DC-voltage can be controlled by the firing angle α and the mean value is proportional with $(1+cos\alpha)/2$ (if the firing angle has a value between 0 and π). The mean value of the DC-voltage is twice the mean value of the DC-voltage in the case of a half-wave rectifier.

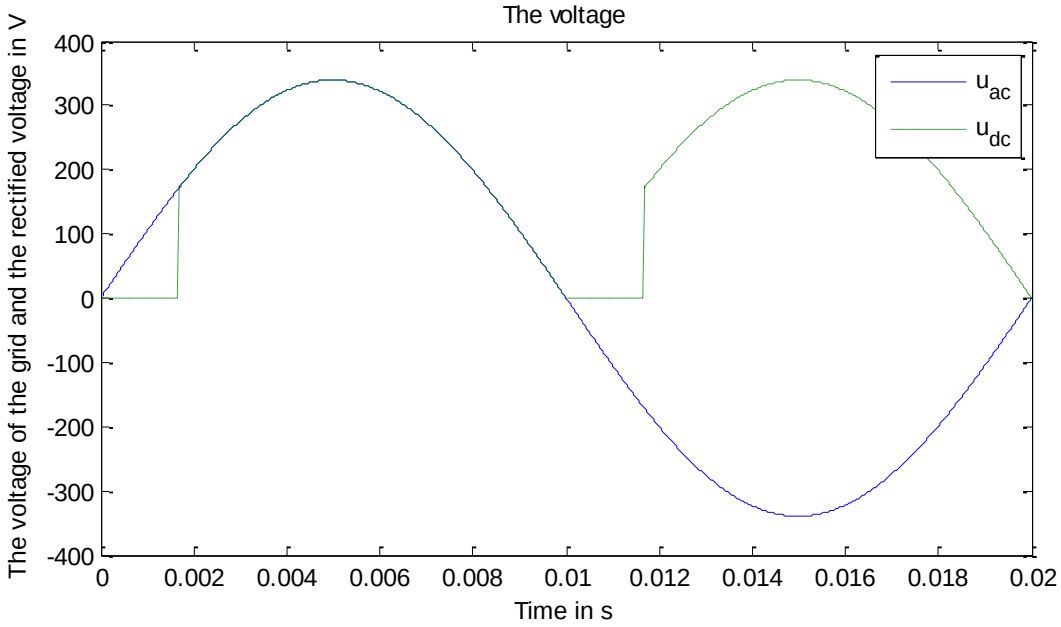


Fig. 3.16. The obtained DC-voltage by the single-phase controllable full-wave bridge rectifier with a firing angle $\alpha = \pi/6$, a grid voltage with an rms value of 240V and a frequency of 50Hz. The load is resistive.

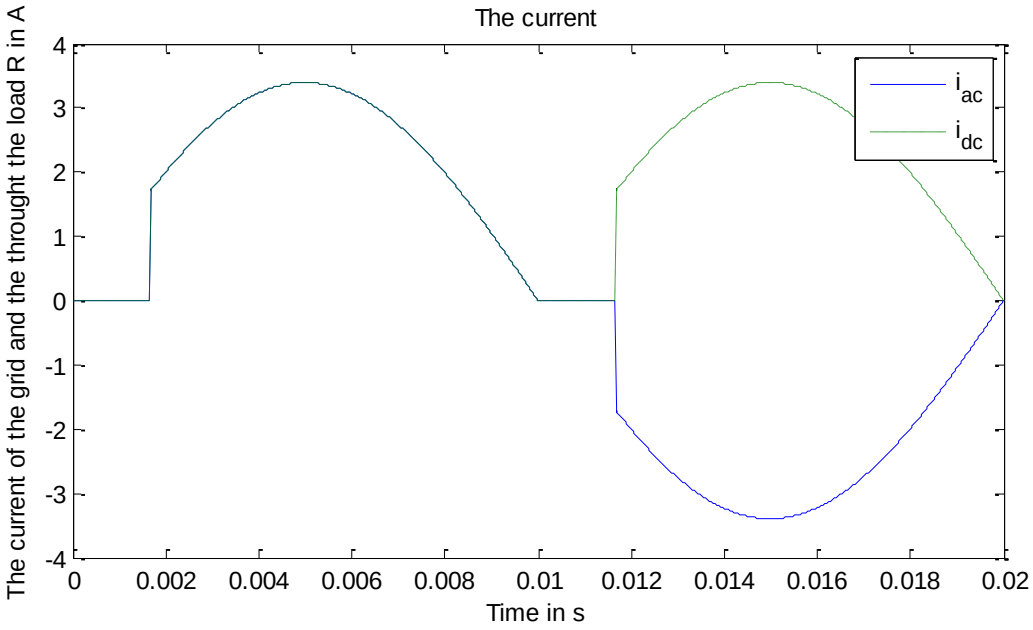


Fig. 3.17. The grid current iac and the load current idc for a single-phase controllable full-wave rectifier with a firing angle $\alpha = \pi/6$

When the firing angle is larger than π, the grid voltage is negative when firing T1 and T2 or the grid voltage is positive when firing T3 and T4. This implies the thyristors will not switch on since the forward voltages across the thyristors are negative. This is not always the case when the load is not strictly resistive, but this is explained in paragraph ***Single-phase controllable full-wave bridge rectifier with non-resistive load***.

Due to the resistive load, the instantaneous value of the load current is proportional to the output voltage implying the load current has the same shape and phase as visualized in Fig. 3.17. The harmonic distortion of the grid current is given in equations (3-6), (3-7) and (3-8). The ripple factor of the DC-voltage is defined by equation (3-9) and depends on the firing angle α as shown in Table 3-2.

Table 3-2: The THD and the RF of the single-phase controllable full-wave rectifier for different firing angles

Firing angle α in rad	THD of i_{ac} equation (3-6) in %	THD of i_{ac} equation (3-7) in %	THD of i_{ac} equation (3-6) in %	RF of u_{dc} equation (3-9)
0	0	0	0	0.483
$\frac{\pi}{6}$	15.12	15.12	14.95	0.614
$\frac{2\pi}{6}$	37.75	37.75	35.32	0.875
$\frac{3\pi}{6}$	65.08	65.08	54.54	1.21
$\frac{4\pi}{6}$	102.65	102.65	71.63	1.69
$\frac{5\pi}{6}$	174.00	174.00	86.70	2.63
$\frac{179\pi}{180}$	1102	1102	99.6	15.61

π	NaN	NaN	NaN	NaN

As shown in Table 3-2, the THD of the grid current and the RF of DC-voltage increase as the firing angle increases. When determining the THD of the grid current, notice that equations (3-6) and (3-7) are equal to each other. Indeed, this rectifier does not introduce a DC-component in the grid current implying equations (3-6) and (3-7) are exactly the same. When the firing angle is equal to π, the grid current as well as the DC-voltage are zero explaining why the THD and the RF are "Not a Number" (NaN).

Single-phase controllable full-wave bridge rectifier with non-resistive load

As already mentioned, the load will have a large influence on the conductive behavior of the thyristors. In the case of a resistive load, the load current and the DC-voltage have the same shape and phase. Notice however this is not the case when considering inductive-resistive loads, capacitive-resistive loads and active loads. Here, we will restrict ourselves to the inductive-resistive case and in part three the other load types will be studied in the case of a single-phase controllable full-wave bridge rectifier.

An inductor opposes a current change. Equation (3-10) shows the well-known relationship between the change of the current i_L through the inductor and the voltage u_L across the inductor.

$$\mathbf{u_L = -L\frac{di_L}{dt}} \tag{3-10}$$

When using this formula, two important remarks must be made. The first remark highlights that in equation (3-10), where the minus sign due to Lenz law is taken into account, the direction of the voltage coinsides with the direction of the current. When the magnitude of the current increases the sign of the voltage u_L opposes to that of the current. In this case, the coil is transforming electric energy into magnetic energy i.e. the coil is consuming electrical energy. When the magnitude of the current decreases the sign of the voltage u_L equals to that of the current. In this case the coil is transforming earlier stored magnetic energy into electrical energy the inductor behaves as an electrical source.

The second remark highlights that when the inductor current i_L is a constant DC current, the voltage across this inductor equals zero. When the mean value of the current i_L is a constant DC current, the mean value of the voltage across this inductor will also be zero. When integrating the positive part of the voltage U_L and when integrating the negative part of the voltage U_L, the same value is obtained.

Understanding the behavior of the inductor is important to study the working principle of a lot of power electronic circuits. This is also the case for the circuit shown in Fig. 3.18.

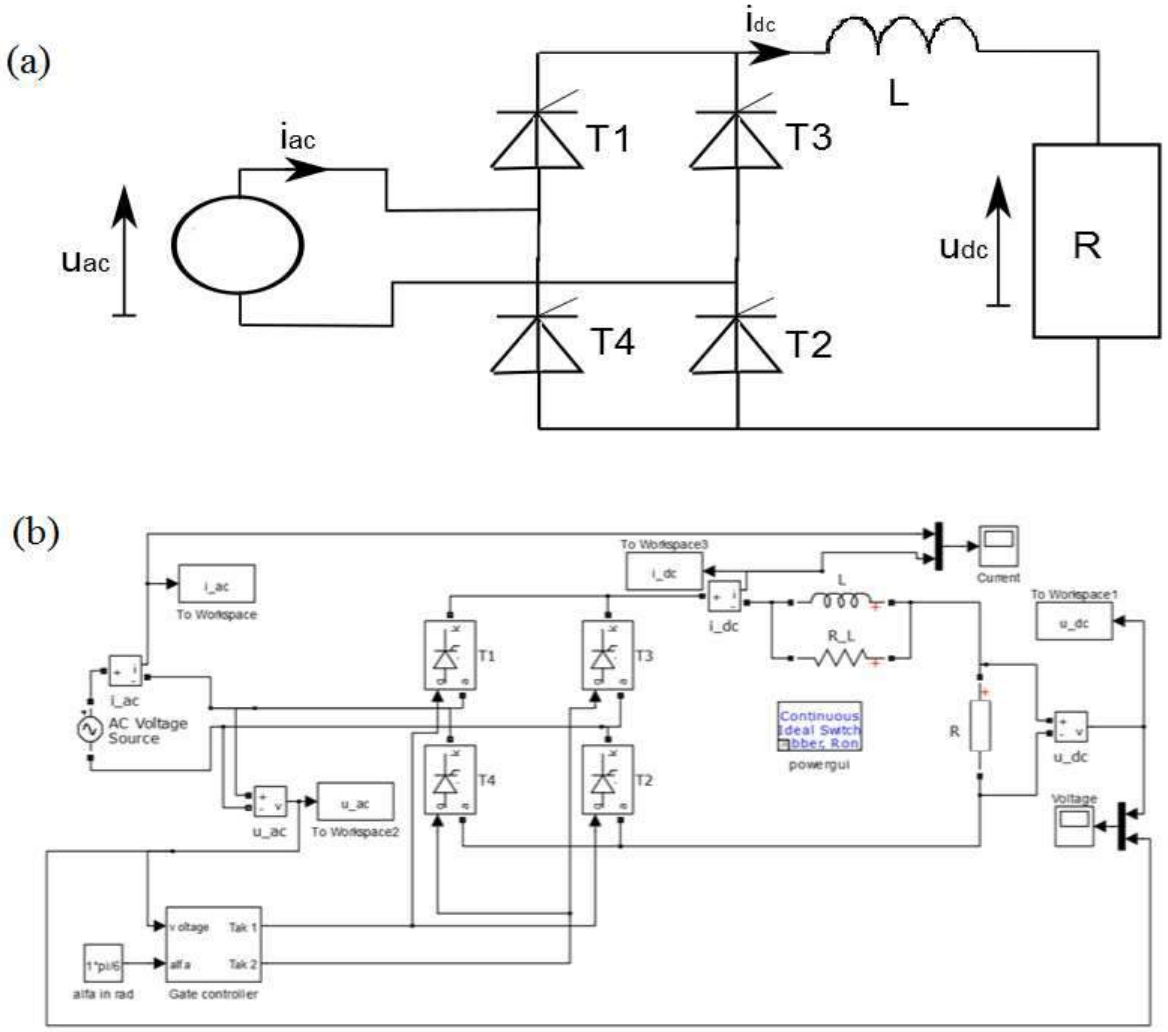


Fig. 3.18. The circuit of the single-phase controllable full-wave bridge rectifier with inductive-resistive load: (a) electrical circuit (b) Simulink model

In Fig. 3.18, at DC-side an inductor L is placed is series with the load resistor R. In the present text, three values for the inductor will be considered - a very high value of 200mH, a normal value of 20mH and a low value of 5mH. The restive load has a value of 10 Ω. For simulation reasons, an additional resistor R_L in parallel with the inductor L is needed. This resistor can be omitted when discussing the working principle since it has a large simulation value of 1e5 Ω. The grid voltage and the DC voltage across the load are visualized in Fig. 3.19. The grid current and the load current are visualized in Fig. 3.20.

Before discussing the simulation results, notice that these results are obtained in steady-state. It is important to see that the ripple on the DC-voltage has almost disappeared when using the large inductor value of 200mH (the visualized DC-voltage is the DC-voltage over the resistance R). In general, the inductor is used to obtain a constant current since an ideal inductor has almost no practical applications when fed by a DC-source. The inductor is mainly used as a filter. As the inductor value decreases, the ripple in the current increases implying also the ripple in the output voltage u_{dc} increases. When comparing it with the purely resistive load, i.e. without any inductor at DC-side, the ripple of the DC-voltage is strongly reduced when using the inductor of 20mH (Fig. 3.16.). The ripple reduction due to an inductor of 5mH is also noticeable but smaller than that when considering 20mH.

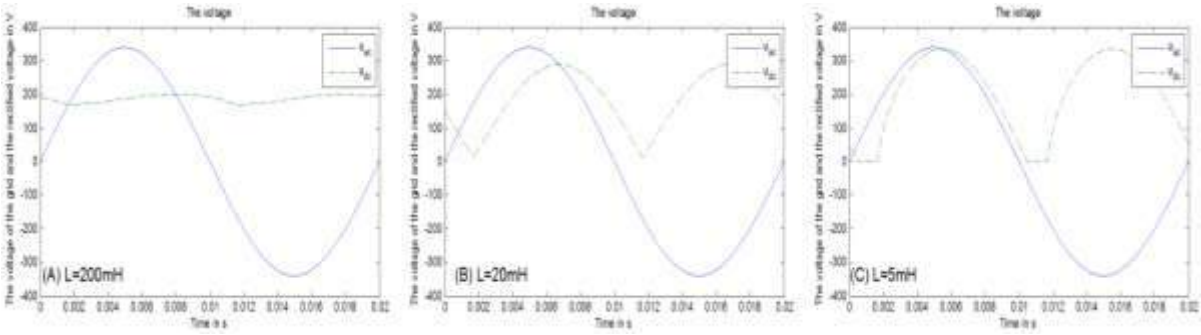


Fig. 3.19: The DC-voltage of the single-phase controllable full-wave bridge rectifier with a firing angle$\alpha = \pi/6$, a grid voltage with an rms value of 240V and a frequency of 50Hz. Using an inductor of 200mH (a), 20mH (b), 5mH (c).

When the thyristors T1 and T2 switch on, the output current starts to rise. As the current rises, the inductor consumes electrical energy and transforms this energy into magnetic energy. While storing this energy, the current still increases since the voltage u_{ac} is larger than u_{dc} giving a negative voltage across the inductor. As u_{dc} rises, the voltage drop across the inductor becomes less negative and finally becomes zero which implies the DC-current attains a maximum.

At this point, u_{dc} equals u_{ac} and the forward voltages across the thyristors T1 and T2 become zero. If these thyristors would switch off immediately, the instantaneous current change would be very large which is impossible due to the inductor. The inductor appears as an electrical source (transforming the stored magnetic energy back into electrical energy) which lowers the voltage level at the cathode of thyristor T1 and increases the voltage level at the anode of thyristor T2. Due to the positive voltage across inductor, the forward voltage of these thyristors remains higher than zero and they remain conducting. Notice however the DC-current flowing through the inductor decreases.

At this point, the magnetic energy in the inductor starts to decrease implying the current decreases. The higher the inductance of the coil, the more magnetic energy is stored and the slower the current decreases. When the inductor has a very large inductance (situation (a)) the current almost does not decrease and the current does not become zero. Even an angle π after firing thyristors T1 and T2, the current is still flowing.

At this point, since the firing angle α is the same for T1, T2, T3 and T4, thyristors T3 and T4 get a current pulse on their gates. In Fig. 3.19 (a), this happens at the instant of time 12ms where the anode voltage is larger at T3 than at T1. The cathode voltages of T1 and T3 are the same (equal to the anode voltage of T1 since the thyristors are ideal). At the same time, the cathode voltage of T4 is smaller than the cathode voltage of T2. The anode voltages of T2 and T4 are the same (equal to the cathode voltage of T2 since the thyristors are ideal).

Since the conditions for firing the thyristors T3 and T4 are satisfied, these two thyristors will switch on. Due to the ideal behavior of the thyristors, the cathode voltages of T1 and T3 will equal the largest anode voltage of T1 and T3, i.e. the anode voltage of T3. Due to this process, the cathode voltage of T1 is larger than its anode voltage and T1 switches off. A similar process occurs between T2 and T4, but the anode voltages of T2 and T4 will be equal to the smallest cathode voltage of T2 and T4, i.e. the anode voltage of T4. Due to this process, the cathode voltage of T2 is larger than its anode voltage and T2 switches off.

The process of transferring the current from T1 and T2 to T3 and T4 is called commutation and this process will be explained in more detail later on. After the commutation, the load current is delivered by thyristors T3 and T4. If the magnitude of u_{dc} is still larger than u_{ac}, the coil will still function as an electrical source while the DC-current decreases (the inductor voltage is positive). When the situation occurs that the magnitude of the voltage u_{ac} is larger than u_{dc}, the voltage across the inductor regains its negative value. The inductor stores energy since the current i_L increases.

Indeed, from Fig. 3.18. it is clear that $u_L = u_{dc} - u_{ac}$ and if u_{ac} is larger than u_{dc}, the inductor voltage u_L is negative. This implies energy is stored in the inductor. The current $i_L(=i_{dc})$ still increases until u_{dc} becomes equal to u_{ac}. From this point on, the inductor will act as an electrical source to prevent a switching off of the thyristors until the period π passes again after the fringing angle α and the current pulse fires thyristors T1 and T2.

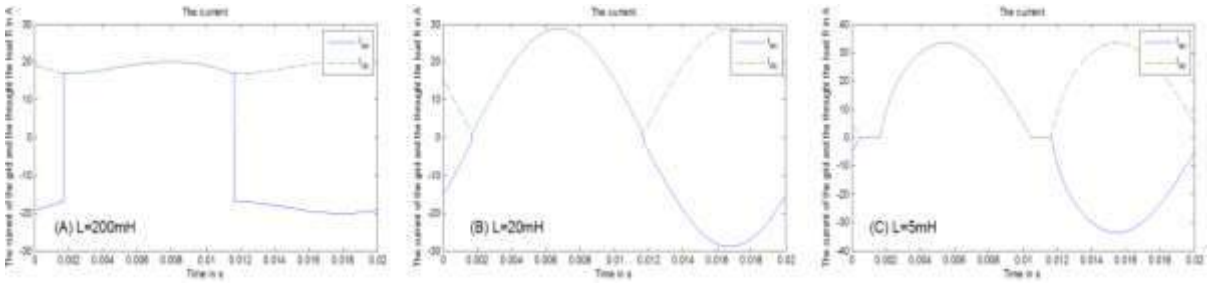


Fig. 3.20. The grid current iac and the load current idc for a single-phase controllable full-wave rectifier with a firing angle $\alpha = \pi/6$. Using an inductor of 200mH (a), 20mH (b), 5mH (c).

The main differences between the situations (a) and (b) in Fig. 3.19. and Fig. 3.20. are the wave-forms. Also in situation (b) commutation occurs but due to the smaller inductor value the ripple on the DC-voltage is larger (as visualized in Fig. 3.19.). Due to this phenomenon, sometimes an additional inductor is placed in the DC-circuit in order to obtain a smoother DC-current implying a smoother DC-voltage across the resistor. This inductor functions as a low pass filter.

Associated with this advantage, there is also a disadvantage. As visualized in Fig. 3.20., in situation (a) the grid current resembles a square wave, while grid current in situation (b) resembles a sine wave. This will be proven when the THD and the RF are determined for these three situations. Before studying situation (c), the mean values of the DC-voltages for situations (a) an (b) are calculated using equation (3-1) (with θ the period of the DC-voltage which equals π):

$$U_{DC,\alpha} = \frac{1}{\theta}\int_0^{\theta} u_{dc}(\omega t)\, d\omega t = \frac{1}{\theta}\int_0^{\theta} u_{ac}(\omega t)\, d\omega t = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} \sqrt{2}U_{ac}\sin(\omega t)\, d\omega t$$
$$= \frac{2\sqrt{2}U_{ac}}{\pi}\cos(\alpha)$$

As long the thyristors conduct, the grid voltage is fed to the DC-load. The inductor functions as a filter in order to obtain across the resistor an output voltage with smaller variations. The inductor acts as a current source and keeps the current constant. In case the firing angle equals $\pi/6$, the mean value of the output voltage equals $\frac{2\sqrt{2}240}{\pi}\cos\left(\frac{\pi}{6}\right) = 187.12\ V$ as shown in Fig. 3.19.

The larger the inductor, the more the grid current approximates a square wave. As the inductor value goes to infinity, the grid current converges to an ideal square wave. The Fourier series applied on such a square wave gives a spectrum containing only odd ordered harmonics and an n-th order harmonic component has a magnitude which is inversely proportional with n. This leads to a THD of 48.4% by using equations (3-6) and (3-7). This square wave is shifted in time with respect to the grid voltage and this time shift is proportional with the firing angle α. Since the zero crossings of the fundamental component coincide with the zero crossings of the square, this first order harmonic lags an angle $\varphi = \alpha$ with respect to the grid voltage.

Notice that the $\cos(\varphi)$ value does not equal the power factor (PF) due to the higher order current harmonics. The definition of the power factor is given in equation (3-11) and in the case of a single phase controlled full wave bridge rectifier with a large inductive load and sinusoidal grid voltage,

$$PF = \frac{P}{S} = \frac{U_{ac} I_{ac,1} \cos(\varphi)}{U_{ac} I_{ac}} = \frac{I_{ac,1} \cos(\alpha)}{I_{ac}} \tag{3-11}$$

The power factor depends on the firing angle and the ratio between the RMS value of the fundamental current component and the RMS value of the entire grid current. This allows prove that

$$PF = \frac{\cos(\alpha)}{\sqrt{1 + THD^2}}$$

Here, THD denotes the Total Harmonic Distortion of the grid current. When considering situation (c), an additional phenomenon occurs instead of the commutation behavior. After firing thyristors T1 and T2, the DC-current increases until u_{dc} equals u_{ac} and meanwhile the inductor stores magnetic energy. When u_{dc} equals u_{ac}, the current gains its maximum value. When u_{dc} becomes larger than u_{ac}, the inductor voltage becomes positive implying the DC-current decreases according to equation (3-10). The inductor transforms the stored magnetic energy back into electrical energy and prevents a switching off of thyristors T1 and T2.

The smaller the inductor, the smaller the amount of magnetic energy stored in the inductor corresponding with the same current. This implies the current will decrease faster when the inductance is smaller. This means the inductor current i_L has a larger probability to reach zero in the period π. If i_L becomes zero, also the current in the thyristors T1 and T2 becomes zero. This implies T1 and T2 switch off and during the remainder of the period π the output voltage and the output current remain zero.

The situation changes when firing the thyristors T3 and T4 by current pulses in their gates. The earlier described phenomenon repeats itself when firing T3 and T4 instead of T1 and T2 i.e. the load current increases, reaches a maximum and goes back to zero. This process is called discontinuous conduction mode. In the case of discontinuous conduction mode, it is more difficult to calculate the mean value of the current since one also needs to calculate the instant of time where the current becomes zero.

Table 3-3: The THD and the RF of the single-phase controllable full-wave bridge rectifier for different firing angles when feeding an inductive-resistive load

Firing angle α in rad	THD of i_{ac} equation (3-6) in %			THD of i_{ac} equation (3-7) in %			THD of i_{ac} equation (3-6) in %			RF of u_{dc} equation (3-9) in %		
	(A)	(B)	(C)	(A)	(B)	(C)	(A)	(B)	(C)	(A)	(B)	(C)
0	47.96	29.11	6.22	47.96	29.11	6.22	43.24	27.95	6.20	0.03	0.30	0.46
$\frac{\pi}{6}$	42.46	2.15	10.66	42.47	2.15	10.66	39.09	2.15	10.59	0.06	0.45	0.58
$\frac{2\pi}{6}$	32.45	15.81	30.92	32.45	15.81	30.92	30.86	15.61	29.54	0.14	0.65	0.82
$\frac{3\pi}{6}$	8.09	36.30	54.91	8.09	36.30	54.91	8.07	34.12	48.13	0.58	0.90	1.10
$\frac{4\pi}{6}$	40.91	63.67	86.03	40.91	63.67	86.03	37.87	53.71	65.22	0.95	1.23	1.50
$\frac{5\pi}{6}$	97.63	113.7	139.1	97.63	113.7	139.1	69.86	75.09	81.18	1.65	1.85	2.18
π	NaN			NaN			NaN			NaN		

To study the influence of the firing angle α on the THD of the grid current and on the RF of the rectified voltage, the results of Table 3-3 are useful. Three different inductor values are considered, i.e. 200mH (situation (A)), 20mH (situation (B)) and 5mH (situation (C)). In Table 3-3, the firing angles giving discontinuous conduction mode are marked in yellow. Notice the THD of the grid current i_{ac} decreases as the firing angle increases, as long as no discontinuous conduction mode occurs. As the firing angle α increases, the shorter the time provided to the inductor to store magnetic energy. This implies a larger variation in the grid current which also means this current resembles more a sinus wave implying a smaller THD.

When the firing angle is too large in relationship with the inductor value, the inductor is not able to be an electrical source over the entire period π. In such a situation, the discontinuous conduction mode occurs and the THD increases as the firing angle increases. Indeed, when the firing angle is larger the more the grid current approximates a current pulse. This implies the deviation from the ideal shaped sine wave increases and also the THD increases. The grid current wave was sinusoidal the moment just before the discontinuous conduction mode occurs implying at this firing angle the THD equals zero.

Indeed, by changing the inductor value to 18.38mH in combination with a firing angle $\alpha = \pi/6$ the THD obtained by equations (3-6), (3-7) and (3-8) equals 0.0033%. Moreover, $\varphi = \varphi = \pi/6$.

Commutation

As already mentioned, during the commutation process the load current is transferred from one switching element to another switching element. In the present case, the switching elements are thyristors. It is important to notice that the commutation occurs when the current delivered by the grid is not zero. In this case, one speaks of forced commutation.

In the present case, it is the large inductor at the DC-side which tries to keep the current constant. The case when the commutation process occurs instantantly, i.e. with zero time delay, causes problems. This implies the current of the thyristor which is switching off, should go from the load current to zero instantly. At the same moment, the current of the thyristor which is switching on should go from zero to the load current also instantly. When considering a real thyristor there is not only a maximum allowed current, there is also a maximum change in the current. When the derivative of the current trough the thyristor is too large (due to a current rise) hot spots are created inside the thyristor. Shortly after firing this thyristor, this local hot spot exists since only a part of the thyristor close to the gate conducts. Some time is needed before the whole thyristor conducts implying the current rise must be limited. When the current rise is too high, the elements are overheated and the thyristor can be damaged. To protect the thyristors, the commutation process requires some time interval.

Fortunately, there is a process which opposes the fast change of the thyristor current. The grid impedance is not resistive but inductive-resistive and its inductive part opposes the fast current change. This process is visualized in Fig. 3.21. Fig. 3.21 part (b) is a transformed circuit based on Fig. 3.18. In order to obtain the same results, the inductance value must be transformed. For the single-phase controlled full-wave bridge rectifier, $L_{net}^{*}=2L_{net}$ is needed since the current changes from $-I_{dc}$ to I_{dc} in the commutation time whereas in the transformed model the current changes from 0 to I_{dc}. By doubling the grid inductance, the same voltage drop occurs while the range of the current changes half. The commutation process can be divided in three parts:

1. Just before the current pulse in the gate, only thyristor T_a is active that means the load current I_{dc} equals the current i_{Ta} through thyristor T_a. The instantaneous DC-voltage u_{dc1} equals the voltage u_a.
2. Just after the current pulse in the gate where thyristor T_b is fired, thyristor T_a is not switched off yet. By applying Kirchhoff's current law at the cathodes of thyristors T_a and T_b, one obtains that $I_{dc} = i_{Ta} + i_{Tb}$. The current i_{Ta} is decreasing and the current i_{Tb} is increasing as long as the commutation occurs and its duration equals μ. The larger the grid impedance and the larger I_{dc}, the larger μ.
3. When the commutation process is completed, the current i_{Tb} through thyristor T_b equals the load current I_{dc} and the instantaneous DC-voltage u_{dc1} equals the voltage u_b. The current i_{Ta} through thyristor T_a equals zero.

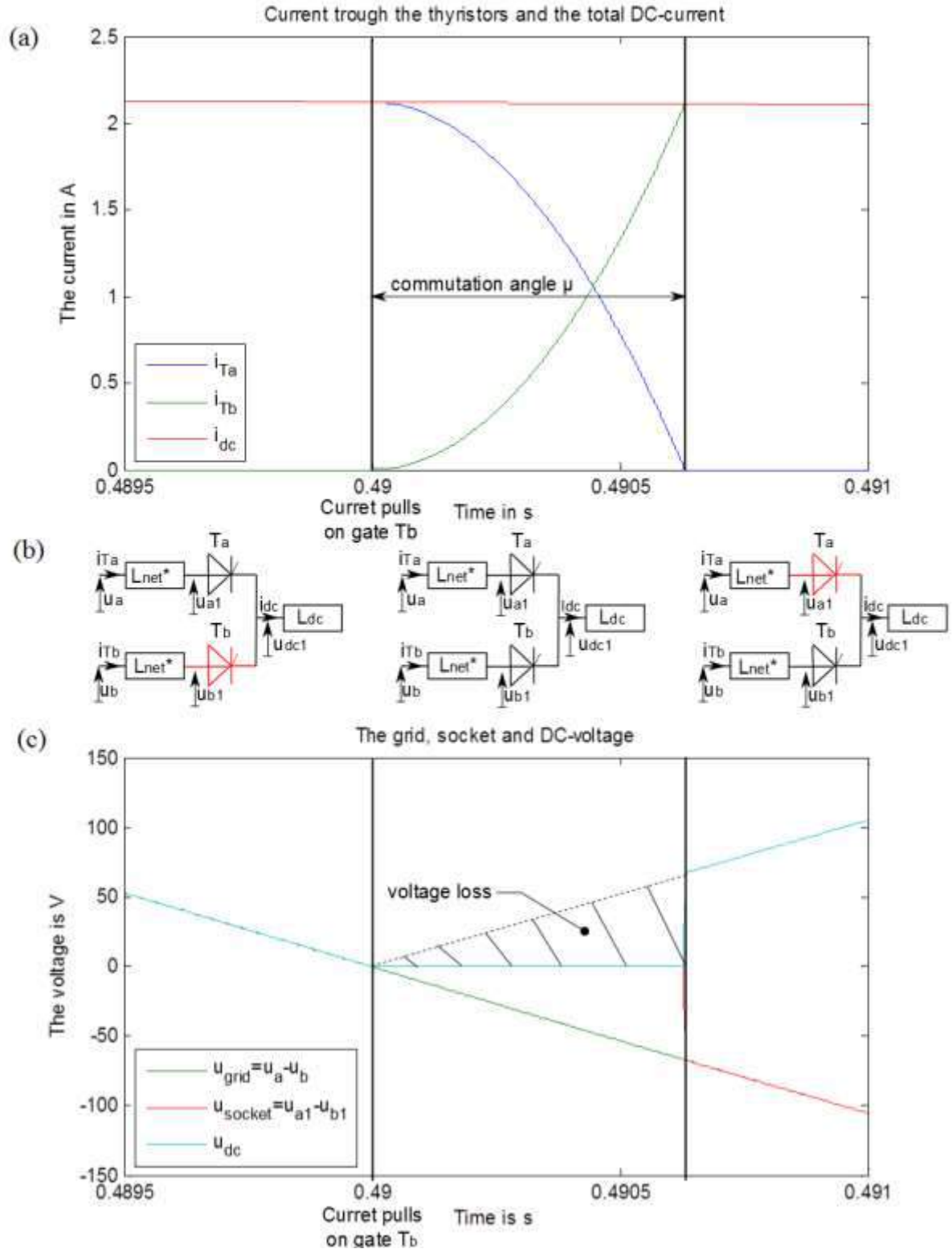


Fig. 3.21: Commutation process, the evolution of the current trough the thyristors and the DC-coil (a), the change in conduction of the thyristors (b) and the evolution of the grid, socket and DC-voltage (c)

During the commutation process, the sum of the currents through thyristors T_a and T_b remains constant i.e. the constant load current (the large DC-coil keeps I_{dc} constant). When applying Kirchhoff's current law at the cathodes of thyristors T_a and T_b , taking the derivative with respect to time and multiplying with the grid inductor L_{net} gives equation (3-12).

$$\mathbf{0} = \boldsymbol{L_{net}} * \frac{di_{Ta}}{dt} + \boldsymbol{L_{net}} * \frac{di_{Tb}}{dt} \quad (3\text{-}12)$$

Substituting equation (3-10) in (3-12) leads to the instantaneous DC-voltage (equation (3-10)) during the commutation

$$\boldsymbol{u_{dc}} = \frac{u_a + u_b}{2} \quad (3\text{-}13)$$

Since we study a single phase controllable full-phase bridge rectifier, u_a equals $-u_b$. This implies the instantaneous DC-voltage is zero during the commutation, as it is visualized in Fig. 3.21. This also means that the mean DC-value will be lower than $\frac{2\sqrt{2}U_{ac}}{\pi}\cos(\alpha)$ due to the commutation process.

Indeed, after firing thyristor T_b an instantaneous DC-voltage equal to u_b was expected. There is a voltage loss due to the commutation process. This can be calculated, but first the duration of the commutation process must be known. The commutation process finishes when the current i_{Tb} through thyristor T_b equals to the load current I_{dc},. Since i_{Ta} equals zero, thyristor T_a is switched off (Kirchhoff's current law $i_{Ta} = I_{dc} - i_{Tb}$). Based on equation (3-10) $\mathbf{u_L} = -\mathbf{L}\frac{\mathbf{di_L}}{\mathbf{dt}}$ and due to (3-13) $\boldsymbol{u_{dc}} = \frac{u_a + u_b}{2}$. This allows to calculate the commutation angle μ by solving equation (3-14):

$$\boldsymbol{I_{dc}} = \boldsymbol{i_{Tb}}(\mu) = -\frac{1}{L_{net}} \int_{\alpha}^{\alpha+\mu} \boldsymbol{u_{dc}}(\boldsymbol{\omega t}) - \boldsymbol{u_b}(\boldsymbol{\omega t})\, \boldsymbol{d\omega t} = \frac{1}{L_{net}} \int_{\alpha}^{\alpha+\mu} \frac{u_b(\omega t) - u_a(\omega t)}{2} \boldsymbol{d\omega t} \quad (3\text{-}14)$$

Equation (3-14) gives the parameters which influence the commutation angle μ:

- The higher the load current I_{dc} the longer it takes i_{Tb} to reach I_{DC} and the larger the commutation angle.
- The higher the inductance of the grid impedance, the slower the rise of the current i_{Tb} and the larger the commutation angle.
- The larger the difference between u_b and u_a, the faster the current i_{Tb} will rise. In case of the single phase controllable full-phase bridge rectifier, $u_a = -u_b$. Equation (3-14) becomes $I_{dc} = \frac{1}{4L_{net}} \int_{\alpha}^{\alpha+\mu} \sqrt{2}\, U_{ac} \sin(\omega t)\ d\omega t$. As the firing angle approaches π/2, the commutation angle μ decreases. As the firing angle approaches 0 or π, the commutation angle increases.

It is possible to calculate the voltage loss due to the commutation process. After the gate current pulse, the instantaneous DC-voltage does not equal u_b but equals $\frac{u_a + u_b}{2}$ as expressed in equation (3-13). The voltage loss due the commutation process can be calculated by integrating the difference between the ideal output voltage and the obtained output voltage:

$$Area_u = \int_0^{\mu} u_b - u_{dc}\, d\omega t = \int_0^{\mu} \frac{u_b - u_a}{2}\, d\omega t = 2L_{net} I_{dc}$$

The commutation losses occur twice each period of the grid voltage (having a pulsation $\omega = 2\pi f$) This leads to equation (3-15), which is the real mean value of the DC-voltage:

$$U_{dc} = \frac{2\sqrt{2}U_{ac}}{\pi}\cos(\alpha) - \frac{2\omega}{2\pi}2L_{net}I_{dc} = \frac{2\sqrt{2}U_{ac}}{\pi}\cos(\alpha) - \frac{2\omega L_{net}}{\pi}I_{dc} \quad (3\text{-}15)$$

The decrease of the mean value of the DC-voltage is not the only disadvantage of the commutation process. During the commutation process, the thyristors T_a and T_b are conducting at the same time. This means there is some kind of short circuit in the grid. This phenomenon influences the grid voltage, as visualized in Fig. 3.22.

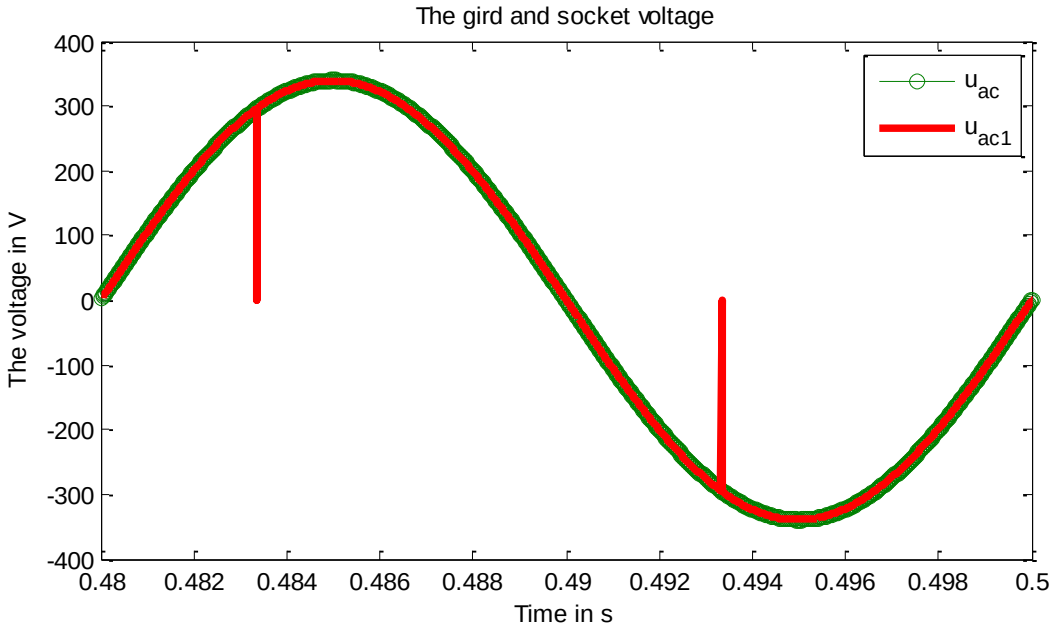


Fig. 3.22: The AC voltage of the grid: uac is the grid voltage and uac1 is the voltage after the inductor i.e. the socket voltage

As shown in Fig. 3.22, the grid voltage generated by the electrical generator is still sinusoidal, but the voltage at the socket where the bridge rectifier has been plugged has changed. A sinusoidal voltage with two dips is obtained. These voltage dips can influence other devices fed by the grid implying it is a good practice to avoid these dips. By placing an additional coil in each grid phase before the bridge rectifier solves the problem so that it can act as a lowpass filter, which filters the high frequency dips out of the socket voltage.

Discontinuous conduction mode

The basic idea of the discontinuous conduction mode is already explained. When the current through an ideal thyristor equals zero, this thyristor will turn off. This means that a thyristor will conduct the current less than π radians. This influences the mean value of the DC output voltage since a part of the period π, the instantaneous DC-voltage is zero instead of the expected value. The mean value of the DC-voltage is now determined using equation (3-1):

$$U_{DC} = \frac{1}{\theta}\int_0^{\theta} u_{dc}(\omega t)\, d\omega t = \frac{1}{\pi}\int_{\alpha}^{\beta} u_{dc}(\omega t)\, d\omega t \text{ with } \pi \leq \beta < \pi + \alpha$$

Where the angle β stands for the angle where the current trough the thyristor becomes zero. When the load is purely resistive, the angle β equals π. As the load becomes more inductive, β increases. When the load is sufficiently inductive, commutation occurs and the angle β equals

$\pi+\alpha$. This implies that in the discontinuous conduction mode, the angle β has a value between π and $\pi+\alpha$.

The discontinuous conduction mode occurs since the instantaneous current value through the thyristor and the load becomes zero. This can occur due to two reasons. The first reason is that the DC-current ripple is too large in comparison with the mean value of the DC-current. The second reason is that the mean value of the DC-current is too small in comparison with the DC-current ripple. These two reasons are almost the same, but there is a crucial difference between them.

The current ripple is controlled by the inductor, while the mean value is controlled by the resistor. When a very high load (small resistor) is considered, the ripple in the DC-current may be high since the mean value is high. In such a situation, commutation occurs and no discontinuous mode is obtained. When decreasing the load (increasing the resistance), the mean value of the current decreases but there are no fundamental changes until this mean value reaches $I_{dlück}$. The value $I_{dlück}$ is defined as the mean DC-current value where the instantaneous value of the load current is zero at the moment the other thyristor is switched on. When the load further decreases, the mean value of the current further decreases and becomes lower than $I_{dlück}$ implying the discontinuous conduction mode occurs.

When the inductor value L is sufficiently large, the instantaneous value of the rectified grid voltage has a positive and a negative part between two firing activities. In the case of discontinuous conduction mode, the negative part is reduced and partially replaced with a zero voltage implying the main value of the DC-voltage increases for this specific firing value.

In general, the discontinuous conduction mode is not wanted since the mean value of DC-voltage is difficult to be controled. This explains why in most applications the value of $I_{dlück}$ has to be as low as possible. The easiest way to decrease $I_{dlück}$ is decreasing the ripple on the DC-current i.e. by placing an additional inductor in the DC-circuit.

Capacitive-resistive load

To obtain a more constant DC voltage, in many application a capacitor is used as shown in Fig. 3.23. In reality, a capacitor is almost never used when considering a thyristor rectifier, but they are common practice when using diodes or IGBT's. Working with a capacitor, two equations ((3-16) and (3-17)) are very important:

$$\boldsymbol{Q(t) = Cu_c(t)} \tag{3-16}$$

$$\boldsymbol{Q(t) = \int_0^t i_c(t)\,dt} \tag{3-17}$$

Equation (3-16) describes the relationship between the electric charges stored in the capacitor and the voltage across the capacitor. Equation (3-17) describes the relationship between the current that flows to the capacitor and the charges stored in the capacitor (at t=0, the capacitor is assumed to be uncharged). In equation (3-17), the current is positive when the current flows to the capacitor charging it. The current is negative when the current flows from the capacitor and discharges the capacitor. A capacitor is able to consume power and store energy or to act as a power source. A capacitor is a device which opposes a change in the

voltage. When the voltage supplying the circuit with the capacitor is increasing than there is a voltage difference between the capacitor and the source. This implies a current will flow to the capacitor which adds charges of the capacitor. In other words, electrical energy is consumed and transformed into electrostatic energy.

As the capacitor value C increases, more charges are needed to obtain the desired voltage rise. While loading and also unloading the capacitor, the polarity of the voltage across it does not change but the polarity of the current changes.

A capacitor is not suited to be combined with a thyristor rectifier. As shown in Fig. 3.23, there is a thyristor bridge rectifier with a capacitor to stabilize the DC-voltage. In order to turn on a thyristor, two conditions must be fulfilled at the same time. First, the forward voltage has to be positive and, second, a current pulse on the gate is required.

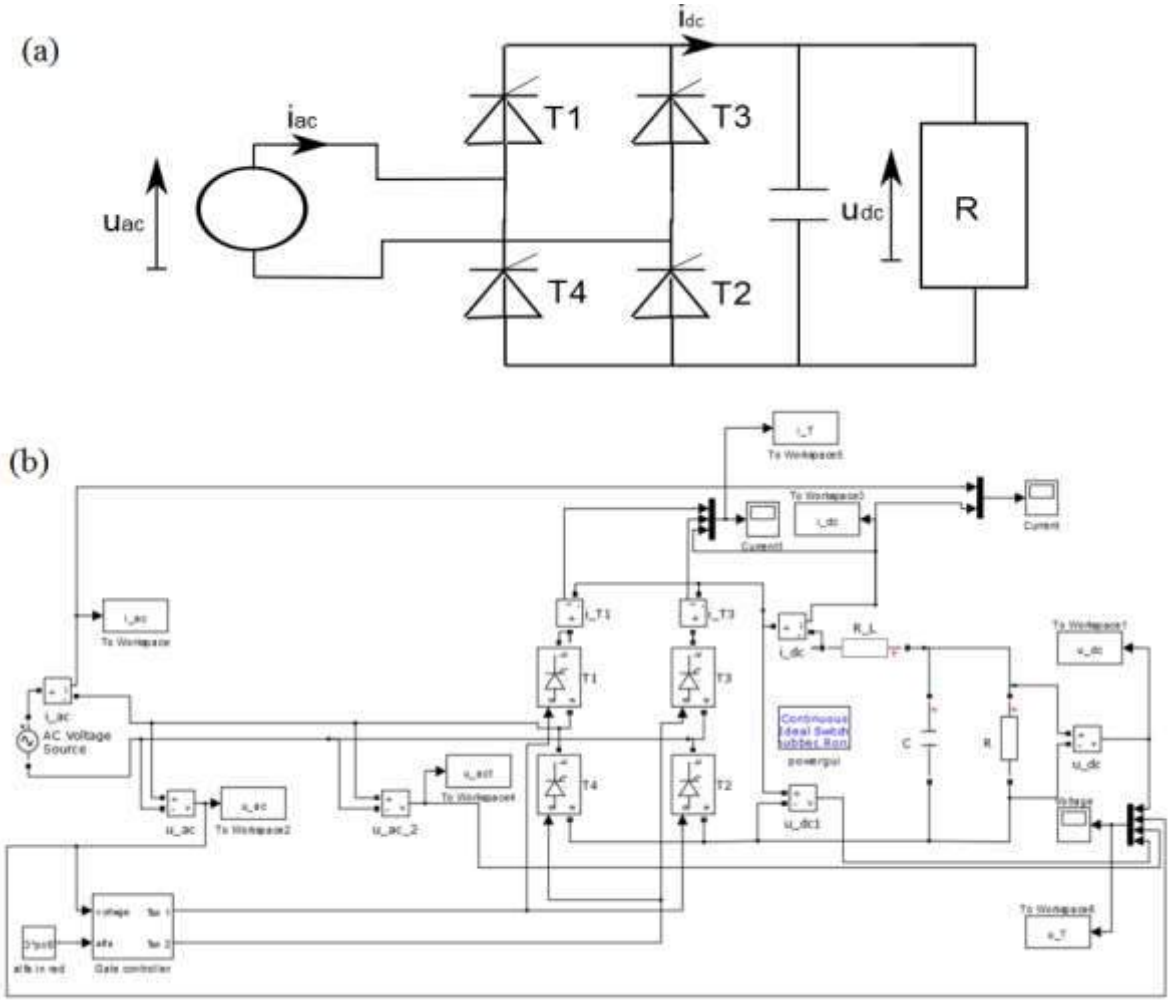
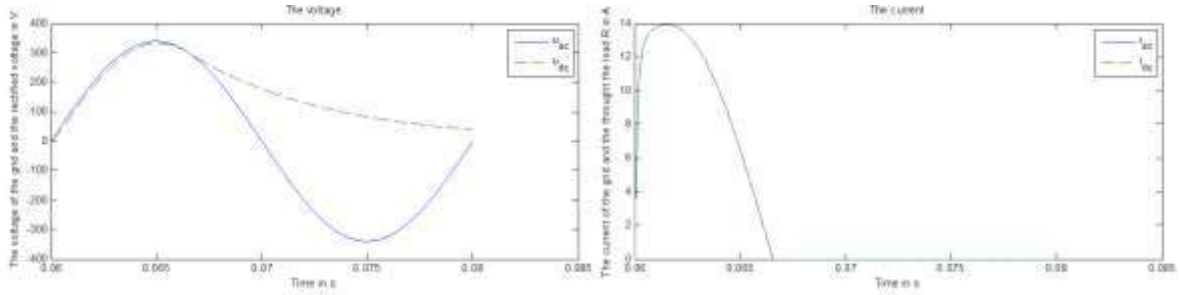


Fig. 3.23: The circuit of the single-phase controllable full-wave bridge rectifier with capacitive-resistive load: (a) electrical circuit (b) Simulink model.

Two problems arise when studying the behavior reflected in Fig. 3.23. When the thyristors have a very small firing angle α, i.e. α=0, the capacitor will charge until its voltage equals the voltage of the grid. Indeed, at this point the current of the grid and the current through the thyristors equal zero and the thyristors switch off. When the next current pulse is applied to the gates of the thyristors T3 and T4 during the negative cycle of the grid voltage and the capacitor has not yet fully discharged over the load, than these thyristors will not switch on

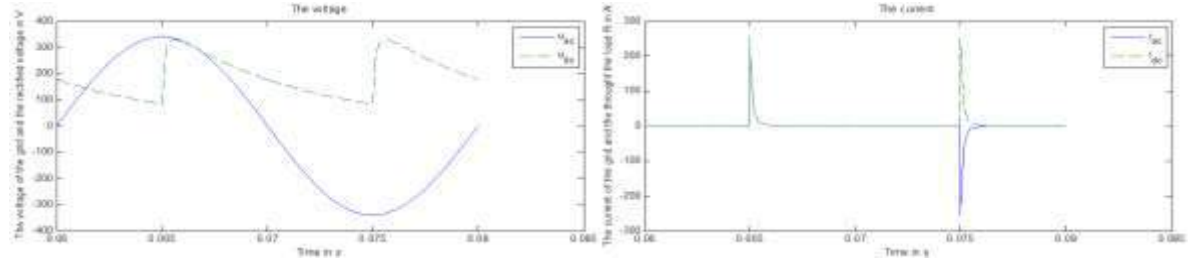
since their forward voltage drop is negative. In order to switch on thyristors T1 and T2 or T3 and T4, the capacitor must be discharged. In such a situation, the capacitor is not able to stabilize the DC-voltage. The voltage and current waveforms are shown in Fig. 3.24:



(a) (b)

Fig. 3.24. The evolution of the voltages (a) and the currents (b) when combining a thyristor bridge rectifier with a capacitor and a firing angle α which equals zero

Instead of using a very small firing angle α, also a larger firing angle, for example $\alpha = \pi/2$, can be used. The input voltage is maximal when firing the thyristor gates and the thyristors would be activated due to the current pulse. However, another disadvantage occurs in the current through the thyristor. When activating the thyristor with a firing angle $\alpha = \pi/2$, the voltage difference between the rectified grid voltage and the capacitor voltage is maximal. There is only a small resistor between the rectified grid voltage and the capacitor voltage. This implies the current through this resistor and the current rise is very high. This will probably destroy the thyristor due to the creation of hot spots. The evolution of the current is shown in Fig. 3.25.



(a) (b)

Fig. 3.25. The evolution of the voltages (a) and the currents (b) when combining a thyristor bridge rectifier with a capacitor and a firing angle α which equals $\pi/2$.

Notice the firing angle almost does not change the mean value of the DC-voltage, i.e. the capacitor value reaches the peak value of the grid voltage which cannot be changed. Due to this reason the capacitor is mostly used in combination with diodes or IGBT's. The diodes will start to conduct when the rectified grid voltage equals to the capacitor voltage. This gives a DC-voltage which is maximally stabilized and the current pulses are limited as shown in

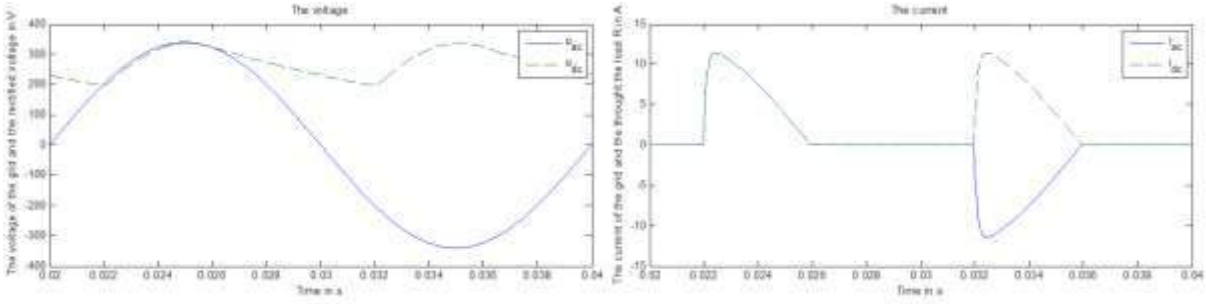
(a) (b)

Fig. 3.26. When using thyristors, it is difficult to know the optimal firing angle to obtain the behavior shown in (a) (b)

Fig. 3.26. (it depends on the capacitor value and the resistive load in parallel with the capacitor).

Notice that Fig. 3.24, Fig. 3.25 and (a) (b)

Fig. 3.26 are obtained without a grid inductance. As mentioned while discussing the commutation process, the grid has an inductance which opposes the fast changes in the grid current. Due to the grid inductances, the fast current rise will be lower but still too high for the thyristors as shown in Fig. 3.25. Using a capacitor in combination with a thyristor rectifier bridge is still not an option.



(a) (b)

Fig. 3.26. The evolution of the voltages (a) and the currents (b) when combining a diode bridge rectifier with a capacitor

An active load

An active load is a load which can work as a consumer or as source for a very long time like a DC-machine. The main difference between an inductive-resistive load and a DC-machine is the back-EMF. This back-EMF is caused by the rotation of the rotor in a fixed magnetic field. Due to the mechanical inertia, the speed of the machine can be assumed to be constant during e.g. 20 ms implying also the back-EMF remains constant. The back-EMF can be represented as a DC-source u_{dc} which is constant for a specific speed of rotation as shown in Fig. 3.27.

When the firing angle of the thyristors is very small and the instantaneous value of the rectified grid voltage is lower than the back-EMF, the thyristors will not switch on. In this case, the rotor will decelerate until the back-EMF is lower than the instantaneous value of the rectified grid voltage when firing the thyristor. When the instantaneous value of the rectified grid voltage is larger than the back-EMF while firing the thyristor, this leads to a current through the thyristors and the inductor L. This current will increase, as long the instantaneous value of the rectified grid voltage is higher than the back-EMF.

When the instantaneous value of the rectified grid voltage equals to the back-EMF, the current reaches its maximum value and starts to decrease. As long as the current through the inductor is not equal to zero, the thyristor will not switch off. Even when the instantaneous value of the rectified grid voltage becomes negative, the thyristor will not switch off due to the inductor. When the instantaneous value of the rectified grid voltage is lower than the back-EMF, the inductor will use its stored magnetic energy to keep the current flowing by acting as a source. Indeed, an inductor opposes to the change of the current. The instantaneous value of the rectified grid voltage u_{dc1} before the DC-inductor is visualized in combination with the current in Fig. 3.28.

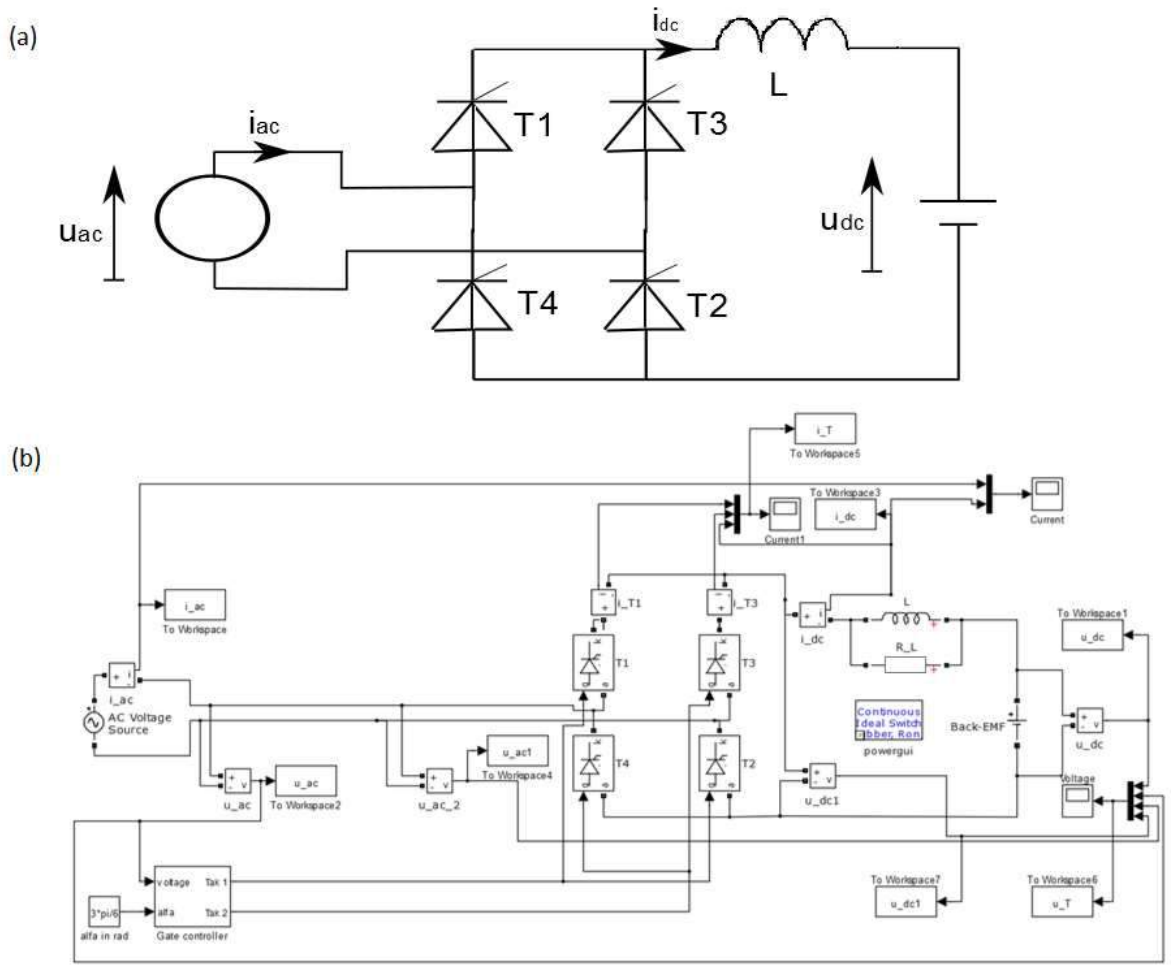
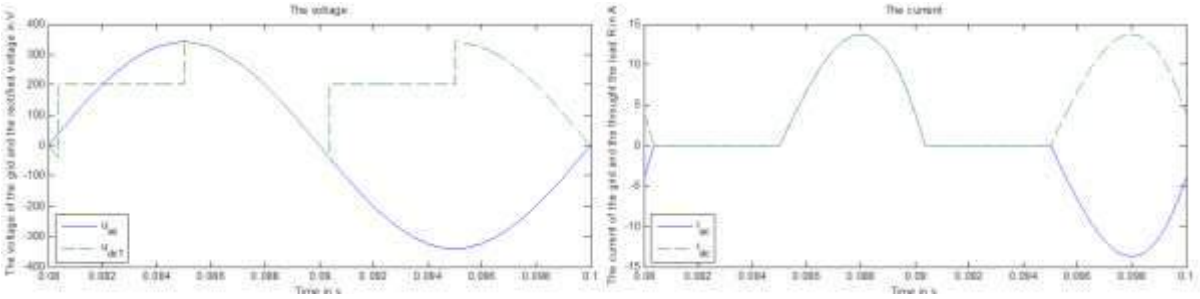


Fig. 3.27. The circuit of the single-phase controllable full-wave bridge rectifier with active load: electrical circuit (a) Simulink model (b)

It is important to notice the discontinuous conduction mode can also occur as shown in Fig. 3.28. In Fig. 3.28, the firing angle $\alpha = \pi/2$ implying the rectified grid voltage is larger than the back-EMF when firing the thyristors. The current increases and reaches a maximum when the rectified grid voltage becomes equal to the back-EMF. Due to a further decrease of the rectified grid voltage, this rectified grid voltage becomes lower than the back-EMF implying the current decreases.

When this current becomes zero, the thyristors switch off and also the inductor current becomes and remains zero (discontinuous conduction mode occors). The back-EMF has a value of 200V implying also the mean value of the rectified grid voltage should be 200V. In Fig. 3.28 this property is obtained due to the discontinuous conduction mode (without discontinuous conduction mode the mean DC-value would be zero).



(a) (b)

Fig. 3.28. The evolution of the voltages (a) and the currents (b) when combining a thyristor bridge rectifier with an active load

Power factor correctors

The line-commutated rectifiers have the disadvantage of the network currents with a large THD. Moreover, in general they also have a weak power factor. Since AC to DC converters are also frequently used in household products, they are an important source of power quality problems. In [Selection of transformers for commercial buildings, Dwyer, R. ; Electrotek Concepts Inc., Knoxville, TN, USA ; Mueller, D.R.] the authors show that rectifiers are responsible for 50% to 90% of the power demand in modern commercial buildings. Due to this reason the last years the improved concepts of controllable rectifiers are developed and a few of them will be discussed.

The single-phase Boost Rectifier

The single-phase Boost Rectifier is an important rectifier type giving a high power factor. This rectifier type, shown in Fig. 3.29, consists of a single-phase uncontrollable bridge rectifier and a DC-DC boost converter. Due to this boost converter, a constant sufficiently high DC-voltage is obtained and a sinusoidal grid current having a large power factor is obtained.

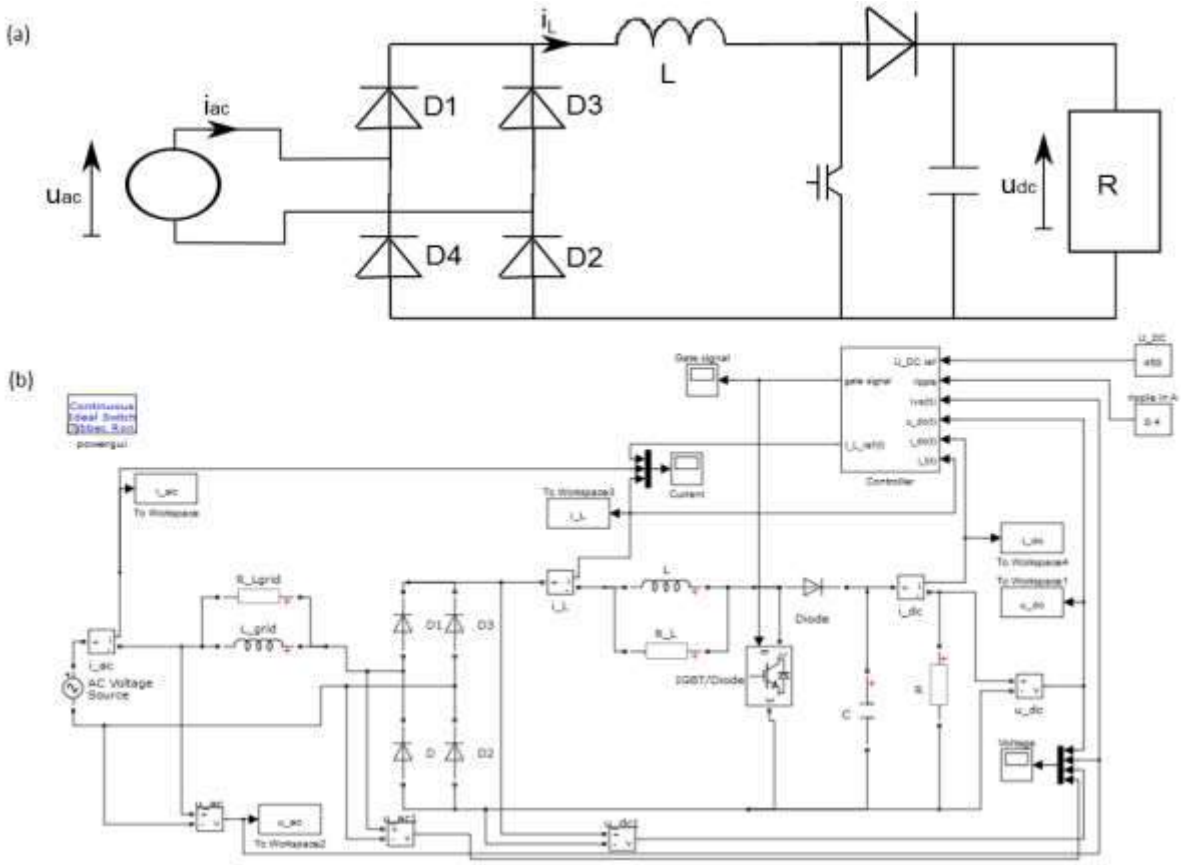


Fig. 3.29. The circuit of the single-phase boost rectifier: (a) electrical circuit, (b) Simulink model.

This boost converter controls the current through the DC-coil L and the DC-voltage across the capacitor. The sinusoidal grid current is obtained by measuring the inductor current and by using a suitable control strategy. This strategy is based on the assumption that the voltage across the capacitor is always higher than the instantaneous rectified voltage of the diode bridge rectifier.

Two situations occur: (i) when the IGBT is conducting and the voltage across the DC-coil opposes the direction of the current i_L through the DC-coil, (ii) when the IGBT is not conducting and the voltage across the DC-coil has the same polarity as the current i_L through the DC-coil.

In situation (i), the DC-coil acts as a consumer and converts electric into magnetic energy which is stored. When the voltage across the coil opposes the direction of the current, equation (3-10) implies the current will increase. In situation (ii), the DC-coil acts as a source and converts the stored magnetic energy into electrical energy. When the voltage across the coil has the same polarity like the current, equation $\mathbf{u_L = -L\frac{di_L}{dt}}$ implies the current will decrease.

When the instantaneous value of the current through the DC-coil is lower than the required reference current i_{Lref}, the IGBT is closed implying an increase of the instantaneous current value. When the current through the DC-coil is higher than the required reference current i_{Lref}, the IGBT is opened implying a decrease of the instantaneous current value. In order to realize this approach, it is important to determine the required reference current i_{Lref}.

To obtain the correct reference current i_{Lref}, a number of measurements must be performed. Basically, the equivalent resistor R_{ac_eq} for the entire circuit must be determined as seen from the grid side. When assuming the power supplied by the grid is only used to supply the DC-load (meaning the converter has an efficiency of 100%), this equivalent resistor R_{ac_eq} equals

$$R_{ac\_eq}(t) = \frac{U_{ac}^2}{P_{ac}(t)} = \frac{U_{ac}^2}{P_{dc}(t)} = \frac{U_{ac}^2 R_{dc}(t)}{U_{dc}^2} = \frac{U_{ac}^2 u_{dc(t)}}{U_{dc}^2 i_{dc(t)}} \tag{3-18}$$

Here, U_{ac} is the RMS-value of the grid voltage, U_{dc} is the desired mean DC-voltage and $R_{dc}(t)$ is the instantaneous value of the DC-resistor. It is realistic to consider a DC-resistor $R_{dc}(t)$ which is time-varying, here the DC-resistor is assumed to be slowly time-varying, i.e. its value is constant in one period of the grid frequency (20 ms). This assumption is necessary to obtain a perfect absolute sine function for $i_{L\_ref}(t)$. The instantaneous value of the DC-resistor can be obtained by measuring the instantaneous DC-voltage and the instantaneous DC-current. By calculating the equivalent resistor $R_{ac\_eq}(t)$, the reference current through the coil i_{L_ref} is determined by dividing the absolute value of the instantaneous ac-voltage by the equivalent resistor $R_{ac\_eq}(t)$ giving:

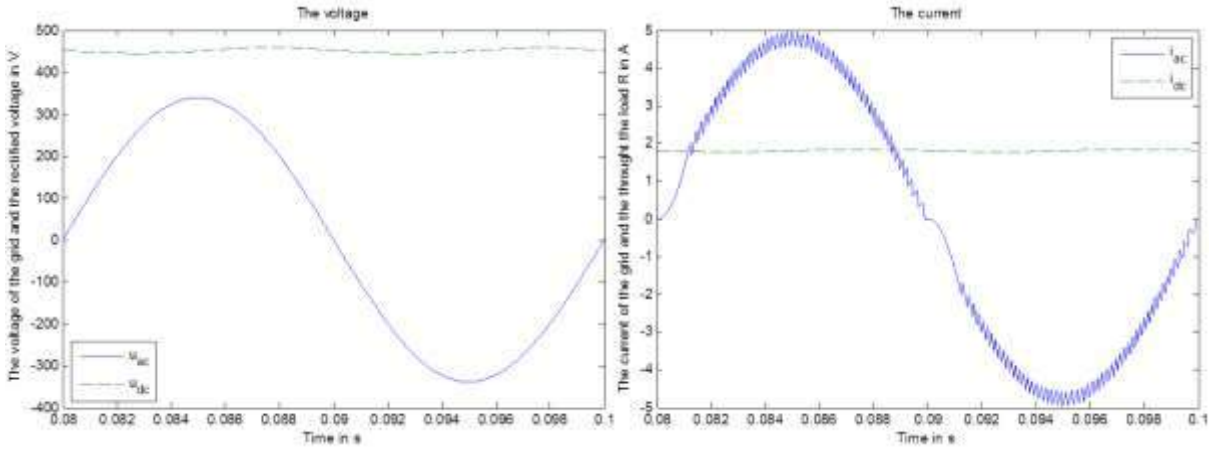
$$i_{L\_ref}(t) = \frac{1}{R_{ac_{eq}}(t)} |u_{ac}(t)| \tag{3-19}$$

Based on this reference current $i_{L\_ref}(t)$, a hysteresis controller is used to control the instantaneous value of the current $i_L(t)$ by means of a lower limit and an upper limit. When the current $i_L(t)$ is lower than the lower limit, the IGBT must be closed in order to obtain an increase of $i_L(t)$. The IGBT remains closed until the current $i_L(t)$ becomes higher than the upper limit. At this moment, the IGBT must be opened in order to obtain a decrease of $i_L(t)$. The IGBT remains open until the current $i_L(t)$ is below the lower limit. This lower limit and this upper limit are obtained by adding an opposite offset to the reference current $i_{L\_ref}(t)$. This implies the limits also change in time.

As shown in (a) (b) Fig. 3.30, such a single-phase boost rectifier allows obtaining grid currents having a very low THD. The ripple of the grid current depends on the width of the hysteresis band of the controller. The smaller this hysteresis band, the smaller the ripple of the grid current. However, due to the smaller hysteresis band the IGBT will switch more often. This implies there are more switching losses and the efficiency will be lower. A compromise is required between the ripple on the current and the losses.

The THD of the grid current using $THD_i = \frac{\sqrt{\sum_{i=2}^{\infty} I_i^2}}{I_1}$, $THD_i = \frac{\sqrt{I_{total}^2 - I_1^2}}{I_1}$ and $THD_i = \frac{\sqrt{\sum_{i=2}^{\infty} I_i^2}}{\sqrt{\sum_{i=1}^{\infty} I_i^2}}$ equals 4.37%. Although this result depends on the chosen DC-coil, capacitor, hysteresis band and load, it gives an indication of a realistic THD value. Notice the THD will decrease as the load current increases. Indeed, the ripple on the current does not depend on the load current but it depends on the width of the hysteresis band controller. As

the load current increases, the ratio between the ripple and the load current decreases which reduces the THD.

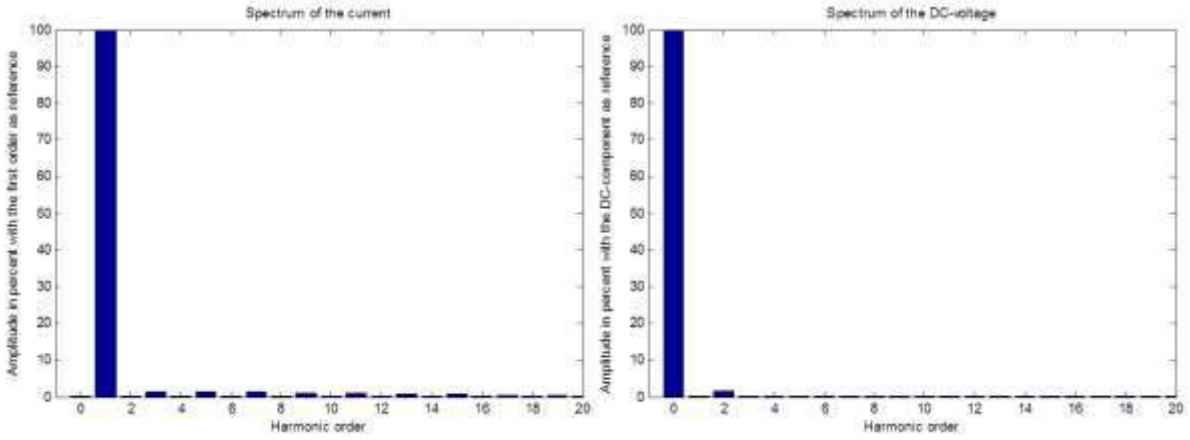


(a) (b)

Fig. 3.30. the AC and the DC voltage (a) and the AC and the DC current when using a single-phase boost rectifier (b)

A similar result is valid when considering the power factor. As shown in (a) (b)

Fig. 3.30, the fundamental component of the grid current has the same phase as the grid voltage. This implies the power factor is mainly determined by the distortion power, i.e. by the THD. As the load current increases, the THD decreases implying the power factor increases. Fig. 3.31 visualizes the spectrum of the grid current which mainly contains the fundamental component.



(a) (b)

Fig. 3.31. Spectrum of the grid current (a) and the DC-voltage using a single-phase boost rectifier (b)

Notice the DC-voltage is always higher than the peak value of the grid voltage. To obtain sufficient dynamics of the rectifier, the DC-voltage should at least exceed the peak value of the grid voltage by 10%. The ripple on the DC-voltage is mainly controlled by the capacitor, the DC-coil and the hysteresis band. As shown in Fig. 3.31 the ripple is very small and in the present example the RF (3-9)

$\boldsymbol{RF = \frac{V_{s,ac}}{U_{dc}}}$ ($V_{s,ac}$ is the RMS-value of the AC-signal added with the DC-component, which equals the square root of the quadratic sum of the RMS-values of all the harmonics except the harmonic with order zero. U_{dc} is the mean value of the DC-voltage i.e. the harmonic with order zero) equals to 0.0112. (a) (b)

Fig. 3.30 shows the behavior in case continuous conduction mode is obtained. When the current becomes zero during the switching period of the IGBT, the discontinuous conduction mode occurs. The discontinuous conduction mode is a control strategy since continuous conduction mode does not allow the current to decrease under the lower limit. When considering the discontinuous conduction mode, two different control strategies exist. It is possible to use a fixed switching frequency or it is possible to use a variable switching frequency.

The discontinuous conduction mode allows obtaining a higher efficiency since the IGBT needs a lower number of switching events. Unfortunately, the current waveform contains current peaks as visualized in Fig. 3.32 which implies a higher THD of the grid current. Due to this reason, in the present section we restrict the continuous conduction mode.

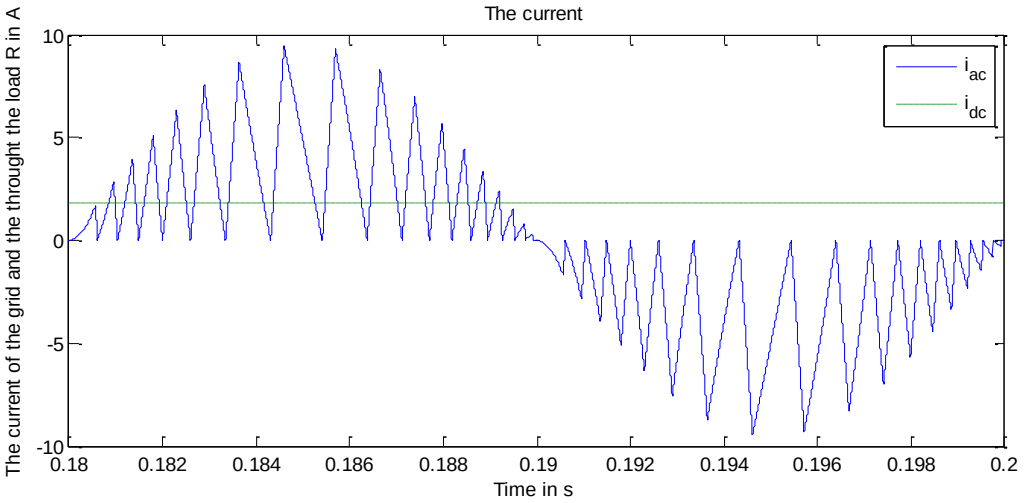


Fig. 3.32. The grid current waveform when using the discontinuous conduction mode having a variable switching frequency on a single-phase boost rectifier

In the present section, the switch used to control the current in de DC-coil is an IGBT. Instead of using an IGBT, it is also possible to use a TCR, a transistor, MOSFET. Actually any fully controllable semiconductor switch (meaning you can turn it on and off when you want) can be used. It is important this semiconductor switch withstands the maximum current value and the maximum voltage value. Moreover, the switch needs a sufficiently high switching frequency.

The single-phase Voltage Doubler PWM Rectifier

The single-phase voltage doubler PWM rectifier, as visualized in Fig. 3.33, has four states. To understand the working principle of this rectifier, the four states will be explained separately. The steady state explanations are given where the voltages of both individual capacitors are higher than the maximum voltage of the grid. It is also important to know the working principle of the trigger signals. When IGBT1 gets the needed positive voltage on the gate which implies IGBT1 can conduct, then the voltage on the gate of the IGBT2 must be zero. When the voltage of the gate of IGBT1 equals to zero, then the voltage of the gate of the IGBT2 must be positive which implies IGBT2 can conduct.

The first state is obtained when IBGT2 gets the needed trigger voltage on the gate and the instantaneous coil current is positive, as visualized in Fig. 3.34.(a). In this case IGBT2 can and

will conduct because $-U_{c2}$ is lower than the instantaneous grid voltage (also when this grid voltage is negative) and the difference between these voltages is the voltage across the coil. In this state the coil current will increase. The diode D1 will not conduct in this state since the sum of the instantaneous grid voltage and the voltage across the coil equals $-U_{c2}$ (which is the voltage at the anode of the diode D1) is smaller than the voltage U_{c1} across the capacitor C1 (which is the voltage at the cathode of the diode D1). In this state, the coil current will increase.

The second state is obtained when IBGT1 gets the needed trigger voltage on the gate and the instantaneous coil current is positive, as visualized in Fig. 3.34.(b). In this case IGBT1 can, but will not conduct since the coil current is positive. The diode D1 will conduct, because the inductor wants to obtain a constant current. This coil will transform stored magnetic energy into electrical energy and becomes an electric source. Across the coil, a voltage appears and by adding this positive voltage with the instantaneous grid voltage a total voltage which equals the voltage u_{c1} across the capacitor C1 is obtained. In this state, the coil current will decrease.

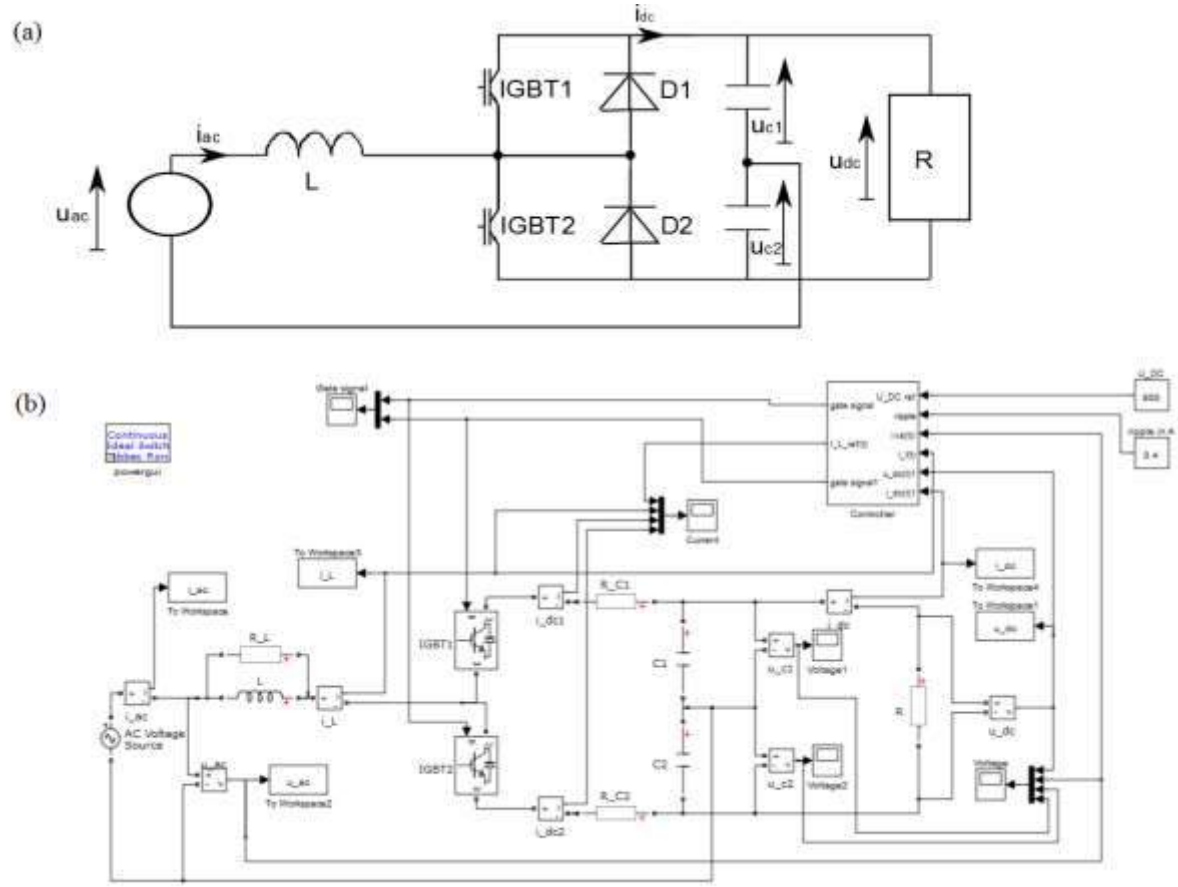


Fig. 3.33: The single-phase Voltage Doubler PWM Rectifier

The third state is obtained when IBGT1 gets the needed trigger voltage on the gate and the instantaneous coil current is negative, as visualized in Fig. 3.34.(c). In this case IGBT1 can and will conduct because U_{c1} is higher than the instantaneous grid voltage. Across the coil, a positive voltage appears which implies the coil current will decrease, i.e. become more negative. The diode D2 will not conduct since the sum of the instantaneous grid voltage and voltage across the coil equals U_{c1} (which is the voltage at the cathode of the diode D2) is

higher than the voltage $-U_{c2}$ at the anode of the diode D_2. In this state, the coil current will decrease, i.e. become more negative.

The fourth state is obtained when IBGT2 gets the needed trigger voltage on the gate and the instantaneous coil current is negative, as visualized in Fig. 3.34.(d). In this case IGBT2 can, but will not conduct since the current is negative. In this state the coil current will increase in value, i.e. the current becomes less negative. The diode D2 will conduct in this case since the inductor tends to obtain a constant current. This coil will transform stored magnetic energy into electrical energy and becomes an electric source. Across the coil, a voltage appears and by adding this voltage with the instantaneous grid voltage a total voltage which equals to the voltage $-U_{c2}$ is obtained. In this state, the coil current increases, i.e. becomes less negative.

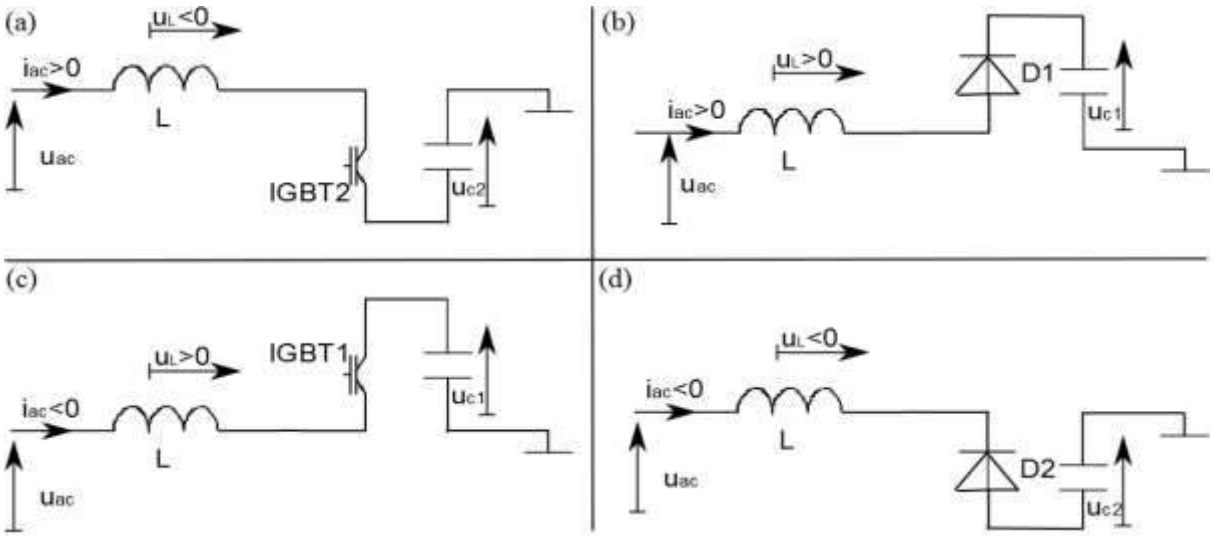


Fig. 3.34. The four states of the single-phase Voltage Doubler PWM Rectifier

Based on these four states, the switching logic can be obtained. When the coil current has to increase, IGBT2 has to be activated. When the coil current has to decrease, IGBT1 has to be activated. This leads to the use of a hysteresis controller to obtain the correct sinusoidal grid current, similar with the results in 0, the needed sinusoidal reference current has to be obtained.

To obtain the correct reference current i_{Lref}, a number of measurements are required. Basically, the equivalent resistor R_{ac_eq} for the entire circuit must be determined as seen from the grid side. When assuming the power supplied by the grid is only used to supply the DC-load (meaning the converter has an efficiency of 100%), this equivalent resistor R_{ac_eq} equals (3-18) and the reference current is obtained by:

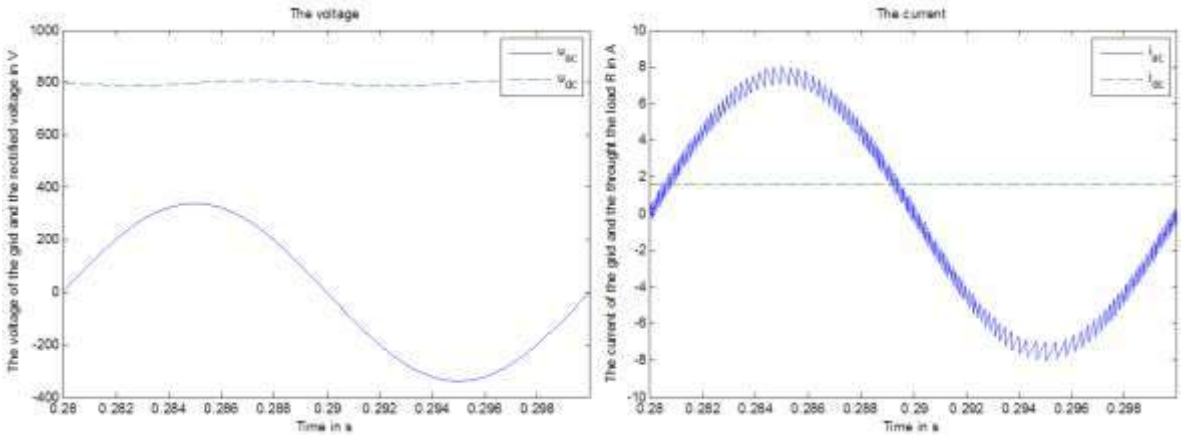
$$i_{L\_ref} = \frac{1}{R_{ac_{eq}}(t)} u_{ac}(t) \tag{3-20}$$

Based on this reference current i_{L_ref}, a hysteresis controller is used to control the instantaneous value of the current $i_L(t) = i_{ac}(t)$ by means of a lower limit and an upper limit. When the current $i_L(t)$ is lower than the lower limit, the IGBT2 must be closed in order to obtain an increase of $i_L(t)$. The IGBT 2 remains closed until the current $i_L(t)$ becomes higher than the upper limit. At this moment, the IGBT2 must be opened and the IGBT1 must be

closed in order to obtain a decrease of $i_L(t)$. The IGBT1 remains closed until the current $i_L(t)$ becomes smaller than the lower limit. This lower limit and this upper limit are obtained by adding an opposite offset to the reference current $i_{L\_ref}(t)$. This implies the limits also change in time. Notice that when IGBT1 is open, IBGT2 is closed when IGBT1 is closed, IGBT2 is open.

As shown in Fig. 3.35, such a single-phase Voltage Doubler PWM Rectifier allows obtaining grid currents having a very low THD. The ripple of the grid current depends on the width of the hysteresis band of the controller. The smaller this hysteresis band, the smaller the ripple of the grid current. However, due to the smaller hysteresis band, the IGBTs will switch more often. This implies there are more switching losses and the efficiency will be lower. A compromise is needed between the ripple on the current and the losses.

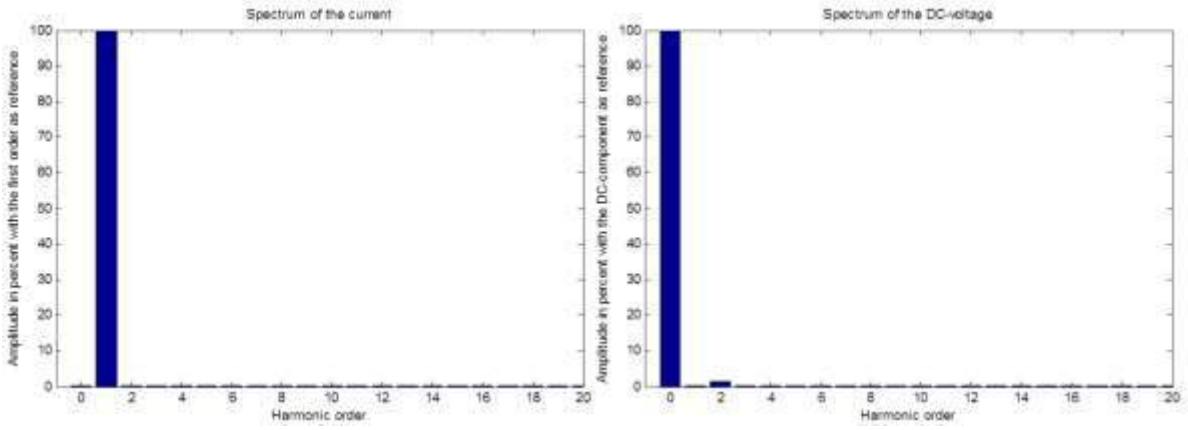
The THD of the grid current using (3-6), (3-7) equals 5.41 % and using (3-8) equals 5.40%. Although this result depends on the chosen DC-coil, capacitor, hysteresis band and load, it gives an indication of realistic THD values. Notice the THD will decrease as the amplitude of the load current increases. Indeed, the ripple on the current does not depend on the amplitude of the load current but only depends on the width of the hysteresis band controller. As the amplitude of the load current increases, the ratio between the ripple and the load current decreases which reduces the THD.



(a) (b)

Fig. 3.35. The AC and the DC voltage (a) the AC and the DC current (b) when using a single-phase Voltage Doubler PWM Rectifier

A similar result is valid when considering the power factor. As shown in Fig. 3.35, the fundamental component of the grid current has the same phase as the grid voltage. This implies the power factor is mainly determined by the distortion power i.e. by the THD. As the load current increases, the THD decreases implying the power factor increases. Fig. 3.36 visualizes the spectrum of the grid current which mainly contains the fundamental component.



(a) (b)

Fig. 3.36. Spectrum of the grid current (a) the DC-voltage (b) using a single-phase Voltage Doubler PWM Rectifier

Notice the DC-voltage, for each capacitor, is always higher than the peak value of the grid voltage. To obtain sufficient dynamics of the rectifier, the DC-voltage, for each capacitor, should at least exceed the peak value of the grid voltage by 10%. The ripple on the DC-voltage is mainly controlled by the capacitor, the DC-coil and the hysteresis band. As shown in Fig. 3.36. the voltage ripple is very small and in the present example the RF equals 0.0089.

In the present section, the switches used to control the coil current are IGBTs. Instead of using IGBTs, it is also possible to use TCRs, transistors, MOSFETs, Actually any fully controllable semiconductor switch (meaning you can turn it on and off when you want) can be used. It is important this semiconductor switch withstands the maximum current value and the maximum voltage value. Moreover, the switch needs a sufficiently high switching frequency.

The single-phase PWM rectifier in bridge connection

The single-phase PWM rectifier in bridge connection is visualized in Fig. 3.37. To obtain the four states similar with the states discussed in 0, the bipolar switching strategy must be used. When considering the single-phase PWM rectifier in bridge connection, two types of switching strategies can be used: bipolar and unipolar. Using the bipolar switching strategy, the gate signals to IGBT1 and IGBT4 are the same, meaning also IGBT 2 and IGBT 3 have also the same gate signals at the same time. This bipolar switching strategy has the advantage it is easy to implement. Only one single controller is needed, i.e. the controller for bridge 1 containing IGBT1 and IGBT2.

When using the unipolar switching strategy, both bridges (IGBT1 and IGBT2; IGBT3 and IGBT4) have their own controller. This means this switching strategy is more expensive but the THD of the grid current can be improved (in the present case, the THD of the grid current improves just slightly).

Only the bipolar switching strategy will be studied in the present text:

To understand the working principle of this rectifier, the four states will be explained separately. The steady state explanations are given where the capacitor voltage is higher than the maximum grid voltage. When IGBT1 gets the needed positive gate voltage, IGBT4 gets the same positive gate voltage implying IGBT1 and IGBT4 can conduct while the gate voltages of IGBT2 and IGBT 3 are zero. When the gate voltage of IGBT1 is zero, then the

gate voltage of IGBT 4 is also zero and the gate voltages of IGBT2 and IGBT 3 are positive implying IGBT2 and IGBT3 can conduct.

The first state is obtained when IBGT2 and IBGT3 get the positive trigger voltage on their gates and the instantaneous coil current is positive, as visualized in Fig. 3.34 (a). In this case IGBT2 and IGBT3 both can and will conduct because $-u_c$ is lower than the instantaneous grid voltage. This implies a negative coil voltage which implies the current will increase. The diodes D1 and D4 will not conduct in this state since the sum of the instantaneous grid voltage and the coil voltage is equal to $-u_c$. The cathodes of D1 and D4 have the same potential due to the conducting IGBT3. With respect to these cathodes, both anodes have a potential $-U_C$.

The second state is obtained when IBGT1 and IGBT4 get the positive trigger voltage on their gates and the instantaneous coil current is positive, as visualized in Fig. 3.38 (b). In this case IGBT1 and IGBT4 can, but will not conduct, because the coil current is positive. In this state the coil current will decrease. The diodes D1 and D4 will conduct since the inductor wants to obtain a constant current. This coil will transform stored magnetic energy into electrical energy and becomes an electric source. The sum of the generated coil voltage and the instantaneous grid voltage equals to the voltage u_c across the capacitor C. In this state, the coil current decreases.

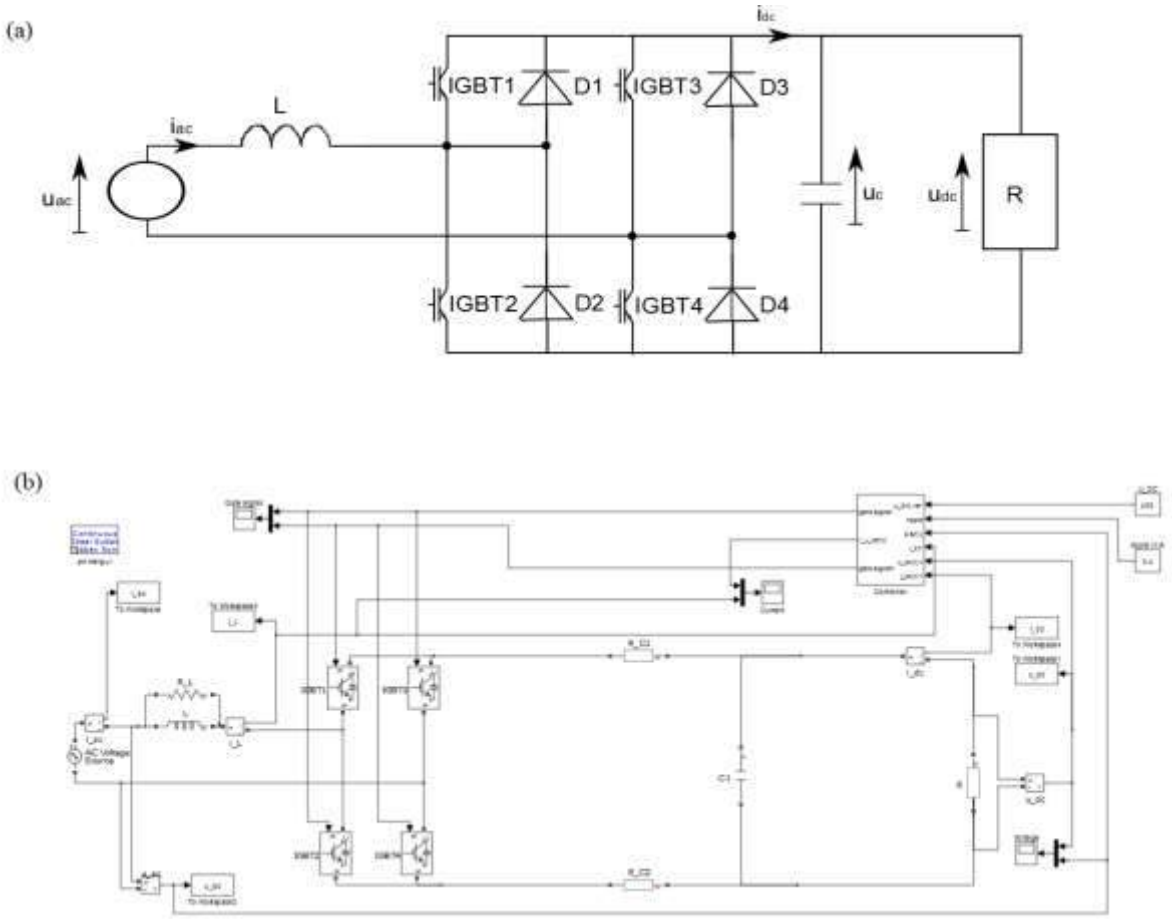


Fig. 3.37. The single-phase PWM rectifier in bridge connection

The third state is obtained when IBGT1 and IGBT4 get the positive trigger voltage on their gates and the instantaneous coil current is negative, as visualized in Fig. 3.38.(c). In this case IGBT1 and IGBT4 can and will conduct because u_c is higher than the instantaneous grid

voltage. This implies a possitive coil voltage and the coil current will decrease, i.e. becoming more negative. The diodes D2 and D3 will not conduct since the sum of the instantaneous grid voltage and the voltage across the coil equals $+u_c$. The cathodes of D2 and D3 have the same potential due to the conducting IGBT1. With respect to these cathodes, both anodes have a potential $-U_C$. In this state, the coil current decreases, i.e. becomes more negative.

The fourth state is obtained when IBGT2 and IGBT3 get the positive trigger voltage on their gates and the instantaneous coil current is negative, as visualized in Fig. 3.38.(d). In this case IGBT2 and IGBT3 can, but will not conduct since the coil current is negative. In this state the current will increase, i.e. the current becomes less negative. The diodes D2 and D3 will conduct since the inductor wants to obtain a constant current. This coil will transform stored magnetic energy into electrical energy and becomes an electric source. The sum of the generated coil voltage and the instantaneous grid voltage equals $-u_c$. In this state, the current through the coil increases, i.e. becomes less negative.

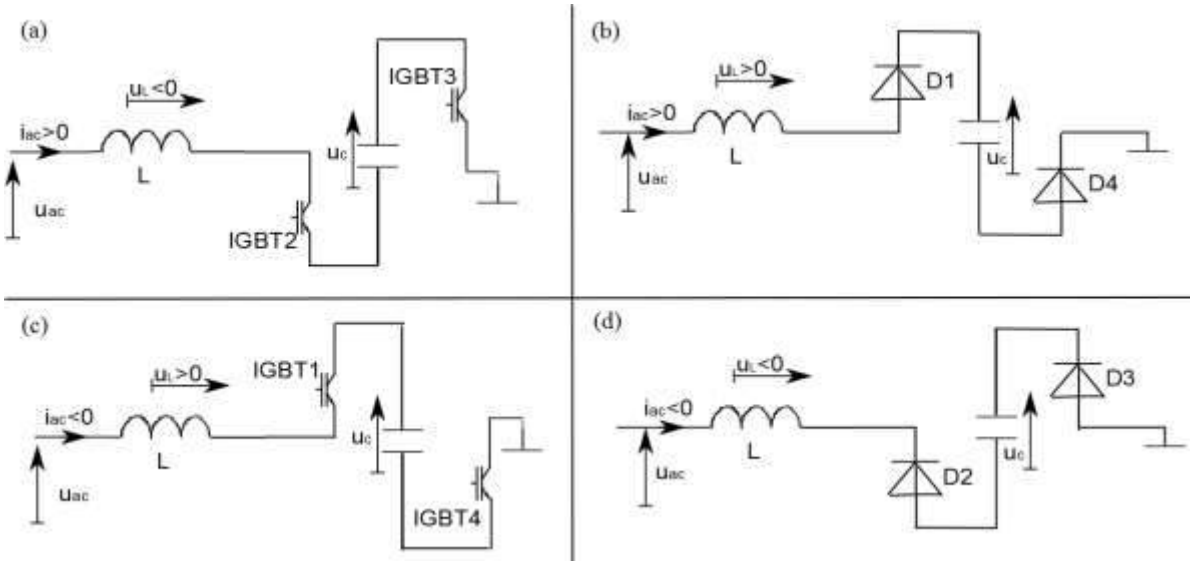


Fig. 3.38. The four states of the single-phase PWM rectifier in bridge connection, bipolar switching strategy

Based on these four states, the switching logic can be obtained. When the coil current has to increase IGBT2 and IGBT3 should be activated. When the current through the coil has to decrease IGBT1 and IGBT4 should be activated. This leads to the use of a hysteresis controller in order to obtain the correct sinusoidal grid current. Similar to the results in 0, the required sinusoidal reference current has to be determined.

To obtain the correct reference current $i_{Lref}(t)$, a number of measurements must be performed. Basically, the equivalent resistor R_{ac_eq} for the entire circuit must be determined as seen from the grid side. When assuming the power supplied by the grid is only used to supply the DC-load (meaning the converter has an efficiency of 100%), this equivalent resistor R_{ac_eq} equals (3-18) and the reference current is obtained by:

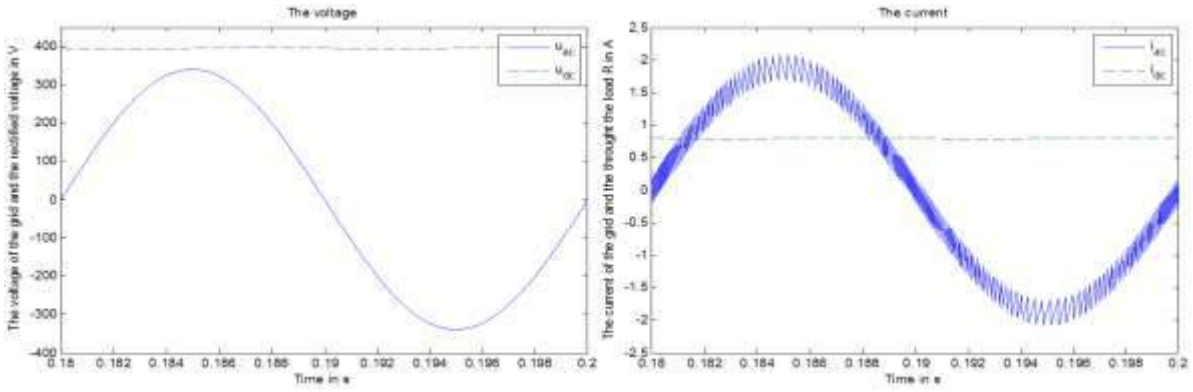
$$i_{L\_ref} = \frac{1}{R_{ac_{eq}}(t)} u_{ac}(t) \tag{3-21}$$

Based on this reference current $i_{L\_ref}(t)$, a hysteresis controller is used to control the instantaneous value of the current $i_L(t)$ by means of a lower limit and an upper limit. When the

current $i_L(t)$ is lower than the lower limit, the IGBT2 and IGBT3 must be closed in order to obtain an increase of $i_L(t)$. The IGBTs remain closed until the current $i_L(t)$ becomes higher than the upper limit. At this moment, the IGBT1 and IGBT4 must be closed in order to obtain a decrease of $i_L(t)$. The IGBT1 and IGBT4 remain closed until the current $i_L(t)$ becomes smaller than the lower limit. This lower limit and this upper limit are obtained by adding an opposite offset to the reference current $i_{L\_ref}(t)$. This implies the limits also change in time. Notice that when IGBT1 and IBGT4 are open, IBGT2 and IGBT4 are closed. When IGBT1 and IGBT4 are closed, IGBT2 and IGBT3 are open.

As shown in Fig. 3.39, such a single-phase PWM rectifier in bridge connection allows obtaining grid currents having a very low THD. The ripple of the grid current depends on the width of the hysteresis band of the controller. The smaller this hysteresis band, the smaller the ripple of the grid current. However, due to the smaller hysteresis band the IGBTs will switch more often. This implies there are more switching losses and the efficiency will be lower. A compromise is needed between the ripple of the current and the losses.

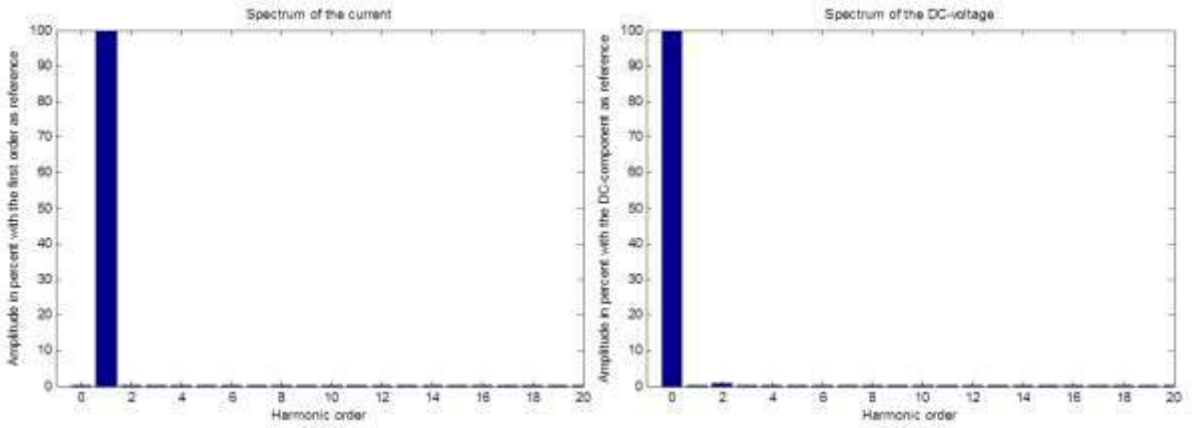
The THD of the grid current using (3-6), (3-7) equals 8.66 % and using (3-8) equals 8.63%. Although this result depends on the chosen coil, capacitor, hysteresis band and load, it gives an indication of a realistic THD value. Notice the THD will decrease as the amplitude of the load current increases. Indeed, the ripple on the current does not depend on the amplitude of the load current but it depends on the width of the hysteresis band of the controller. As the amplitude of the load current increases, the ratio between the ripple and the load current decreases which reduces the THD.



(a) (b)

Fig. 3.39. The AC and the DC voltage (a) the AC and the DC current (b) when using a single-phase PWM rectifier in bridge connection

A similar result is valid when considering the power factor. As shown in Fig. 3.39, the fundamental component of the grid current has the same phase as the grid voltage. This implies the power factor is mainly determined by the distortion power, i.e. by the THD. As the amplitude of the load current increases, the THD decreases implying the power factor increasing. Fig. 3.40 (a) visualizes the spectrum of the grid current which mainly contains the fundamental component.



(a) (b)

Fig. 3.40. Spectrum of the grid current (a) the DC-voltage (b) using a single-phase PWM rectifier in bridge connection

Notice the DC-voltage is always higher than the peak value of the grid voltage. To obtain sufficient dynamics of the rectifier, the DC-voltage should at least exceed the peak value of the grid voltage by 10%. The ripple on the DC-voltage is mainly controlled by the capacitor, the coil and the hysteresis band. As shown in Fig. 3.40 the voltage ripple is very low and in the present example the RF equals to 0.0047.

Notice the single-phase PWM rectifier in bridge connection and the single-phase Voltage Doubler PWM Rectifier are able to regenerate i.e. they are able to inject power back into the grid. These rectifiers regenerate power with a high power factor implying a low THD.

A unipolar switching strategy is a more complex than a bipolar switching strategy and this unipolar switching strategy will not be discussed in this chapter. The main advantage of the unipolar switching strategy is that there are eight states instead of four states. The first two extra states are obtained when IGTB1 and IGBT3 get a positive gate signal while the grid current is respectively positive and negative. The other two extra states are obtained when IGTB2 and IGBT4 get a positive gate signal while the grid current is respectively positive and negative. In these four extra states, the grid is disconnected from the DC-side since the current flows through an IGBT and a diode. In such a situation, the capacitor becomes the source for the DC-side. With the appropriate control strategy, this can slightly improve the THD of the grid current.

In the present section, the switches used to control the current in the coil are IGBTs. Instead of using IGBTs, it is also possible to use TCRs, transistors, MOSFETs. Actually any fully controllable semiconductor switch (meaning you can turn it on and off when you want) can be used. It is important such a semiconductor switch withstands the maximum current value and the maximum voltage value. Moreover, the switch needs a sufficiently high switching frequency.

3.3. Three-phase rectifiers

When considering industrial applications, in general a three phase grid is available which allows the usage of three-phase rectifiers. By using these three-phase rectifiers, a symmetrical load of the three-phase grid is possible. These types of rectifiers are used in a more industrial

environment and generally these rectifiers have a high output power (higher than 15kW). There are different kinds of divisions, one could make the division on the fact whether the output voltage is controllable or uncontrollable. Another division could be made on the fact whether the rectifier is rectifying the full AC-wave or only half of the AC-wave.

3.3.1. Three-phase uncontrollable rectifiers

The three-phase uncontrollable rectifiers are also known as the three-phase diode rectifiers. The ideal diode has a zero forward voltage drop and a zero reverse recovery time. When considering rectifiers which rectify the grid voltage these assumptions are valid since the voltage drop over the diode is much smaller than the amplitude of the grid voltage. Moreover, the recovery time of a real diode is small in comparison with the period of the grid voltage (20 ms in case of a 50 Hz frequency).

Three-phase uncontrollable star rectifiers with resistive load

Fig. 3.2 shows the circuit of a single-phase uncontrollable half-wave rectifier. There are two types of star or wye rectifiers, more precisely those with common cathode and those with common anode. Both types will rectify the phase voltage. With the common cathode, the instantaneous DC-voltage will be equal to the highest instantaneous phase voltage which is positive at that moment. This means only the phase with the highest instantaneous phase voltage will supply current. The cathodes of the diodes connected with the other two phases have a higher potential than their anodes.

When the rectifier has a common anode, the instantaneous DC-voltage will be equal to the lowest (most negative) instantaneous phase voltage which is negative at that moment. This means only the phase with the lowest instantaneous phase voltage that will supply current at that moment. The anodes of the diodes connected with the other two phases have a lower potential than their cathodes.

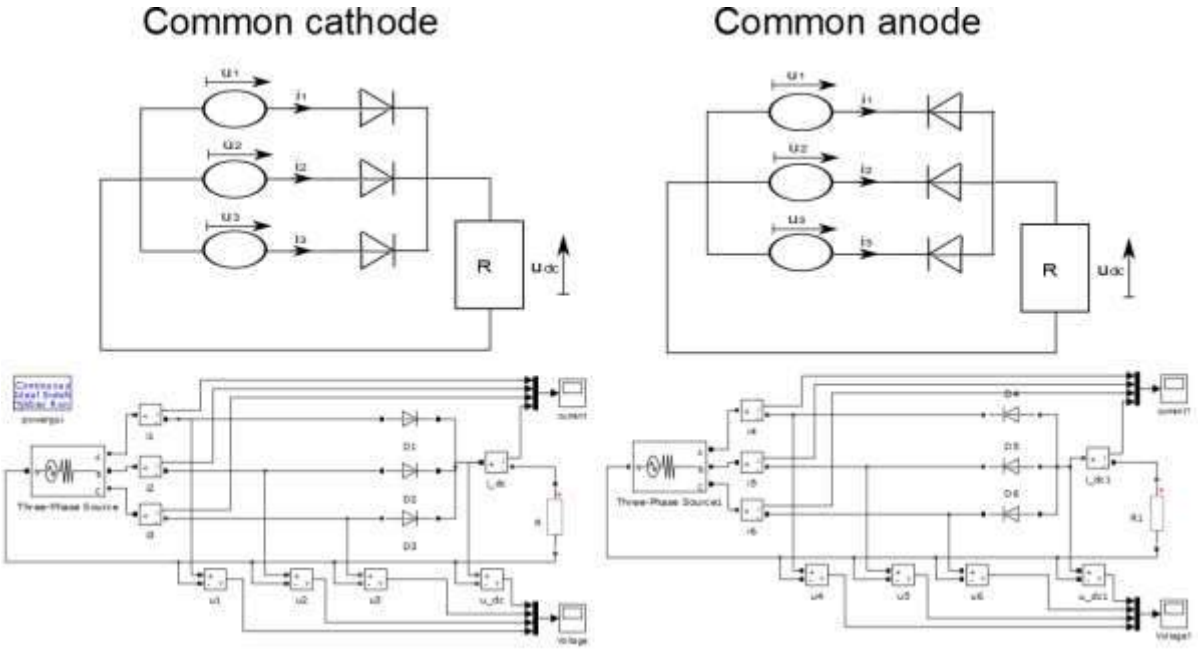


Fig. 3.41. The three-phase star rectifiers

Here, only the three-phase star rectifier (half-wave rectifier) with common cathodes will be discussed. After studying the rectifier with common cathodes, the reader should be able to study the three-phase star rectifier with common anodes.

The obtained DC-voltage u_dc equals to the maximum positive value of the three AC phase voltages u_ac, as shown in Fig. 3..42. Indeed, a three-phase star rectifier with common cathode only passes the highest phase voltage. The DC-voltage (a voltage is a DC voltage when the sign of the voltage does not change) is not constant but it can be described with a Fourier series. In general, the DC-powered devices are only interested in the average of the voltage, using equation (3-1).

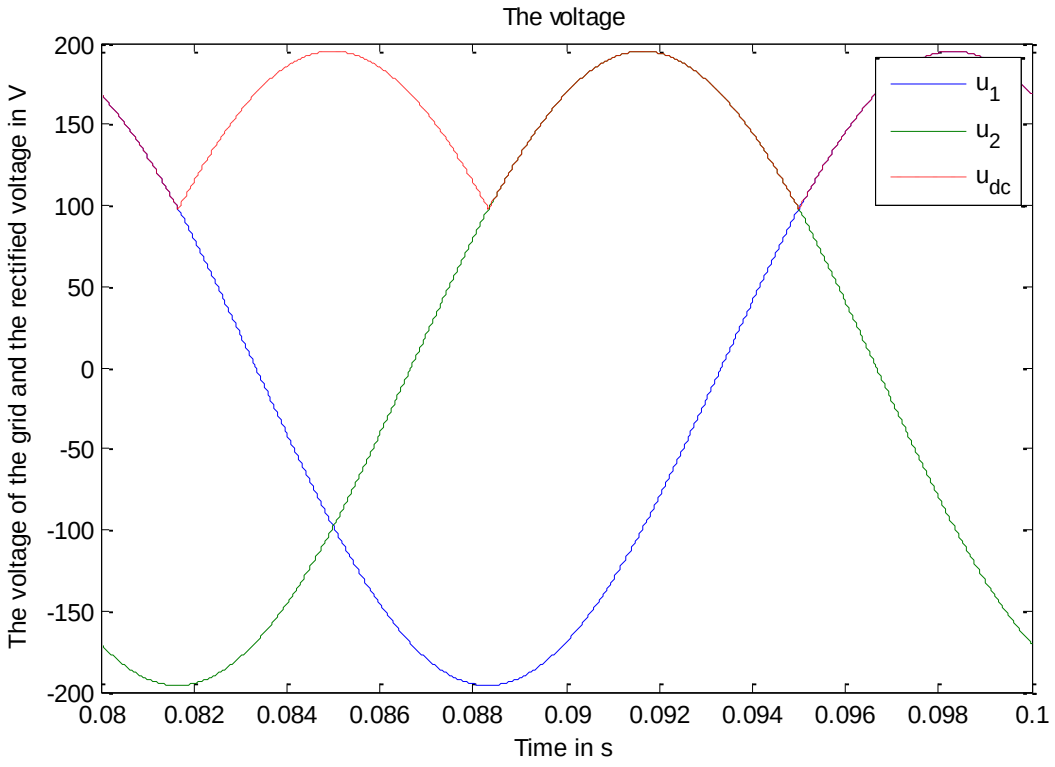


Fig. 3.42. The DC-voltage of the single-phase uncontrollable half-wave rectifier in case of an AC voltage with an rms value of 240V and a frequency of 50Hz

Studying Fig.3.42, a period of u_{dc} can be divided in three parts originating from the three phases of the grid. This leads to a mean value (θ: the period of u_{dc} equals $\frac{2\pi}{3}$ with respect of the fundamental u_3 and value equals u_3 in the domain $[\frac{\pi}{6}\ \frac{5\pi}{6}]$) which equals to:

$$U_{DC} = \frac{1}{\theta}\int_0^{\omega T/2} u_3(\omega t)\, d\omega t = \frac{3}{2\pi}\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} u_3(\omega t)\, d\omega t = \frac{3\sqrt{3}\sqrt{2}}{2\pi} U_{ac} i_{L\_ref} = \frac{1}{R_{ac_{eq}}(t)} u_{ac}(t) \quad (3\text{-}22)$$

References

M.H. Rashid, Power Electronics Handbook, Elsevier – Academic Press, 2011.

G. Merlevede, Vermogenelektronica, Acco

3.3.2. Three phase line-commutated diode rectifiers

Introduction

In an industrial environment, a three phase grid is almost always available implying the use of three phase rectifiers as common practice. A distinction can be made between:

- Half wave three-phase diode rectifiers,
- Halve wave three-phase thyristor rectifiers,
- Full wave three-phase diode rectifiers,
- Full wave three-phase thyristor rectifiers.

In the present section, diode rectifiers will be studied. We assume these diodes are ideal, i.e. the voltage drop of the conducting diode will be neglected, there is no leakage current in case of a reverse polarization, switching occurs without time delay, i.e. no time is needed to switch the diode on or off.

Half wave three-phase diode rectifier

Fig.3.43 visualizes a half wave three-phase diode rectifier. A transformer is supplying three phase voltages v_1, v_2 and v_3 which are assumed to be sinusoidal, which have three times the same amplitude and which have phase differences of 120°. The instants t_1,t_2, t_3, t_4, t_5 and t_6 in Fig. 3.43 are the natural commutation points implying the diodes D_1, D_2 and D_3 are conducting during 120° (during one third of 20 ms). Fig.3.43 also visualizes the rectified voltage which appears across the resistive load.

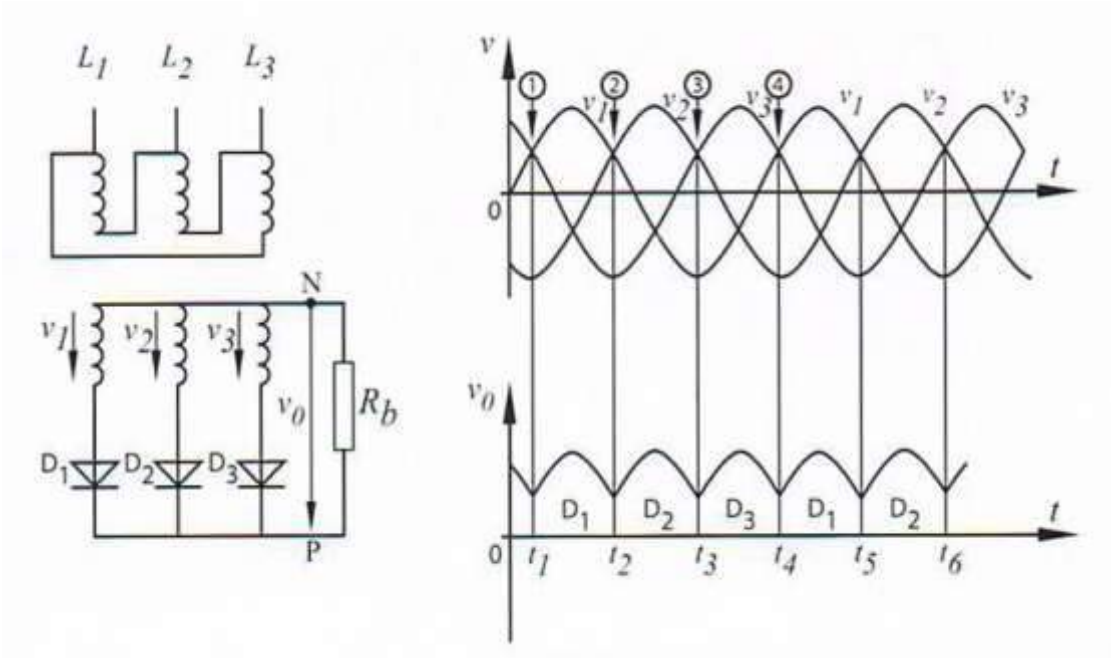


Fig. 3.43. Half wave three-phase rectifier (source: Pollefliet)

Fig.3.44 visualizes the rectified voltage. Without loss of generality, the zero point of ωt is assumed to correspond with the maximum of the phase voltage v_1 implying $v_1(t) = \hat{v}\cos(\omega t)$. The average value of the rectified voltage equals to:

$$V_{di} = \frac{1}{2\pi/3}\int_{-\pi/3}^{+\pi/3} \hat{v}\cos(\omega t)\, d(\omega t) = \frac{3\sqrt{3}}{2\pi}\hat{v} i_{L\_ref} = \frac{1}{R_{ac_{eq}}(t)} u_{ac}(t) \qquad (3\text{-}23)$$

In case V_f is the RMS value of the secondary phase voltage of the transformer, $\hat{v} = \sqrt{2}V_f$ implying

$$V_{di} = \frac{3\sqrt{6}}{2\pi} V_f i_{L\_ref} = \frac{1}{R_{ac_{eq}}(t)} u_{ac}(t) \qquad (3\text{-}24)$$

When the phase voltage has an RMS value of 230 V, a voltage V_{di} of 269 V is obtained.

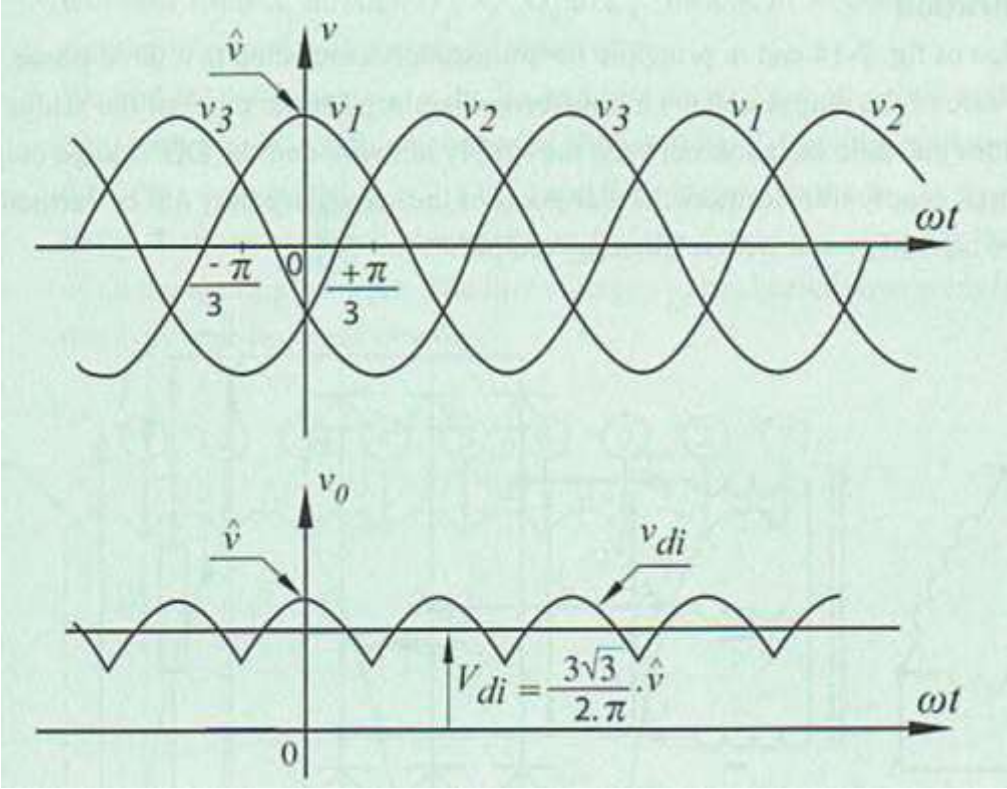


Fig. 3.44. Rectified voltage of the half wave three-phase diode rectifier (source: Pollefliet)

The rectified voltage in Fig.3.43 and Fig.3.44 is obtained in the case when the diodes commutate immediately. In reality, the transformer or the feeding grid will have an ohmic-inductive impedance. Due to this inductive behavior, a sudden increase or decrease of the grid or transformer current is not possible. In case the current commutates from diode D_1 to diode D_2 (at t_2), during a so-called overlap angle μ, diodes D_1 and D_2 are both conducting at the same time. Fig.3.45 visualizes the situation during the commutation process. Since D_1 and D_2 are conducting at the same time, the phases 1 and 2 are actually short-circuited. Since both diodes are conducting (the resistive part of the grid impedance has been neglected), the same voltage level occurs at their anodes and this voltage level equals to:

$$v_K(t) = \frac{v_1(t) + v_2(t)}{2} i_{L\_ref} = \frac{1}{R_{ac_{eq}}(t)} u_{ac}(t) \qquad (3\text{-}25)$$

$$v_K(t) = \frac{v_1(t) + v_2(t)}{2} .$$

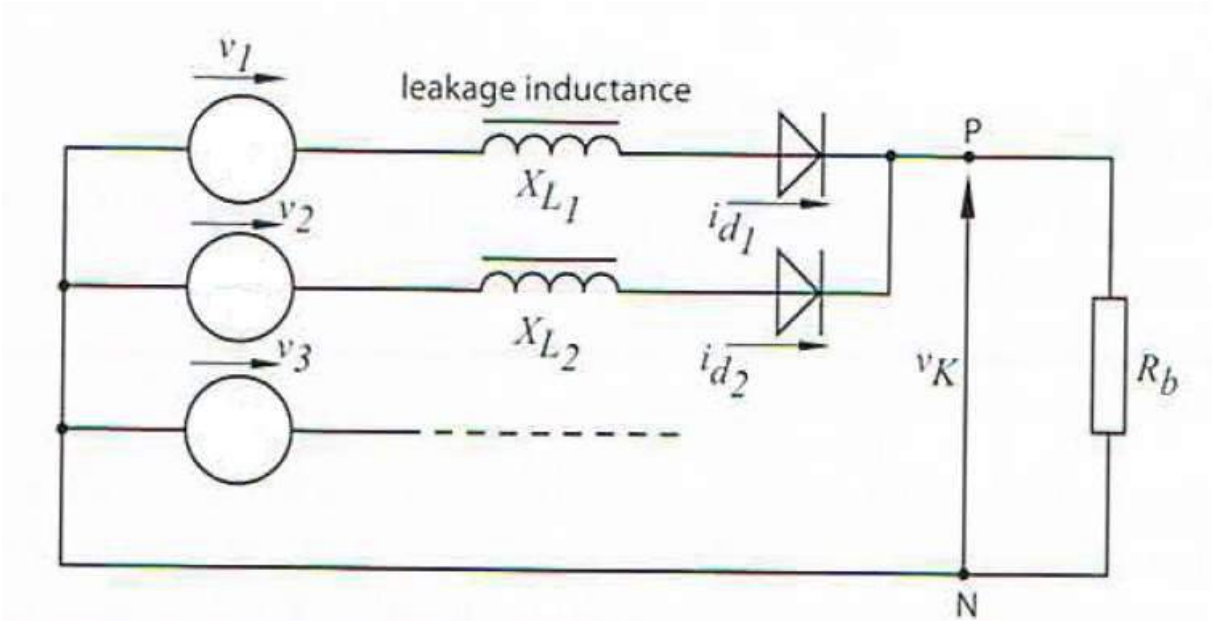


Fig. 3.45. Behavior of the commutation process (source: Pollefliet)

After t_2, the phase voltage v_2 becomes higher than v_1 which implies a positive voltage appears across the inductance of the second phase. The current of this second phase is increasing. Meanwhile, a negative voltage appears across the inductance of the first phase implying the current of this first phase is decreasing. Finally, after the commutation process, only diode D_2 is conducting.

During the commutation processes, $v_K(t)$ is smaller than the maxima of the instantaneous values of the phase voltages which gives a DC voltage as visualized in Fig. 3.46. During the overlap angles μ, the rectified output voltage is lower that leads to the voltage losses indicated by the shaded surfaces. This implies the average value of the output voltage decreases due to the non instantaneous commutation process.

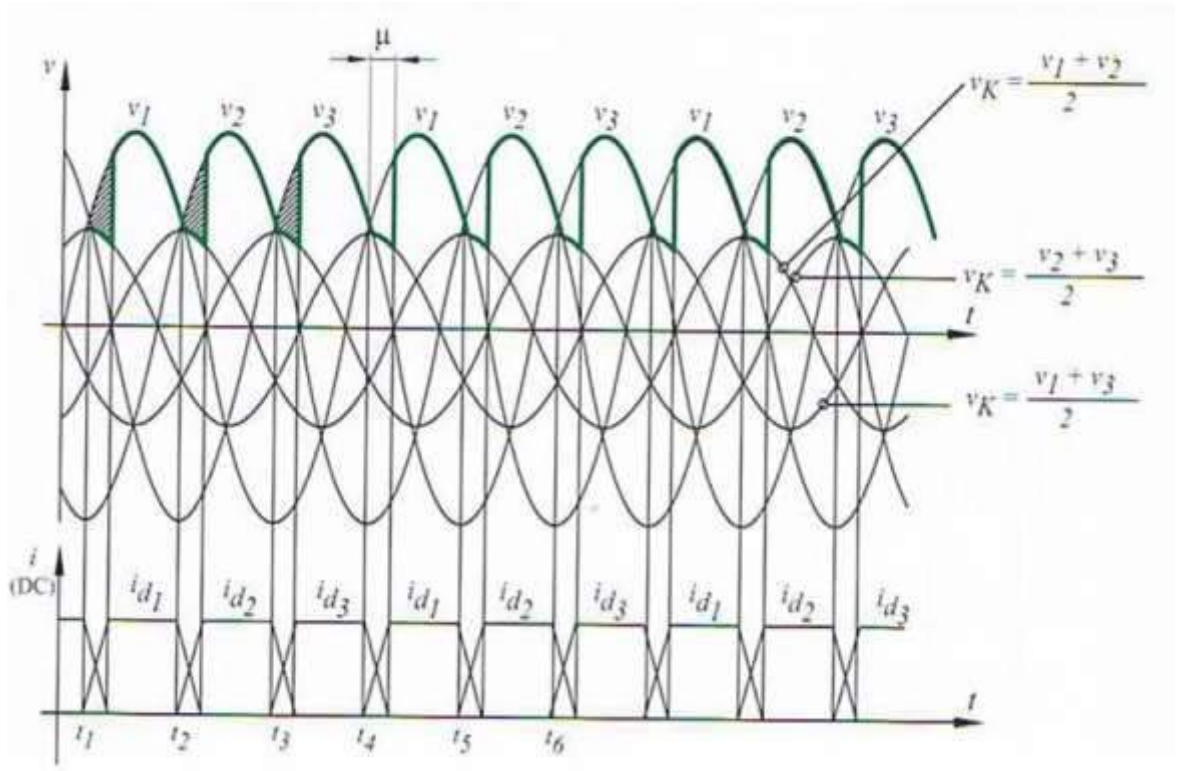


Fig. 3.46. Voltage and current waveforms due to non instantaneous commutation (source: Pollefliet)

In Fig. 3.43, a positive DC output voltage is obtained since the grid voltages are feeding the anodes and since the cathodes of the diodes are connected with each other. When connecting the anodes, a negative DC voltage is obtained. The working principle when connecting the anodes is very similar.

In Fig.3.43 and Fig. 3.45 the load is purely ohmic. The output voltage is visualized in Fig. 3.43 and this voltage is not constant with respect to the time implying the output current is also not constant with respect to time. Is case the load contains a sufficiently large inductance, the load current is (almost) constant. In such a situation the currents visualized in Fig.3.46 are obtained.

Since the diode rectifier is uncontrolled, the output voltage is fixed in case the AC supply voltage has a fixed RMS value. When the transformer has a changeable winding ratio, the output voltage of the rectifier can be controlled.

Full wave three-phase diode rectifier

Fig.3.47 visualizes a full wave three-phase diode rectifier. This diode bridge can be connected with the existing grid but it is also possible to use a transformer between the grid and the rectifier. Changing the winding ratio of this transformer allows to change the rectified DC voltage level since the diode bridge in uncontrolled. Due to the transformer, there is a galvanic isolation between the AC-grid and the DC-load. In Fig. 3.47 the star point of the secondary winding has not been earthed implying it is allowed to earth the DC-output.

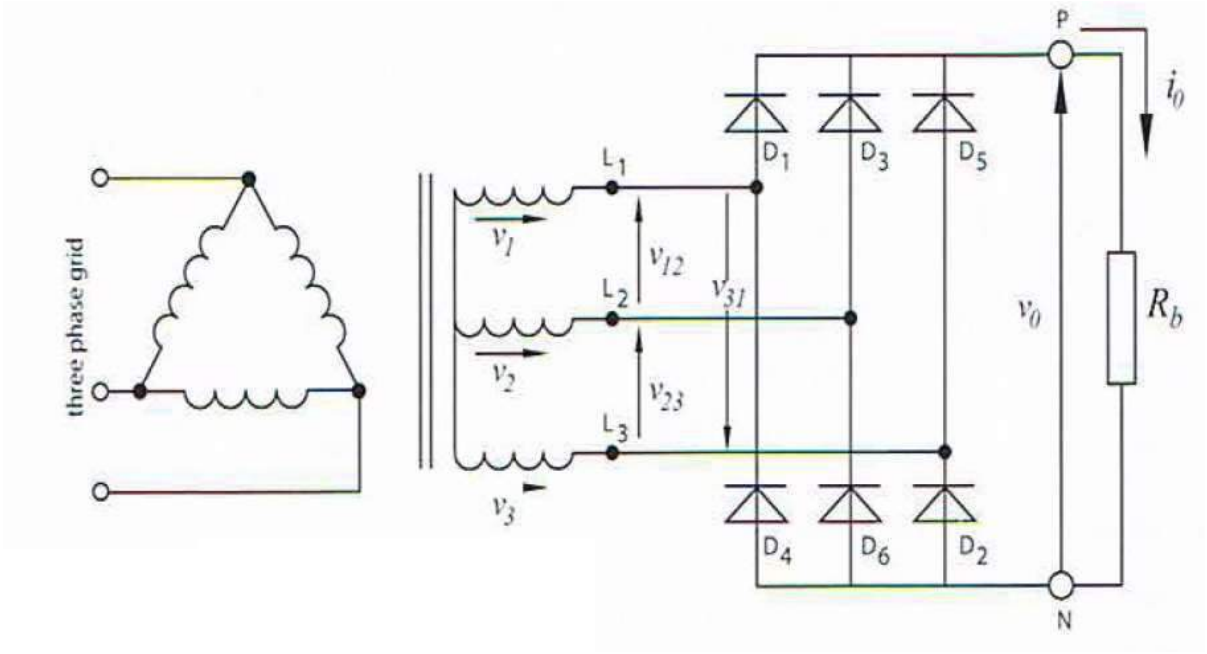


Fig. 3.47. Three-phase diode bridge rectifier (source: Pollefliet)

The voltages v_1, v_2 and v_3 of the secondary windings are phase voltages and the voltages v_{12}, v_{23} and v_{31} are line voltages. These line voltages are visualized in Fig. 3.48. In case for instance v_{12} is the largest instantaneous line voltage, then current will flow from L_1 to L_2 and this current will flow through diode D_1, load R_b and diode D_6. When the instantaneous largest voltage is v_{23}, then diodes D_3 and D_2 will conduct. When the largest instantaneous voltage is v_{31}, then diodes D_5 and D_4 will conduct.

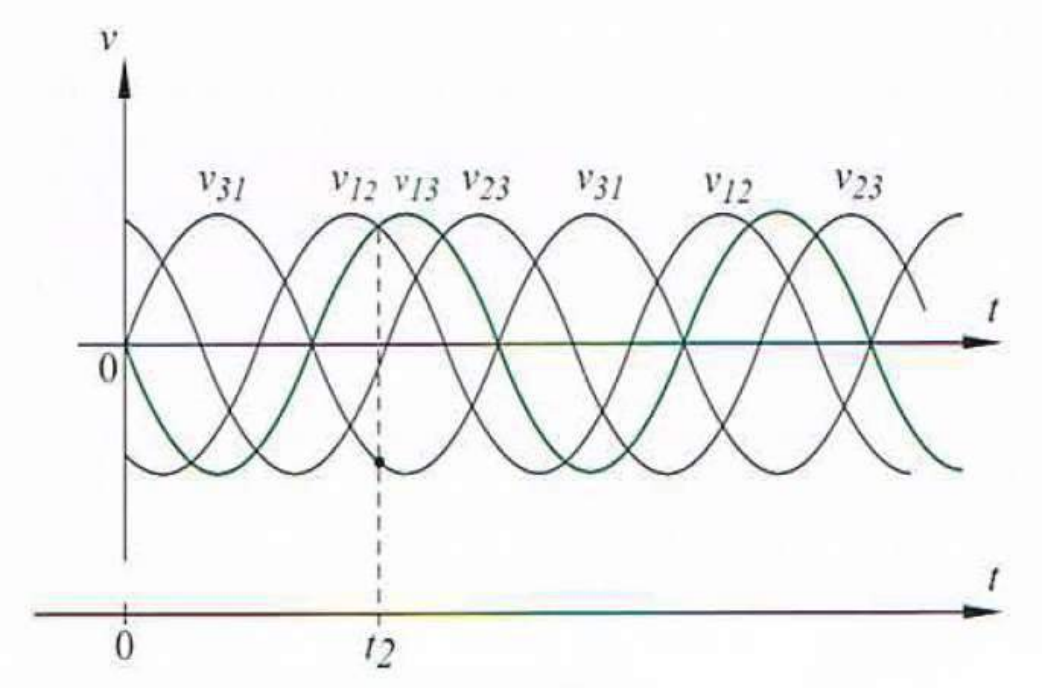


Fig. 3.48. Line voltages (source: Pollefliet)

In case v_{31} has the largest negative value as shown in Fig.3.48 from the instant t_2, a current will flow through D_1 and D_2. It is easier to use the positive voltage $v_{13} = -v_{31}$ instead of the negative voltage v_{31}. Since this is also the case for the other line voltages, it is a good practice

to work with voltages v_{12}, v_{23}, v_{31} and v_{21}, v_{32}, v_{13} as visualized in Fig. 3.49. The instantaneous maximum of these voltages determines which diodes are conducting as also visualized in Fig. 3.49.

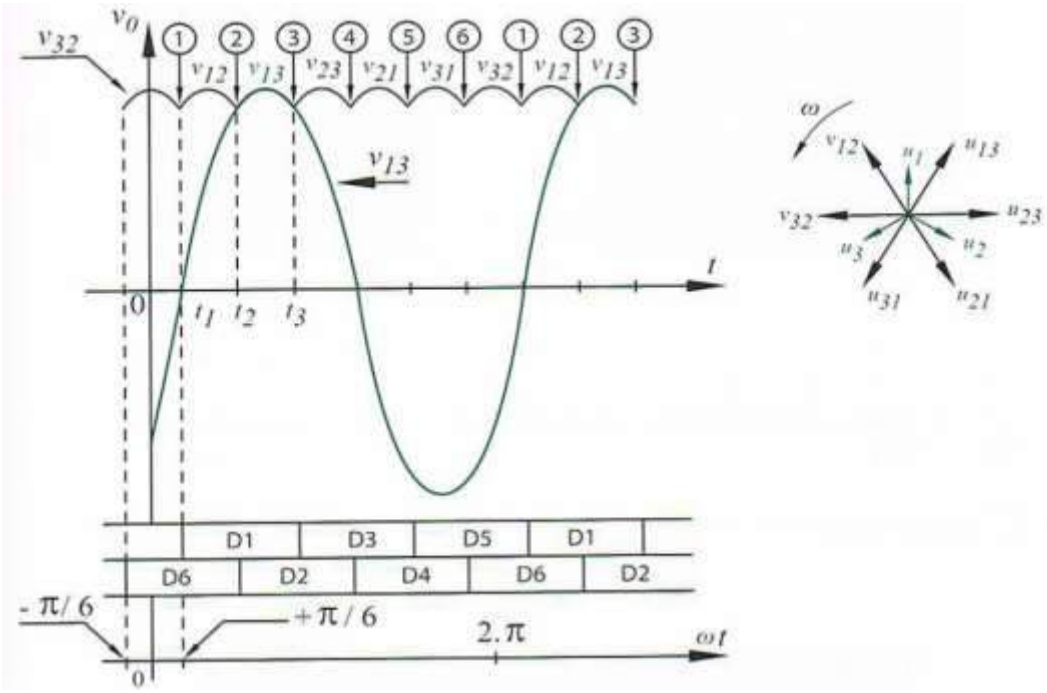


Fig. 3.49. Instantaneous values of the line voltages (source: Pollefliet)

At instant t_1 in Fig. 3.49, v_{12} becomes the line voltage with the largest instantaneous value implying the current is flowing from L_1 to L_2 through D_1, R_b and D_6. At instant t_2 in Fig. 3.49, v_{13} becomes the line voltage with the largest instantaneous value implying the current is flowing from L_1 to L_3 through D_1, R_b and D_2. This means D_2 has taken over from D_6, i.e. there is a commutation from D_6 to D_2. At instant t_3 in Fig. 3.49, v_{23} becomes the line voltage with the largest instantaneous value implying the current is flowing from L_2 to L_3 through D_3, R_b and D_2. This means there is commutation from D_1 to D_3. These instants t_1, t_2, t_3, … are the points of natural commutation.

Always one diode of the upper half of the bridge is conducting and always one diode of the lower half of the bridge is conducting. When ignoring the voltage drops across the diodes, the output voltage always equals the instantaneous maximum value of v_{12}, v_{13}, v_{23}, v_{21}, v_{31}, v_{32}. The output voltage is visualized in Fig.3.50 in combination with the output current in case the load is purely resistive.

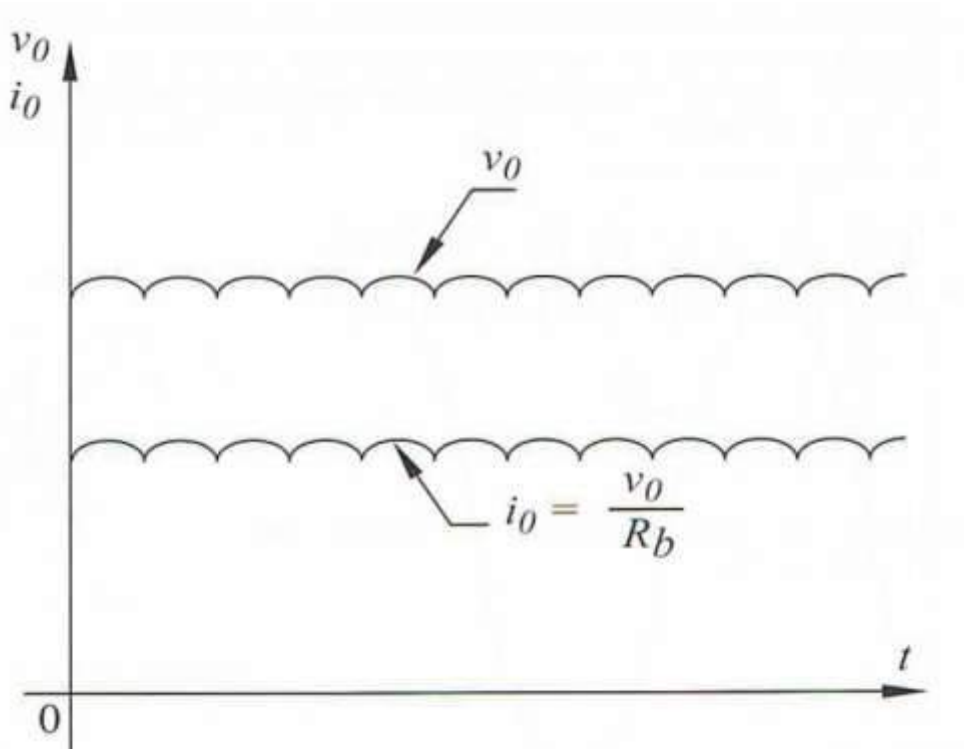


Fig. 3.50. Output voltage and output current of a diode bridge rectifier (source: Pollefliet)

Notice the frequency of the output DC voltage (300 Hz) is 6 times frequency of the grid voltage (50 Hz) which will be rectified. This implies the rectifier of Fig. 3.47 is a six pulse rectifier, i.e. the pulse number p equals 6.

Fig.3.50 visualizes the rectifier voltage. Without loss of generality, the zero point of ωt is assumed to correspond with the maximum of the line voltage v_{12} implying $v_{12}(t) = \sqrt{2}\, V_{line}\, cos(\omega t)$. The average value of the rectified voltage equals to:

$$V_{di} = \frac{1}{2\pi/6} \int_{-\pi/6}^{+\pi/6} \sqrt{2}\, V_{line} \cos(\omega t)\, d(\omega t) = \frac{3\sqrt{2}}{\pi} V_{line}\, \boldsymbol{i_{L\_ref}} = \frac{1}{\boldsymbol{R_{ac_{eq}}(t)}} \boldsymbol{u_{ac}(t)} \quad (3\text{-}26)$$

$V_{di} = \frac{1}{2\pi/6} \int_{-\pi/6}^{+\pi/6} \sqrt{2}\, V_{line} \cos(\omega t)\, d(\omega t) = \frac{3\sqrt{2}}{\pi} V_{line}$ .In case a line voltage of three times 400 V has been rectified, a mean DC voltage of 540 V is obtained.

Fig.3.51 visualizes a three phase full wave rectifier where the DC load is ohmic inductive. The inductor at DC side is assumed to be sufficiently large in order to obtain a constant DC current $i_O = I_d$. Fig.3.51 visualizes the output voltage and the output current. Fig.3.51 also visualizes the phase currents of the secondary windings of the transformer. This current is not a sine, i.e. it contains a 50 Hz first order harmonic and higher order harmonics. The current does not contain a DC component as it is in the case for a half wave rectifier which is an important advantage (neither the AC grid nor the transformer is designed to supply a DC-current).

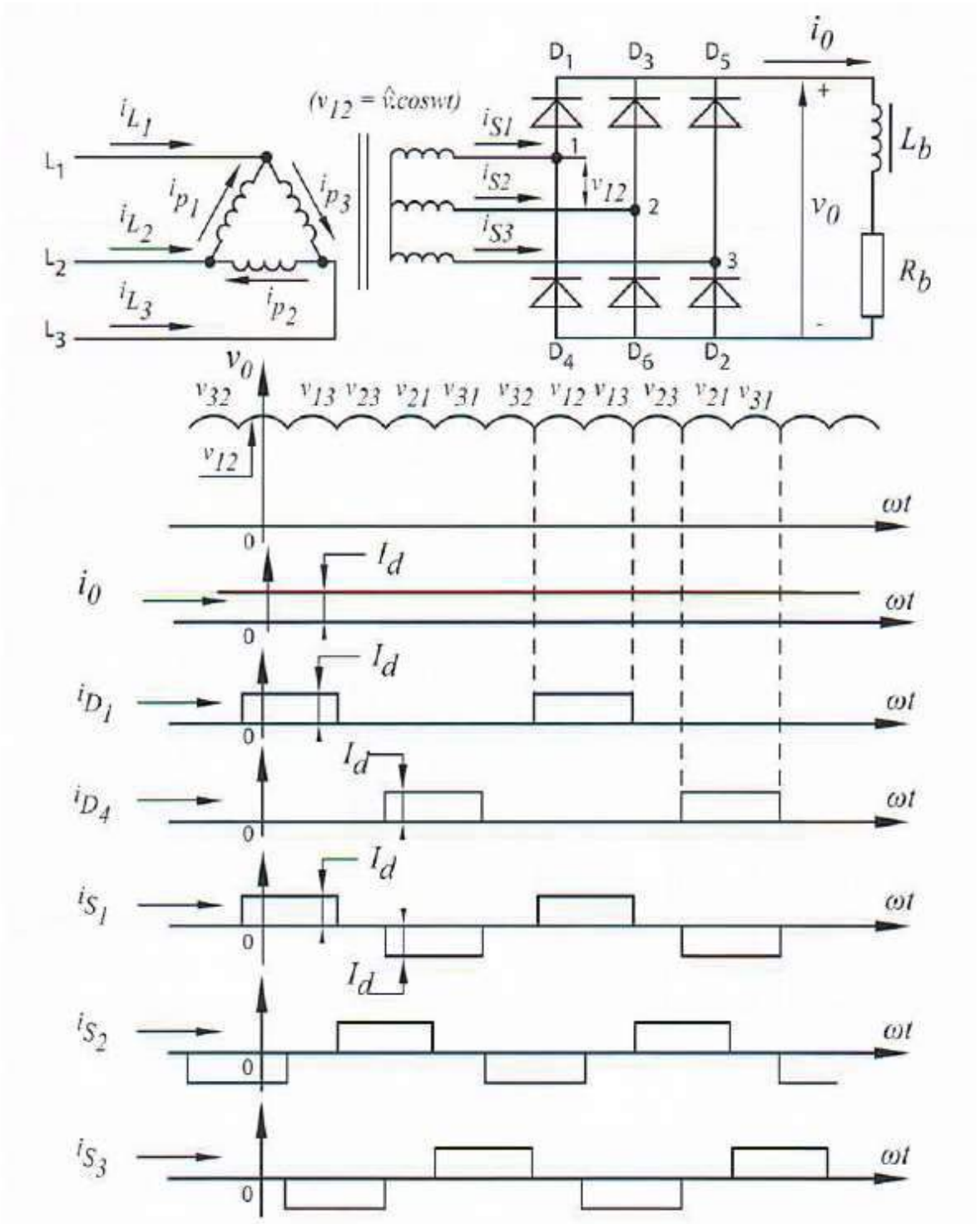


Fig. 3.51. Diode bridge rectifier with inductive load (source: Pollefliet)

References:

J. Pollefliet, Electronic Power Control: part 1: Power Electronics, Academia Press, Gent, Belgium, 2011

3.3.3. Three phase line-commutated thyristor rectifiers

Introduction

When using a three phase line-commutated diode rectifier, the rectifier is not able to change the DC output voltage. By replacing the diodes by thyristors and by choosing appropriate firing angles, the required DC output voltage will be obtained.

We assume these thyristors are ideal, i.e. the voltage drop of the conducting thyristor will be neglected, there is no leakage current in case the thyristor is not conducting, switching occurs without time delay, i.e. no time is needed to switch the thyristor on or off.

Full wave three-phase thyristor rectifier

Fig.3.52 visualizes a full wave three-phase thyristor rectifier. The voltages v_1, v_2 and v_3 of the secondary windings are phase voltages and the voltages v_{12}, v_{23} and v_{31} are line voltages. Also the voltages v_{21}, v_{32} and v_{13} are visualized. In Fig.3.52 the rectifier bridge containing thyristors Th_1, Th_2, Th_3, Th_4, Th_5 and Th_6 is loaded by an ohmic load R_b.

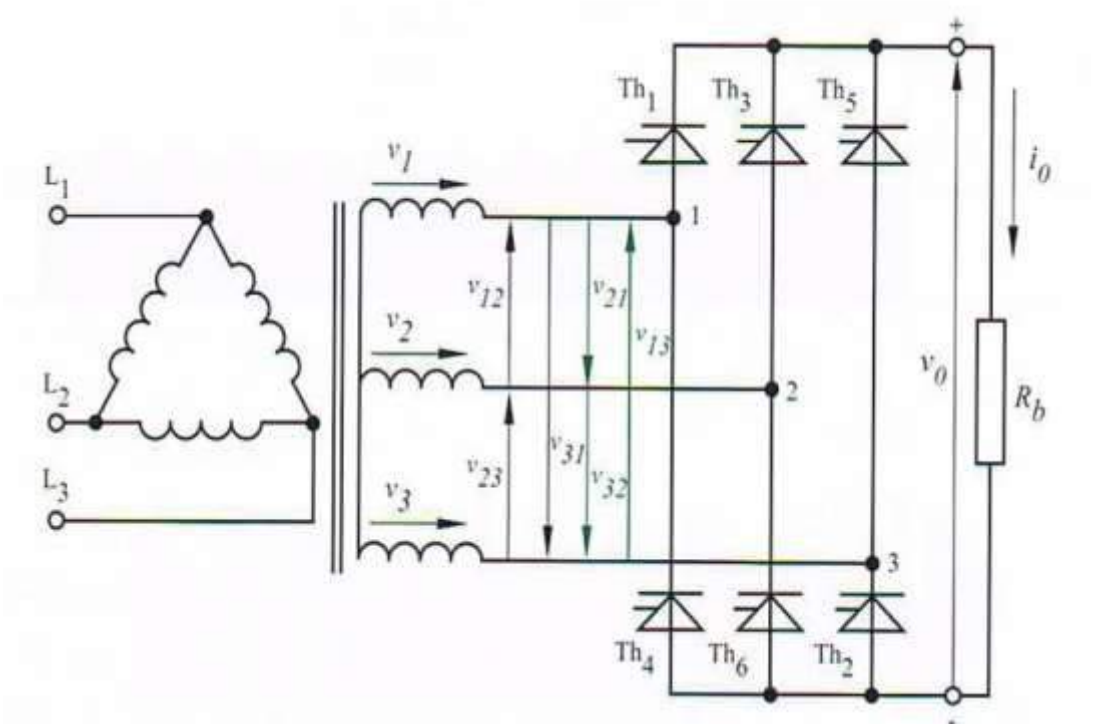


Fig. 3.52. Three-phase thyristor bridge rectifier (source: Pollefliet)

In case all thyristors are controlled with he help of a DC voltage between their respective gates and cathodes, they all behave as a diode implying the rectifier bridge behaves as a diode rectifier bridge. Fig.3.53 visualizes the voltages v_{12}, v_{23}, v_{31}, v_{21}, v_{32} or v_{13} having the largest instantaneous value. This determines the natural commutation points and which thyristors are conducting. Table 3-3 gives an overview of the line voltages with the largest instantaneous values acting as a driving voltage to conduct two thyristors.

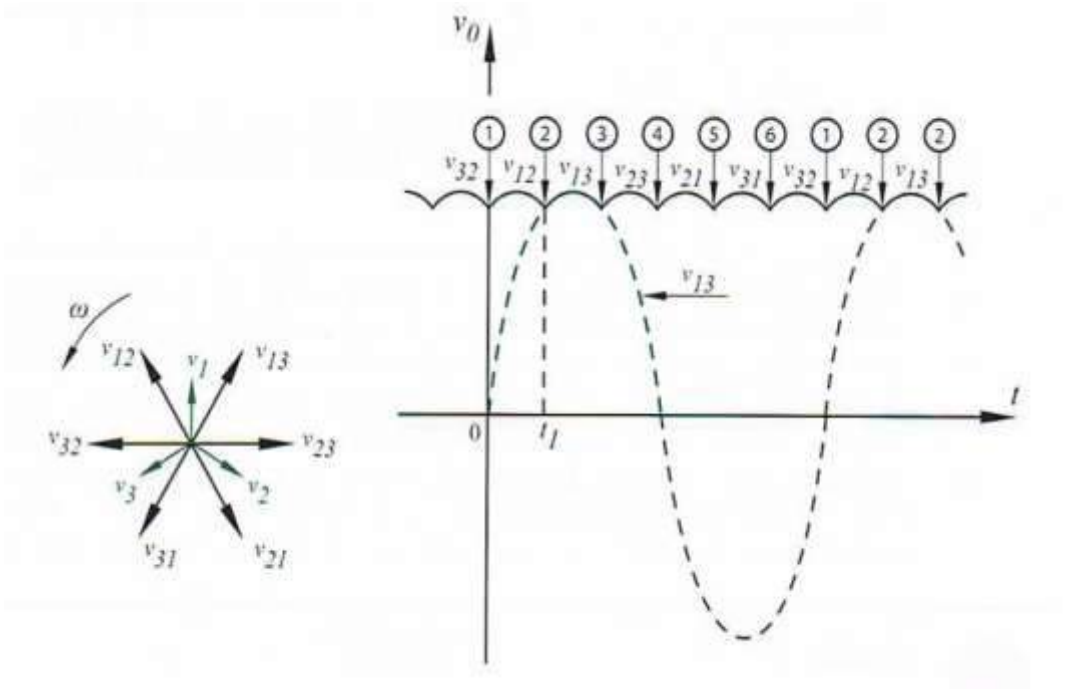


Fig. 3.53. Line voltages (source: Pollefliet)

Table 3-3: Overview conducting thyristor pairs

Driving voltage	Thyristor pair
v_{12}	Th_6 and Th_1
v_{13}	Th_1 and Th_2
v_{23}	Th_2 and Th_3
v_{21}	Th_3 and Th_4
v_{31}	Th_4 and Th_5
v_{32}	Th_5 and Th_6

By replacing the constant DC voltage between the gates and the cathodes by current pulses, the behavior of the thyristor bridge rectifier is obtained. The instantaneous times when the pulses are applied determine the shape of the DC output voltage and its average value. The firing angle α determines the time delay between the natural commutation points and the firing pulses sent to the gates of the appropriate thyristors.

Controlling the output voltage in the case of an ohmic load

The firing angle

Fig.3.54 visualizes the line voltages v_{12}, v_{23}, v_{31}, v_{21}, v_{32} and v_{13}. Fig.3.54 also visualizes the firing pulses of the six thyristors. These firing pulses coincide with the natural commutation points implying a firing angle $\alpha = 0°$.

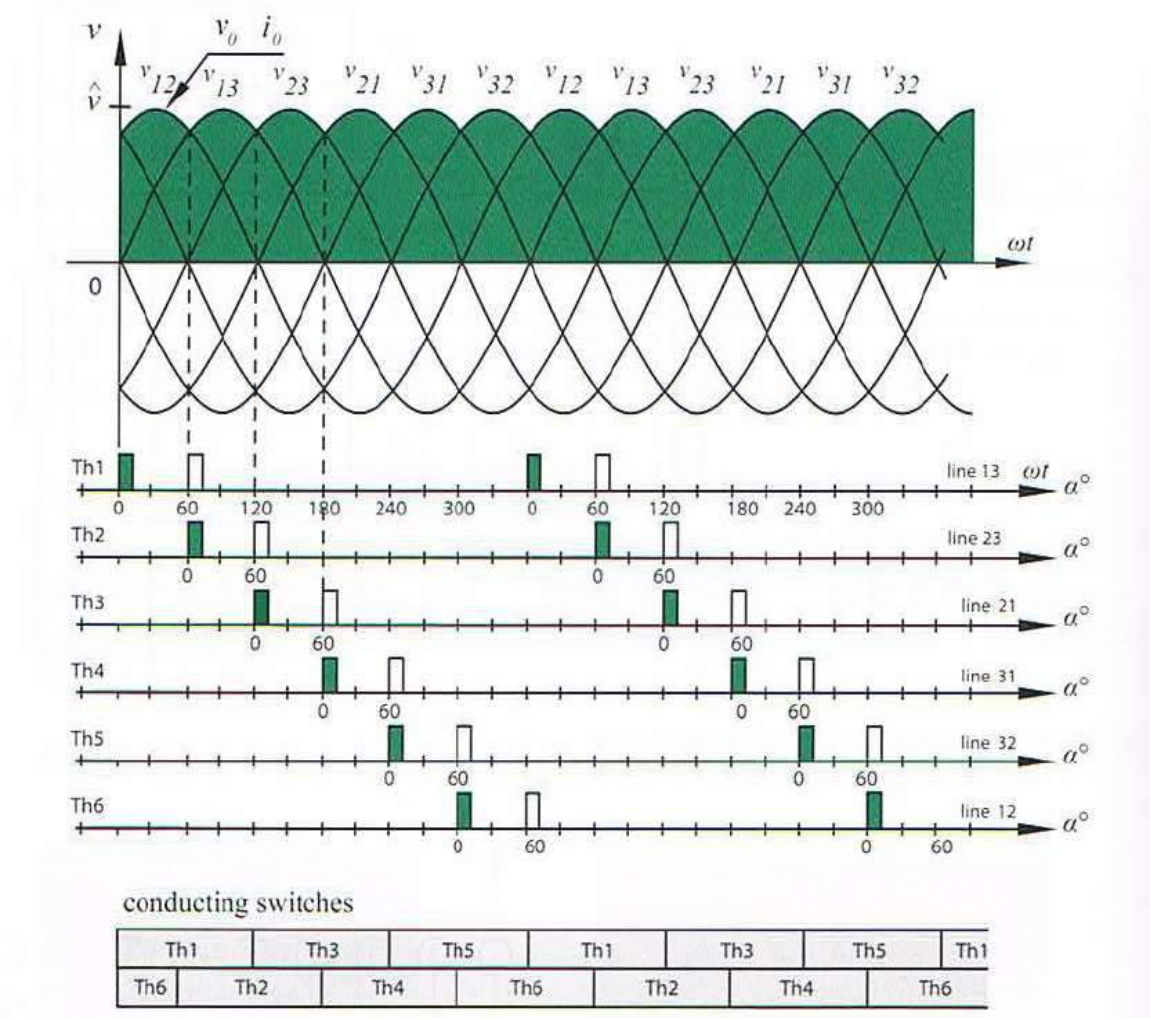
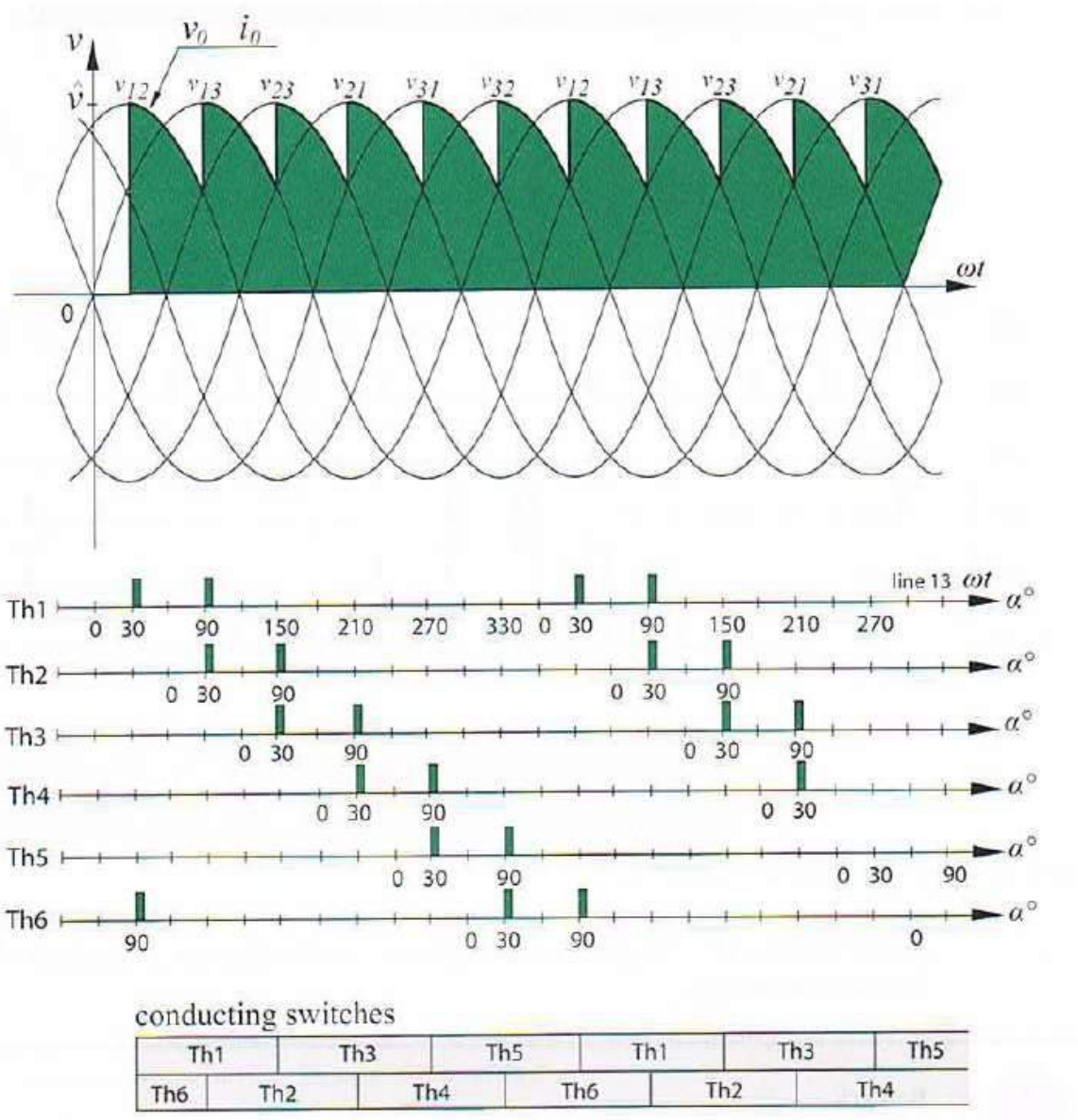


Fig. 3.54. Output voltage in case $\alpha = 0°$ (source: Pollefliet)

A gate pulse at $\omega t = 0°$ causes Th_1 to conduct since v_{12} is the most positive voltage at this moment. In order to allow the current to flow though the load, also Th_6 must conduct. This implies also a gate pulse to the gate of Th_6 is needed at $\omega t = 0°$. Since consecutively v_{12}, v_{13}, v_{23}, v_{21}, v_{31} and v_{32} are the most positive voltages, consecutively the gates of Th_6 + Th_1, Th_1 + Th_2, Th_2 + Th_3, Th_3 +Th_4, Th_4 + Th_5 and Th_5 + Th_6 are fired (always waiting an angle $\omega t = 60°$ which equals one sixth of a period). Fig. 3.54 also visualizes the output voltage.

Fig.3.55 visualizes the firing of the gates of the thyristors performed in the same way as in Fig. 3.54 but with a firing angle delay $\alpha = 30°$. Due to this firing angle delay, a lower average value of the output voltage is obtained. In case $\alpha = 60°$, the output voltage visualized in Fig. 3.56 is obtained implying even a lower average value of the output voltage is obtained.



conducting switches

Th1	Th3	Th5	Th1	Th3	Th5
Th6	Th2	Th4	Th6	Th2	Th4

Fig.3.55. Output voltage in case $\alpha = 30°$ (source: Pollefliet)

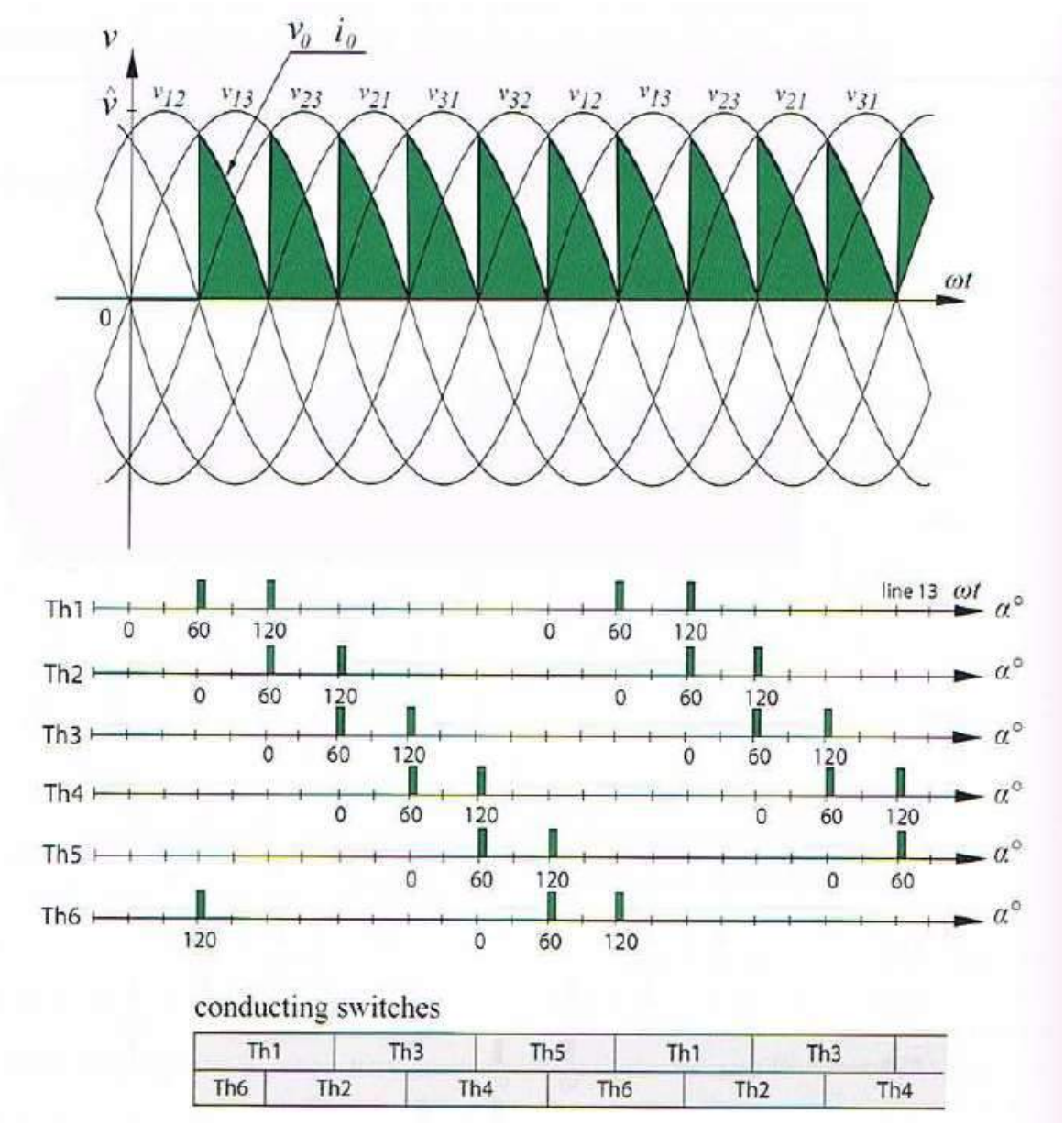


Fig. 3.56: Output voltage in case $\alpha = 60°$ (source: Pollefliet)

When considering the output voltages visualized in Fig.3.54, Fig.3.55 and Fig.3.56, always two thyristors are conducting. This implies the shape of the output voltage (and its average value) does not change when the resistive load is replaced with an inductive load. Fig.3.57 visualizes the shape of the output voltage in case $\alpha = 90°$ and the load is resistive. Fig.3.57 also visualizes the firing pattern of the gates of the thyristors. As also visualized in Fig. 3.57, a discontinuous current is obtained, i.e. the thyristors do not conduct during $120°$.

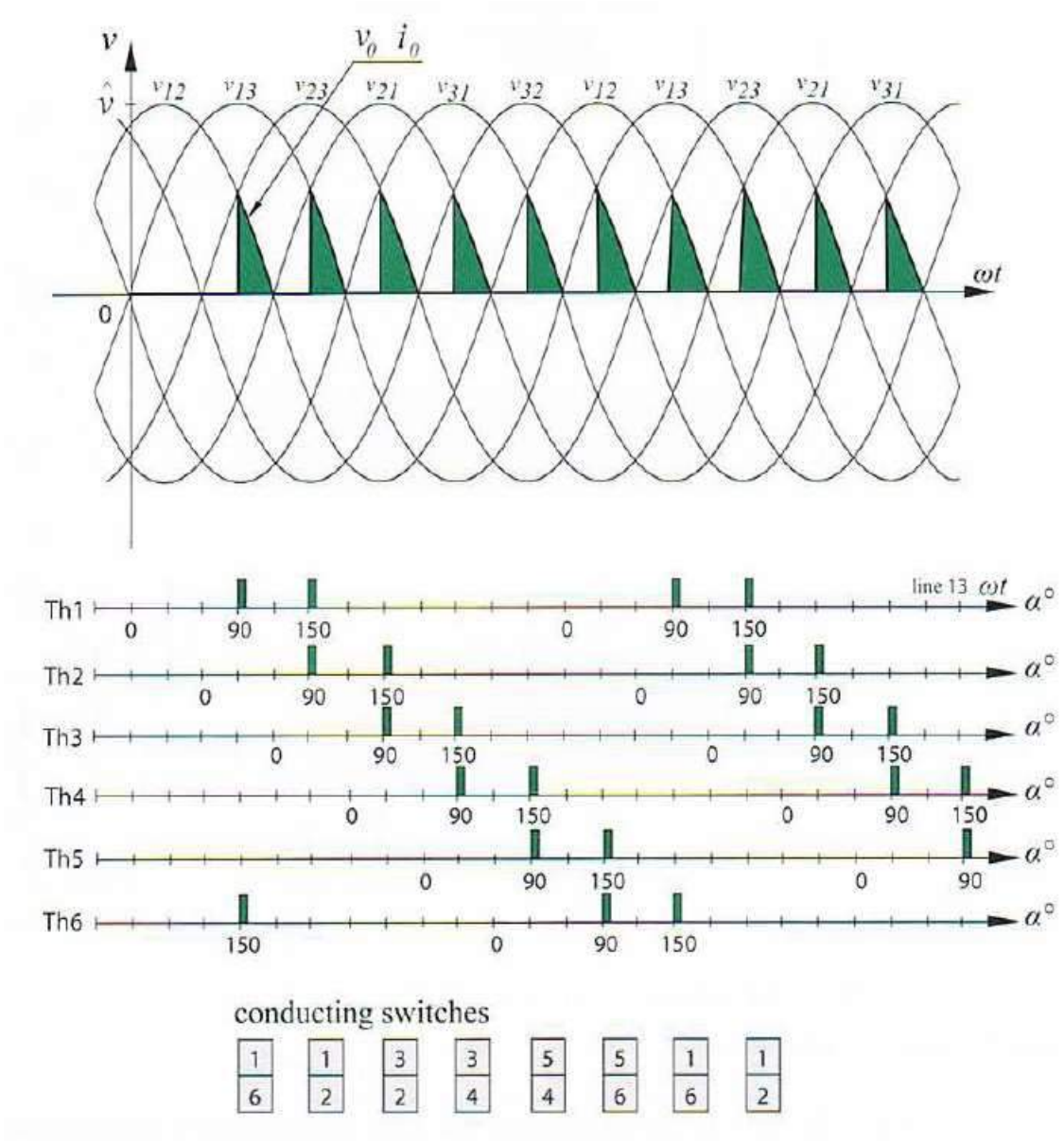


Fig. 3.57: Output voltage in case $\alpha = 90°$ (source: Pollefliet)

In case the firing angle $\alpha = 120°$, the output voltage is always zero as visualized in Fig.3.58.

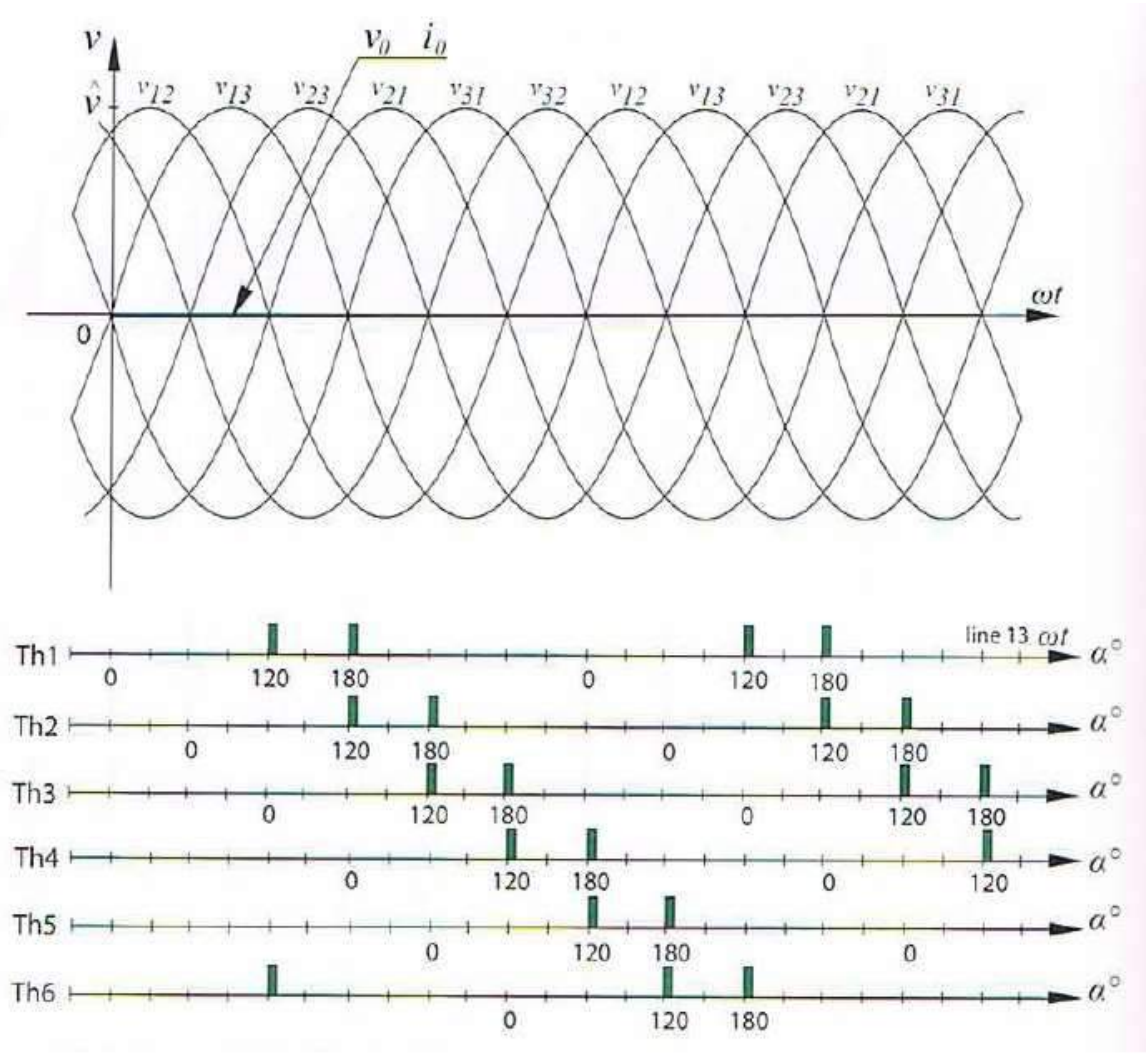


Fig. 3. 58. Output voltage in case $\alpha = 120°$ (source: Pollefliet)

The average value of the output voltage

By calculating the average value of the output voltage in continuous current mode ($0° < \alpha \leq 60°$), one obtains, based on Fig. 3.59, that:

$$V_{di\alpha} = \frac{1}{2\pi/6} \int_{\alpha+60°}^{\alpha+120°} \hat{v}\, sin\omega t\, d\omega t = \frac{3\,\hat{v}}{\pi} \cos(\alpha) \qquad i_{L\_ref} = \frac{1}{R_{ac_{eq}}(t)} u_{ac}(t) \qquad (3\text{-}27)$$

where $\hat{v}$ is the amplitude of the line voltage.

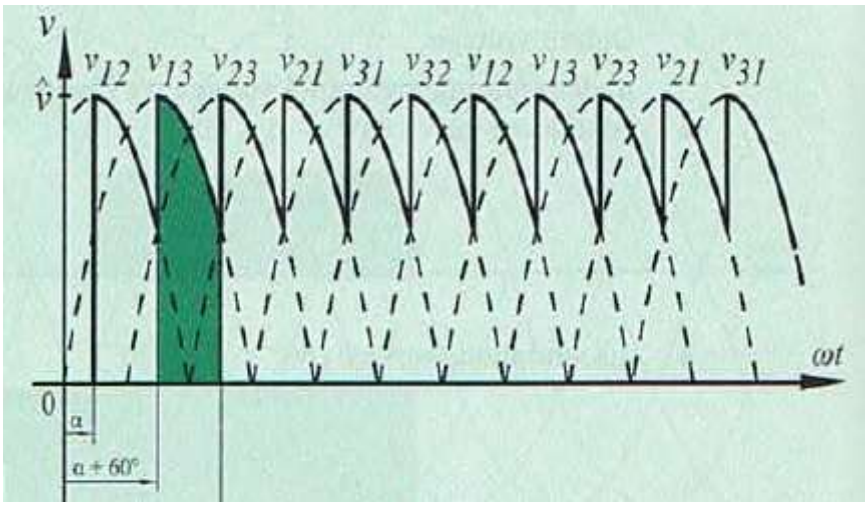


Fig. 3.59. Output voltage in case $0° < \alpha \leq 60°$ (source: Pollefliet)

When considering discontinuous mode ($60° < \alpha \leq 120°$) with a resistive load, Fig. 3.60 implies that the average value of the output voltage equals to:

$$V_{di\alpha} = \frac{1}{2\pi/6} \int_{\alpha+60°}^{180°} \hat{v}\, sin\omega t\, d\omega t = \frac{3\,\hat{v}}{\pi}\left(1 + \frac{cos(\alpha)}{2} - \frac{\sqrt{3}}{2}\, sin(\alpha)\right)$$

$$i_{L\_ref} = \frac{1}{R_{ac_{eq}}(t)}\, u_{ac}(t) \quad (3\text{-}28)$$

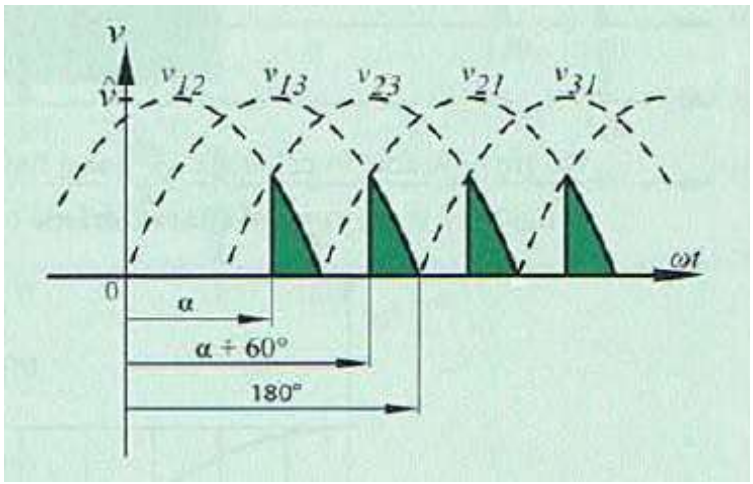


Fig. 3.60. Output voltage in case $60° < \alpha \leq 120°$ (source: Pollefliet)

When combining these two formulas, the so-called control characteristic of Fig. 3.61 of the six pulse thyristor rectifier bridge is obtained in the case of a resistive load.

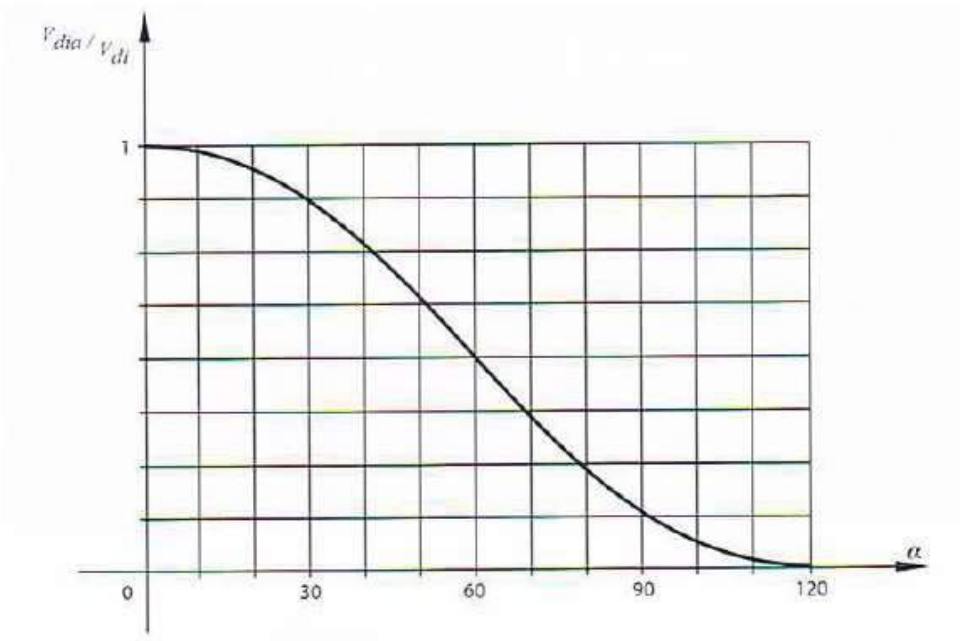


Fig. 3.61. Control characteristic of a thyristor rectifier with an ohmic load (source: Pollefliet)

Controlling the output voltage in the case of an inductive load

An ohmic inductive load

Fig.3.62 visualizes the same thyristor rectifier as Figure 1 but the load is a series circuit containing a resistor R_b and an inductor L_b. With a firing angle α up to 60°, the same output voltage is obtained like that with a resistive load i.e. the output voltages of Fig. 3.64, Fig. 3.65 and Fig. 3.66 are obtained. In the case of a resistive load, the output current has the same shape as the output voltage. In the case of an ohmic inductive load, the output current waveform is different and depends on the ratio L_b/R_b.

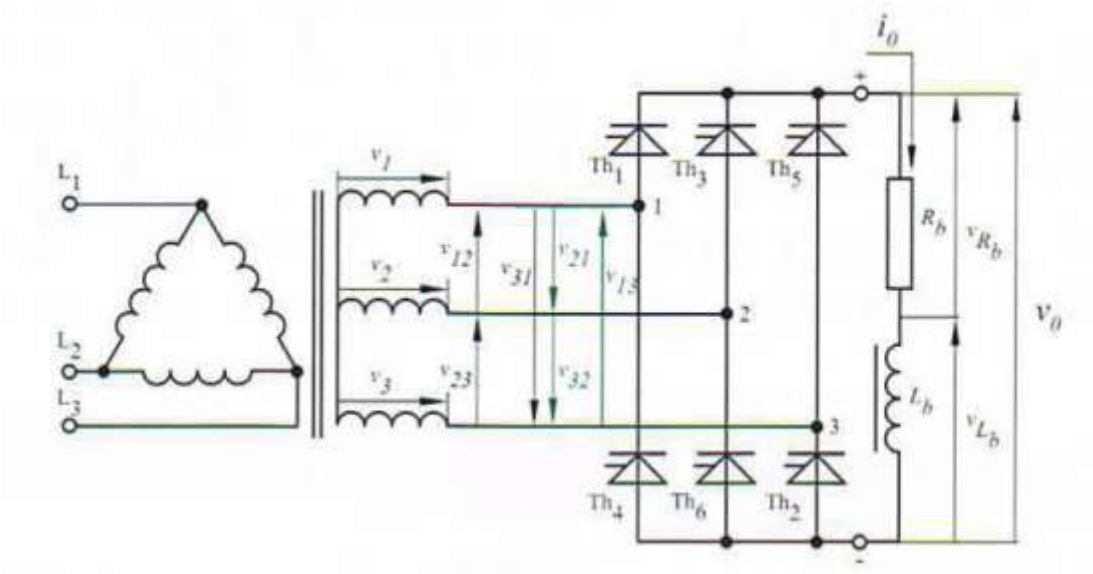


Fig. 3.62. Three phase thyristor rectifier bridge with ohmic inductive load (source: Pollefliet)

Fig.3.63 visualizes the voltage and the current waveform of the rectifier in Fig. 3.64 when the firing angle $= 60°$. At t_0, pulses are sent to the gates of Th_1 and Th_6 implying the positive

v_{12} voltage appears across the ohmic inductive load. Due to a positive voltage across L_b, the output current i_O increases and energy is stored in the magnetic field of the inductor. At t_1, the voltage $R_b i_O$ across the resistor equals v_{12} (which is decreasing). At t_1, the output current reaches a maximum value. Between t_1 and t_2, the voltage across the resistor is higher than v_{12} implying a negative voltage occurs across the inductor. The output current decreases.

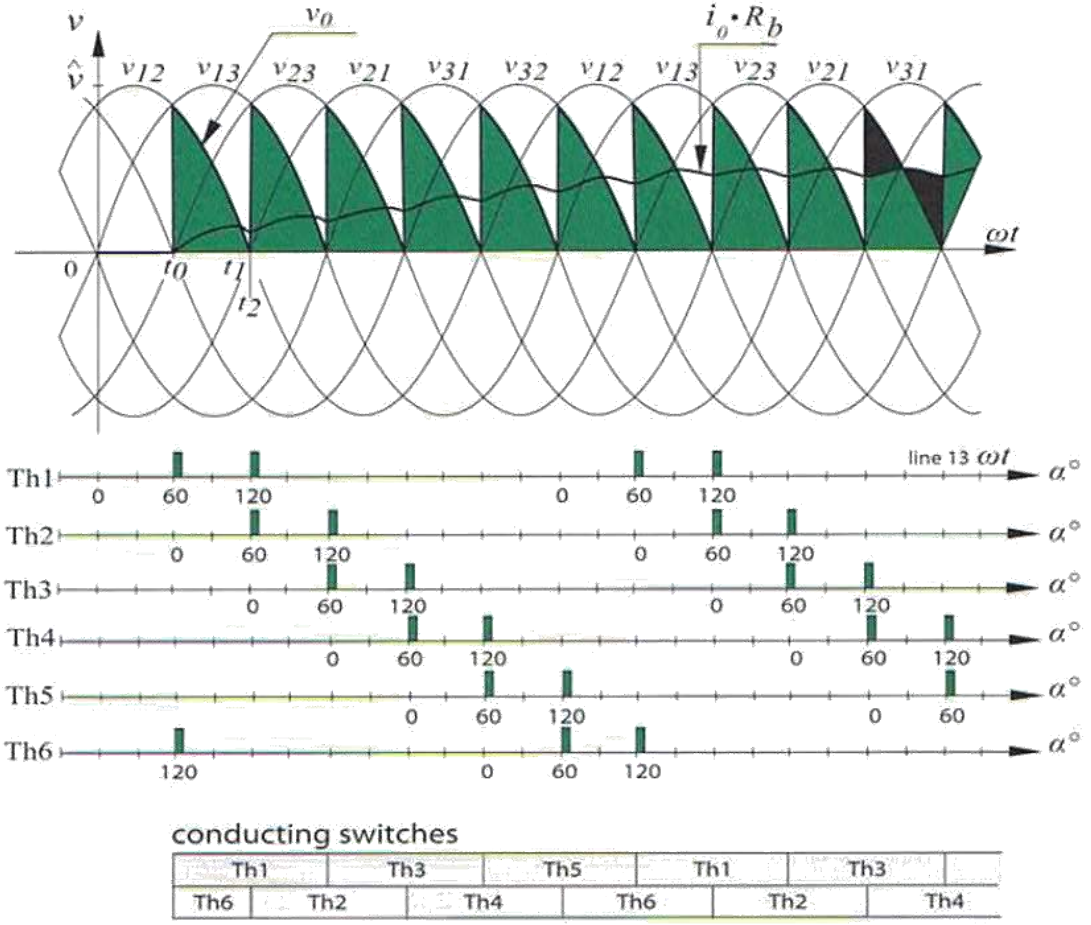


Fig. 3.63. Output voltage and current with ohmic inductive load for $\alpha = 60°$ (source: Pollefliet)

At t_2, the output current is not zero. The increase of the output current between t_0 and t_1 is larger than the decrease of the output current between t_1 and t_2. At t_2, Th_1 and Th_2 receive a gate pulse. This implies the current commutates from Th_6 to Th_2 and line voltage v_{13} instead of v_{12} appears at the output. Since v_{13} is larger than the voltage $R_b i_O$ across the resistor, again a positive voltage appears across the inductor. The output current increases implying the voltage across the resistor increases and becomes larger than v_{13} implying a new decrease of the output current.

As visualized in Fig. 3.63., a transient phenomenon occurs where a net increase of the output current is obtained. As the average value of this output current increases, the average value of the voltage across the resistor increases. This implies the positive voltages across the inductor become smaller and the negative voltages across the inductor become more negative. Finally, the steady state situation of Fig.3.64 is obtained. This steady state condition is determined by the equal surface area criterion ($A_1 = A_2$). Since A_1 equals to A_2, the increase of the output current equals to the decrease of the output current.

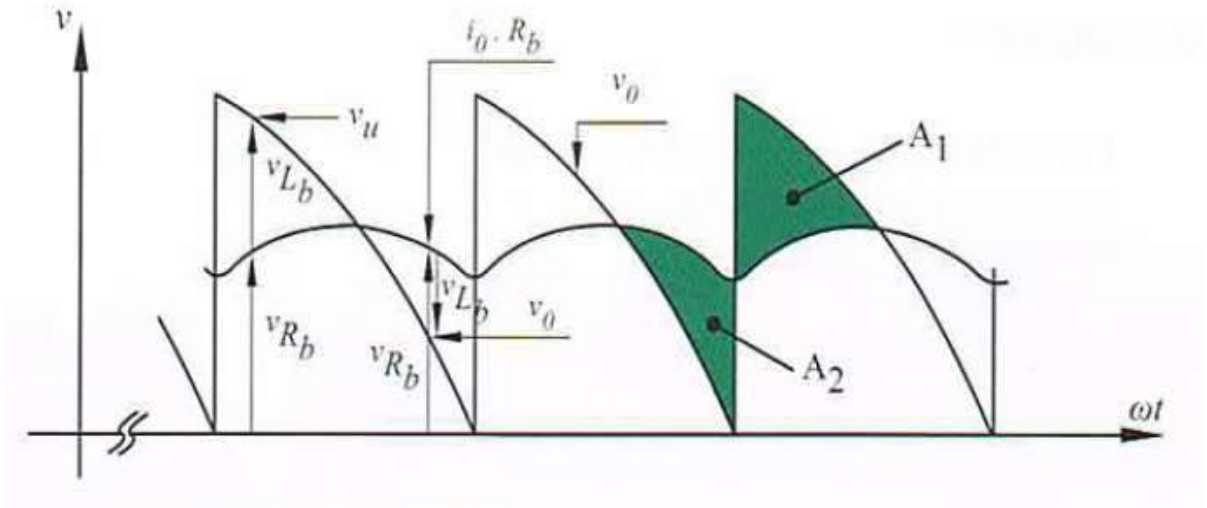


Fig. 3.64. Steady state condition of the output current (source: Pollefliet)

In Fig. 3.65., a firing angle of 90° instead of a firing angle of 60° is considered. Between t_0 and t_1, the rectified voltage is higher than the voltage across the resistor implying the output current is increasing. Between t_1 and t_2, the rectified lower is smaller than the voltage across the resistor implying the output current is decreasing. Even for negative values of the output voltage, the current is still positive implying the thyristors remain conducting.

When comparing Fig. 3.65 with Fig. 3.66, the thyristors are conducting during a longer period of time. In Fig. 3.65, also negative output voltages appear which is not the case in Fig. 3.57. This implies the average value of the output voltage is smaller in Fig. 3.65. The black areas at the right of Fig.3.65 visualize the output voltage.

In case of firing angles α between 0° and 60°, the average value of the output voltage is the same when comparing an ohmic load and an ohmic-inductive load. In the case of firing angles α between 60° and 90°, the average value of the output voltage is smaller due to the inductive part of the load. As the ratio L_b/R_b increases, the average value of the output voltage decreases.

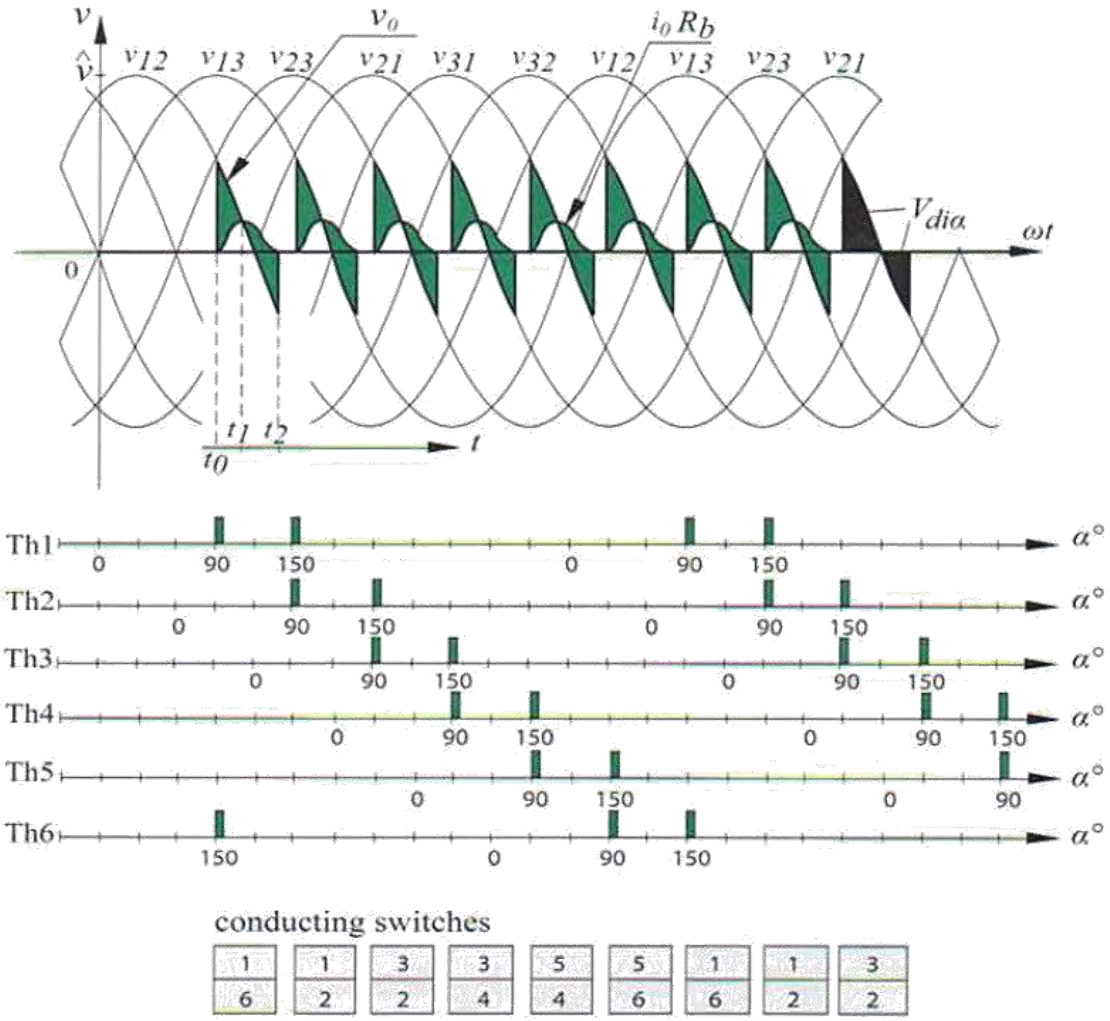


Fig. 3.65. Current and voltage waveforms for $\alpha = 90°$ (source: Pollefliet)

Inverter mode

In case the thyristor rectifier of Fig. 3.52 or Fig. 3.62 is loaded with an ohmic load or an ohmic inductive load, active power is consumed from the grid and provided to the load which consumes this power (actually the resistor). However, the thyristor rectifier allows an active power reversal. In case,

- the firing angle α is larger than 90°,
- the load is sufficiently inductive,
- the load contains a co-operating emf E,

the emf E is able to generate electrical power and send this power to the grid. The rectifier behaves as an inverter.

Fig.3.66 visualizes the thyristor rectifier bridge with a load containg a resistive part, an inductive part and a co-operating emf E. Notice that the output voltage $v_O = -E + v_{R_b} + v_{L_b}$. Suppose $\alpha = 120°$ and the output voltage is visualized in Fig. 3.67.

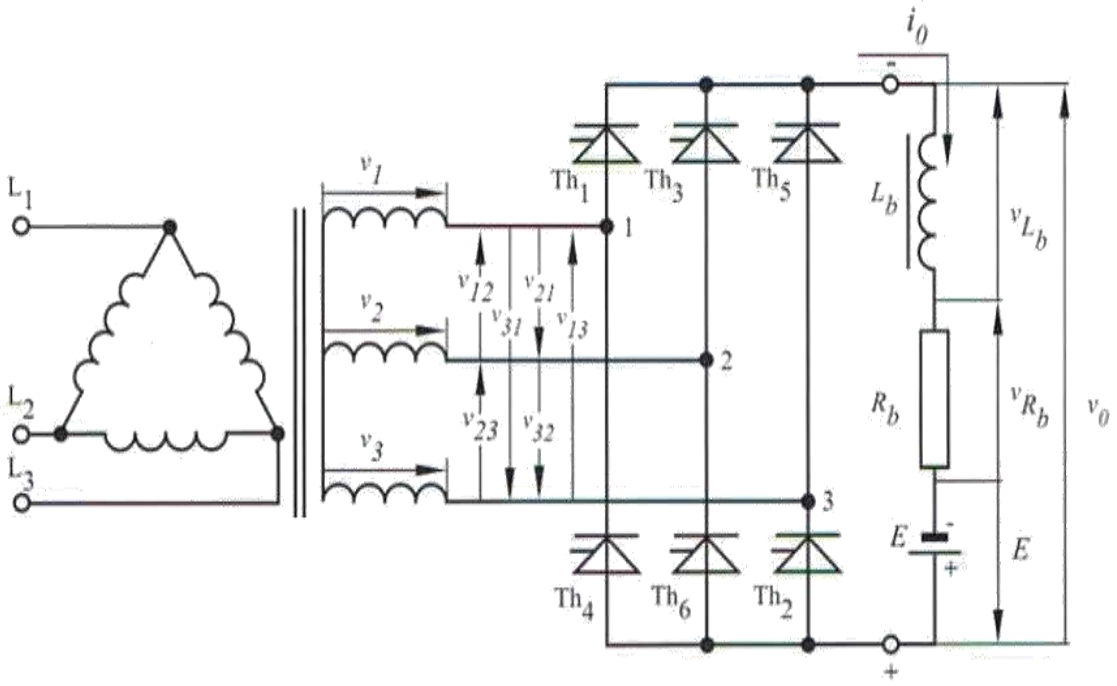


Fig. 3.66. Thyristor rectifier bridge with co-operating emf (source: Pollefliet)

At t_0, in Fig. 3.67.(a) and Fig. 3.67.(c) pulses are sent to the gates of Th_1 and Th_6. Due to E, the cathode of Th_1 is negative with regard to the anode of Th_6 implying Th_1 and Th_6 start to conduct. The output voltage v_O will follow v_{12}. As visualized in Fig. 3.67.(a), the voltage $-E + R_b i_O$ is more negative than v_{12} implying a positive voltage across L_b. Between t_0 and t_1, the output current increases due to this positive inductor voltage. At t_1, the voltage across the inductor becomes negative implying the output current decreases. Fig. 3.67(a) shows a transient behavior where between t_0 and t_2, a net increase of the current occurs.

Fig. 3.67.(b) shows a steady state behavior where due to the average value of the output current (and the voltage drop across the resistor), the voltage across the inductor has an average value which equals zero, i.e. the equal surface criterion is valid. The increase of the output current equals to the decrease of the output current.

Fig. 3.67.(c) visualizes the situation where all thyristors are conducting during 120° due to the inductor. With $\alpha = 120°$, an output voltage with a negative average value is obtained and since this output current is positive the load consumes a negative power, i.e. the load generates an electrical power which is injected into the feeding AC-grid.

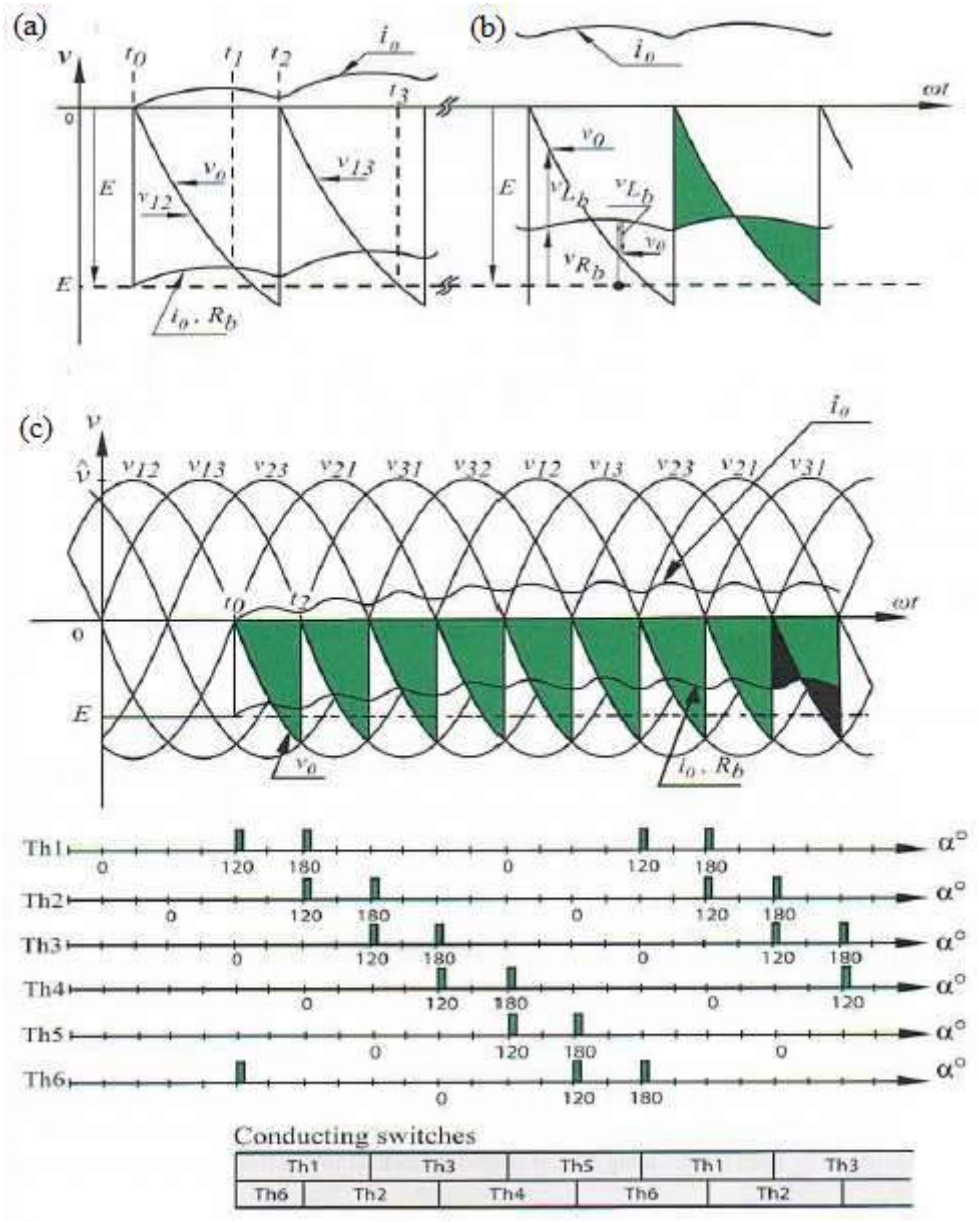


Fig. 3.67. Output and current waveform in case for $\alpha = 120°$ (source: Pollefliet)

The average value of the output voltage

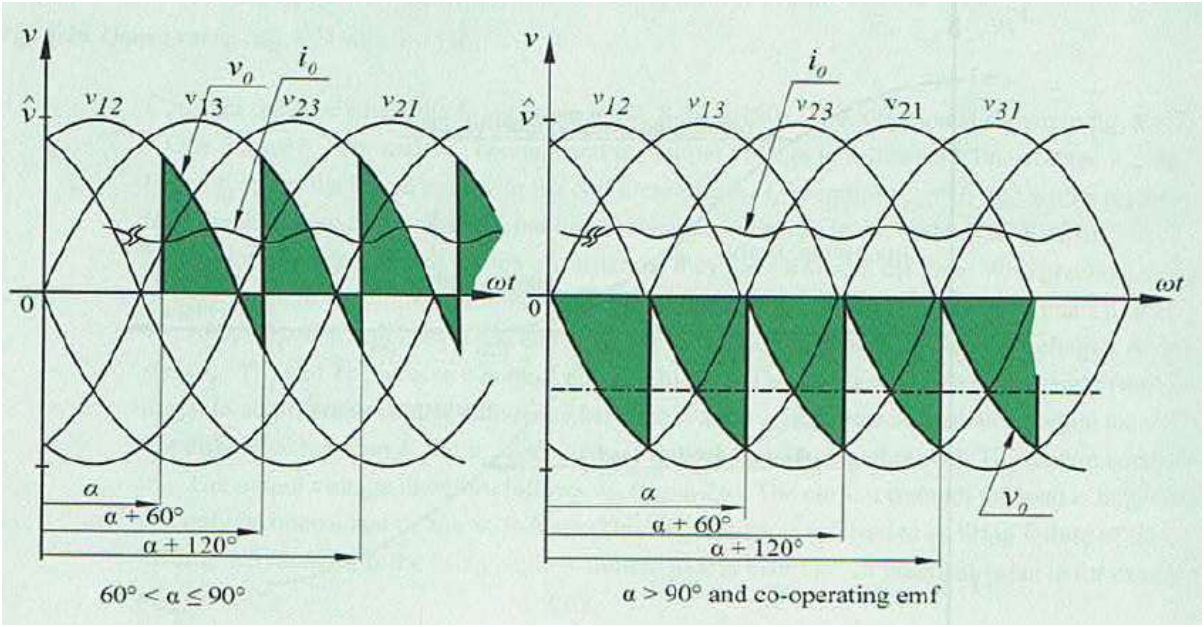
In case $0° < \alpha \leq 60°$, the output voltage waveform obtained by the ohmic inductive load equals to the output voltage waveform obtained by the ohmic load. This implies:

$$V_{di\alpha} = \frac{1}{2\pi/6}\int_{\alpha+60°}^{\alpha+120°} \hat{v}\, sin\omega t\, d\omega t = \frac{3\,\hat{v}}{\pi}\cos(\alpha) \qquad i_{L\_ref} = \frac{1}{R_{ac_{eq}}(t)}u_{ac}(t) \qquad (3\text{-}29)$$

where $\hat{v}$ is the amplitude of the line voltage. In case $60° < \alpha \leq 90°$ and the load is sufficiently inductive to maintain a continuous current, the average of the output voltage equals (see Fig. 3.68.(a))

$$V_{di\alpha} = \frac{1}{2\pi/6}\int_{\alpha+60°}^{\alpha+120°} \hat{v}\, sin\omega t\, d\omega t = \frac{3\,\hat{v}}{\pi}\cos(\alpha) \qquad i_{L\_ref} = \frac{1}{R_{ac_{eq}}(t)}u_{ac}(t) \qquad (3\text{-}30)$$

which is the same expression as in case $0° < \alpha \leq 60°$.



(a) (b)

Fig. 3.68. Voltage output waveforms (source: Pollefliet)

In case $90° < \alpha \leq 180°$ and there is a co-operating emf E, the voltage waveform is visualized in Fig. 3.68.(b). Also in this situation,

$$V_{di\alpha} = \frac{1}{2\pi/6}\int_{\alpha+60°}^{\alpha+120°} \hat{v}\, sin\omega t\, d\omega t = \frac{3\,\hat{v}}{\pi}\cos(\alpha) \qquad i_{L\_ref} = \frac{1}{R_{ac_{eq}}(t)}u_{ac}(t) \qquad (3\text{-}31)$$

Fig.3.69 visualizes the control characteristic of the thyristor rectifier in the case of an ohmic inductive load (with a sufficiently large inductor and with an additional emf E when $\alpha > 90°$). This characteristic is compared with the control characteristic in the case of an ohmic load. In case $\alpha > 90°$ the output voltage has a negative sign without a reversal of the output current that indeed implies inverter operation.

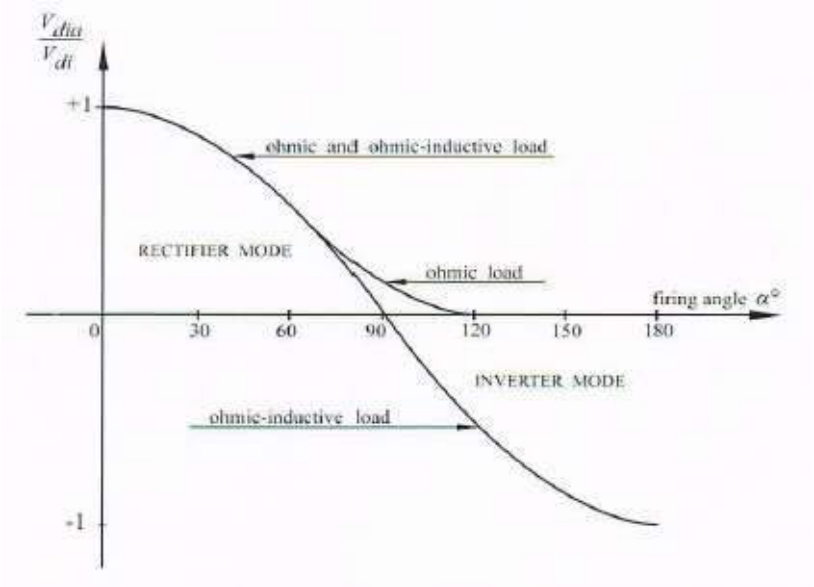


Fig. 3.69. Control characteristic thyristor rectifier with an ohmic inductive load (source: Pollefliet)

References:

J. Pollefliet, Electronic Power Control: part 1: Power Electronics, Academia Press, Gent, Belgium, 2011.

3.3.4. Active Front End

Introduction

Traditionally, a frequency converter contains a diode or thyristor rectifier to obtain a DC-voltage (an inverter converts this DC-voltage into a PWM voltage approximating a sine voltage). In the case of a classical diode rectifier two problems or limitations arise.

- The grid current consumed by the diode rectifier does not have a sinusoidal shape, i.e. it contains a lot of harmonics causing pollution of the grid.
- The diode rectifier is only able to consume active power, i.e. no active power can be injected into the grid by the rectifier.

When replacing the diode rectifier with a thyristor rectifier, the problems about the current harmonics remain, but a thyristor rectifier is able to function as an inverter i.e. it is possible to inject active power into the grid. Fig.3.70 visualizes a frequency converter containing a thyristor rectifier (two rectifier bridges in anti-parallel), a capacitor and a PWM inverter feeding an induction machine.

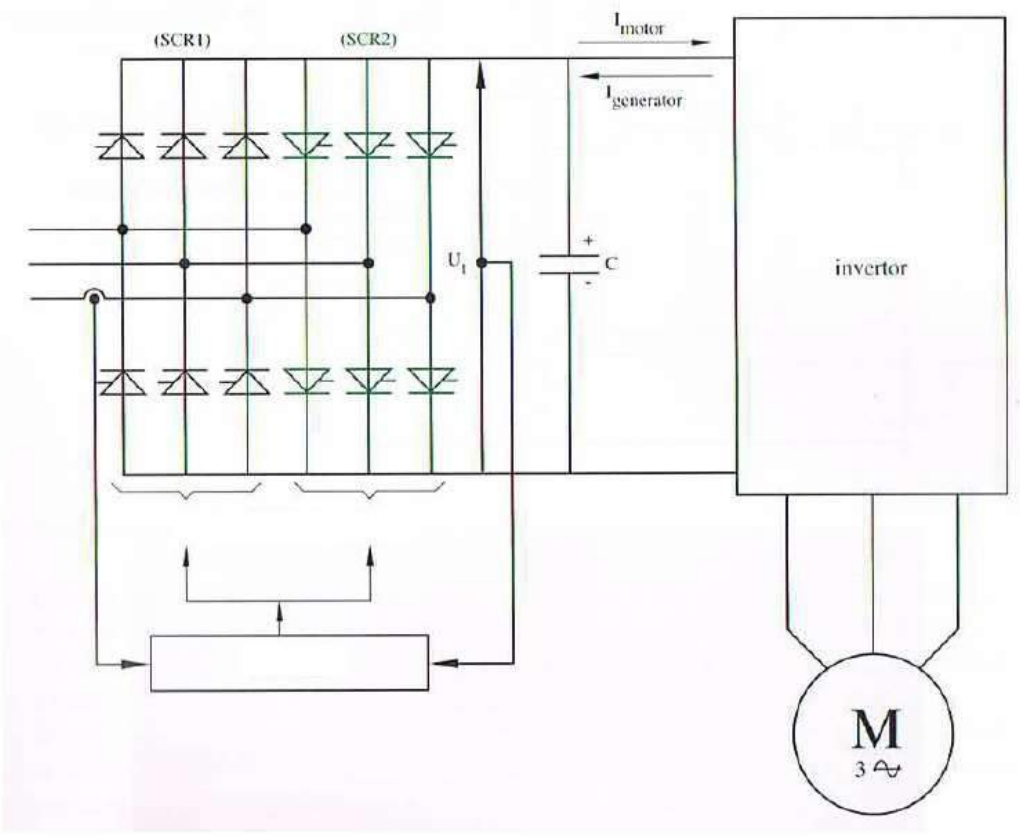


Fig. 3.70. Frequency converter with two thyristor bridges in anti-parallel (source: Pollefliet)

In case the induction machine is motoring, the left thyristor rectifier bridge SCR1 extracts active power from the grid and sends this power to the PWM inverter which feeds the induction motor. Thus the thyristor rectifier bridge SCR1 has a firing angle α smaller than $90°$ implying a positive voltage across the capacitor.

In case the induction machine is generating, the right thyristor rectifier bridge SCR2 sends active power to the grid which is coming from the induction generator and the PWM inverter. This right thyristor rectifier bridge SCR2 has a firing angle α larger than 90° implying a positive voltage across the capacitor since this right rectifier SCR2 is mounted upside down.

Active Front End

Instead of using two thyristor rectifier bridges mounted in anti-parallel, it is also possible to use an Active Front End (AFE). Such a three phase Active Front End is visualized in Fig. 3.71. Its internal working principle is similar to that of a single phase Active Front End which has already been discussed. The detailed discussion of the internal working principle of such a three phase Active Front End has been omitted here.

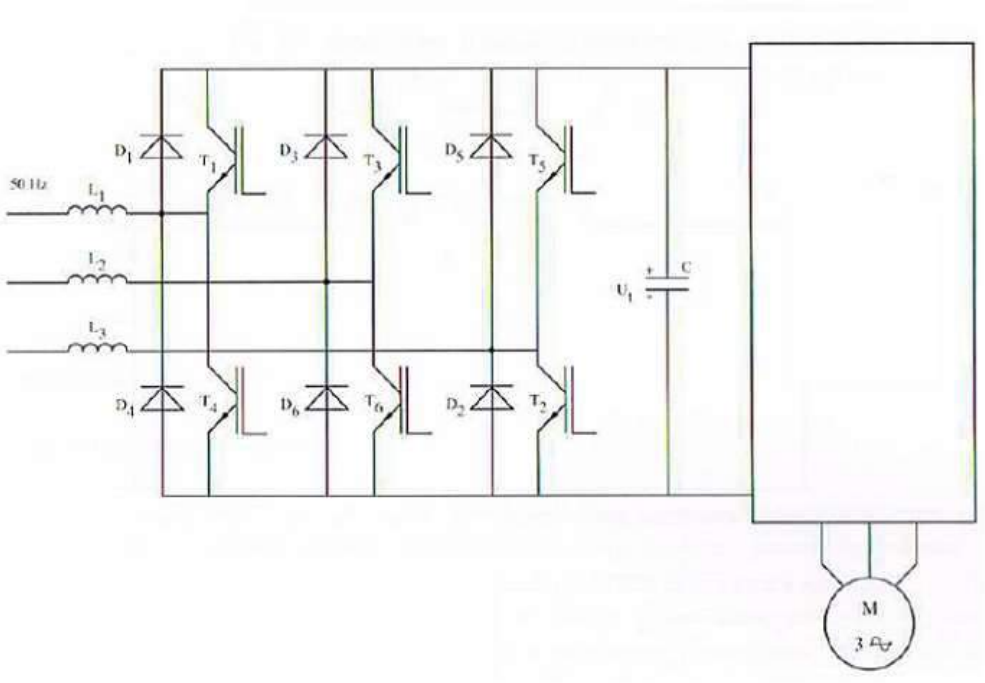


Fig. 3.71. Frequency converter containing an Active Front End (source: Pollefliet)

Using an Active Front End as visualized in Fig. 3.71 accounts for three important advantages.

- It is possible to obtain a grid current with a small THD (Total Harmonic Distortion), i.e. the shape of the grid current approximates the ideal sinusoidal shape.
- It is possible to consume active power from the grid when the induction machine is motoring. It is also possible to inject active power in the grid when the induction machine is generating.
- It is possible to adjust the reactive power consumed or generated by the Active Front End, i.e. the Active Front End can be used to improve the power factor of the grid.

Controlling active and reactive power

When considering the Active Front End of Fig. 3.71., the inductors L_1, L_2 and L_3 at grid side are very important and $L_1 = L_2 = L_3 = L$. Suppose the induction machine is generating implying the PWM inverter is sending power to the DC-link having a voltage U_t across the capacitor C. The Active Front End functions as an inverter by converting the DC-voltage U_t to a three phase AC-voltage represented by the complex number $\overline{U}_{inv}$. In steady state, this AC-voltage $\overline{U}_{inv}$ has the same frequency as the grid voltage $\overline{U}_{grid}$ but its amplitude and phase can be controlled with the Active Front End. Fig.3.72 visualizes this situation.

Fig. 3.72. Inductor behaviour at grid side

Using complex numbers, the inductor L has complex impedance $\overline{\overline{Z}} = j\omega L$ and the grid current equals to

$$\bar{I}_{in} = \frac{\overline{U}_{grid} - \overline{U}_{inv}}{j\omega L}. \quad , \tag{3-32}$$

Without loss of generality, assume $\overline{U}_{grid}$ has a phase 0 i.e. $\overline{U}_{grid} = U_{grid}$. The Active Front End is able to control the amplitude U_{inv} and the phase θ of $\overline{U}_{inv} = U_{inv}e^{j\theta}$. The power

$$\overline{S} = P + jQ = \overline{U}_{grid}\overline{I}_{in}^{*} = U_{grid}\left(\frac{U_{grid} - U_{inv}e^{j\theta}}{j\omega L}\right)^{*} \quad , \tag{3-33}$$

or equivalently

$$\overline{S} = P + jQ = -\frac{U_{grid}U_{inv}sin\theta}{\omega L} + jU_{grid}\frac{\left(U_{grid} - U_{inv}cos\theta\right)}{\omega L}. \quad , \tag{3-34}$$

is sent from the grid to the Active Front End. Notice this power $\overline{S}$ is the power of one single phase ($\overline{U}_{grid}$ and $\overline{U}_{inv}$ are phase voltages) implying the total three phase power is three times that large.

Reactive power

In case $\overline{U}_{inv}$ has the same phase as $\overline{U}_{grid} = U_{grid}$ i.e. $\theta = 0$, the grid current is reactive, i.e.

$$\bar{I}_{in} = \frac{U_{grid} - U_{inv}}{j\omega L} = j\,\frac{\left(U_{inv} - U_{grid}\right)}{\omega L}. \quad , \tag{3-35}$$

In case $\overline{U}_{inv}$ has the same phase as $\overline{U}_{grid}$ and $U_{inv} < U_{grid}$, the current $\bar{I}_{in}$ lags the grid voltage $\overline{U}_{grid}$ implying reactive power is consumed by the Active Front End. More precisely,

$$\overline{S} = P + jQ = jU_{grid}\frac{\left(U_{grid} - U_{inv}\right)}{\omega L} \quad , \tag{3-36}$$

i.e. the grid is supplying a $Q > 0$ to the Active Front End (due to one single phase).

In case $\overline{U}_{inv}$ has the same phase as $\overline{U}_{grid}$ and $U_{inv} > U_{grid}$, the current $\overline{I}_{in}$ leads the grid voltage $\overline{U}_{grid}$ implying reactive power is generated by the Active Front End and injected into the grid. More precisely, the grid is feeding $Q < 0$ to the Active Front End.

To summarize, by controlling the amplitude of $\overline{U}_{inv}$ the consumed or generated reactive power can be controlled.

Active power

By controlling the phase difference θ between $\overline{U}_{inv}$ and $\overline{U}_{grid}$, the consumed or injected active power can be controlled. In case $\overline{U}_{inv} = U_{inv}e^{j\theta}$ lags $\overline{U}_{grid}$, $\theta < 0$ implying

$$P = -\frac{U_{grid}U_{inv}sin\theta}{\omega L} > 0 \quad , \tag{3-37}$$

is supplied to the Active Front End by the grid.

In case $\overline{U}_{inv}$ leads $\overline{U}_{grid}$, $\theta > 0$ implying a $P < 0$ is supplied from the grid to the Active Front End, i.e. the Active Frond End injects active power into the grid.

By changing the phase difference θ, the active power can be controlled. This means the angle θ (and associated with it the active grid power P) must be adjusted to the power consumed or generated by the induction machine.

Practical realization of the Active Front End

When considering the Active Front End of Fig.3.71, the use of semiconductors with a gate-turn-off capability is indispensable. For instance an IGBT allows realizing valves which can be switched ON and OFF whenever required. This allows a commutation of the valves hundreds times in one single period (contrary to for instance a line-commutated thyristor which is switched ON and OFF only once in a single period). Using these semiconductors having this gate-turn-off capability allows

- to obtain a grid current which resembles a sinusoidal shape very well,
- to control the active power (as explained by adjusting the angle θ in the voltage $\overline{U}_{inv}$),
- to control the reactive power (as explained by adjusting U_{inv}).

The Active Front End of Fig.3.71 is also visualized in Fig.3.73 and it is important to have the appropriate DC-voltage V_D across the capacitor C_D. Using a feedback control loop, the DC link voltage V_D (named U_t in Fig. 3.71) is compared with a reference voltage V_{REF}. The error signal obtained by this comparison is used to control the gates of the IGBT's.

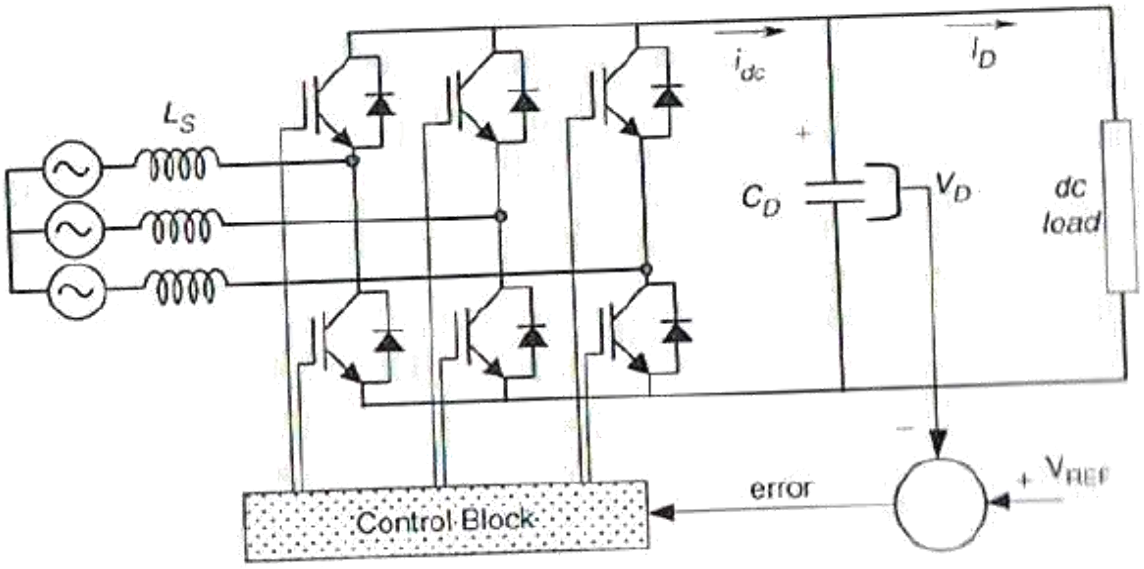


Fig. 3.73. Control of the Active Front End (source: Rashid)

Working principle

In the case of rectifier operation, the current I_D is positive and the DC load consumes power $P = V_D I_D$. Due to I_D, the capacitor is discharged when the current i_{dc} is too small. When V_D is decreasing, this means the AC supply must send more power to the capacitor C_D. The control block controls the gates of the IGBTs in order to increase the active current sent from the AC-side to the DC-side. More precisely, by making θ more negative the active power P extracted from the grid increases. This allows the DC-voltage V_D to recover.

In case the current i_{dc} is too large in comparison with I_D, the voltage V_D is increasing. The control block controls the gates of the IGBTs in order to decrease the active current sent from the AC-side to the DC-side. More precisely, by making θ less negative the active power P extracted from the grid decreases. This allows the DC-voltage V_D to decrease to its original appropriate value.

In case of inverter operation, the current I_D is negative and the capacitor C_D is charged when the current i_{dc} is not sufficiently negative. When V_D is increasing, this means the capacitor must send more power to the Active Front End. The control block controls the gates of the IGBT's in order to increase the current sent from the DC-side to the AC-side. More precisely by increasing $\theta > 0$, more active power is injected into the grid. This allows the DC-voltage V_D to decrease to its original appropriate value.

In case the current i_{dc} is too negative in comparison with I_D, the voltage V_D is decreasing. This means the capacitor must send less power to the Active Front End. The control block controls the gates of the IGBTs in order to decrease the current sent from the DC-side to the AC-side. More precisely by decreasing $\theta > 0$, less active power is injected into the grid. This allows the DC-voltage V_D to recover.

The PWM principle is used to obtain the switching pattern of the IGBTs. In case V_D is the voltage across the capacitor C_D, the switching of the IGBTs accounts for the PWM pattern

visualized in Fig. 3.74. (actually no sinusoidal shaped voltage is obtained but a PWM voltage which approximates the desired sinusoidal voltage represented by $\overline{U}_{inv}$ in Fig. 3.72.). Its fundamental wave is also visualized in Fig. 3.74 and this fundamental V_{MOD} corresponds with the voltage $\overline{U}_{inv}$ in Fig. 3.72.

By changing the amplitude of V_{MOD} (or equivalently U_{inv}) the reactive power exchange between the grid and the Active Front End can be controlled. By changing the phase of V_{MOD} the active power exchange between the grid and the Active Front End can be controlled. The voltage level of V_D is used to control the phase of V_{MOD} as already explained. Fig.3.75 shows how the PWM pattern changes in order to change the amplitude of V_{MOD}. Displacing the PWM pattern changes the phase shift i.e. changes θ.

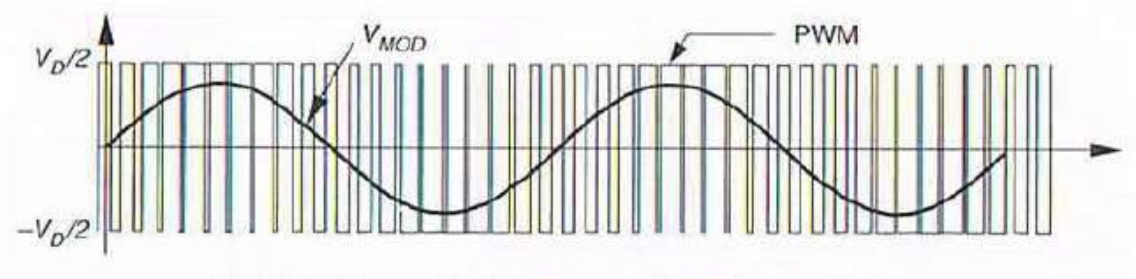


Fig. 3.74. A PWM pattern and its fundamental wave (source: Rashid)

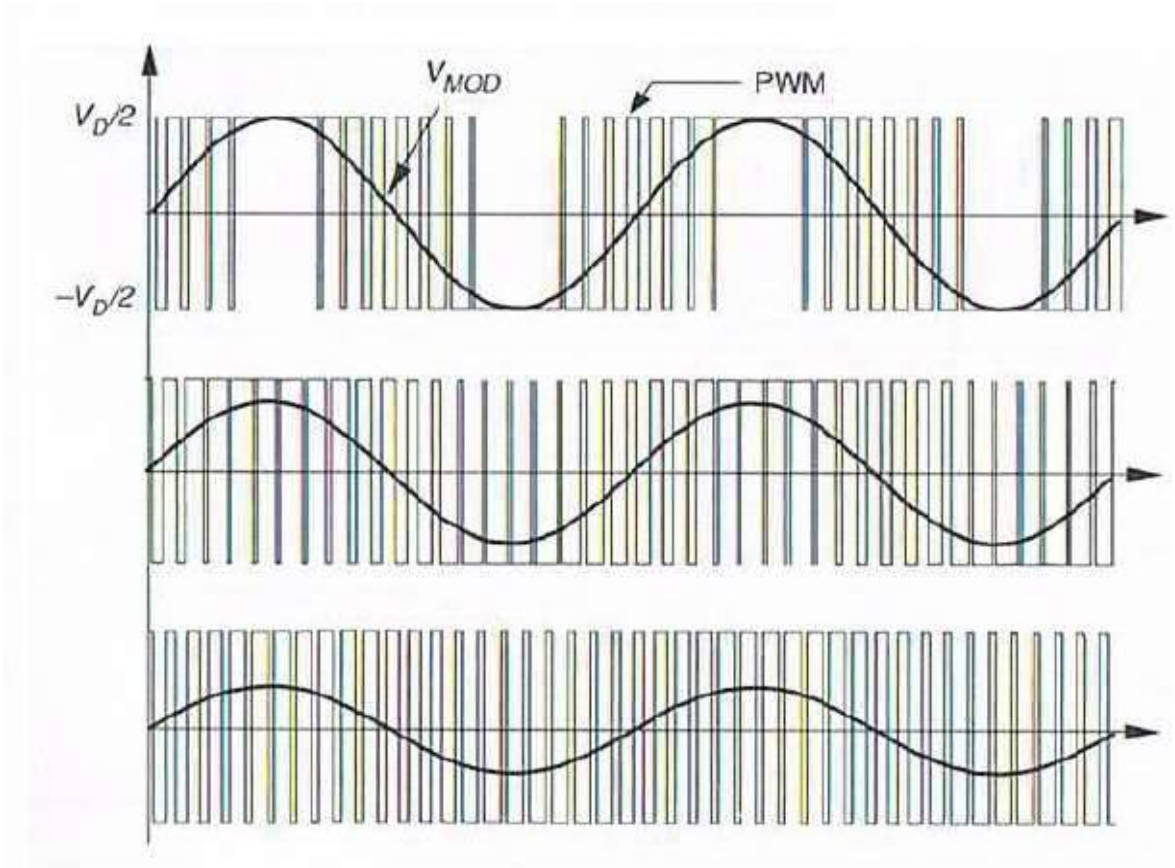


Fig. 3.75. Changing V_{MOD} using the PWM pattern (source: Rashid)

Notice the PWM waveforms visualized in Fig. 3.74 and Fig. 3.75 are the voltages obtained between the middle point of the DC voltage across capacitor C_D and the corresponding phase (the voltages take the values $+V_D/2$ and $-V_D/2$). Using the Kirchoff's voltage law, the line voltages are also known.

The three phases are numbered as 1, 2 and 3. The waveform between phase 1 and the middle point of the capacitor equals to V_{PWM}^{1}, the waveform between phase 2 and the middle point of the capacitor equals to V_{PWM}^{2} and the waveform between phase 3 and the middle point of the capacitor equals V_{PWM}^{3}. This implies line voltages

$$V_{PWM}^{12} = V_{PWM}^{1} - V_{PWM}^{2} \quad , \tag{3-38}$$

$$V_{PWM}^{23} = V_{PWM}^{2} - V_{PWM}^{3} \quad , \tag{3-39}$$

$$V_{PWM}^{31} = V_{PWM}^{3} - V_{PWM}^{1} \quad , \tag{3-40}$$

and phase voltages (N is the neutral of the grid)

$$V_{PWM}^{1N} = \frac{\left(V_{PWM}^{12} - V_{PWM}^{31}\right)}{3} \quad , \tag{3-41}$$

$$V_{PWM}^{2N} = \frac{\left(V_{PWM}^{23} - V_{PWM}^{12}\right)}{3} \quad , \tag{3-42}$$

$$V_{PWM}^{3N} = \frac{\left(V_{PWM}^{31} - V_{PWM}^{23}\right)}{3} \quad . \tag{3-43}$$

These are the phase voltages corresponding to those visualized in Fig. 3.72.

Four quadrant operation

By changing amplitude and phase of V_{MOD} (called $\overline{U}_{inv}$ in Fig. 3.72), actually a four quadrant operation becomes possible:

- rectifier working with a leading power factor (the Active Front End consumes active power P but generates reactive Q),
- rectifier working with a lagging power factor (the Active Front End consumes active power P and consumes reactive power Q),
- inverter working with a leading power factor (the Active Front End generates active power P and generates reactive power Q),
- inverter working with a lagging power factor (the Active Front End generates active power P and consumes reactive power Q).

Fig. 3.76.(a) visualizes the Active Front End containing its control loop. The grid voltage v ($\overline{U}_{grid}$ in Fig. 3.72.), the grid current I_S ($\overline{I}_{in}$ in Fig. 3.72.) and the inverter voltage V_{MOD} ($\overline{U}_{inv}$ in Fig. 3.72.) are also visualized. In case of a rectifier operation at unity power factor (Fig. 3.76.(b)), the current I_S has the same phase as the grid voltage v. This situation (see the vector diagram) is obtained in case V_{MOD} lags the grid voltage ($\delta = |\theta|$). When comparing Fig.

3.76.(b) with Fig. 3.76.(c), there is a phase shift of $180°$ between the grid currents implying a leading instead of a lagging voltage V_{MOD}.

In Fig. 3.76.(d), the current leads the grid voltage implying the grid consumes reactive power and the Active Front End generates this reactive power. Notice the amplitude difference between the grid voltage V and the voltage V_{MOD}. In Fig. 3.76.(e), the current lags the grid voltage implying the grid supplies reactive power consumed by the Active Front End.

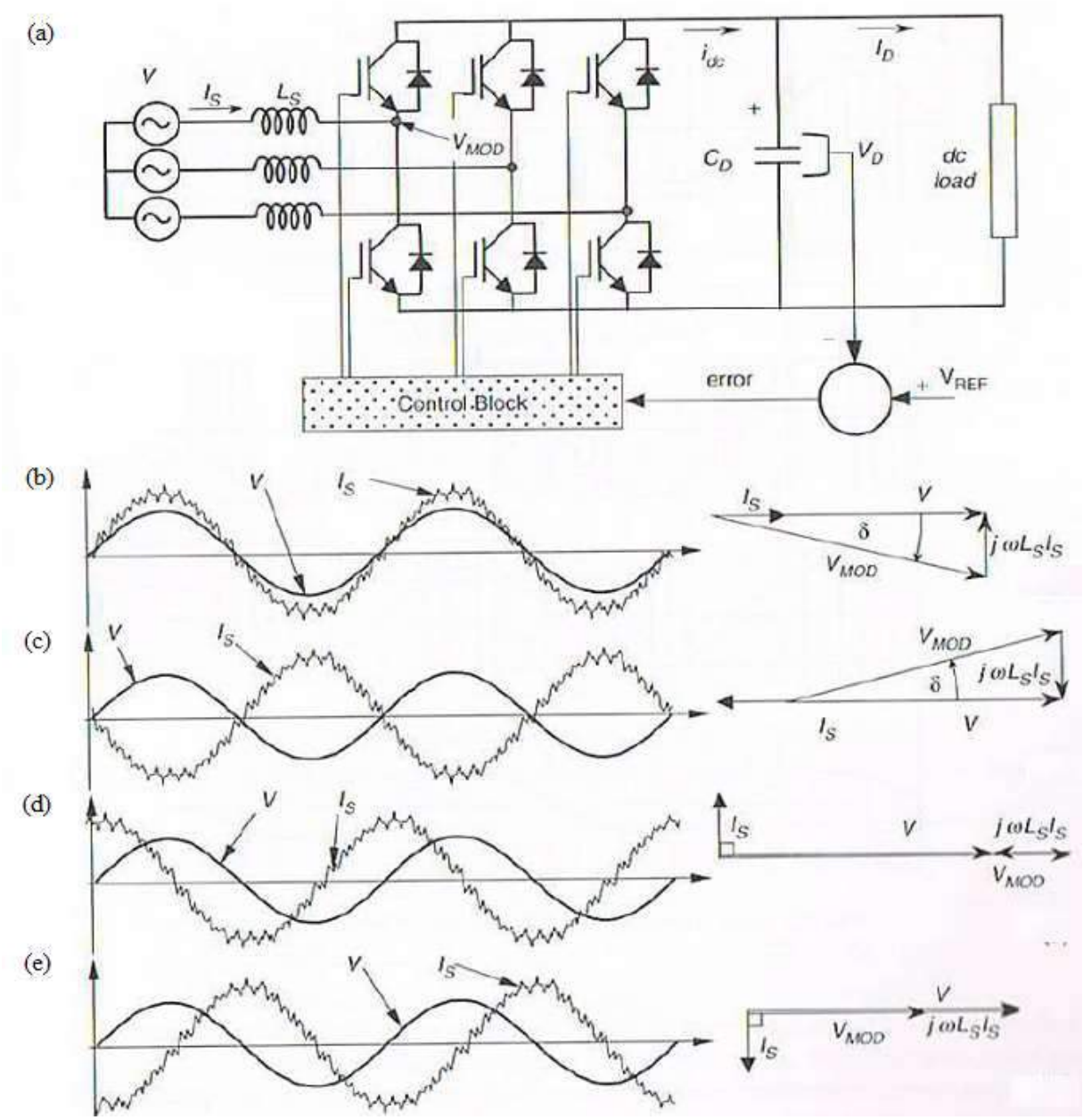


Fig. 3.76. Phasor diagrams (source: Rashid)

Practical waveforms

As visualized in Fig. 3.76., the grid voltages can be assumed to have sinusoidal shapes. Since the voltages V_{MOD} (or equivalently $\bar{U}_{inv}$) are PWM voltages, the grid currents I_S (or equivalently $\bar{I}_{in}$) do not have the ideal sinusoidal shape but due to the inductors the sinusoidal shape is approximated. Fig.3.77 not only visualizes I_S but the IGBT current i_{Tn} and the

flywheel diode current i_{Dp} (see also Fig. 3.78.) as well. When applying a gate voltage to have a conducting IGBT, the instantaneous value of the current increases. When the IGBT does not conduct, due to the inductance L_S (L_2 in Fig. 3.71.) a decreasing current is flowing through the flywheel diode.

Notice the changing duty cycle corresponds to the PWM approach. Due to this changing duty cycle, I_S is mainly increasing when the IGBT is conducting during a longer time period than the flywheel diode. In a similar way, I_S is mainly decreasing when the IGBT is conducting during a shorter time period than the flywheel diode.

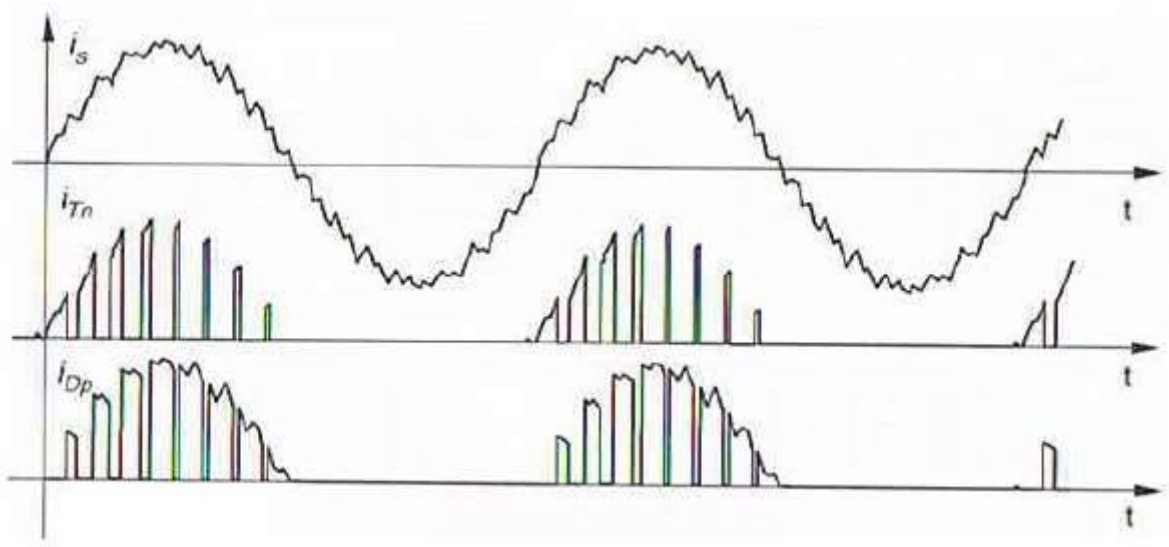


Fig. 3.77. Current waveforms (source: Rashid)

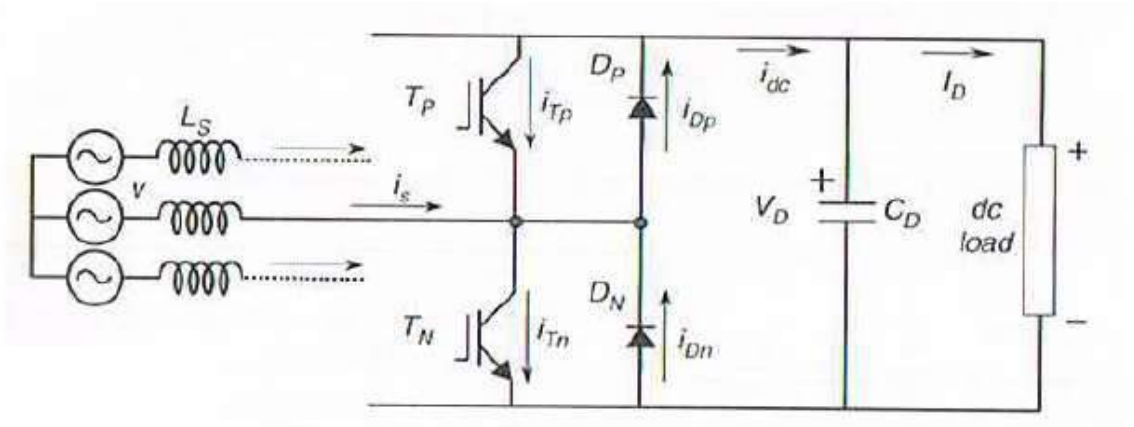


Fig. 3.78. Internal structure of the Active Front End (source: Rashid)

Control strategy

Current controlled PWM rectifier

The control strategy which uses V_D to control the gate pulses of the IGBTs is visualized in Fig. 3.73. A more detailed realization is visualized in Fig. 3.79. Also in Fig. 3.79, the capacitor voltage V_D is compared with a reference voltage V_{REF}. The error signal e is fed to a

controller G_C which can be a P-controller but it can also be a PI-controller or another controller type. The choice of this controller is important to have a stable control loop.

The output of the controller G_C is the amplitude I_{MAX} of the desired grid current (the current reference). Actually a sinusoidal grid current is needed having the grid frequency and a phase angle φ. This angle φ depends on the desired reactive power exchange in order to improve the power factor of the grid. By measuring the first phase voltage $V_M sin(\omega t)$, a frequency and phase reference is obtained. By taking the desired angle φ into account, $sin(\omega t + \varphi)$ and $sin(\omega t + \varphi - 120°)$ and $sin(\omega t + \varphi + 120°)$ are known. By multiplying these functions with I_{MAX}, the reference currents are obtained and they are compared with the actually measured grid currents (in case two currents are measured, the third one is also known since the sum of the three line currents equals zero).

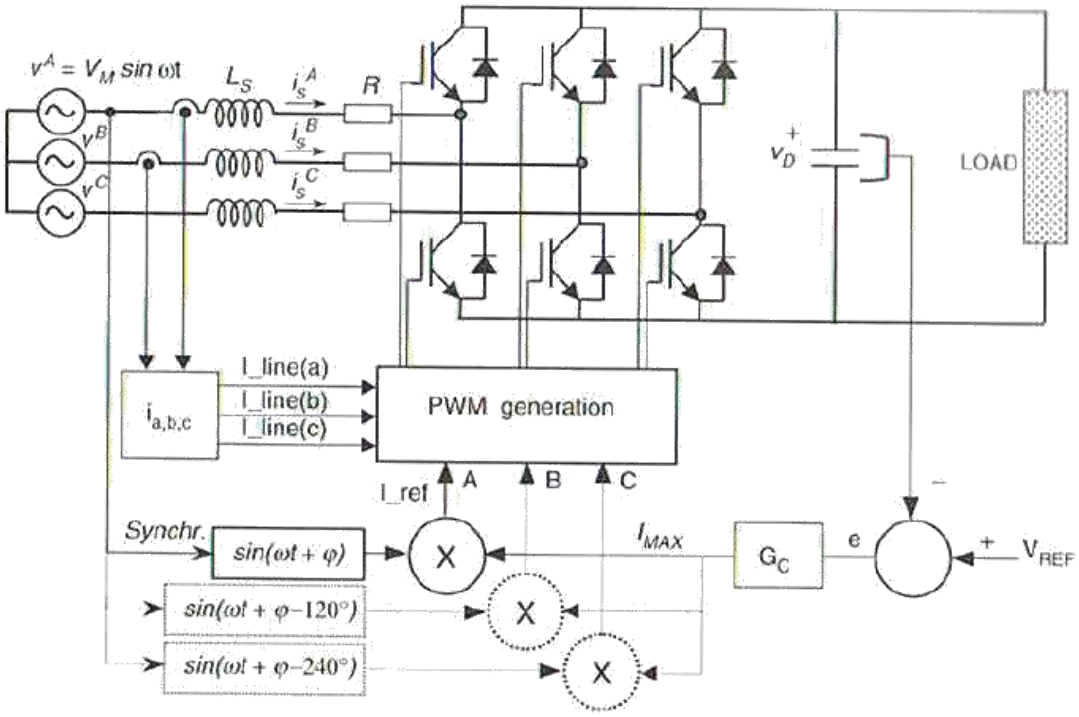


Fig. 3.79. Voltage source current controlled PWM rectifier (source: Rashid)

When comparing the actual grid currents with the reference grid currents to obtain the needed PWM pattern to control the IGBTs, different electronic approaches are possible. Fig. 3.80 visualizes one of these possibilities. The actual line current of the grid is compared with the desired line current (the reference current) giving an error signal. This error is processed through a PI gain stage before the comparison with a triangular carrier wave takes place (an appropriate choice of k_p and k_i is needed but this discussion is omitted here). This comparison allows control of the gates of the IGBTs.

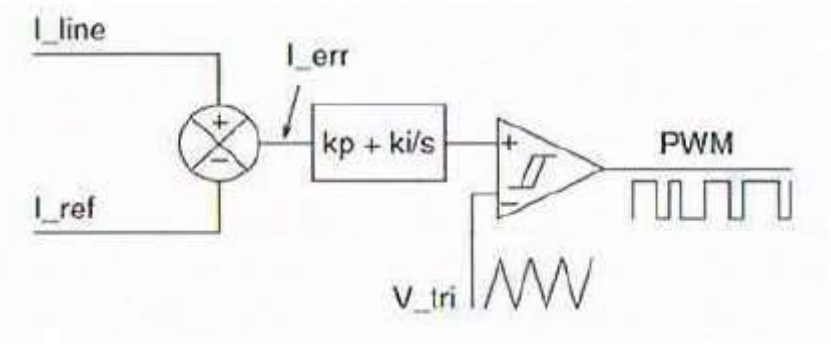


Fig. 3.80. Determination of the PWM signals to control the IGBT's (source: Rashid)

Voltage controlled PWM rectifier

Fig.3.80 visualizes a voltage controlled PWM rectifier which is an alternative for the current controlled PWM rectifier of Fig. 3.79. The phase voltage of the grid equals $v(t) = V_M sin(\omega t)$ and due to the resistance R and the inductance L_S, one obtains that :

$$v(t) = R\, i_S(t) + L_S \frac{d\, i_S(t)}{d\, t} + v_{MOD}(t) \quad , \tag{3-44}$$

where $i_S(t)$ is the grid current consumed by the Active Front End. In reality, the active power consumed (or generated) by the load is time-varying implying the amplitude $I_{max}(t)$ of the grid current is also time-varying. Similar with the situation discussed in Fig. 3.79, the phase angle φ is assumed to be constant. More precisely,

$$i_S(t) = I_{max}(t)\, sin(\omega t + \varphi) \quad , \tag{3-44}$$

which implies that:

$$\begin{aligned} V_M \sin(\omega t) &= R I_{\max}(t)\sin(\omega t+\varphi) + \omega L_S I_{\max}(t)\cos(\omega t+\varphi) + \\ &+ L_S \sin(\omega t+\varphi)\frac{dI_{\max}(t)}{dt} + v_{MOD}(t) \end{aligned} \quad . \tag{3-45}$$

By defining $X_S = \omega L_S$, one obtains in case $\varphi = 0$ that :

$$v_{MOD}(t) = \left(V_M - R I_{max}(t) - L_S \frac{d\, I_{max}(t)}{d\, t}\right) sin(\omega t) - X_S I_{max} cos(\omega t). \quad , \tag{3-46}$$

This expression gives the needed $v_{MOD}(t)$ as visualized in Fig. 3.81. Notice the block $-R - sL_S$ where the Laplace operator s accounts for taking the derivative of $I_{max}(t)$.

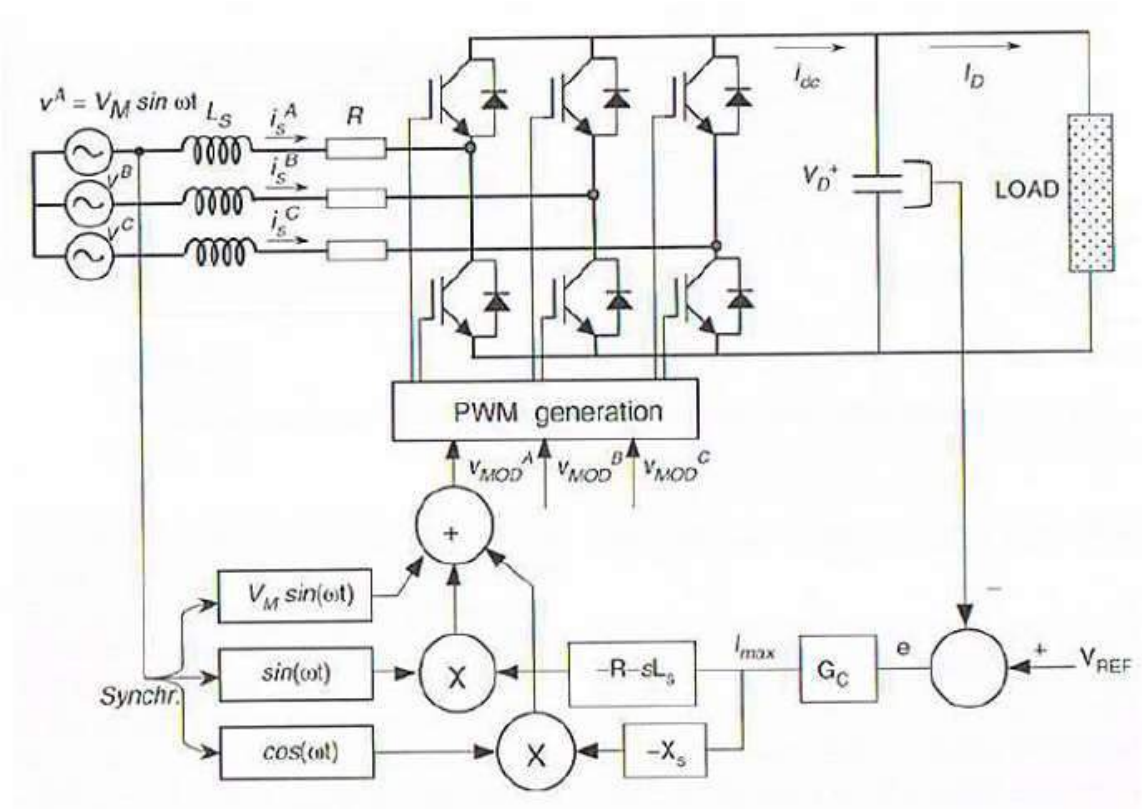


Fig. 3.81. Voltage source voltage controlled PWM rectifier

When comparing the configuration of Fig. 3.81 with the configuration of Fig. 3.79, the first one has the advantage when no current measurements are needed. It is sufficient to measure one single phase voltage. However, Fig.3.81 needs an accurate knowledge of the resistance R and the inductor L_S.

References

Pollefliet J., Elektronische vermogencontrole: elektronische motorcontrole, Academia Press, Gent, Belgium, 2011.

M.H. Rashid, Power Electronics Handbook, Elsevier – Academic Press, 2007.

4. Inverters

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4.1. Introduction

Inverters are the devices which are able to generate an AC waveform from a DC source. These devices have many applications and for instance driving an electrical motor is a classical application. These adjustable speed and position drives improve the efficiency of the motor system and allow a user friendly speed and position control. Inverters also convert the generated DC photovoltaic solar power into the useful AC grid voltage which allows injecting the power in the grid. An uninterruptible power supply (UPS) converts the DC power of a battery into an AC voltage in order to feed critical loads when a blackout occurs. Inverters are also used in active filters, voltage compensators, Static Var Compensators and Flexible AC Transmission Systems (FACTS).

In order to generate an AC sinusoidal waveform, one must be able to control the magnitude, the frequency and the phase. There are two important approaches to control the output of the inverter, i.e. the voltage-source inverters (VSI) and the current-source inverters (CSI). The VSI controls the output voltage waveform and the VSI is the most widely used inverter type. The VSI behaves like a voltage source and voltage sources are required by many industrial applications such as the adjustable speed and position drives. The CSI controls the output current waveform. These devices are more frequently used in medium-voltage industrial applications since they generate less harmonics. They are more expensive but they obtain high quality voltage waveforms which is necessary in a number of applications.

Irrespective of using the VSI or the CSI variant, the AC waveform is obtained by discrete instantaneous output values since power switches are used to construct this waveform. The waveform is obtained by fast switching of these power switches that leads to fast transitions in the waveform instead of the smooth sinusoidal waveform. The expected sinusoidal waveform is the fundamental of the obtained AC waveform. This property is required in order to obtain the appropriate modulation technique which controls the instants of time and the sequences used to switch the power switches on and off. The mostly used modulation techniques (i) are the carrier based technique known as the Pulse Width Modulation (PWM) technique, (ii) the Space-Vector (SV) technique and (iii) the Selective Harmonic Elimination (SHE) technique. These modulation techniques all have their advantages and disadvantages. One specific disadvantage of this discretely shaped AC waveform is that it affects and restricts the applications of the inverters.

For example when using VSI the load fed by the inverter should be inductive rather than capacitive. Indeed, the VSI generates an AC voltage waveform containing high $\frac{\partial V}{\partial t}$ values implying a capacitive load leads to large current spikes. An inductive load leads to a smooth current waveform. Indeed, a capacitor is a low impedance for high frequencies while an inductor is a sufficiently large impedance for the high frequencies in the spectrum due to the high $\frac{\partial V}{\partial t}$ values. When feeding a capacitive load from a VSI, a low pass filter (which is actually an inductor) is required to avoid high current peaks. This low pass filter should be located between the VSI output and the capacitive load.

When using a CSI, the load fed by the inverter output should be capacitive rather than inductive. Indeed, the CSI generates an AC current waveform containing high $\frac{\partial i}{\partial t}$ values implying an inductive load leads to large voltage spikes. A capacitive load leads to a smooth voltage waveform. Indeed, an inductor is a high impedance for high frequencies, while a capacitor is a sufficiently low impedance for the high frequencies in the spectrum due to the high values. When feeding an inductive load from a CSI, one needs a capacitor (which behaves as a low pass filter) to avoid high voltage spikes. This low pass filter should be located between the CSI output and the inductive load.

All circuits are explained using simulations made with Simulink [Matlab 2013] by using the library Simscape. In this library, a lot of the power electronic components are predefined and ready to be used in the electronic circuit.

In this chapter, all electronic components are assumed to be ideal.

4.2. Single-phase Voltage Source inverter

When considering the single-phase voltage source inverter, only two topologies are used: the half-bridge inverter and the full-bridge inverter. The power range of the single-phase voltage source inverter is low, but single-phase voltage source inverters are widely used.

4.2.1. Half-bridge VSI

Fig. 4.1 shows the half-bridge VSI containing a DC voltage source, two buffer capacitors, two power switches and two freewheel diodes. The DC voltage source can be any kind of DC voltage source like for instance batteries (used in automotive applications, UPS systems, photovoltaic power installations) or rectifiers rectifying the grid voltage (see chapter Rectifiers). The two capacitors are needed to provide a neutral point. This is obtained by using two capacitors having the same capacitance. This implies the voltages across these capacitors are the same and the total voltage provided by the DC voltage source divided in two. These capacitors also reduce the current harmonics on DC-side due do the inverter i.e. the voltage source mainly supplies a constant DC current. The two switches cannot be operated separately. Indeed, when both power switches are closed at the same time, a fatal short-circuit appears. The possible states of these power switches are listed in Table 4-4.

Table 4-4: Possible states of the power switches for a half-bridge single-phase VSI

State	State switches	Vo		Conducting components	
1	S1: on and S2: off	$u_{dc}/2$		S1	$i_o>0$
				D1	$i_o<0$
2	S1: off and S2: on	$-u_{dc}/2$		S2	$i_o>0$
				D2	$i_o<0$
3	S1: off and S2: off	$-u_{dc}/2$	$i_o>0$	D2	$i_o>0$
		$u_{dc}/2$	$i_o<0$	D1	$i_o<0$

State 1 and state 2 are the defined states, i.e. the value of the output voltage is known. To prevent a short-circuit or an undefined state, the power switches are controlled in a complementary way. When one switch is closed, the other one is open.

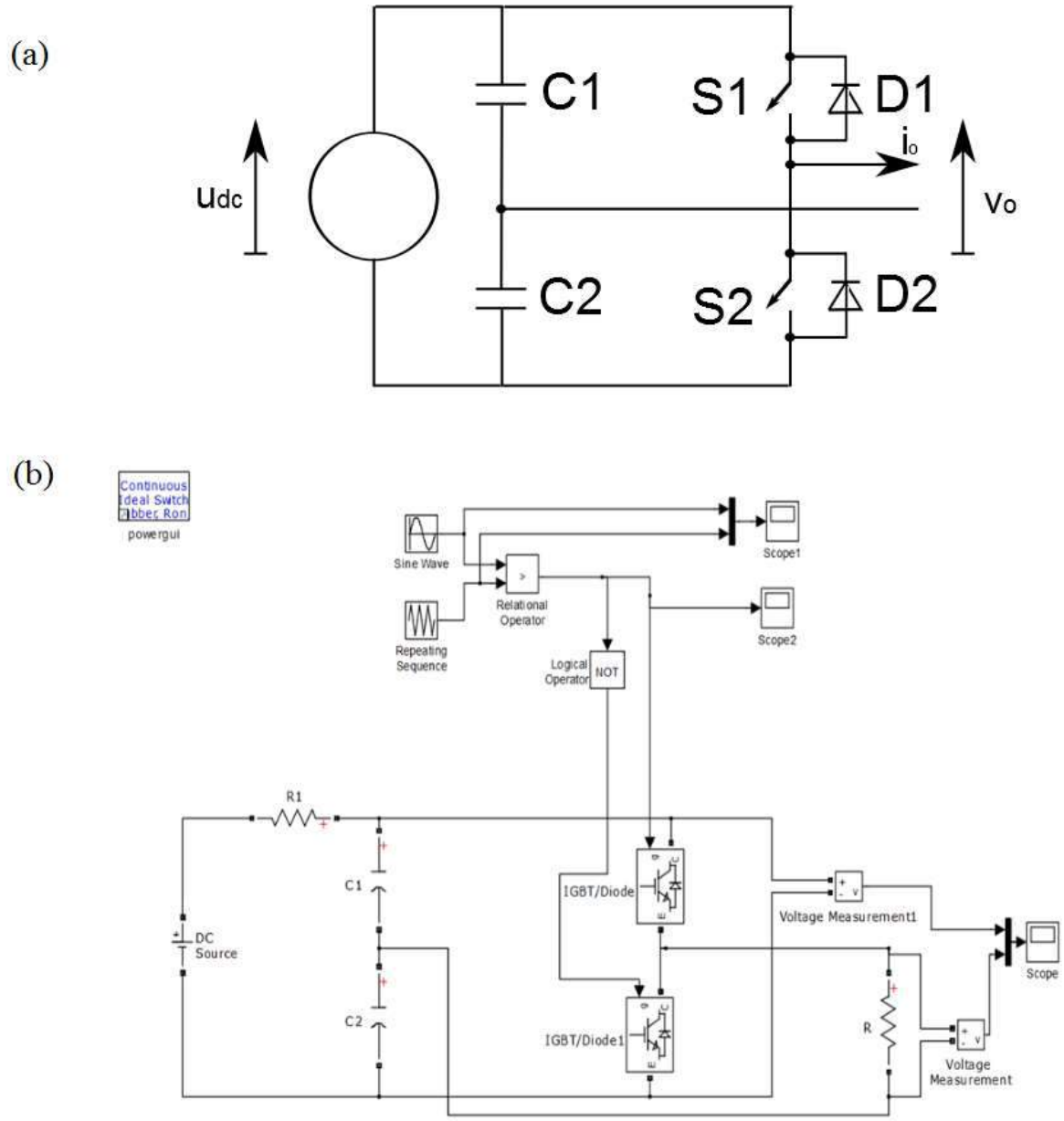


Fig. 4.1: The circuit of the single-phase half-bridge VSI with gate controller: electrical circuit (a) Simulink model (b)

As already mentioned, there are many control strategies to obtain the desired output voltage. The most commonly used strategy is the PWM strategy. Before explaining this PWM strategy, the simplest control strategy, i.e. the square wave modulating technique, is explained.

Square wave modulating technique

The square wave modulating technique is the simplest modulating technique. In the simulation, a constant DC voltage source of $\frac{3\sqrt{2}\sqrt{3}}{\pi}240 \approx 560\ V$ is used representing the rectified three phase grid voltage. During the first half period of the desired AC voltage

waveform, the first power switch is closed. During the second half period, the second power switch is closed. When the first power switch is closed, the second switch is open. When the second switch is closed, the first switch is open. This way, a square wave is obtained as shown in Fig. 4.2.

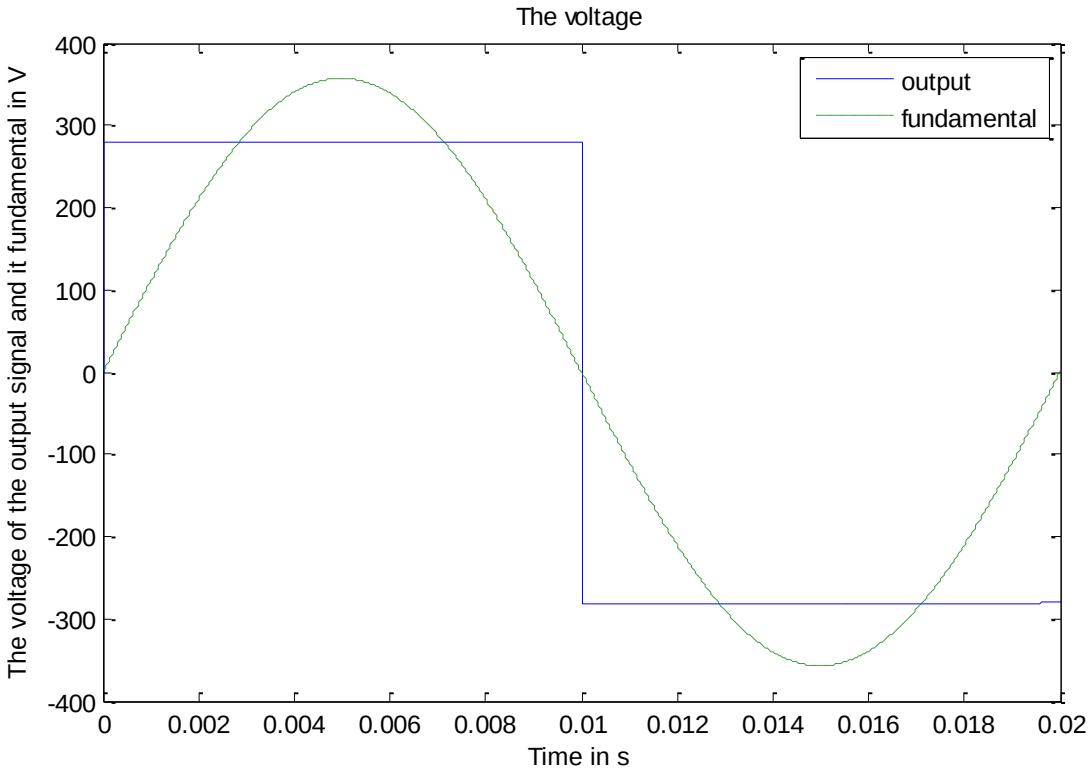


Fig. 4.2. Square-wave modulating technique applied in a single-phase half-bridge inverter

In Fig. 4.2 the output voltage is shown in blue and the fundamental of this voltage is shown in green. To obtain the fundamental of a signal, the Fourier analysis has to be applied. When calculating the Fourier series of the output voltage v_o using (notice we use a general x as variable since x can be time, angle, distance, etc.):

$$f(x) = \frac{a_0}{2} + \sum_{n=1}^{\infty}(a_n \cos(n\,x) + b_n \sin(n\,x)) \tag{4-1}$$

$$a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)\cos(n\,x)\,dx \quad \text{for all positive integer values } n \text{ (from 0 to } \infty) \tag{4-2}$$

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(x)\sin(n\,x)\,dx \quad \text{for all positive integer values } n \text{ (from 0 to } \infty) \tag{4-3}$$

the frequency spectrum is obtained, as visualized in Fig. 4.3.

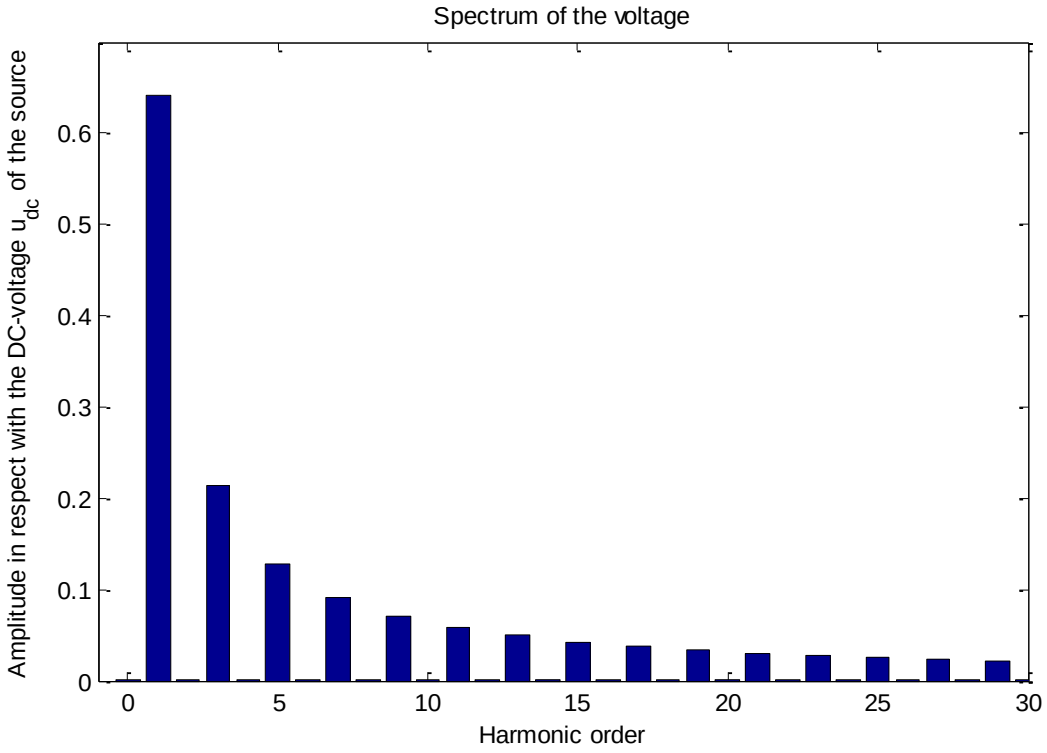


Fig. 4.3. The spectrum of the output voltage using the square-wave modulating technique applied in a single-phase half-bridge inverter

The spectrum of the output voltage is referred to the DC input voltage. The inverter aims to obtain an output voltage having a sufficiently large amplitude and a small THD_v (in the ideal case, the THD_V equals zero). As Fig. 4.3 shows, this low THD_V is not obtained. THD_V values of 48.34%, 48.34% and 43.52% are obtained by respectively using equations (4-4), (4-5) and (4-6).

$$THD_v = \frac{\sqrt{\sum_{i=2}^{\infty} V_i^2}}{V_1} \tag{4-4}$$

$$THD_v = \frac{\sqrt{V_{total}^2 - V_1^2}}{V_1} \tag{4-5}$$

$$THD_v = \frac{\sqrt{\sum_{i=2}^{\infty} V_i^2}}{\sqrt{\sum_{i=1}^{\infty} V_i^2}} \tag{4-6}$$

The Total Harmonic Distortion (THD) measures and quantifies the distortion of the voltage waveform in comparison with a sinusoidal waveform. The THD compares the global impact of the higher order harmonic components with the fundamental component. There are a number of definitions to determine the THD. Although equation (4-4) is frequently used, one must always be aware also (4-5) or (4-6) can be used.

The amplitude of the fundamental component equals $\frac{4}{\pi}\frac{1}{2}$=0.636 times the input DC voltage. This fundamental component is the largest amplitude which can be realized by using this single-phase half-bridge inverter circuit. This is an advantage, it is possible to obtain high

amplitude for the fundamental component and the control strategy is simple. The output voltage contains a lot of large higher order harmonics which is an important disadvantage. All harmonics are odd order harmonics. By applying the Fourier transform, the amplitude of a harmonic component is inversely proportional with the order. This leads to a high THD. Moreover, the frequency components are also close to the fundamental frequency implying it is difficult to filter out these higher order harmonics. Another disadvantage is the fact that it is not possible to change the amplitude of the output voltage (unless the voltage of the DC source is changed).

PWM modulating technique

In order to overcome the main disadvantage of the square-wave modulating technique, Pulse Width Modulation was introduced. The idea behind this modulating technique is visualized in Fig. 4.4. Instead making an ideal sine-form, it is simpler to make discrete sine as shown in Fig. 4.4(a). The difference between column 1 and 2 is the time step used when making the discrete sine (in column 2 a smaller time step is used). The smaller the time step, the better this discrete sine function approximates an ideal sine. When using a VSI, it is not always possible to change the voltage value of the DC voltage source (when using a diode rectifier). Even with a constant DC voltage source, it is possible to obtain the same main voltage by applying in one period, time of the maximum voltage and time of the minimum voltage.

$$U_{dis}(t) = \frac{\frac{U_{dc}}{2}T_{on} + \frac{-U_{dc}}{2}T_{off}}{T} \quad for\ t = [0 + (i-1)T : i\,T - 1\,]i = \mathbb{Z} \tag{4-7}$$

$$U_{dis}(t) = \frac{U_{dc}}{2}D(t) + \frac{-U_{dc}}{2}\big(1 - D(t)\big) \tag{4-8}$$

$$for\ D = [0{:}1]\ and\ t = [0 + (i-1)T : i\,T - 1\,]i = \mathbb{Z}$$

Here, T_{on} represents the time step that the power switch S1 is closed and T_{off} represents the time step that the power switch S2 is closed. Notice that the time step T equals the sum of T_{on} and T_{off}. This leads to the duty cycle D which is defined by (4-9).

$$D(t) = \frac{T_{on}(t)}{T}\ for\ t = [0 + (i-1)T : i\,T - 1\,]i = \mathbb{Z} \tag{4-9}$$

For every time step T, the duty cycle has to be found as shown in Fig. 4.4(b). By comparing the instantaneous value of a triangle waveform with the desired sinusoidal waveform, T_{on} and T_{off} are known. As visualized in Fig. 4.4.(c), the output voltage has to be high when the desired output voltage is higher than the triangle waveform or carrier wave implying the power switch 1 must be closed (which determines T_{on}). When the desired output voltage is lower than the triangle waveform or carrier wave, the power switch 2 must be closed (which determines T_{off}). The duty cycle is determined by T_{on} and T_{off}.

In case a smaller time step T of equivalently higher switching frequency is used, the PWM voltage provides a better approximation of the ideal desired sinusoidal waveform. The spectrums of the obtained PWM signals contain the frequency of the carrier wave as shown in Fig. 4.4.(d). In Fig. 4.4(d1), the switching frequency is 10 times higher than the frequency of the desired fundamental waveform. In Fig. 4.4(d2), the switching frequency is 20 times higher

than the frequency of the desired fundamental waveform. The harmonic components occurring in the spectrums of the PWM-signals have a higher order when the switching frequency is higher. These high frequencies are an advantage since it is simpler to filter out these higher frequencies.

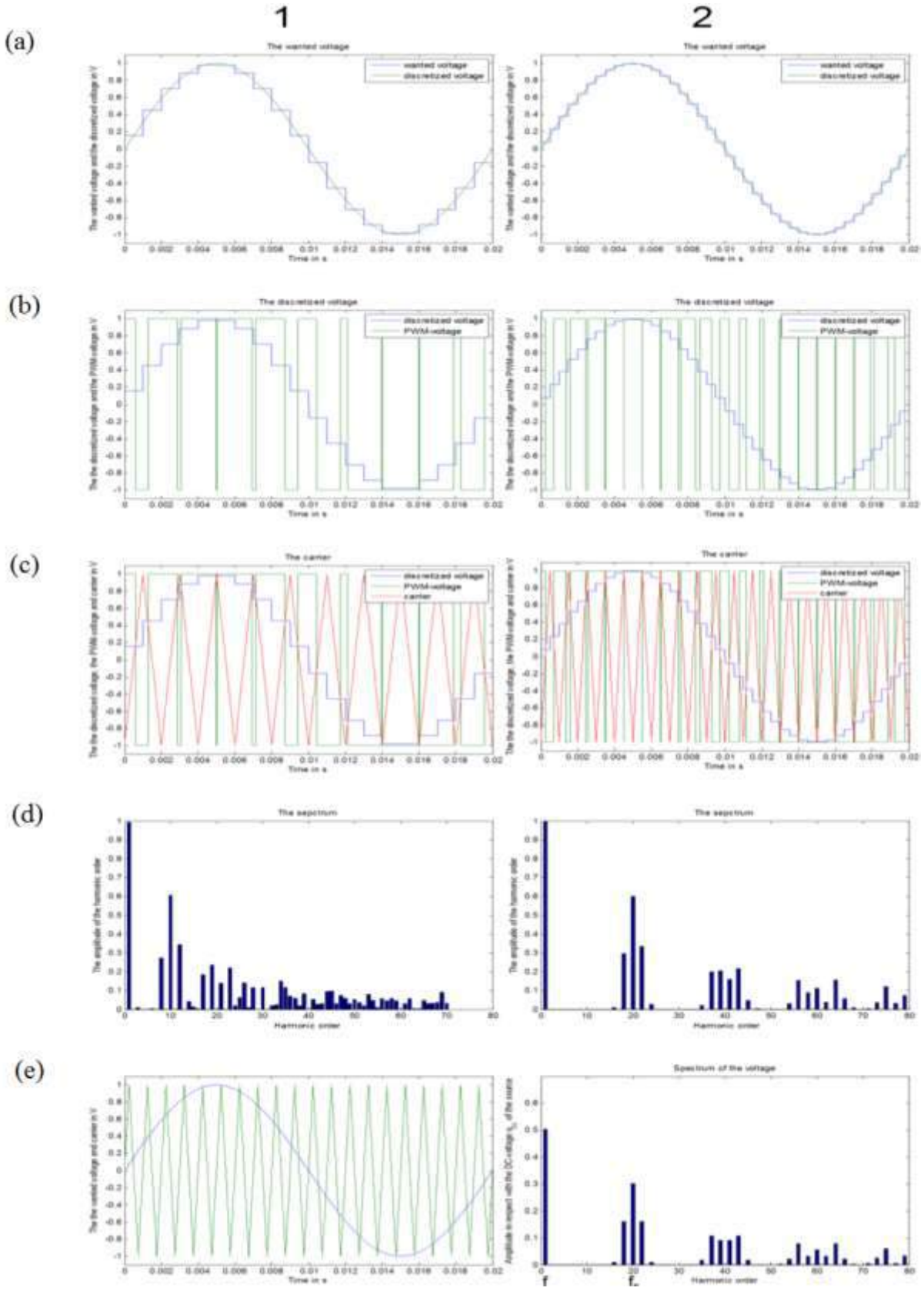


Fig. 4.4 PWM modulating technique

Instead of using this discrete signal, one will use a real sinusoidal waveform in combination with a carrier wave, as shown in Fig. 4.4.(e1). This real sinusoidal waveform is easier to generate and when considering the spectrum in Fig. 4.4.(e2), this spectrum having the same switching frequency as Fig. 4.4.(d2) is smoother and contains more symmetry than the spectrum in Fig. 4.4.(d2).

Before studying the frequency spectrum, first consider Fig. 4.4.(e1). In Fig. 4.4, all the voltages have a value between -1V and 1V. This voltage level is not crucial, but it is essential the control voltage (the sinusoidal waveform) which is compared with the carrier wave has a lower amplitude than the real PWM signal. The real PWM signal switches between $\frac{u_{dc}}{2}$ and $\frac{-u_{dc}}{2}$ when considering the half-bridge inverter. These real PWM signal voltages are obtained by power electronic devices and are too high to be used in the control electronics. By using these low control voltages, the real output voltage can be controlled.

A number of parameters have to be defined. The first parameter is the amplitude-modulation ratio m_a (4-10), which equals to the ratio of the amplitudes of the control signal and the carrier wave.

$$\boldsymbol{m_a = \frac{\widehat{v_c}}{\widehat{v_\Delta}}} \tag{4-10}$$

The frequency-modulation ratio m_f (4-11) equals to the ratio of the frequencies of the carrier wave and the control signal.

$$\boldsymbol{m_f = \frac{f_\Delta}{f_c}} \tag{4-11}$$

Using $D(t) = \frac{m_a\, sin(\omega t)+1}{2}$ in equation (4-8) leads to equation (4-12)

$$\boldsymbol{v_{o1} = \frac{u_{dc}}{2} m_a\, sin(\omega t)\ for\ m_a \leq 1} \tag{4-12}$$

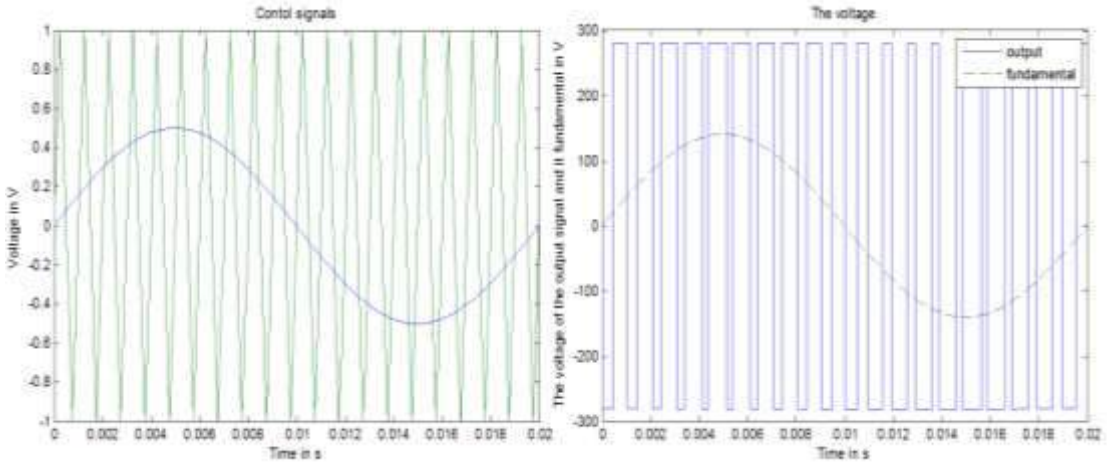


Fig. 4.5. Control signals and PWM signal with fundamental when using an amplitude-modulation ratio m_a of 0.5

The amplitude of the fundamental wave in the output voltage is proportional to the amplitude-modulation ratio m_a. The proportional behavior is only valid when m_a is smaller or equal to one. When the amplitude-modulation ratio is higher than one, overmodulation occurs

which will be discussed later. When the amplitude-modulation ratio is lower than one, the PWM signal still switches between $\frac{u_{dc}}{2}$ and $\frac{-u_{dc}}{2}$ for the half-bridge inverter. Since the amplitude of the control signal is lower than the amplitude of the carrier wave, the amplitude of the fundamental of the PWM output voltage is lower than $\frac{u_{dc}}{2}$ as shown in Fig. 4.5.

When considering the harmonics in Fig. 4.4. (e1), the harmonic components depend on the switching frequency. Using Fourier analysis, the harmonic orders which appear in the spectrum in the case of sinusoidal PWM (the PWM technique is used to modulate a sinoidal waveform) are described by (4-13) $\boldsymbol{h = lm_f \pm k}$:

$$\boldsymbol{h = lm_f \pm k} \tag{4-13}$$

When considering equation (4-13), k has an odd value when l is even and k has an even value when l is odd. When mf is an even number as in Fig. 4.4, the harmonic orders can be even and odd (for mf=20 the harmonic order is: h=20, 18 and 22, 16 and 24, 39 and 41, 37 and 43, 35 and 45, ….). When mf is an odd number, this only leads to odd harmonics (for mf=19 the harmonic order is h=19, 17 and 21, 15 and 24, 37 and 39, 35 and 41). Odd ordered harmonics are preferred above even ordered harmonics because they lead to symmetrical voltage signals. Even ordered harmonics lead to asymmetric voltage signals. These asymmetric voltage signals require better electrical insulation properties and accounts for a higher stress on the components. [G.T. Heydt, Y. Liu, "Second harmonic components in power system voltages and currents", IEEE Transactions on Power Delivery, Vol. 20, No. 1, January 2006, pp. 521-523.]

Until now, m_f was assumed to be an integer value. This property is not essential, but it provides a number of advantages. When the frequency modulation ratio is an integer value, synchronous PWM is obtained. This means the carrier wave contains m_f periods in one single period of the control signal. This leads to the harmonic orders obtained with equation (4-13), as shown in Fig. 4.6(a). When the frequency modulation ratio m_f is not an integer value, asynchronous PWM is obtained. Asynchronous PWM has the advantage that the switching frequency f_s is kept constant when changing the frequency of the output voltage. This property is not obtained in case of synchronous PWM where $m_f = \frac{f_s}{f} = cst$. The disadvantage of asynchronous PWM is the introduction of subharmonics and interharmonics as shown in Fig. 4.6(b).

Subharmonics are harmonic components which have a lower frequency than the fundamental component giving an order lower than one. These subharmonics will also lead to interharmonics increasing the THD of this output voltage. The increase of the THD is not the main problem. When comparing the spectrum when using synchronous PWM (Fig. 4.6.(a)) and the spectrum when using asynchronous PWM (Fig. 4.6.(b)), it is easier to design a filter for synchronous PWM than for asynchronous PWM. When considering synchronous PWM, the frequency gap between the fundamental wave and the lowest high order harmonic component is larger that makes the construction of an appropriate low pass filter easier. Additionally, in the case of asynchronous PWM subharmonics occur and a low pass filter is not able to filter out these subharmonics without eliminating the fundamental frequency. A band pass filter is needed to eliminate the subharmonics, the interharmonics and the high

order harmonics. When these subharmonics are not eliminated high currents will occur in AC motors. Indeed, due to the frequencies close to 0 Hz very high currents will flow in the inductive coils of AC motors. Due to this fact, asynchronous PWM is never used in variable speed drives.

In general, the use of synchronous PWM is often preferred but in some situations asynchronous PWM is allowed. Since the switching losses increase and since the importance of the subharmonic components decrease with increasing switching frequency, a rule of thumb claims that asynchronous PWM is allowed when m_f>21. This leads to a spectrum as shown in Fig. 4.6.(c), which shows the impact of the subharmonics is very small. Since f_s is kept constant, it is simpler to realize the PWM technique.

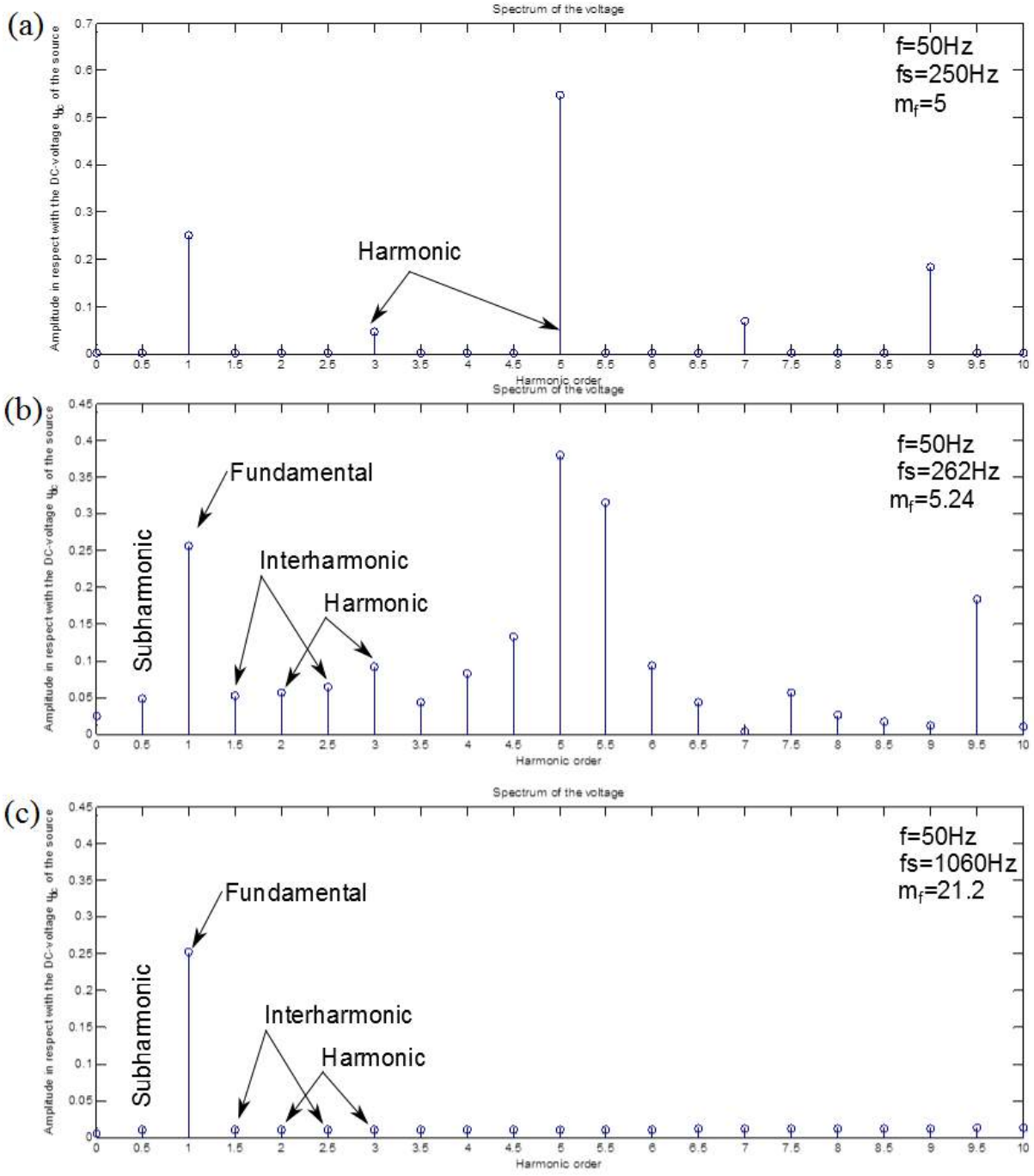


Fig. 4.6. Spectrum of synchronous PWM (a), asynchronous PWM m_f>21 (b), asynchronous PWM m_f<21 (c), with the same m_a of 0.5

When using synchronous PWM, the switching frequency is varying in a frequency range due to the changes in the desired frequency of the fundamental wave. Due to the changes in the switching frequency, it is more difficult to eliminate this switching frequency using a filter. A simple example illustrates the problem. Consider a frequency-modulation ratio m_f which equals 19 and the fundamental wave has a frequency ranging from 1Hz to 100Hz. Table 4-5 gives the expected switching frequencies. It is highly complicated to make one single filter to eliminate the switching frequency in the output voltage. When using a low pass filter which eliminates frequencies higher than 19 Hz, the switching frequency is eliminated. However, this filter would also eliminate the fundamental component when this frequency is higher than 19 Hz.

Table 4-5: Simple example for synchronous PWM with mf=19 or 201 and f=[1 : 100]

f	m_f	f_s	m_f	f_s
1 Hz	19	19 Hz	201	201 Hz
100Hz	19	1900 Hz	201	20100 Hz

To prevent the elimination of the fundamental wave, one could use a filter which only eliminates the frequencies higher than 100 Hz. However, in this situation the carrier remains when f is lower than 5 Hz (in case m_f = 19). Another approach can be the use of a much higher m_f value of for example 201 implying that even at low frequencies f, the carrier frequency is larger than 100Hz. When considering the frequency range of the carrier frequencies in case m_f=201, the switching frequencies obtain a large part of the audible frequency range which is irritating to hear. Moreover, in case of a high m_f value the switching losses become too high.

The solution to overcome these problems is applying the gearing technique. When applying this gearing technique, the frequency modulation ratio is high for low frequencies f. This implies the frequency components in the spectrum are higher than the highest obtainable frequency f. As shown in Fig. 4.7., the frequency modulation ratio is kept constant in a well-chosen frequency range similar with synchronous PWM. When the frequency f exceeds a threshold value the frequency modulation ratio decreases to the next odd integer. The threshold frequency is the frequency where the obtained switching frequency equals the switching frequency obtains with the highest use frequency-modulation ratio and lowest used frequency f. This is visualized in Fig. 4.7.

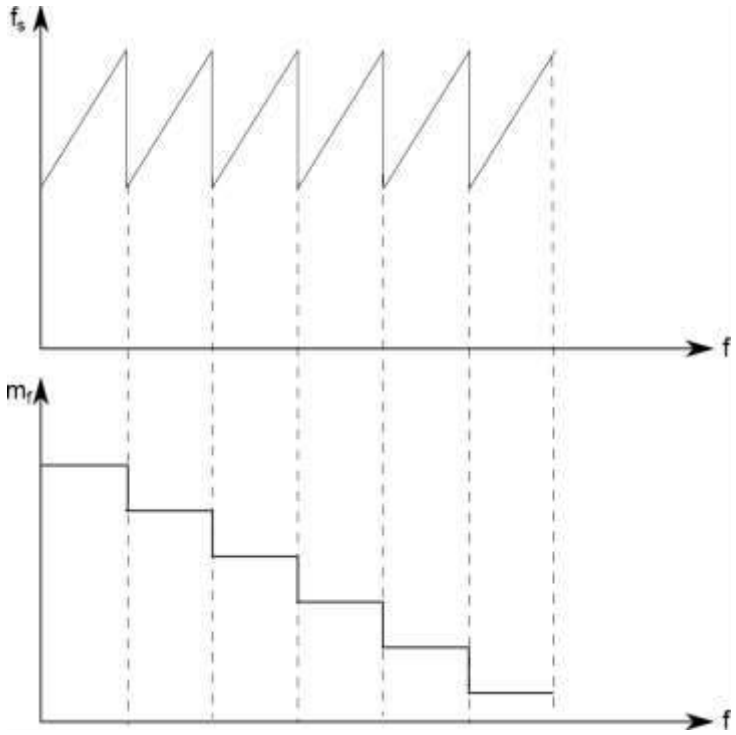
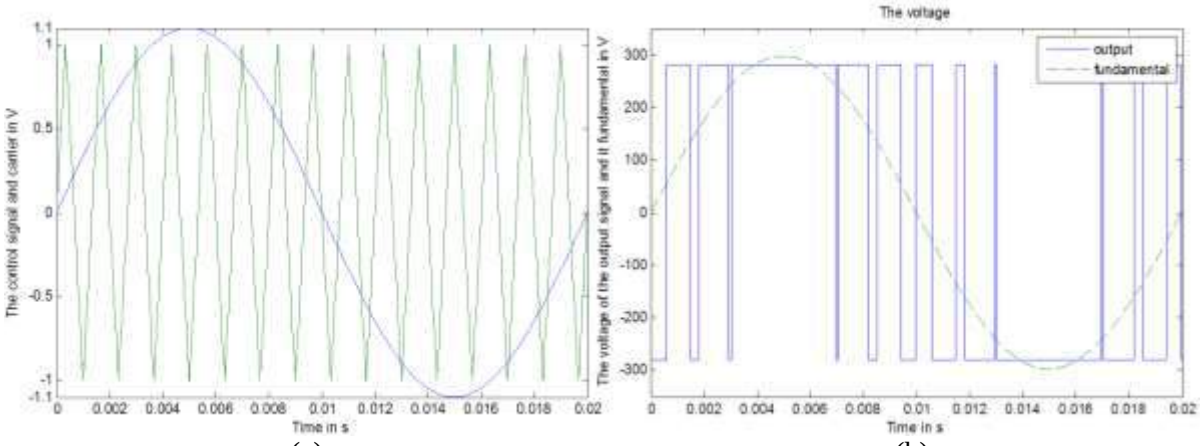


Fig. 4.7. The gear technique

When the amplitude modulation ratio m_a is larger than one, overmodulation occurs. When the amplitude modulation ratio m_a is larger than one, the amplitude of the control signal is higher than the amplitude of the carrier wave as shown in Fig. 4.8.(a).

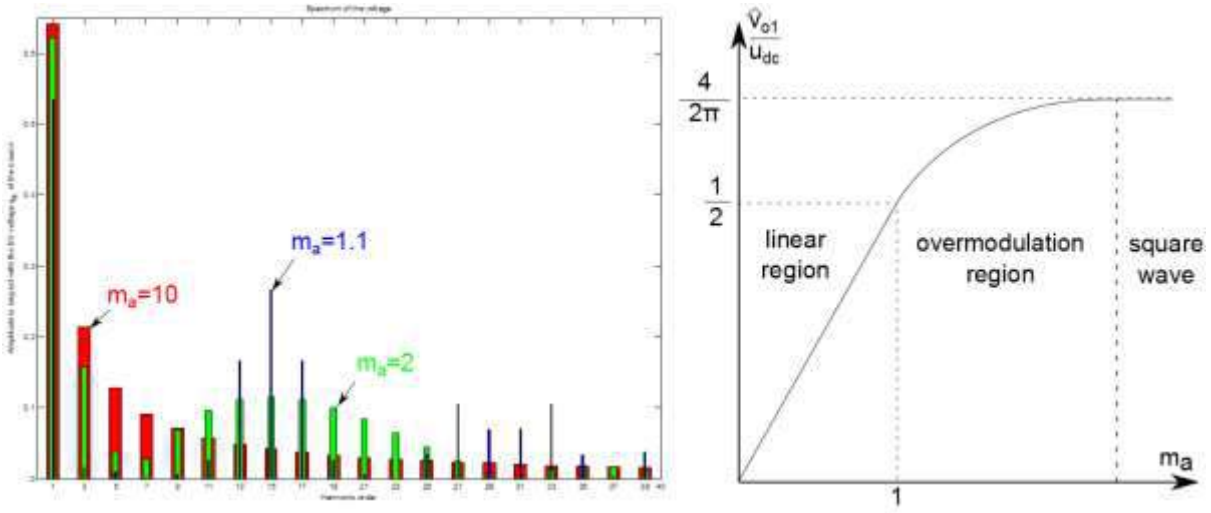


(a) (b)

Fig. 4.8. The control signal and carrier when overmodulation (m_a=1.1) occurs (a) PWM signal and its fundamental (b)

When the instantaneaous value of the control signal is higher than the instantaneous value of the carrier, then the power switch S1 is closed. When the instantaneous value of the control signal is lower than the instantaneous value of the carrier wave, the power switch S2 is closed. Due to the m_a value larger than one, the PWM strategy does not work anymore. This means equation (4-12) is not valid implying there is no linear relationship between the amplitude modulation ratio and the amplitude of the fundamental wave. The amplitude of the fundamental wave still increases when m_a increases, as shown in Fig. 4.8.(b). However, due to overmodulation low order harmonics (like the third order, the fifth order, ..) occur (Fig. 4.9.(a)). When the amplitude modulation ratio increases, the amplitude of the fundamental

wave will approach the maximum amplitude of $\frac{4}{\pi}\frac{u_{dc}}{2}$, but also the amplitudes of the lower order harmonics will increase. When m_a is sufficiently high, the PWM-signal becomes a square-wave containing the well-known harmonic contents.



(a) (b)

Fig. 4.9. Spectrum when using overmodulation (a) Different regions using sinusoidal PWM (b)

Selective Harmonic Elimination

The technique of Selective Harmonic Elimination, is a technique based on a combination of PWM and square wave modulation. This technique aims to control the output voltage while eliminating some harmonics (for instance the even harmonics in combination with the third order harmonic, the fifth order harmonic,….). To eliminate the even order harmonics, the output voltage needs a symmetric positive and negative alternation in combination with a quarter-wave symmetry.

Actually, the SHE technique uses the square wave modulation technique with some additional degrees of freedom. Every additional inverting point (the instant of time where the output voltage changes from $u_{DC}/2$ to $–U_{DC}/2$ of from $–u_{DC}/2$ to $u_{DC}/2$) to the square wave in one half period gives such an additional degree of freedom. The most commonly used Selective Harmonic Elimination technique uses three degrees of freedom. More precisely, by realizing three inverting points in a half period it is possible to eliminate two harmonics of the spectrum. These inverting points make indentations in the square wave leading to the elimination of well-chosen harmonic components.

It is important to note that the amplitude of the fundamental wave can be controlled. However, this amplitude will always be lower than that of the fundamental wave in case of square wave modulation. By using the SHE technique instead of overmodulation, the magnitudes of the higher order harmonics become lower. The mathematics needed to calculate the inverting point is not considered here.

4.2.2. Single-phase full-bridge VSI

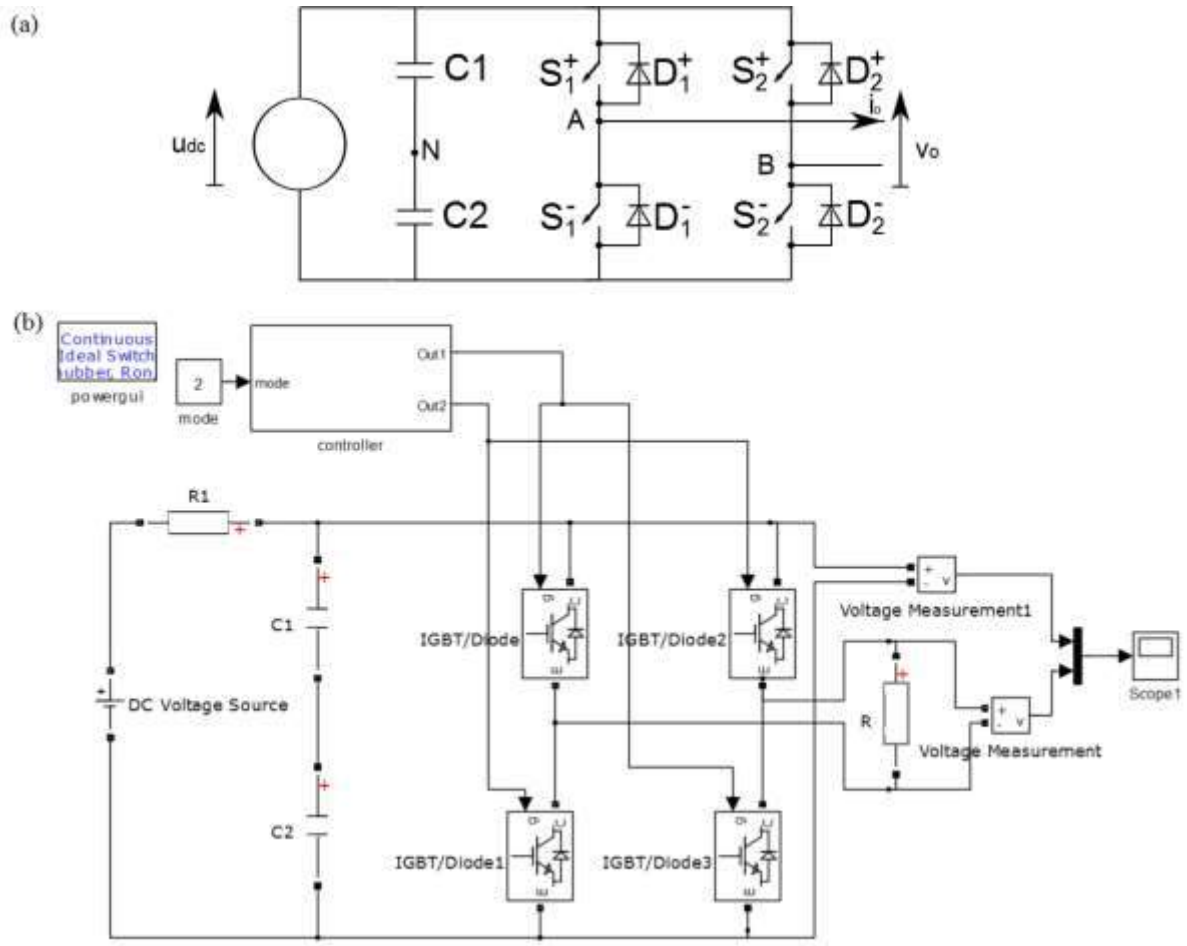


Fig. 4.10. The circuit of the single-phase full-bridge VSI with gate controllers: electrical circuit (a) Simulink model bipolar PWM (b)

The full-bridge VSI, shown in Fig. 4.10., contains two capacitors and two legs. Each leg contains two power switches and two flywheel diodes. The first leg has the power switches S_1^+ and S_1^- and the second leg has the power switches S_2^+ and S_2^-. Similar with the half-bridge VSI, in each leg the second power switch (S_1^- or S_2^-) gets the inverted signal on the gate of the first power switch (S_1^+ or S_2^+). This approach is needed to avoid short circuits or undefined states. Table 4-6 gives an overview of 16 possible states where only states 6, 7, 10 and 11 are useful.

Table 4-6: Possible states

State	S_1^+	S_1^-	S_2^+	S_2^-	V_{AN}		V_{BN}		$V_0 = V_{AN} - V_{BN}$		Component	
1	0	0	0	0	$-u_{dc}/2$	$i_0>0$	$u_{dc}/2$	$i_0>0$	$-u_{dc}$	$i_0>0$	D_1^- D_2^+	$i_0>0$
					$u_{dc}/2$	$i_0<0$	$-u_{dc}/2$	$i_0<0$	u_{dc}	$i_0<0$	D_1^+ D_2^-	$i_0<0$
2	0	0	0	1	$-u_{dc}/2$	$i_0>0$	$-u_{dc}/2$		0	$i_0>0$	D_1^- S_2^-	$i_0>0$
					$u_{dc}/2$	$i_0<0$			u_{dc}	$i_0<0$	D_1^+ D_2^-	$i_0<0$
3	0	0	1	0	$-u_{dc}/2$	$i_0>0$	$u_{dc}/2$		$-u_{dc}$	$i_0>0$	D_1^- D_2^+	$i_0>0$
					$u_{dc}/2$	$i_0<0$			0	$i_0<0$	D_1^+ S_2^+	$i_0<0$
4	0	0	1	1	$-u_{dc}/2$	$i_0>0$	short-circuit		short-circuit		S_2^+ S_2^-	
					$u_{dc}/2$	$i_0<0$					S_2^+ S_2^-	
5	0	1	0	0	$-u_{dc}/2$		$u_{dc}/2$	$i_0>0$	$-u_{dc}$	$i_0>0$	D_1^- D_2^+	$i_0>0$
							$-u_{dc}/2$	$i_0<0$	0	$i_0<0$	S_1^- D_2^-	$i_0<0$
6	**0**	**1**	**0**	**1**	$-u_{dc}/2$		$-u_{dc}/2$		**0**		D_1^- D_2^-	**$i_0>0$**
											S_1^- S_2^-	**$i_0<0$**
7	**0**	**1**	**1**	**0**	$-u_{dc}/2$		$u_{dc}/2$		$-u_{dc}$		D_1^- D_2^+	**$i_0>0$**
											S_1^- S_2^+	**$i_0<0$**
8	0	1	1	1	$-u_{dc}/2$		short-circuit		short-circuit		S_2^+ S_2^-	
9	1	0	0	0	$u_{dc}/2$		$u_{dc}/2$	$i_0>0$	0	$i_0>0$	S_1^+ D_2^+	$i_0>0$
							$-u_{dc}/2$	$i_0<0$	u_{dc}	$i_0<0$	D_1^+ D_2^-	$i_0<0$
10	**1**	**0**	**0**	**1**	$u_{dc}/2$		$-u_{dc}/2$		u_{dc}		S_1^+ S_2^-	**$i_0>0$**
											D_1^+ D_2^-	**$i_0<0$**
11	**1**	**0**	**1**	**0**	$u_{dc}/2$		$u_{dc}/2$		**0**		S_1^+ D_2^+	**$i_0>0$**
											D_1^+ S_2^+	**$i_0<0$**
12	1	0	1	1	$u_{dc}/2$		short-circuit		short-circuit		S_2^+ S_2^-	
13	1	1	0	0	short-circuit		$u_{dc}/2$	$i_0>0$	short-circuit		S_1^+ S_1^-	
							$-u_{dc}/2$	$i_0<0$				
14	1	1	0	1	short-circuit		$-u_{dc}/2$		short-circuit		S_1^+ S_1^-	
15	1	1	1	0	short-circuit		$u_{dc}/2$		short-circuit		S_1^+ S_1^-	
16	1	1	1	1	short-circuit		short-circuit		short-circuit		S_1^+ S_1^- S_2^+ S_2^-	

Using these four states 6, 7, 10 and 11, the DC input voltage can be modulated to the AC output voltage. Similar with the half-bridge VSI, the PWM technique is the most favorable. Since there are four useful states, there are two types of PWM techniques, more precisely the bipolar PWM technique and the unipolar PWM technique.

Bipolar PWM technique

When using the bipolar PWM technique, only two states are used. More precisely, state 7 (a positive signal on the gates of S_1^- and S_2^+) and state 10 (a positive signal on the gates of S_1^+ and S_2^-) are used. The output voltage will switch between u_{dc} and $-u_{dc}$ explain the name 'bipolar'. This bipolar approach is obtained by applying the same signal on the gates of the power switches S_1^+ and S_2^-. The inverted signal is applied to the gates of the other power switch of the same leg. The gate signal of the power switches S_1^- and S_2^+ is inverted and applied to the gates of the power switches S_1^+ and S_2^-. This strategy allows to use the same controller used in the half-bridge VSI. The physical connection of the gates is shown in Fig. 4.10. (b) which leads to Fig. 4.11. Only one single control signal and one single carrier signal is needed to generate the PWM output voltage. Since the output voltage varies between u_{dc} and $-u_{dc}$ equation (4-12) changes to (4-14)

$$v_{o1} = u_{dc} m_a \sin(\omega t) \text{ for } m_a \leq 1 \tag{4-14}$$

for an amplitude modulation ratio smaller than one. When the amplitude-modulation ratio is larger than one, the fundamental wave has an amplitude between u_{dc} and $\frac{4}{\pi} u_{dc}$, ranging from overmodulation to square wave modulation. Half-bridge inverters and full-bridge inverters (using bipolar PWM) have spectrums containing the same harmonic components. In case of a full-bridge inverter, the output voltage is doubled.

When using the PWM voltage containing fast voltage changes is not suited to feed capacitors since these voltage changes lead to high current pulses.

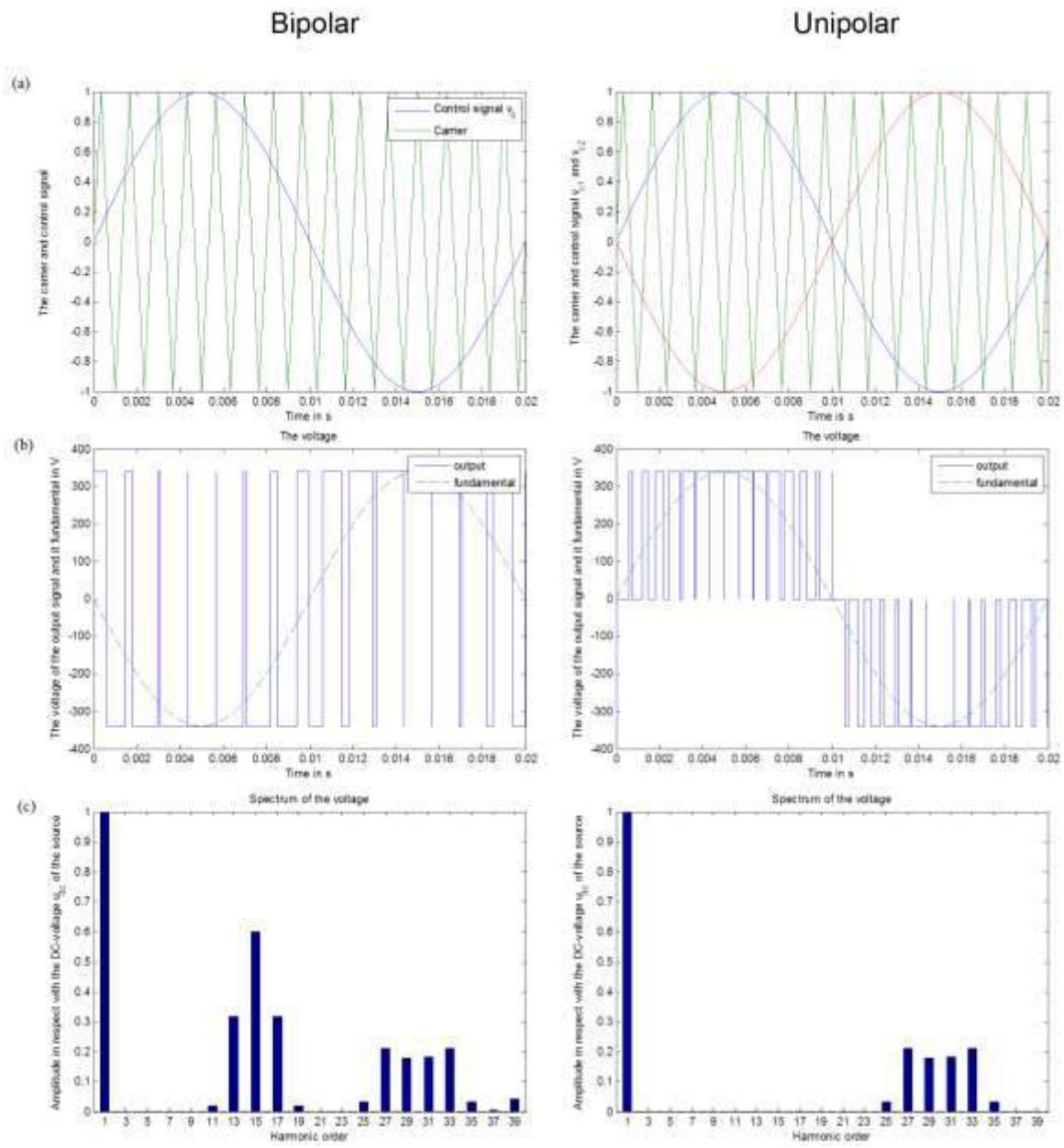


Fig. 4.11. Bipolar and unipolar PWM

Unipolar PWM technique

When using the unipolar PWM technique, the four defined states are used. More precisely, state 6 (a positive signal on the gates of S_1^- and S_2^-), state 7 (a positive signal on the gates of S_1^- and S_2^+), state 10 (a positive signal on the gates of S_1^+ and S_2^-) and state 11 (a positive signal on the gates of S_1^- and S_2^-) are used. The output voltage will switch between u_{dc} and zero or between $-u_{dc}$ and zero explain the name 'unipolar'. This unipolar approach is obtained by applying a control signal for each leg. Notice however that the carrier is the same for both control signals. Because the output voltage is the difference between the two legs, the control signals are anti-phase. This strategy has the need of two comparater, as shown in Fig. 4.12. The physical connection of the gates is shown in Fig. 4.12 which leads to Fig. 4.11. Only two anti-phase control signals and one single carrier signal is needed to generate the PWM output voltage. Since the output voltage varies between u_{dc} and zero of $-u_{dc}$ and zero equation (4-12) changes to (4-14) for an amplitude modulation ratio smaller than one. When the amplitude-

modulation ratio is larger than one, the fundamental wave has an amplitude between u_{dc} and $\frac{4}{\pi}u_{dc}$, ranging from overmodulation to square wave modulation.

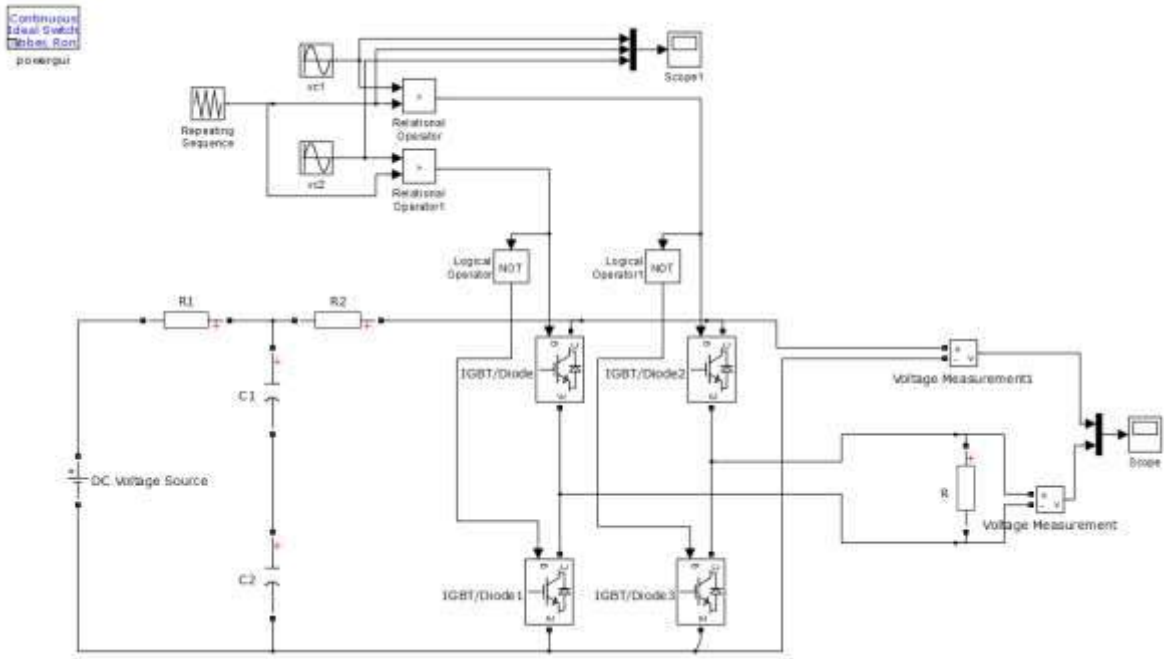


Fig. 4.12. Controller for a unipolar PWM modulation

When using the PWM voltage containing fast voltage changes is not suited to feed capacitors since these voltage changes lead to high current pulses, but the voltage drops are half as big as by its counterpart, bipolar PWM. Another advantage is that the switching frequency looks doubled, making it easier to filter the harmonics, or to reduce the switching frequency to decrease the switching losses. Mostly the frequency modulation ratio is in the case, single phase unipolar invertor, chosen as an even integer, because the even harmonics generated by the first leg and the second leg are in phase. As the output voltage is the difference of these two legs, the even harmonics do not appear in the output voltage, decreasing the number of harmonics.

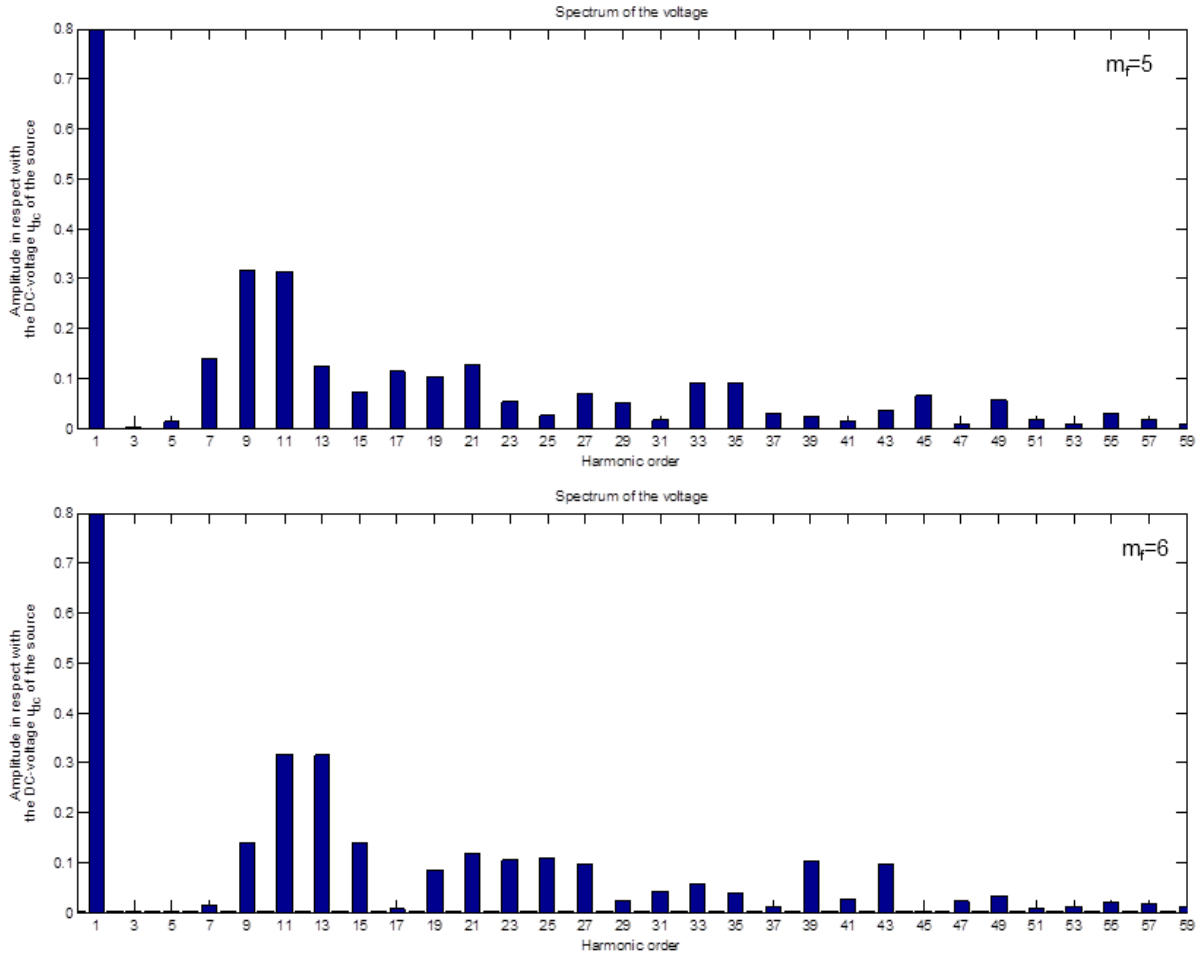


Fig. 4.13. Unipolare PWM with odd and even frequency modulation ratio

References

M.H. Rashid, Power Electronics Handbook, Elsevier – Academic Press, 2011.

G. Merlevede, Vermogenelektronica, Acco

4.3. Three phase inverters

Introduction

The vast majority of the frequency converters contain a rectifier and an inverter as visualized in Fig. 4.14. The grid voltage (having a fixed 50 Hz frequency) is rectified giving a DC-voltage. Using an inverter, this DC-voltage is converted into an AC-voltage which more or less resembles a sine voltage. The first order harmonic of this output AC-voltage is a sine and the inverter generally allows changing the amplitude and/or the frequency of this sine voltage.

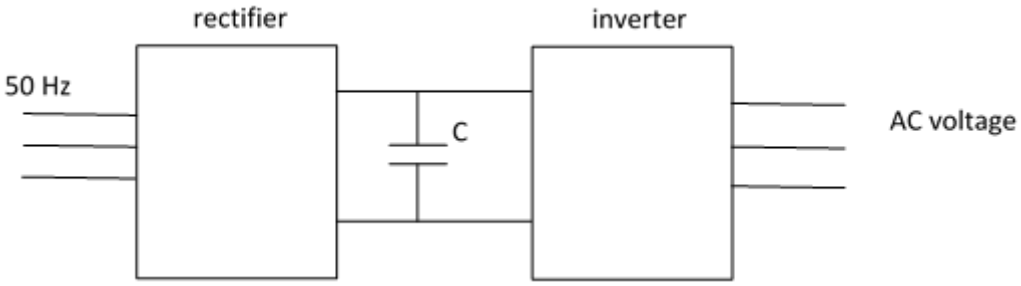


Fig. 4.14. Basic structure of a frequency converter

4.3.1. Square wave type Voltage Source Inverter

A Voltage Source Inverter (VSI) is fed by a DC-voltage. This DC-voltage can be the rectified grid voltage as visualized in Fig. 4.14., but it can also be a battery voltage (for instance in an UPS system). The DC-voltage can also be fed by a rail or a feed wire in a train or tram traction system.

Basic operation principle

Fig. 4.15 visualizes the basic operation principle of a three phase inverter. The DC-voltage V_t supplies the inverter containing 6 semiconductor switches 1, 2, 3, 4, 5 and 6. When considering the square wave-type inverter, each switch is closed during 180° (half of the period of the output voltage) implying always three switches are closed at the same time. In case only one switch of the upper half of the inverter is closed, two switches of the lower half of the inverter are closed. In case only one switch of the lower half of the inverter is closed, two switches of the upper half of the inverter are closed.

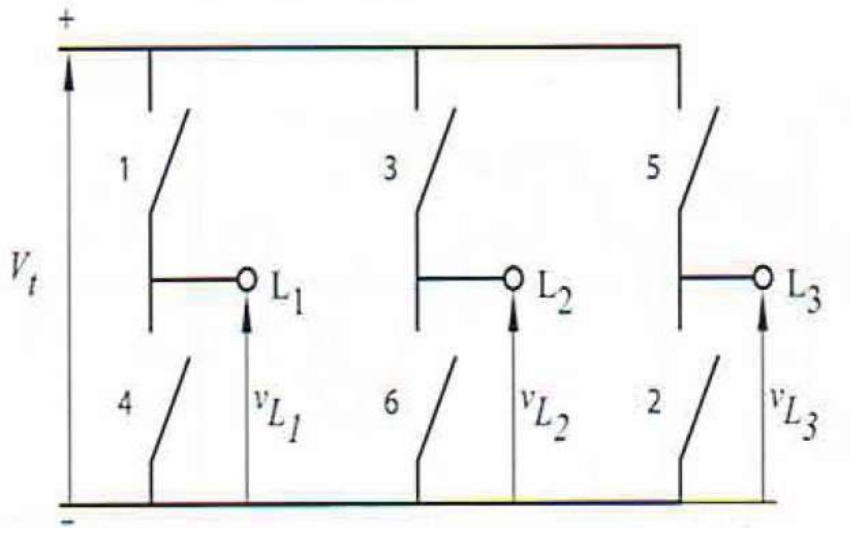


Fig. 4.15. Basic structure of a three phase inverter (source: Pollefliet)

As visualized in Fig. 4.16, the switches in Fig. 4.16 often consist of an IGBT (Insulated Bipolar Gate Transistor) and a flywheel diode. Using the voltage applied to the gate of the IGBT, the IGBT is forced to behave like a closed switch or an open switch.

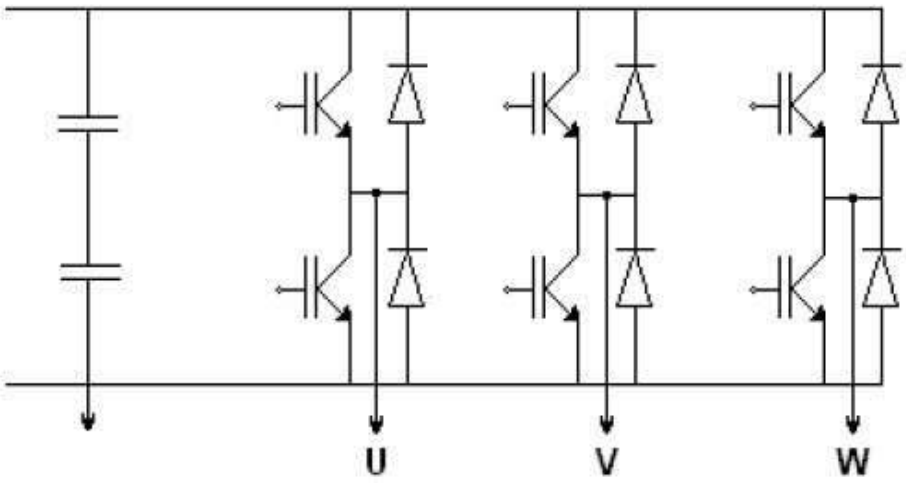


Fig. 4.16. Practical realization of a three phase inverter (source: Knockaert)

The inverter in Fig. 4.15 contains three bridges feeding respectively L_1, L_2 and L_3 (named U, V, W in Fig. 4.16.). Per bridge, it is very important no two switches may conduct simultaneously (for instance switch 1 and switch 4 may not conduct simultaneously) in order to prevent a short circuit of the DC-voltage v_t.

Fig. 4.17 visualizes the voltages $v_{L_1}(t)$, $v_{L_2}(t)$ and $v_{L_3}(t)$ i.e. the potential differences between the negative terminal of the DC-voltage source and respectively L_1, L_2 and L_3. In case switch 1 is closed $v_{L_1}(t) = V_t$ and in case switch 4 is closed $v_{L_1}(t) = 0$. Switches 3 and 6 are operated in a similar way giving $v_{L_2}(t)$ having a phase difference of 120° with respect to $v_{L_1}(t)$. Switches 5 and 2 are also operated in a similar way giving $v_{L_3}(t)$ having a phase difference of 120° with respect to $v_{L_1}(t)$ and $v_{L_2}(t)$.

Fig. 4.17 also visualizes the line voltages $v_{L_1L_2}(t)$, $v_{L_2L_3}(t)$ and $v_{L_3L_1}(t)$ (notice for instance $v_{L_1L_2}(t) = v_{L_1}(t) - v_{L_{21}}(t)$).

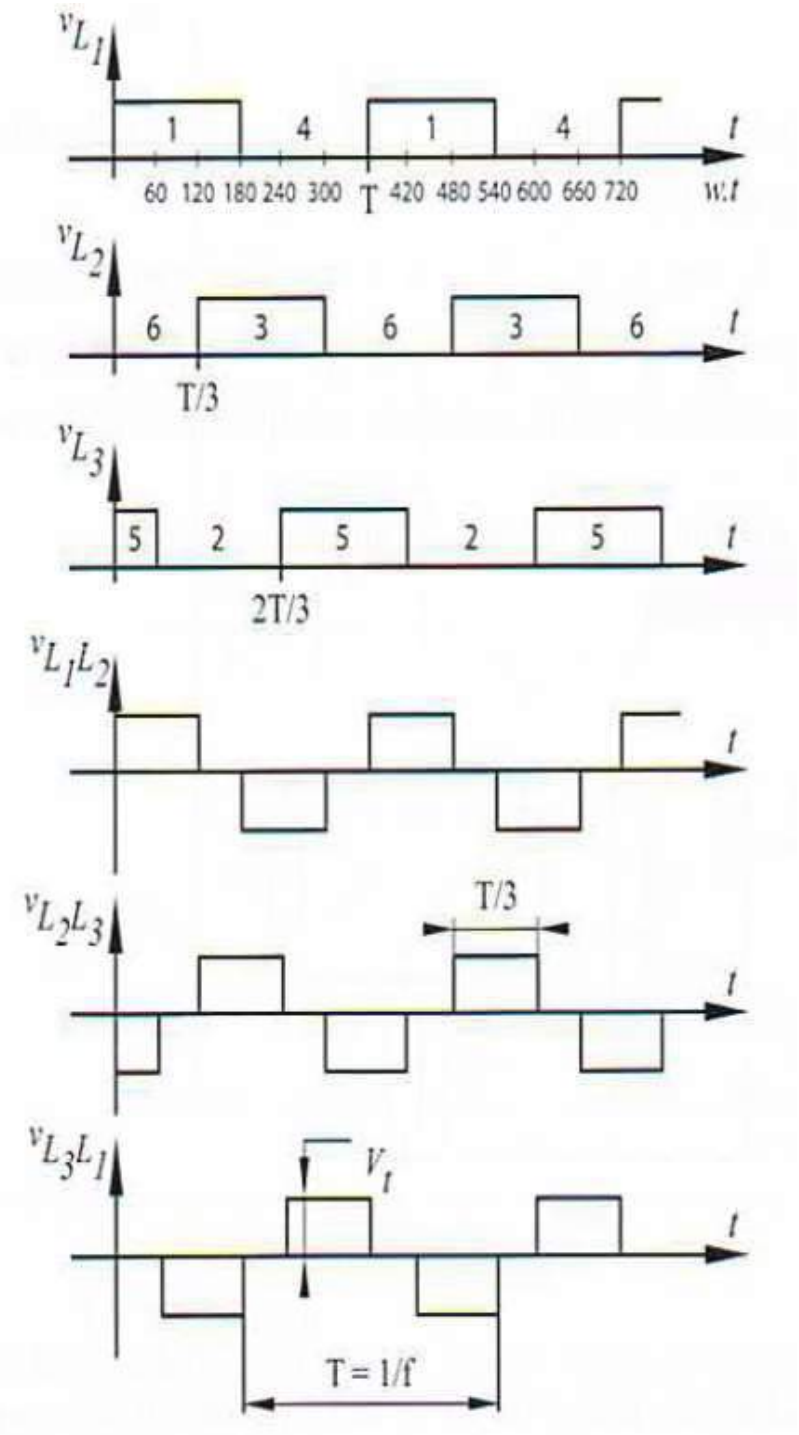


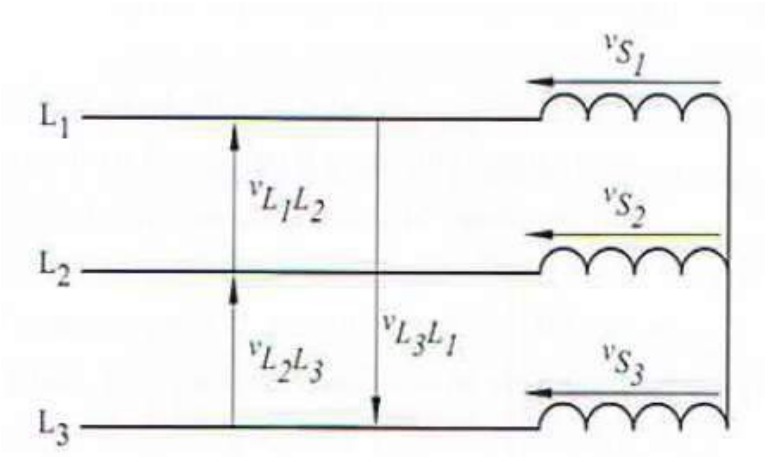
Fig. 4.17. Voltage waveforms of a 180°-type VSI inverter (source: Pollefliet)

Table 4-4: An overview of the closed switches in Fig. 4.15 and Fig. 4.17.

ωt	Closed switches
0° - 60°	5 – 6 – 1
60° - 120°	6 – 1 – 2
120° - 180°	1 – 2 – 3
180° - 240°	2 – 3 – 4
240° - 300°	3 – 4 – 5
300° - 360°	4 – 5 – 6

Voltage waveforms

Fig. 4.17 visualizes the (idealized) line voltages obtained by the inverter. Suppose these line voltages are used to feed an induction motor. When this induction motor is configured in delta, the phase voltages of the motor equal the line voltages. When this induction motor is configured in wye as visualized in Fig. 4.18., the phase voltages $v_{S_1}(t)$, $v_{S_2}(t)$ and $v_{S_3}(t)$ are obtained.



Figu. 4.18. Inverter feeding an induction motor configured in wye (source: Pollefliet)

At each instant of time, the instantaneous value of $v_{S_1}(t)$, $v_{S_2}(t)$ and $v_{S_3}(t)$ can be determined starting from Fig. 4.14 and closing the appropriate switches. For instance when switches 5, 6 and 1 (see Table 4-4) are closed, the situation visualized in Fig. 4.19 is obtained. This implies that $v_{S_1}(t) = v_{S_3}(t) = V_t/3$ and that $v_{S_2}(t) = -2\ V_t/3$. In a similar way, the voltages $v_{S_1}(t)$, $v_{S_2}(t)$ and $v_{S_3}(t)$ can be determined for all switching states of Table 4-4 as visualized in Fig. 4.20 visualizes the inverter feeding the three phase induction motor, the switching sequences of the switches, the line voltages and finally the phase voltages of the induction motor.

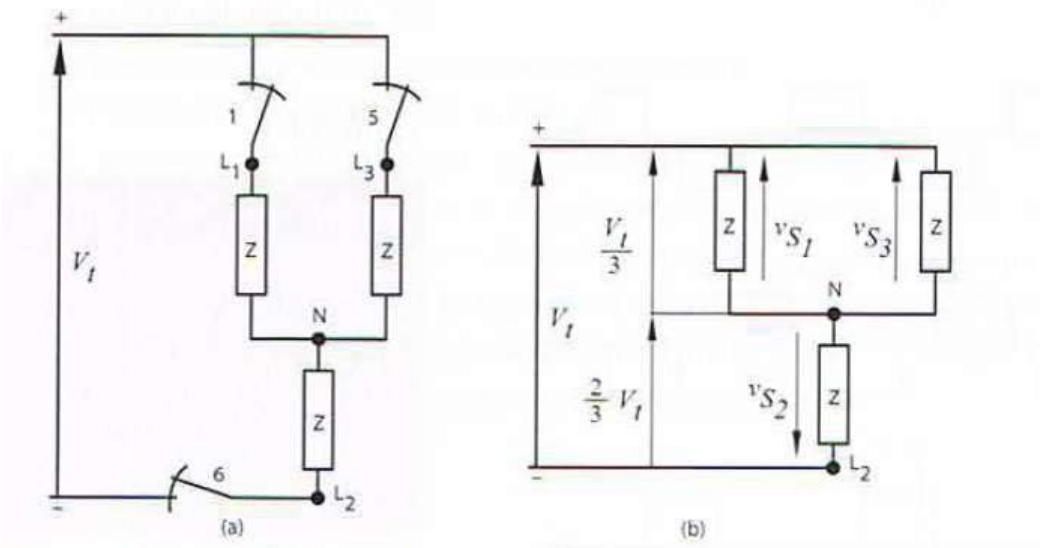


Fig. 4.19. Closing switches 5, 6 and 1 (source: Pollefliet)

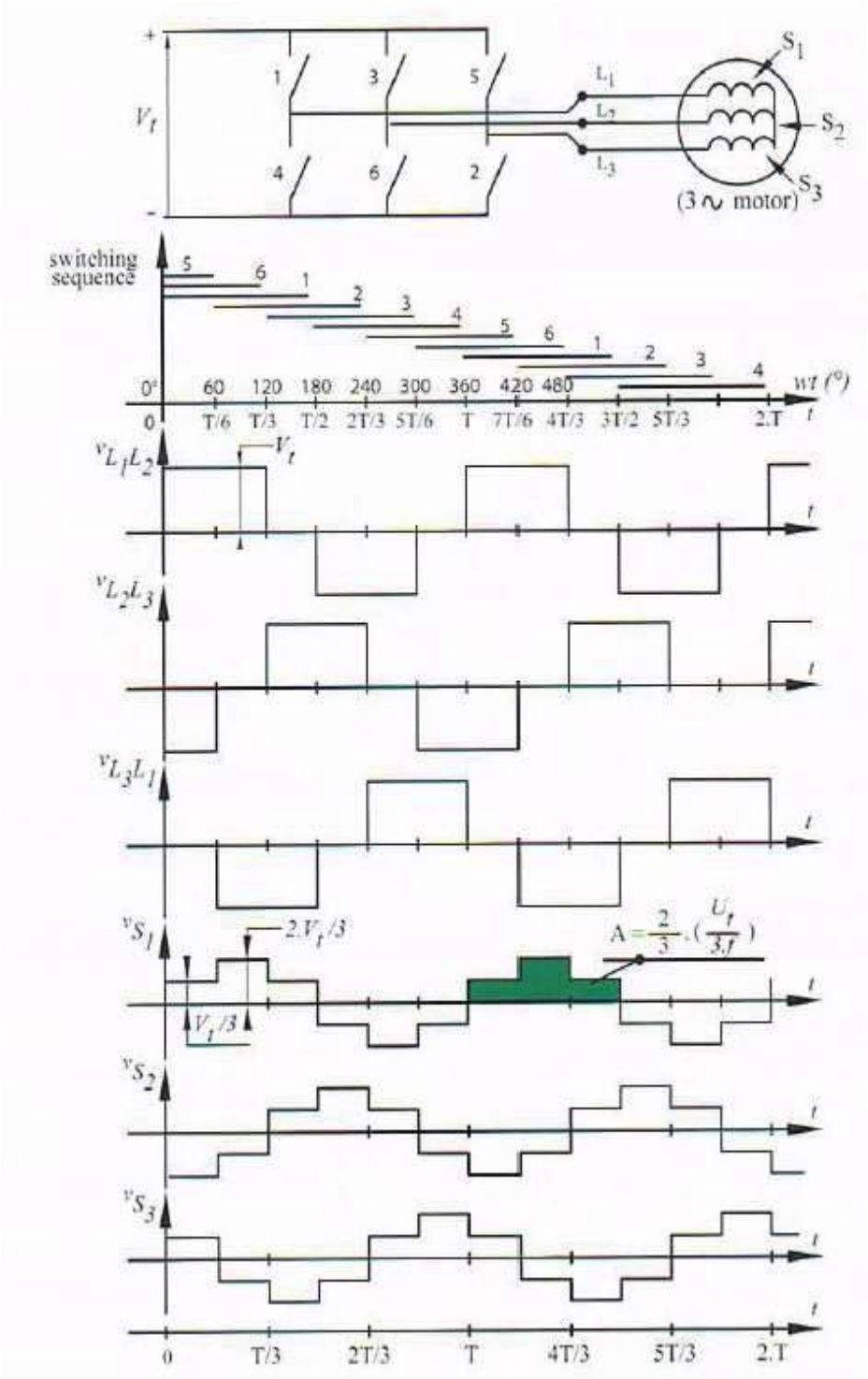


Fig. 4.20. Voltage waveforms of a wye connected induction motor (source: Pollefliet)

Fig. 4.21 not only visualizes such a voltage waveform (here, $v_{S_1}(t)$) but also the associated phase current of $i_{S_1}(t)$. Due to the ohmic-inductive behaviour of the motor coils, a current shape $i_{S_1}(t)$ is obtained which more resembles a sine than $v_{S_1}(t)$.

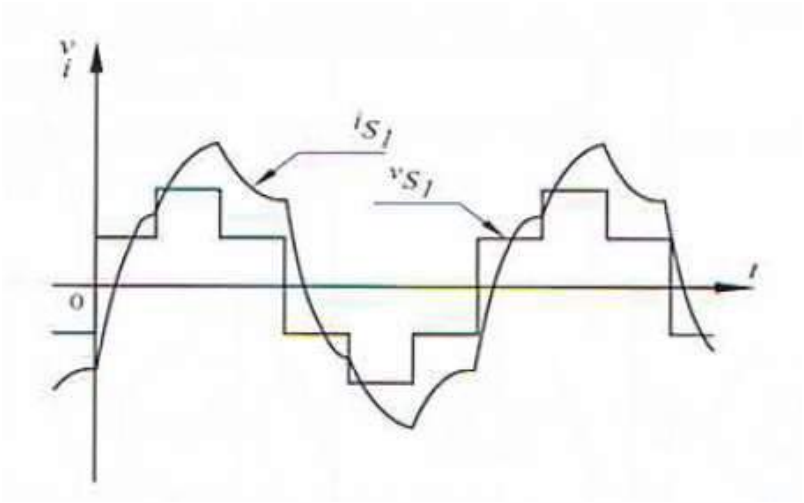


Fig. 4.21. Voltage and current waveform of an induction motor (source: Pollefliet)

Dead time

As already mentioned, in order to prevent a short circuit of V_t, it is absolute not allowed two switches of the same leg are conducting at the same time. As visualized in Fig. 4.20., for instance switch 1 closes at the moment switch 4 opens and similarly switch 4 closes at the moment switch 1 opens. Opening a switch requires some time implying the need for a so called dead time. This dead time is used between the opening of one switch and the closing of the other switch of the leg. In case of transistor switches (including IGBTS), dead times of 1 μs to 3 μs are common.

Evaluation

Harmonic contents

The voltages $v_{L_1L_2}(t)$, $v_{L_2L_3}(t)$ and $v_{L_3L_1}(t)$ in Fig. 4.20 are no sine-form voltages but using Fourier analysis, they can be considered as the sum of a fundamental wave and higher order harmonics. The same remark applies for the voltages $v_{S_1}(t)$, $v_{S_2}(t)$ and $v_{S_3}(t)$ in Fig. 4.20. The calculation of these harmonics is omitted here, but the presence of these higher order harmonics is unwanted.

Due to these higher order harmonics, additional copper and iron losses occur in the induction motor. Due to these higher order harmonics additional noise is generated and variations in the developed torque occur. Therefore, it is useful to develop control strategies in the inverter in order to obtain voltages having smaller higher order harmonics i.e. to obtain voltages which resemble a sinusoidal shape (or to have harmonics with a frequency which is sufficiently high implying the related current components are small due to the inductive effect of the motor coils).

Amplitude and frequency

The approach visualized in Fig. 4.17 and Fig. 4.2 allows to change the frequency of the voltages (indeed, an inverter is quite often part of a frequency converter as visualized in Fig. 4.13.) by changing the period T. Notice however, in case of a fixed DC-voltage V_t it is not

possible to change the amplitude of the voltage. It is not possible to change the amplitude of the fundamental wave in the voltage.

An opportunity to change the amplitude of this fundamental wave is useful since the ratio of this amplitude and the frequency determines the amplitude of the flux in the induction motor which also determines the breakdown torque of the induction motor. When changing the frequency, in a lot of applications the ratio between the amplitude and the frequency of the fundamental wave of the voltage is kept constant.

In order to change the amplitude of the voltages in Fig. 4.20., it is possible to equip the frequency converter with a controllable rectifier allowing to change V_t. In case V_t is fixed, the amplitude of the fundamental wave of the output voltage can also be changed by replacing the 180° conduction blocks by a number of individual pulses.

4.3.2. Pulse Frequency converter

Consider the frequency converter of Fig. 4.22 having a fixed DC-voltage V_t. The inverter contains switches 1, 2, 3, 4, 5 and 6 allowing to obtain the voltages $v_X(t)$, $v_Y(t)$, $v_Z(t)$ and the line voltages $v_{L_1L_2}(t)$, $v_{L_2L_3}(t)$, $v_{L_3L_1}(t)$.

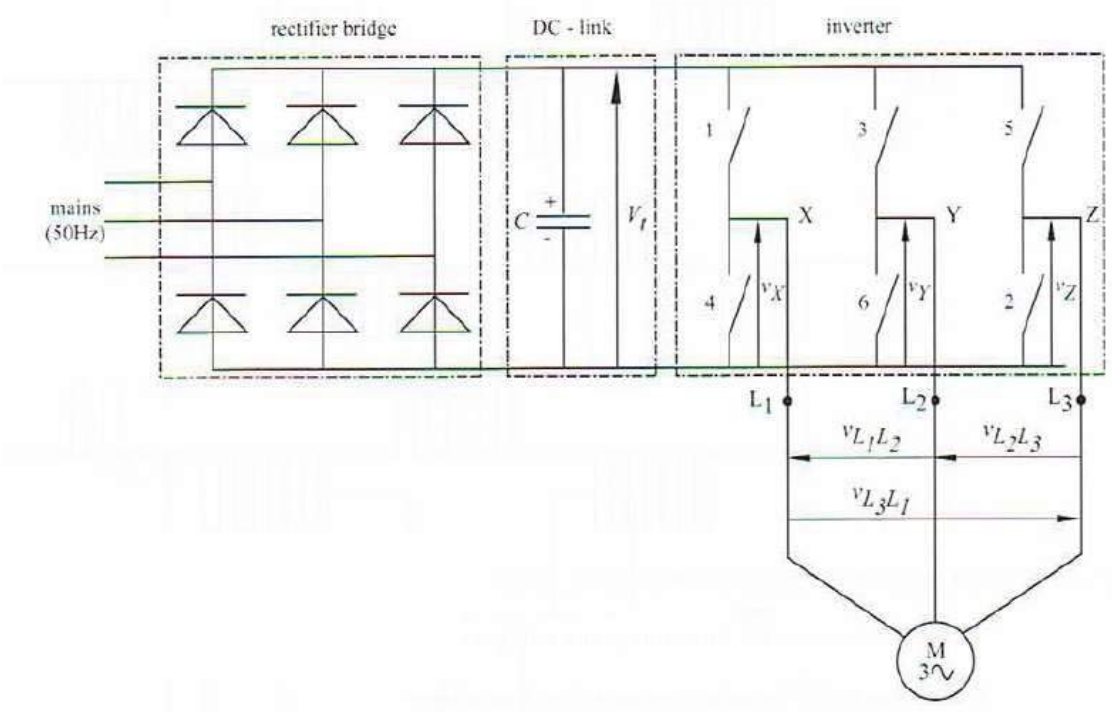


Fig. 4.22. Frequency converter (source: Pollefliet)

In Fig. 4.17 and Fig. 4.20., a switch is closed during 180° i.e. for half a period of the desired output voltage. Instead of opening and closing a switch only once per half period, Fig. 4.23 visualizes the output voltages $v_X(t)$, $v_Y(t)$, $v_Z(t)$ when opening and closing a switch n timer per half period. In Fig. 4.23., the closing time d is constant. Fig. 4.23 also visualizes the line voltages $v_{L_1L_2}(t)$, $v_{L_2L_3}(t)$ and $v_{L_3L_1}(t)$.

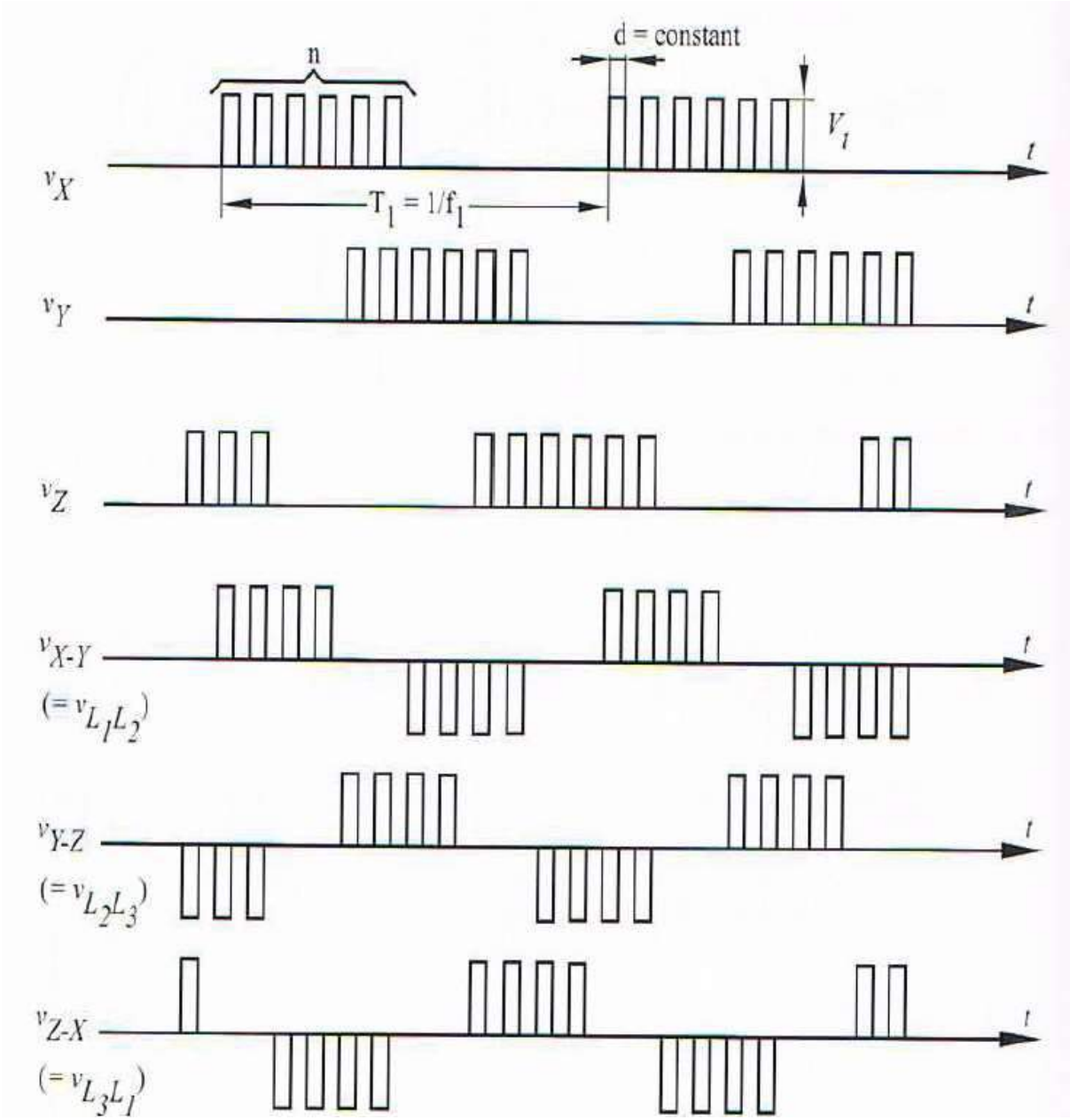


Fig. 4.23. Constant pulse train for the control of an induction motor (source: Pollefliet)

Consider for instance voltage $v_X(t)$, where the number of pulses n and the pulse width d are constant. By changing the time intervals between the pulses, the duration of a half period changes implying a different period T_1 and a different fundamental frequency $f_1 = 1/T_1$.

Verify that the line voltage $v_{L_1L_2}(t) = v_X(t) - v_Y(t)$ contains $2n/3$ pulses. It is possible to proof that the ratio between the RMS value of the fundamental wave of the line voltage voltage $v_{L_1L_2}(t)$ and the fundamental frequency f_1 equals

$$\frac{(V_{L_1L_2})_1}{f_1} = \frac{4\sqrt{3}\, n\, d\, V_t}{\pi}.$$

$$v_{o1} = u_{dc} m_a \sin(\omega t) \text{ for } m_a \leq 1 \qquad (4\text{-}15)$$

Evaluation

In case n, d and V_t are constant, this constant ratio implies a constant amplitude for the stator flux in the induction motor is obtained. This constant amplitude for the stator flux is also obtained when changing the time intervals between the pulses i.e. when changing the output frequency.

Notice there is a maximum frequency which can be realized. Indeed, $n\,d$ is the minimum value for $T_1/2$ which is obtained when all the time intervals between the pulses are zero. This implies

$$f_{1max} = \frac{1}{2\,n\,d}. \quad \boldsymbol{v_{o1} = u_{dc} m_a \sin(\omega t) \text{ for } m_a \leq 1} \tag{4-16}$$

Notice the waveforms in Fig. 4.23 generate a lot of harmonics. In order to reduce the harmonic contents of the voltage waveforms, using PWM (Pulse Width Modulation) is an appropriate approach.

4.3.3. Pulse Width Modulation

Basic approach

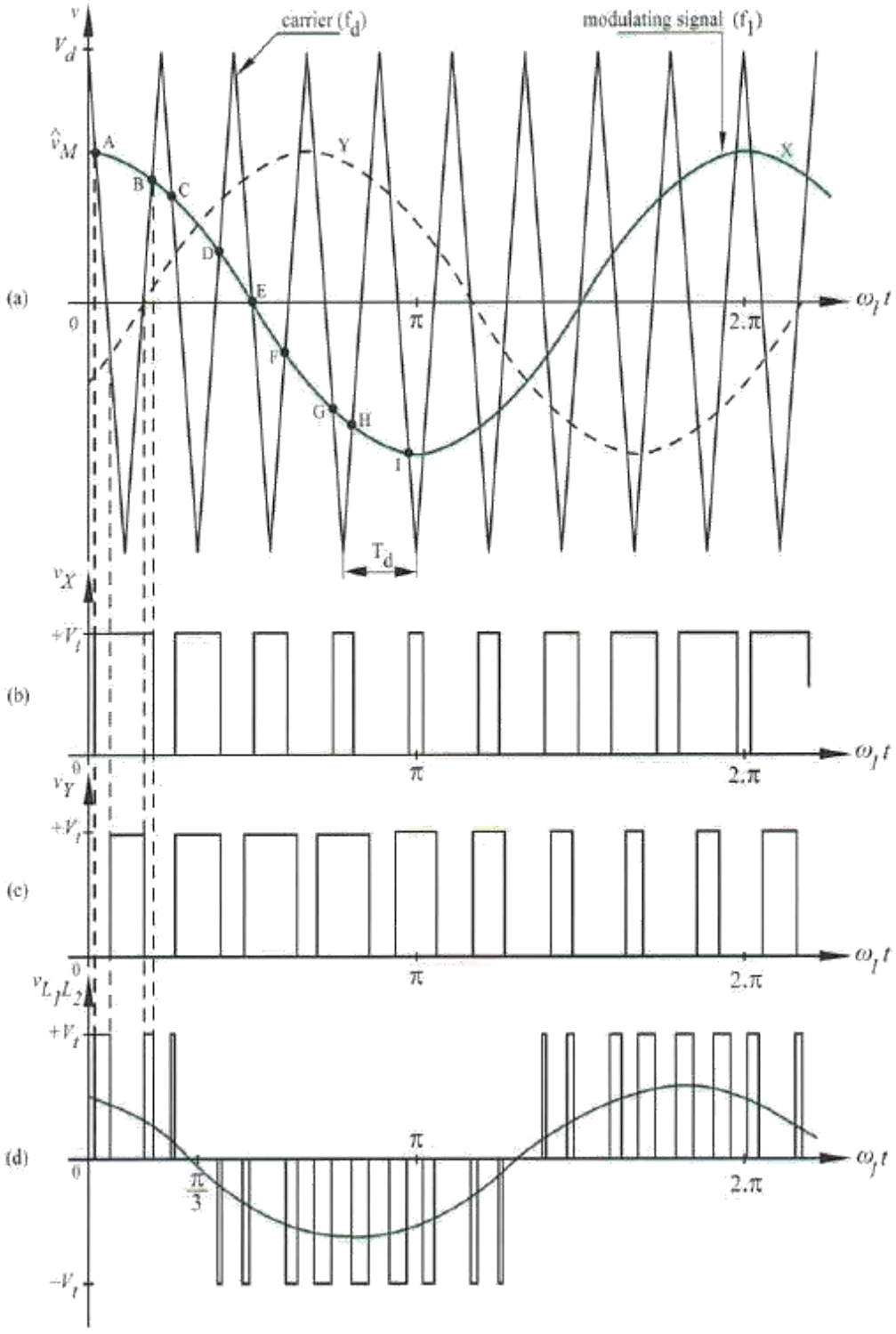


Fig. 4.24. Sinusoidal PWM waveforms (source: Pollefliet)

Fig. 4.24 visualizes how a Pulse Width Modulated voltage can be obtained using inverter in the frequency converter of Fig. 4.22. The intersections of a triangular wave (which is called the carrier having a frequency f_d) and a sinusoidal wave (which is called the modulating

signal having a frequency f_1) determine when the switches in the inverter are opened or closed. In Fig. 4.24.(a) using sine wave X, at the time instants A, C, E, G, I switch 1 will be closed and switch 4 will be opened implying $v_X = V_t$. At the time instants B, D, F, H switch 4 will be closed and switch 1 will be opened implying $v_X = 0$. Finally, the voltage $v_X(t)$ as visualized in Fig. 4.24.(b) is obtained. Instead of considering sine wave X, the intersections of sine wave Y and the triangular carrier determine the opening and closing of switches 3 and 6. This gives rise to the voltage $v_Y(t)$ as visualized in Fig. 4.24.(c).

Using the relationship $v_{L_1L_2}(t) = v_X(t) - v_Y(t)$, the line voltage in Fig. 4.24.(d) is obtained. This voltage is not a sine but its fundamental wave is also visualized in Fig. 4.24.(d). By changing the modulating signal, the fundamental wave of the obtained $v_{L_1L_2}(t)$ also changes. It is possible to choose the frequency, the amplitude and the phase (also the shape of the obtained voltage can be chosen but in the present application we consider a sine) of this fundamental wave.

Between sine wave X and sine wave Y, there is a phase shift of 120°. When adding a third sine wave Z (not visualized in Figure 11), also voltage $v_Z(t)$ and the line voltages $v_{L_2L_3}(t)$ and $v_{L_3L_1}(t)$ can be obtained.

Important parameters and overmodulation

When considering the inverter using Pulse Width Modulation, the pulse number m_f is the ratio between the frequency of the carrier (carrier frequency f_d) and the frequency of the modulating signal (modulating frequency f_1) i.e.

$$m_f = \frac{f_d}{f_1}. \quad \boldsymbol{v_{o1} = u_{dc} m_a \sin(\omega t) \text{ for } m_a \leq 1} \tag{4-17}$$

The ratio between the amplitude $\hat{v}_M$ of the modulating signal and the amplitude V_d of the carrier is the modulation depth m i.e.

$$m_a = \frac{\hat{v}_M}{V_d}. \quad \boldsymbol{v_{o1} = u_{dc} m_a \sin(\omega t) \text{ for } m_a \leq 1} \tag{4-18}$$

In Fig. 4.24, the modulation depth m_a is smaller than unity. In the case when the amplitude of the modulating signal is higher than the amplitude of the carrier, the modulation depth is larger than unity and overmodulation occurs. As the modulation depth is larger than unity and increases, the obtained output voltage of the inverter resembles more and more a square wave. Fig. 4.25 visualizes a PWM voltage with overmodulation.

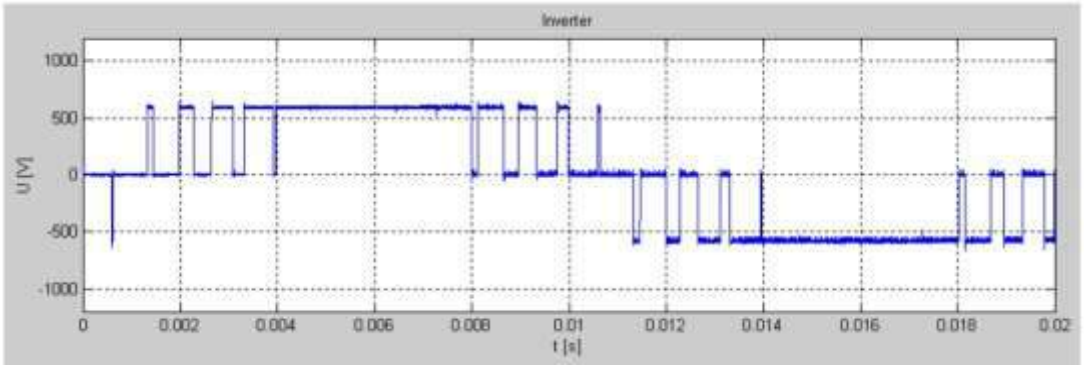


Fig. 4.25. PWM voltage with overmodulation (source: Knockaert)

Fig. 4.26 visualizes the relationship between the modulation depth m_a and the ratio between the RMS value of the fundamental wave and V_t.

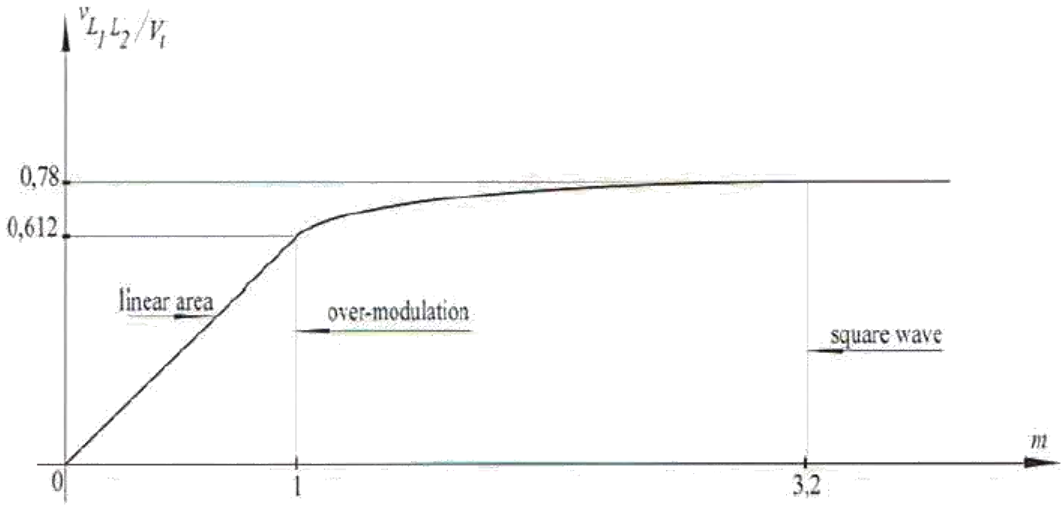


Fig. 4.26. Output line voltage as a function of the modulation depth (source: Pollefliet)

Remarks

During the positive alternance of the line voltage, the voltage switches between V_t and **0**. During the negative alternance of the line voltage, the voltage switches between $-V_t$ and **0**. This approach is called unipolar PWM.

Also using PWM, the output line voltage is not a sine implying not only a desired fundamental wave but also higher order harmonics are obtained. In comparison with the approaches visualized in Fig.4.17 and Fig.4.23, the harmonics have a higher frequency implying they are easier to filter them out. Actually also the inductivity of the motor coils behave as a low pass filter reducing the higher order harmonics in the current.

Standard switching frequencies f_a are between 2 kHz and 4 k Hz but also frequencies of 8 kHz, 16 kHz or 32 kHz are used. In general, pulse numbers N are odd multiples of 3 implying pulse numbers of 9, 15, 21, … are common. Taking odd integer pulse numbers, the harmonic contents of the output voltage is limited. If in addition, the pulse number is an odd numbered multiple of three, all harmonics that are multiples of three disappear in the line voltage. The remaining most dominant harmonics are now:

$$(2N \pm 1)\, f_1 \cdot v_{o1} = u_{dc} m_a \sin(\omega t) \text{ for } m_a \leq 1 \quad (4\text{-}19)$$

By adding a third order harmonic to the modulating signal, the fundamental wave of this modulating signal can be larger without having overmodulation. This added third order harmonic appears in the voltages $v_X(t)$, $v_Y(t)$ and $v_Z(t)$ but this third order harmonic does not appear in the line voltages $v_{L_1L_2}(t)$, $v_{L_2L_3}(t)$ and $v_{L_3L_1}(t)$.

References:

Knockaert J., Peuteman J., Catrysse J. and Belmans R., Hidden reflection phenomenon of inverter-fed induction motors, Proceedings of the 11th European Conference on Power Electronics and Applications EPE 2005, Dresden, Germany, September 11-14, 2005, paper 0289.

Knockaert J., Peuteman J., Catrysse J. and Belmans R., Stairstepping on PWM Inverters Explained, The 4th International Conference on Power Electronics, Machines and Drives PEMD 2008, April 2-4, York, United Kingdom, pp. 495-499.

Mohan N., Undeland T.M. and Robbins W.P., Power Electronics: Converters, Applications, and Design, John Wiley & Sons, 2003.

Pollefliet J., Electronic Power Control: Power Electronics, Academia Press, Gent Belgium, 2011.

4.4. Space-vector modulation

Due to the rise of digital systems, new control strategies including digital modulating techniques are available. The space-vector modulation is one example of such a technique which gives a unique way to compose the PWM signal at the output of a frequency converter. The technique is based on the fact that a three-phase inverter has only eight possible states and tries to make the best PWM signal (meaning less harmonics) with a minimum change of the power switches (meaning less losses). In order to obtain this space-vector modulating technique, the three-phase system has to be transformed to a complex plane, by using the Clarke-transformation.

4.4.1. Clarke Transformation

Consider a symmetrical three-phase system, where the three voltages have the same magnitude and a displacement of $\frac{2\pi}{3}$. In this chapter we assume that the used three-phase load (induction machine, PM synchronous machine, three-phase transformer, three-phase heating system) has an isolated neutral point. This means that the sum of all line voltages and currents are always zero according to Kirchoff's law.

$$u_{ab} + u_{bc} + u_{ca} = 0 v_{o1} = u_{dc} m_a \sin(\omega t) \text{ for } m_a \leq 1 \quad (4\text{-}20)$$

$$u_{ab} + u_{bc} + u_{ca} = 0 v_{o1} = u_{dc} m_a \sin(\omega t) \text{ for } m_a \leq 1 \quad (4\text{-}21)$$

This allows to describe the three-phase load by using only two line voltages and two currents, because the third line voltage and the third current can be calculated by (4-20) and (4-21). In other words, this three phase load can be reduced to a two phase load which has the same properties. To obtain the most optimal transformation, the two phase load needs inductive components (coils) which do not interact with each other, meaning their magnetic axes are perpendicular. The use of this transformation originates from electrical machine theory. About 65% of the industrial electrical consumption is due to three phase electrical machines (source: Anibal De Almeida, Professor, ISR-University of Coimbra / SAVE Study Final Report 2000). The first step in this transformation is obtained by projecting the three different voltages on the alpha-axis and the beta-axis, the equations (4-22) and (4-23) are obtained.

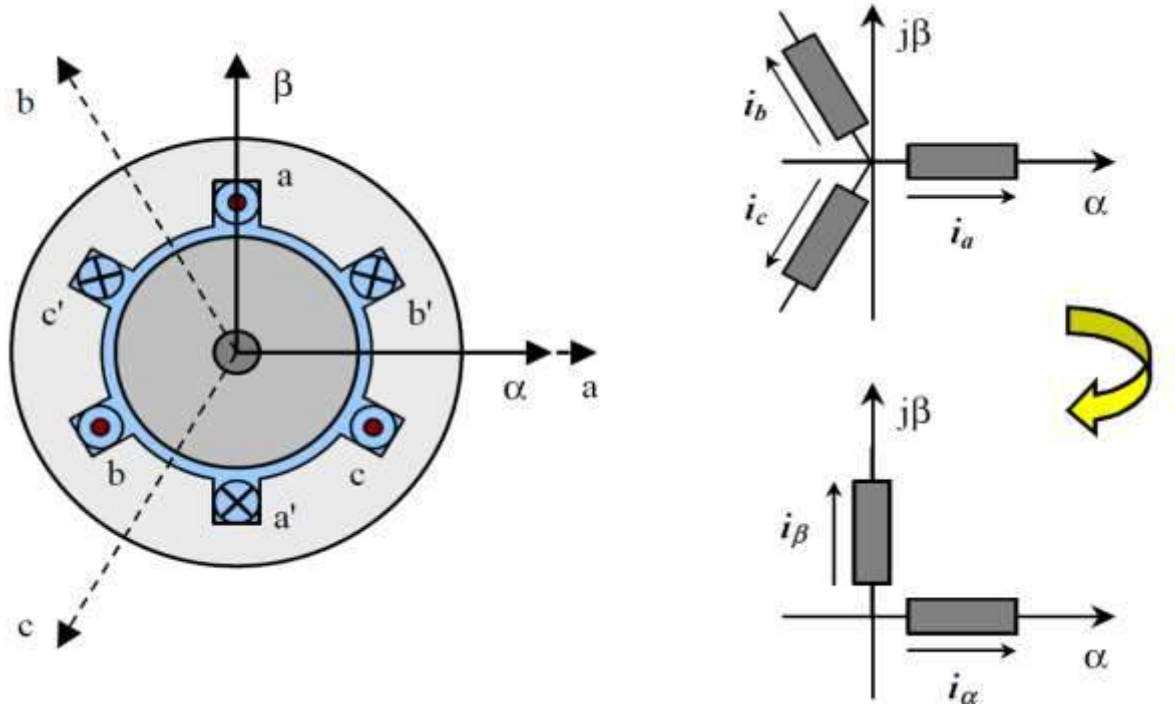


Fig. 4.27. Transformation from a three-phase to a two-phase reference frame (TERÖRDE)

$$u_\alpha = u_{a0} + u_{b0}\cos\left(\frac{2\pi}{3}\right) + u_{c0}\cos\left(\frac{4\pi}{3}\right) = u_{a0} - \frac{1}{2}u_{b0} - \frac{1}{2}u_{c0}$$

$$v_{o1} = u_{dc} m_a \sin(\omega t) \text{ for } m_a \leq 1 \qquad (4\text{-}22)$$

$$u_\beta = u_{b0}\sin\left(\frac{2\pi}{3}\right) + u_{c0}\sin\left(\frac{4\pi}{3}\right) = \frac{\sqrt{3}}{2}u_{b0} - \frac{\sqrt{3}}{2}u_{c0} v_{o1} = u_{dc} m_a \sin(\omega t) \text{ for } m_a \leq 1 \quad (4\text{-}23)$$

There is a small problem with this transformation, this transformation is not power invariant when the same transformation is performed on the current:

$$u_{a0}i_{a0} + u_{b0}i_{b0} + u_{c0}i_{c0} \neq u_\alpha i_\alpha + u_\beta i_\beta$$

$$u_{a0}i_{a0} + u_{b0}i_{b0} + u_{c0}i_{c0} \neq \left(u_{a0} - \frac{1}{2}u_{b0} - \frac{1}{2}u_{c0}\right)\left(i_{a0} - \frac{1}{2}i_{b0} - \frac{1}{2}i_{c0}\right) + \left(\frac{\sqrt{3}}{2}u_{b0} - \frac{\sqrt{3}}{2}u_{c0}\right)\left(\frac{\sqrt{3}}{2}i_{b0} - \frac{\sqrt{3}}{2}i_{c0}\right)$$

$$u_{a0}i_{a0} + u_{b0}i_{b0} + u_{c0}i_{c0} \neq u_{a0}i_{a0} + u_{b0}i_{b0} + u_{c0}i_{c0} + \frac{1}{2}u_{a0}(-i_{b0} - i_{c0}) + \frac{1}{2}u_{b0}(-i_{a0} - i_{c0}) + \frac{1}{2}u_{c0}(-i_{a0} - i_{b0})$$

Using equation (4-21) gives:

$$u_{a0}i_{a0} + u_{b0}i_{b0} + u_{c0}i_{c0} \neq \frac{3}{2}(u_{a0}i_{a0} + u_{0b}i_{b0} + u_{c0}i_{c0})$$

As shown in the equation above, the power difference equals a constant factor $3/2$, which can be resolved. This power variation can be unmade by multiplying the power obtained by the αβ components with $2/3$. This scaling factor can be performed only on the voltage, only on the current or on voltage and current. Different scaling factors can be applied having a product which equals $2/3$ (for example on current and voltage a scaling factor of $\sqrt{\frac{2}{3}}$). In this case of space-vector modulation, one chooses to apply the scaling factor of $2/3$ on the voltage, because it gives a unique property. Applying this scaling factor on the earlier transformation (4-22) and (4-23) gives (4-24).

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} u_{a0} \\ u_{b0} \\ u_{c0} \end{bmatrix} \tag{4-24}$$

This unique property is shown in the following example:

$$\begin{bmatrix} u_{a0} \\ u_{b0} \\ u_{c0} \end{bmatrix} = \begin{bmatrix} U_m \sin(\omega t) \\ U_m \sin(\omega t - \frac{2\pi}{3}) \\ U_m \sin(\omega t - \frac{4\pi}{3}) \end{bmatrix}$$

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} U_m \sin(\omega t) \\ U_m \sin(\omega t - \frac{2\pi}{3}) \\ U_m \sin(\omega t - \frac{4\pi}{3}) \end{bmatrix} =$$

$$\begin{bmatrix} \frac{2}{3}\left(U_m \sin(\omega t) - \frac{1}{2}U_m \sin(\omega t - \frac{2\pi}{3}) - \frac{1}{2}U_m \sin(\omega t - \frac{4\pi}{3})\right) \\ \frac{2}{3}\left(\frac{\sqrt{3}}{2}U_m \sin(\omega t - \frac{2\pi}{3}) - \frac{\sqrt{3}}{2}U_m \sin(\omega t - \frac{4\pi}{3})\right) \end{bmatrix}$$

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \begin{bmatrix} U_m \sin(\omega t) \\ U_m \cos(\omega t) \end{bmatrix}$$

This transformation is unique, because the amplitude of the two phase system equals the amplitude of the three-phase voltage. Notice the pulsations $\omega\ (= 2\pi f)$ of the three-phase voltage system and the two phase system are the same. This also shows that a perfect three-phase voltage is represented as a phasor in the alpha/beta plane, where this phasor has a constant amplitude which rotates at a constant pulsation making a perfect circle in one period.

Using the space-vector modulation technique, three-phase sinusoidal line voltages are wanted. As shown with equation (4-20), this means that the sum of the line voltages is zero, but this does not mean that the sum of the three phase voltages is zero. The phase voltages, the voltages between the phases and the neutral, may consist of the fundamental sinusoidal phase voltages and some homopolar components. A homopolar component is a sinusoidal component having a frequency which is a multiple of the fundamental frequency, which does not appear in the line voltage. The three homopolar components have the same amplitude and

the same phase. In a three phase system, harmonics having an order which is a multiple of three are homopolar, as shown in Fig. 4.14.

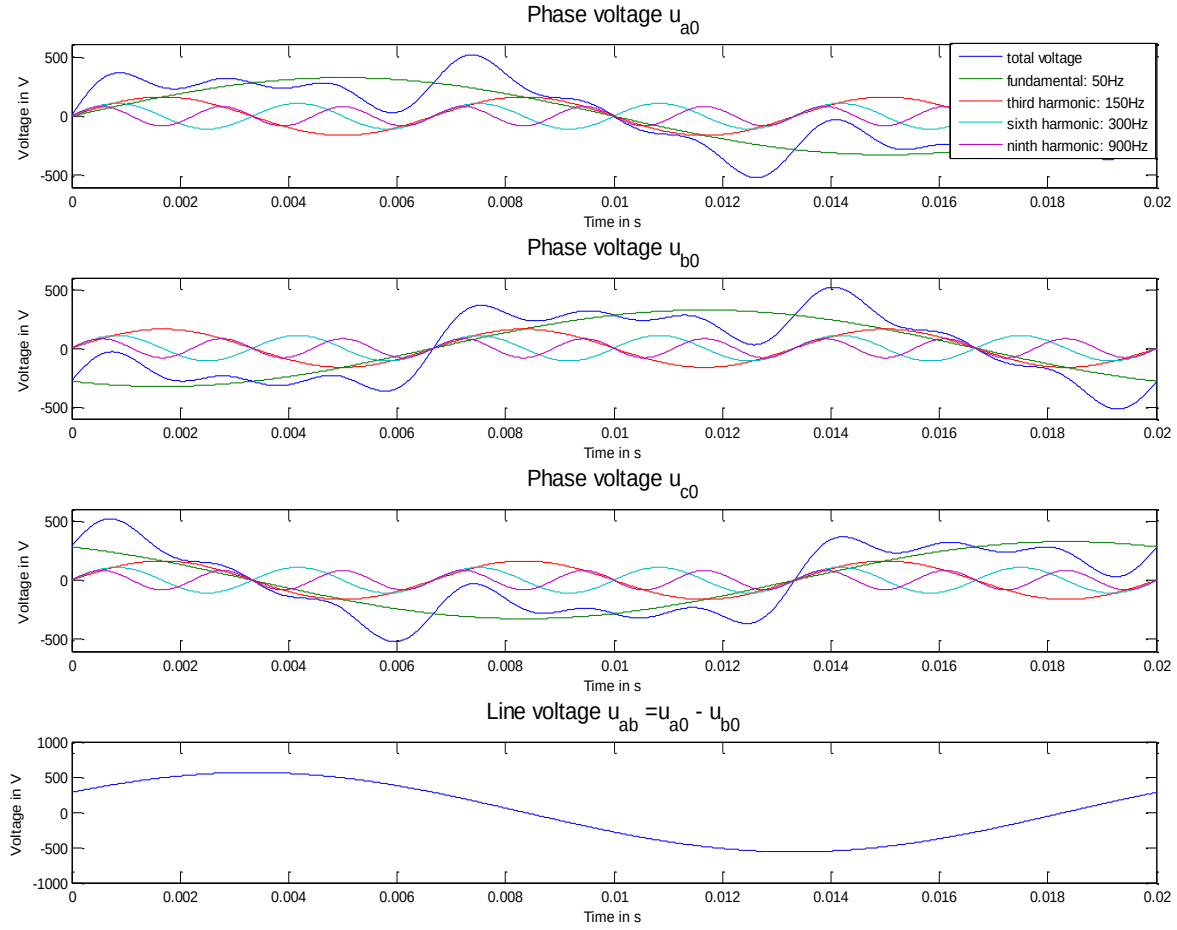


Fig. 4.148. Homopolar components

Fig. 4.14 shows three phase voltages each containing a 50Hz fundamental wave, a third order harmonic, a sixth order harmonic and a ninth order harmonic. By subtracting the first phase voltage and the second phase voltage, a line voltage containing only the 50 Hz fundamental is obtained.

The homopolar component only affects the potential of the isolated neutral point of the three-phase load. Due to the fact that the sum of the line voltages equals zero, these homopolar components have no direct effect on the three phase load. These homopolar components in the phase voltages can increase the amplitude of the fundamentals of the phase and the line voltages, without introducing extra harmonics in the line voltages or without using overmodulation.

These homopolar components will have their effect on the result of the Clarke transformation. The homopolar component implies the neutral potential u_0 will be displaced, as visualized in Fig. 4.29 Since the phase voltages u_{a0}, u_{b0} and u_{c0} equal the sum of the line-to-isolated_neutral voltages u_{an}, u_{bn} or u_{cn} and the neutral potential u_0 (which is called the zero component), the value of u_0 can be obtained. Because the sum of the line-to-isolated_neutral voltages is zero (this is the balanced, symmetrical phase voltage without homopolar components), the mean value of u_{a0}, u_{b0} and u_{c0} equals u_0. More precisely,

$$u_{an} + u_{bn} + u_{cn} = (u_{a0} - u_0) + (u_{b0} - u_0) + (u_{a0} - u_0) = 0$$

$$u_0 = \frac{1}{3}(u_{a0} + u_{b0} + u_{c0})$$

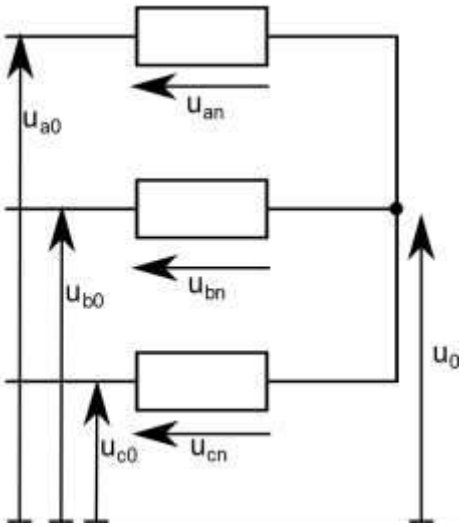


Fig. 4.29. Three phase load with voltage definitions

So adding the zero component to the Clarke transformation leads to:

$$\begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} u_{a0} \\ u_{b0} \\ u_{c0} \end{bmatrix} \tag{4-25}$$

4.4.2. Eight possible states

By using a three-phase inverter, there are only eight possible states which can be obtained. These states are shown in Table 4-5. In this table the number of the state, which switches are closed and the values of the phase voltages are shown. When the upper switch (IGBT1, IGBT3 or IGBT5) of a bridge is closed, than the phase voltage equals U_{DC}. When the lower switch (IGBT2, IGBT4 or IGBT6) is closed, than the phase voltage equals zero. This allows to determine the homopolar voltage and the space-vector voltage. The homopolar voltage is the mean value of the three phase voltages, so the zero component. The space-vector voltage is a spatial representation of the total voltage when every phase voltage has the spatial position of the corresponding phase winding in an electrical machine, i.e. the polar notation $U_\gamma e^{j\varphi}$

of $u_\alpha + ju_\beta$ obtained using $\begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} u_{a0} \\ u_{b0} \\ u_{c0} \end{bmatrix}$.

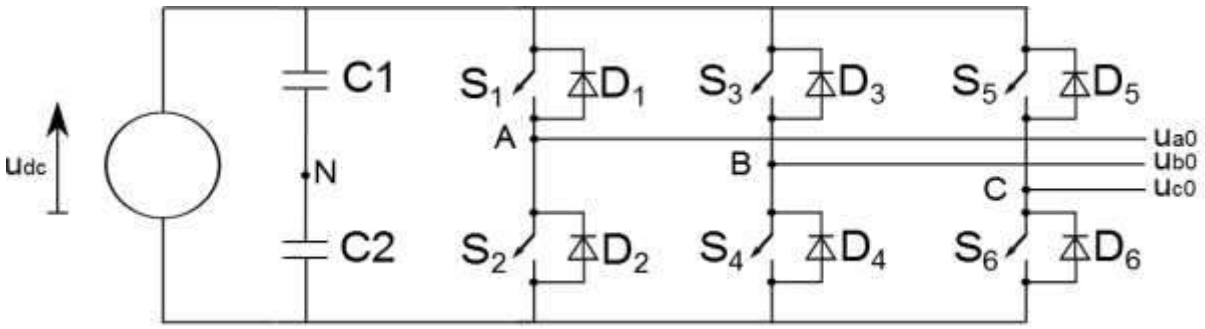


Fig. 4.30. Three phase inverter

Consider state 1. The upper switch IGBT1 (visualized as S_1 in Fig. 4, because this can be an IGBT or a Mosfet or …) is closed and the lower switches IGBT3 and IGBT 4 are closed, implying u_a that equals U_{DC} and that u_b and u_c equal zero. Using equation (4-25), this allows to determine the homopolar voltage (the mean of the three phase voltages) and the space-vector (polar notation $U_\gamma e^{j\varepsilon}$ of $u_\alpha + ju_\beta$, which equals $\frac{2}{3}U_{DC}e^{j0}$). As shown in Table 4-5, the amplitude of the space-vector is constant for all non-zero states but this is not true for the homopolar voltage. Notice that the phase voltage is not of sine-form, due to the fact there is a homopolar component.

Table 4-5: Invertor states and space-vector voltage

State	Switch on (up/down)			Phase voltage			Homopolar voltage	Space-vector voltage Clarke transformation polar notation
	A	B	C	u_{a0}	u_{b0}	U_{c0}		
0	IGBT2	IGBT4	IGBT6	0	0	0	0	0
1	IGBT1	IGBT4	IGBT6	U_{DC}	0	0	1/3 U_{DC}	$\frac{2}{3}U_{DC}e^{j0}$
2	IGBT1	IGBT3	IGBT6	U_{DC}	U_{DC}	0	2/3 U_{DC}	$\frac{2}{3}U_{DC}e^{j\frac{\pi}{3}}$
3	IGBT2	IGBT3	IGBT6	0	U_{DC}	0	1/3 U_{DC}	$\frac{2}{3}U_{DC}e^{j\frac{2\pi}{3}}$
4	IGBT2	IGBT3	IGBT5	0	U_{DC}	U_{DC}	2/3U_{DC}	$\frac{2}{3}U_{DC}e^{j\frac{3\pi}{3}}$
5	IGBT2	IGBT4	IGBT5	0	0	U_{DC}	1/3 U_{DC}	$\frac{2}{3}U_{DC}e^{j\frac{4\pi}{3}}$
6	IGBT1	IGBT4	IGBT5	U_{DC}	0	U_{DC}	2/3 U_{DC}	$\frac{2}{3}U_{DC}e^{j\frac{5\pi}{3}}$
7	IGBT1	IGBT3	IGBT5	U_{DC}	U_{DC}	U_{DC}	U_{DC}	0

Notice that two of these states give an output voltage (space-vector voltage) of zero and six states give a voltage higher than zero.

4.4.3. Making the PWM signal

In normal conditions, the inverter has to produce symmetrical three phase line-voltages. This is obtained when the inverter generates a space vector with a constant magnitude and a

constant angular velocity. Fig. 4.30 shows the possible states $\boldsymbol{U}_0$, $\boldsymbol{U}_1$, $\boldsymbol{U}_2$, … $\boldsymbol{U}_6$, $\boldsymbol{U}_7$ obtained with the inverter and the trajectory of the rotating space-vector $u(t) = 0.8\ U_{in}\ e^{j\omega t}$ (with $U_{in} = \frac{2}{3} U_{DC}$) when the amplitude equals 80% of $\frac{2}{3} U_{DC}$.

With this figure, the PWM signal can be built. Suppose one needs to realize the space-vector $0.8U_{DC}e^{j\frac{2\pi}{9}}$ (when using a frequency of 50Hz, the time equals $2.22ms = \frac{20}{9}$ms ($\frac{2\pi}{9} rad = 40°$)). Considering Fig. 4.31, the space vector is located between state 1 ($\boldsymbol{U}_1$) and state 2 ($\boldsymbol{U}_2$). The space-vector will be build using only four states. The two zero inverter states (states $\boldsymbol{U}_0$ and $\boldsymbol{U}_7$) and the inverter states before and after the space vector ($\boldsymbol{U}_1$ and $\boldsymbol{U}_2$ in the present example) are used. In case the space vector is aligned with an inverter state, only three inverter states are needed. The space-vector $0.8\frac{2}{3} U_{DC} e^{j\frac{2\pi}{9}}$ will be built using the inverter states $\boldsymbol{U}_0$, $\boldsymbol{U}_1$, $\boldsymbol{U}_2$ and $\boldsymbol{U}_7$. The activation of every state is must be so that:

$$0.8\frac{2}{3} U_{DC} e^{j\frac{2\pi}{9}} = D_0 0 + D_1 \frac{2}{3} U_{DC} e^{j0} + D_2 \frac{2}{3} U_{DC} e^{j\frac{\pi}{3}} + D_7 0 \begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} u_{a0} \\ u_{b0} \\ u_{c0} \end{bmatrix}, \quad (4\text{-}26)$$

where $1 = D_0 + D_1 + D_2 + D_7$.

By splitting the problem in a real and an imaginary part, where the real axis is aligned with one of the used inverter states, and dividing both parts with $\frac{2}{3} U_{DC}$ this problem becomes:

$$\begin{bmatrix} 0.8\cos\left(\frac{2\pi}{9}\right) \\ 0.8\sin\left(\frac{2\pi}{9}\right) \end{bmatrix} = 0 + \begin{bmatrix} D_1 \\ 0 \end{bmatrix} + \begin{bmatrix} D_2\cos\left(\frac{\pi}{3}\right) \\ D_2\sin\left(\frac{\pi}{3}\right) \end{bmatrix} + 0 \begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} u_{a0} \\ u_{b0} \\ u_{c0} \end{bmatrix} \quad (4\text{-}27)$$

Which gives a solution for D_1 and D_2 (D_1=0.316 D_2=0.593) and allows to calculate D_0 and D_7. As these states both represent a zero state and to obtain a symmetrical state, on chooses $D_0 = D_7 = \frac{D_z}{2}$. More precisely,

$$1 = D_0 + D_1 + D_2 + D_7 = D_z + D_1 + D_2 \begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} u_{a0} \\ u_{b0} \\ u_{c0} \end{bmatrix} \quad (4\text{-}28)$$

$1 = D_0 + D_1 + D_2 + D_7 = D_z + D_1 + D_2$ so $D_z = 1 - D_1 - D_2$.

These variables represent the duty cycles of the active states.

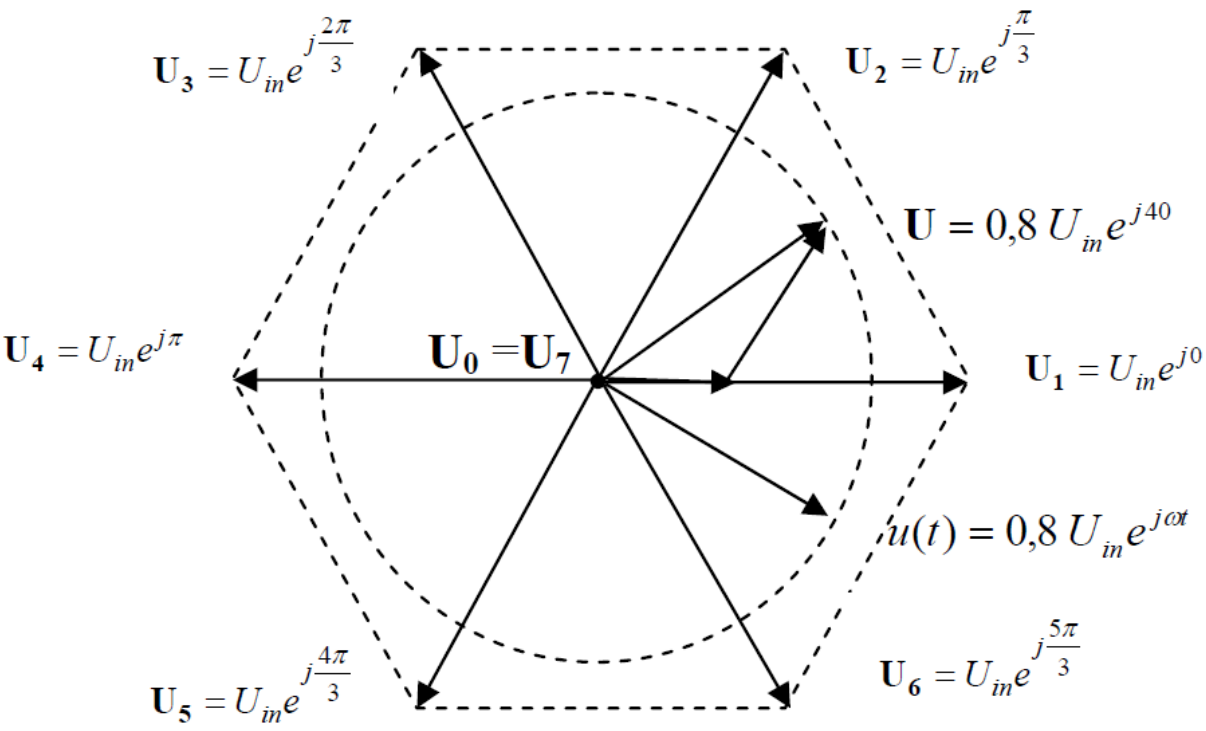


Fig. 4.31. The space-vector states of the inverter and the space-vector trajectory of the desired three phase voltage (Van Craenenbroeck)

The duration of one sample period depends on the discrete time step T_{PWM} where the time point of the calculation (in this case 2.22ms or $\frac{2\pi}{9} rad$) is in the middle of the sample period. This means that the period T_{PWM} is a degree of freedom which can be chosen freely, as long as it is larger than the needed calculation time with some reserve and larger than the minimum allowed switching period $\left(\frac{1}{f_{smax}}\right)$. The smaller is the period T_{PWM}, the higher is the harmonic order, meaning easier to filter, but the higher the switching losses. During the time period T_{PWM} the shape of the next time periode T_{PWM} is calculated for the time point at the middle of the next time period. One of the most common switching sequences, to realize a space-vector located between U_1 and U_2 which minimizes the number of switching operations and returns to its original state, is:

Table 4-6: The number of switching operations

State 0	$T_{PWM}\, D_z/4$	IGBT 2	IGBT 4	IGBT 6
State 1	$T_{PWM}\, D_1/2$	IGBT 1	IGBT 4	IGBT 6
State 2	$T_{PWM}\, D_2/2$	IGBT 1	IGBT 3	IGBT 6
State 7	$T_{PWM}\, D_z/2$	IGBT 1	IGBT 3	IGBT 5
State 2	$T_{PWM}\, D_2/2$	IGBT 1	IGBT 3	IGBT 6
State 1	$T_{PWM}\, D_1/2$	IGBT 1	IGBT 4	IGBT 6
State 0	$T_{PWM}\, D_z/4$	IGBT 2	IGBT 4	IGBT 6

Notice that only one bridge has to switch to go from the previous state to the next state. This property is not only obtained in the present case. When two non-zero inverter states are used, this advantage can always been obtained which can be verified using Table 4-6. Fig.4.32 shows a typical shape of a symmetrical sample period T_{PWM} of the PWM signal.

This symmetry, especially the quarter-wave symmetry, has some advantages in order to reduce the unwanted harmonics. The quarter-wave symmetry makes sure the even harmonics do not occur. This reduction of the harmonics in combination with a reduction of the switching frequency implies that space-vector modulation has a very high performance. To obtain a further reduction of the harmonics, the frequency modulation factor m_f should be a multiple of 6 since there are 6 sectors as visualized in Fig. 4.32, 4.33.

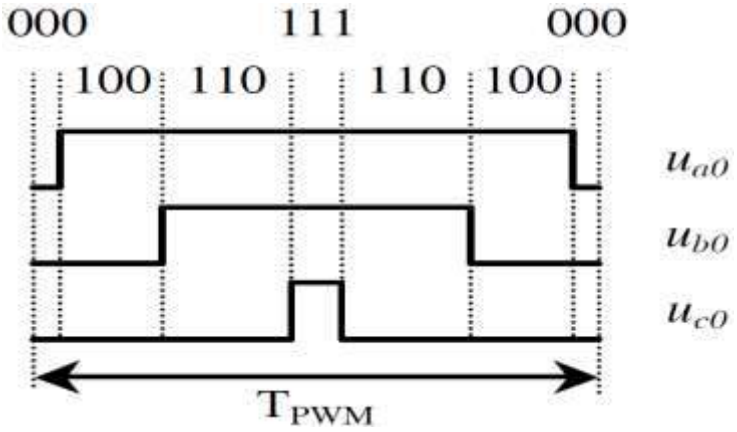


Fig. 4.32. PWM signal (TERÖRDE)

It is important to notice that the above approach is valid as long as the rotating space-vector does not leave the hexagon obtained by the six non-zero inverter states. This means the maximum RMS value of the fundamental of the line-voltage which can be offered by this modulation technique is $U_{ab} = \frac{\sqrt{3}}{\sqrt{2}}\hat{U}_{a0} = \frac{\sqrt{3}}{\sqrt{2}}\frac{\sqrt{3}}{2}\frac{2}{3}U_{DC} = \frac{U_{DC}}{\sqrt{2}}$. The maximum RMS value of the line-voltage without overmodulation which can be obtained using sinusoidal PWM is $U_{ab} = \frac{\sqrt{3}}{\sqrt{2}}\hat{U}_{a0} = \frac{\sqrt{3}}{\sqrt{2}\,2}U_{DC}$. This means that the RMS value of the line-voltage using space-vector modulation is about 15% higher than when using the sinusoidal PWM. When leaving this inner circle, over modulation appears as is shown in Fig. 4.32. :

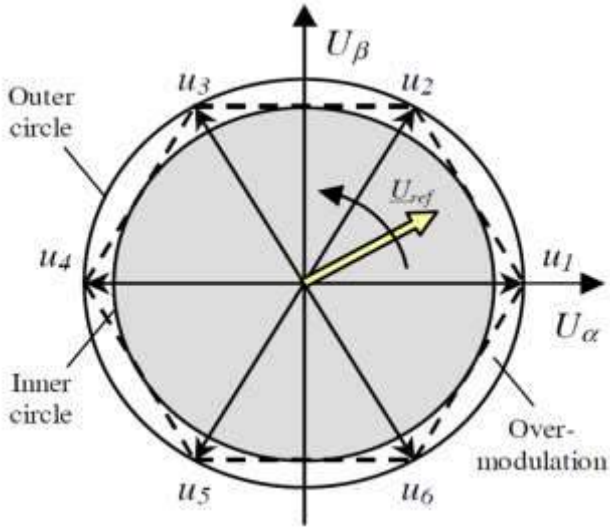


Fig. 4.33. When overmodulation occurs (TERÖRDE)

References

M.H. Rashid, Power Electronics Handbook, Elsevier – Academic Press, 2011.

G., TERÖRDE, Electrical Drives And Control Techniques, Leuven: ACCO, 2004

T. Van Craenenbroeck, J. Driesen, H04A2 Vermogenelektronica Cursustekst, Acco

4.5. CSI

Until now Voltage Source Inverters have been discussed. The input of such a VSI inverter is a constant DC voltage source and the VSI tries to obtain a sinusoidal voltage waveform. An alternative kind of inverters is the Current Source Inverters i.e. the CSI inverters. The input of such a CSI is a constant DC current source and the CSI tries to obtain a sinusoidal current waveform. The DC-link of a frequency converter contains a capacitor in case of a VSI and contains an inductor in case of a CSI.

The CSI must be able to control the magnitude, the frequency and the phase of the output current. When feeding an inductive load, the CSI needs a capacitive filter at the AC-terminals in order to avoid high $\frac{di}{dt}$ values due to the switching strategy. Due to this capacitive filter (which is also shown in Fig. 4.34.), a load voltage with a very low THD (nearly an ideal sinusoidal voltage waveform) is obtained. Due to this reason, such a CSI is used in industrial medium-voltage applications where a low THD is required. The CSI mainly has the three-phase topology shown in Fig. 4.34..

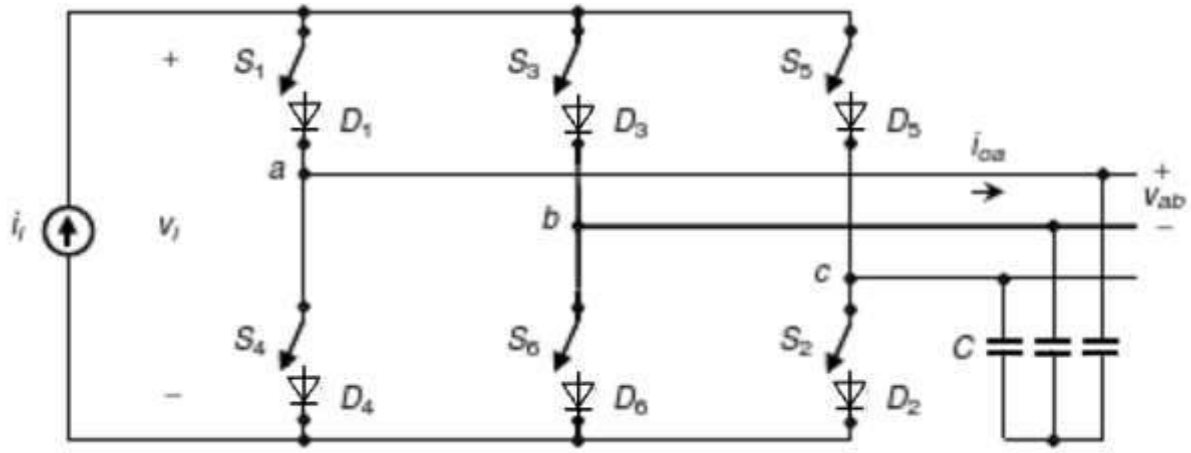


Fig. 4.34. Three-phase CSI topology

When considering the switching strategy, a few basic considerations are important. On the DC side, there is current source (an inductor) which may never encounter an open circuit. This means at least one of the switches at the top (S_1, S_3 or S_5) must be closed and at least one of the switches at the bottom (S_2, S_4 or S_6) must be closed. To avoid a short circuit of capacitors at the AC side, at most one top switch and at most one bottom switch should be closed at the same time.

This implies always one single top switch and one single bottom switch should be closed, which gives rise to 9 valid states in the three-phase CSI. Table 4-7 gives these 9 valid states. States 7 to 9 produce AC line currents which all equal zero. Indeed, in these states the DC

current source is short-circuited using bridge 1 (containing S_1 and S_4), bridge 2 (containing S_3 and S_6) or bridge 3 (containing S_2 and S_5).

Table 4-7: Valid switching states for a three-phase CSI

State	S_1	S_2	S_3	S_4	S_5	S_6	i_{0a}	i_{0b}	i_{0c}
1	1	1	0	0	0	0	i_i	0	$-i_i$
2	0	1	1	0	0	0	0	i_i	$-i_i$
3	0	0	1	1	0	0	$-i_i$	i_i	0
4	0	0	0	1	1	0	$-i_i$	0	i_i
5	0	0	0	0	1	1	0	$-i_i$	i_i
6	1	0	0	0	0	1	i_i	$-i_i$	0
7	1	0	0	1	0	0	0	0	0
8	0	0	1	0	0	1	0	0	0
9	0	1	0	0	1	0	0	0	0

By switching between these states, the line currents (between the output of the inverter and the capacitive filter) are switching between the discrete values i_i, 0 and $-i_i$ (i_i is the DC current obtained by the DC-link). By selecting the correct states in an appropriate order, a proper PWM waveform is obtained. Similar with the VSI approach, also when realizing a CSI there are several modulation techniques. The most used techniques are carrier-based techniques (PWM, with or without a third order harmonic) and space-vector modulation.

Although these modulation techniques are very similar with the techniques used with the VSI approach, some changes are introduced to satisfy the special requirements of the CSI approach. These modulation techniques for CSI will not be discussed in the present chapter.

References

M.H. Rashid, Power Electronics Handbook, Elsevier – Academic Press, 2011.

G. Merlevede, Vermogenelektronica, Acco

4.6. Voltage source based multilevel topologies

Introduction

The multilevel inverters allow improving the shape of the sinusoidal output signal i.e. to improve the THD of this output signal. The three-phase two-level VSI inverters have already been studied and they contain six switches. Such an inverter is called a two-level VSI because the output voltage can take the values of $\frac{V_{dc}}{2}$ and $-\frac{V_{dc}}{2}$ or V_{dc} and zero depending on the reference point. The output voltage of a bridge can take one of two different voltage levels.

In a multilevel inverter, the output voltage of a bridge can take one of N different voltage levels. Fig. 4.35., shows a three-phase three-level VSI inverter. This means that the output voltage of a bridge can take one of three different voltage levels, i.e. $\frac{V_{dc}}{2}$ or $-\frac{V_{dc}}{2}$ or zero. This already reveals the largest problem of the multilevel inverter. To obtain a three phase two-level VSI only six switches are needed whereas for a three phase three-level VSI inverter

twelve switches and 18 diodes are needed. This higher number of switches increases the cost and the complexity of the switching strategy. The question arises what pattern is needed to activate these switches in a correct way.

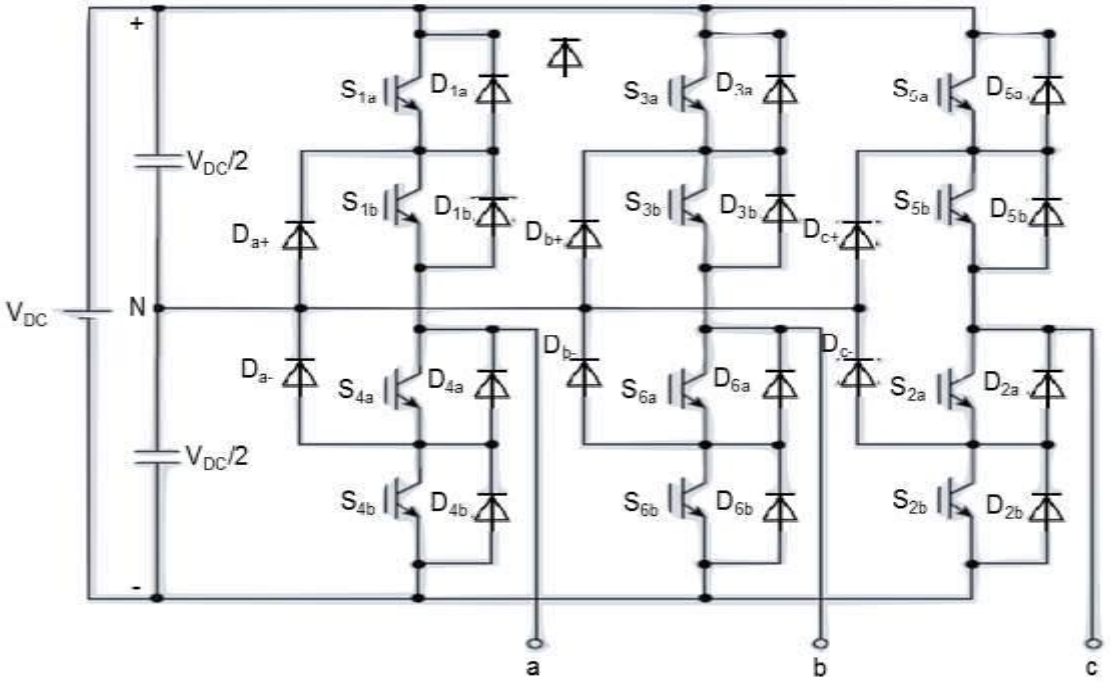


Fig. 4.35. Three-phase three-level inverter topology

First, the valid switching states of this three-level VSI will be checked for bridge a. Because there are three possible voltage output levels, this will lead to three valid switching states, as shown in Table . The bridge contains four switches (S_{1a}, S_{1b}, S_{4a}, S_{4b}) which may never be closed simultaneously in order to prevent a short circuit. To prevent an undefined output voltage state, these four switches may never be opened simultaneously. Analyzing Fig. 4.35. and ignoring the undefined voltage states (the states where S_{1b} and S_{4a} are both open), Table is obtained.

Table 4-8: The valid switching states for a three-level VSI, bridge a

S_{1a}	S_{1b}	S_{4a}	S_{4b}	v_{aN}	Conducting components	Condition
1	1	0	0	$V_{DC/2}$	S_{1a} and S_{1b}	if $i_a > 0$
					D_{1a} and D_{1b}	if $i_a < 0$
0	1	1	0	0	D_{a+} and S_{1b}	if $i_a > 0$
					D_{a-} and S_{4a}	if $i_a < 0$
0	0	1	1	$-V_{DC/2}$	D_{4a} and D_{4b}	if $i_a > 0$
					S_{4a} and S_{4b}	if $i_a < 0$

It is important to notice that the state of S_{1a} is always complementary with the state of S_{4a} and that the state of S_{1b} is always complementary with the state of S_{4b}. The same conclusions can be obtained for bridge b and bridge c, which can be controlled independently because they are mounted in parallel. With the valid switching states is mind, the different control strategies can be discussed.

4.6.1. The sinusoidal PWM technique for three-level VSI

Because this is a three-phase inverter, only the unipolar switching strategy can be used. This means three different sets of control signals are needed in order to obtain the three different output voltages. This implies the explanation can be focused on one single bridge because the other two bridges work similarly each having their own control signals.

There are three valid states, as defined in Table 4-8, which give the output voltages $\frac{V_{dc}}{2}$ or $-\frac{V_{dc}}{2}$ or zero. When considering an ideal sinusoidal waveform (Fig. 4.36.), one can come to the conclusion that only the levels $\frac{V_{dc}}{2}$ and zero are important in the first half period to obtain the optimal PWM-signal. In the second half period, only the levels $-\frac{V_{dc}}{2}$ and zero are important.

In the first half period, the voltage of the sinusoidal waveform is between zero and $\frac{V_{dc}}{2}$ so only these two levels are needed to obtain the correct PWM-signal. In the second half period, the voltage of the sinusoidal waveform is between zero and $-\frac{V_{dc}}{2}$ so only these two levels are needed to obtain the correct PWM-signal. It is not possible to obtain this entire sinusoidal signal using only one single carrier i.e. a second carrier is needed. Both carriers are triangular waveforms having the same peak to peak value $\frac{V_{dc}}{2}$. The best result is obtained when these carriers are in phase and when they have an odd frequency-modulation ratio m_f (the frequency of the carrier is m_f times higher than the frequency of the control signal). Between the carriers, there is an offset of $\frac{V_{dc}}{2}$.

Switch S_{1a} has to be closed, when the control signal v_{ca} is higher than the upper carrier $v_{\Delta 1}$. Switch S_{1b} has to be closed when the control signal v_{ca} is higher than the lower carrier $v_{\Delta 2}$. When v_{ca} is lower than the lower carrier $v_{\Delta 2}$, switch S_{4b} has to be closed and Table shows that S_{1b} is open when S_{4b} is closed (and S_{1b} is closed when S_{4b} is open). The same approach can be used for S_{4a}. Because S_{4a} is open when S_{1a} is closed (and S_{4a} is closed when S_{1a} is open), S_{4a} is closed when the control signal v_{ca} is lower than the upper carrier $v_{\Delta 1}$. This approach is visualized in Fig. 4.37.

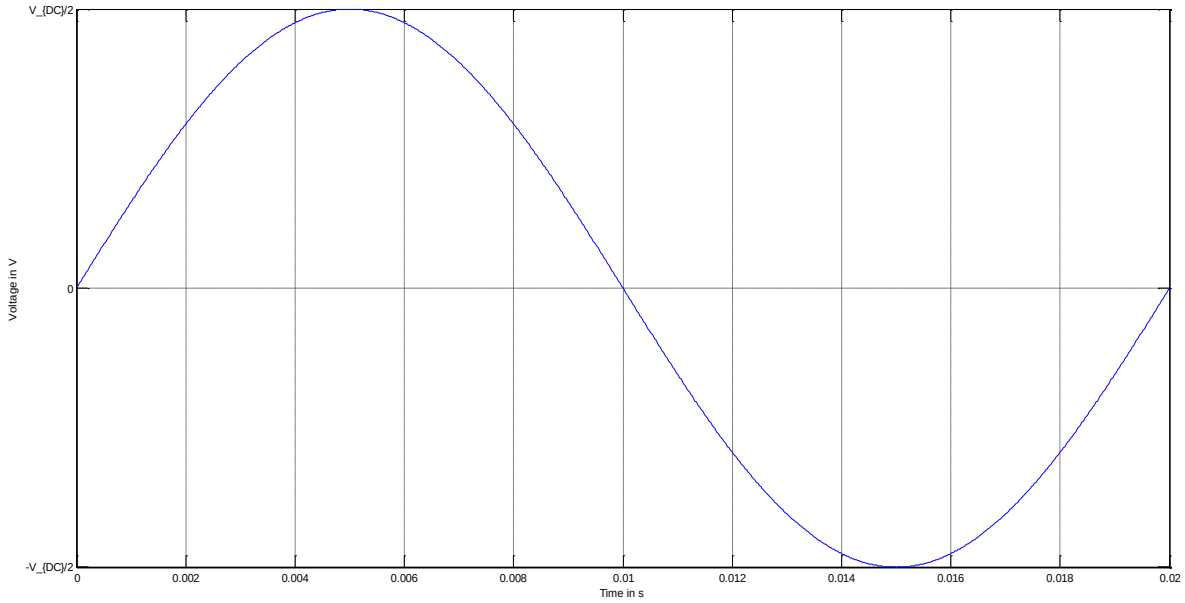


Fig. 4.36. Ideal sinusoidal wave

In order to use the same two carrier signals for bridges b and c, m_f should be an integer multiple of three. The bridge voltage (Fig. 4.37. d) switches only between zero and $V_{dc}/2$ or between zero and $-V_{dc}/2$ which reduces the Total Harmonic Distortion. The spectrum of the output voltage is visualized in Fig. 4.37. e, only harmonic orders which equal $h = l\, m_f \pm k$ occur (where l is even when k is odd and vice versa). The homopolar components disappear in the line voltage, Fig. 4.37. g. All the other features of the carrier-based PWM technique also occur in the multilevel inverter. The fundamental of the phase voltage has a peak value which equals $\hat{v}_{aN1} = m_a \frac{V_{dc}}{2} = \hat{v}_{bN1} = \hat{v}_{cN1}$ and the peak value of the fundamental of the line voltage is $\sqrt{3}$ times larger. The linear operating region applies when $m_a \leq 1$. When $1 < m_a < \frac{4}{\pi}$, overmodulation occurs and in case $m_a = \frac{4}{\pi}$ a square wave is obtained.

Instead of using sinusoidal PWM, an additional third (or a multiple of three) order harmonic can be added to the control signal. This allows to extend the linear operating region until $m_a = 1.15$. These multilevel inverters can be used as inverters to provide energy from the DC-link to the load by generating a sinusoidal line voltage. They can also be used as an active filter (generating non-sinusoidal signals).

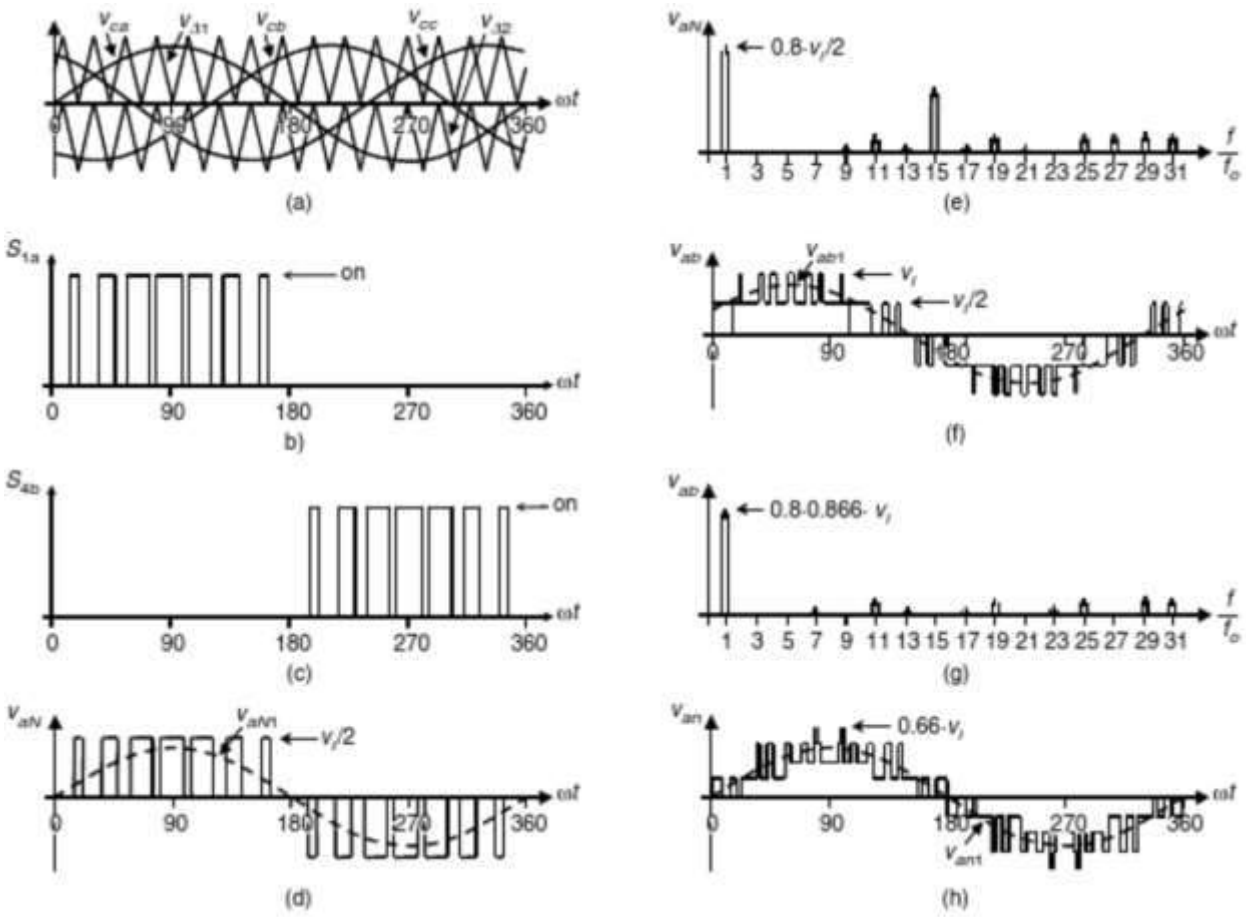


Fig. 4.37. Three-level VSI topology. Relevant waveforms using a sinusoidal PWM (m_f=15, m_a=0.8): modulating and carrier signals (a); switch S_{1a} status (b); switch S_{4b} status (c); inverter phase a voltages (d); inverter phase a voltage spectrum (e); load line voltage (f); load line voltage spectrum (g); load phase a voltage (h)

4.6.2. The sinusoidal PWM technique for N-level VSI

As this is a three-phase inverter, only the unipolar switching strategy can be used. This means three different sets of control signals are needed in order to obtain the three different output voltages. This implies the explanation can be focused on one single bridge because the other two bridges work similarly each having their own control signals.

There are N valid states, which give the output voltages $\frac{V_{dc}}{2} - z\frac{V_{dc}}{N-1}$ for $z = 0 : N-1$. The instantaneous value of the PWM signal always equals the discrete voltage level above or below the ideal instantaneous voltage level. To obtain this N-level PWM signal, N-1 carriers are needed. These carriers are triangular waveforms each having the same peak to peak value $\frac{V_{dc}}{N-1}$. The best result is obtained when these carriers are in phase and when they have an odd frequency-modulation ratio m_f (the frequency of the carrier is m_f times higher than the frequency of the control signal). Between the carriers, there is an offset of $\frac{V_{dc}}{N-1}$.

The higher is the number of levels (N), the lower is the Total Harmonic Distortion of the output voltage. One of the drawbacks of the multilevel inverter is the DC-link. In order to obtain N output levels, N-1 equal capacitors are needed. Not only these equal capacitors are

needed, but more precisely the voltage drops across these capacitors should be the same. Due to the fact (multi)-level inverters do not require a symmetrical current in the DC-link, the DC-voltage is not equally divided across the capacitors.

4.6.3. Space-vector modulation in three-level VSI

The multilevel inverters are also controllable using digital techniques implying also the space-vector modulation technique is an option. Actually the control strategy does not change, the reference phasor is built using the non-zero inverter states. These non-zero inverter states form the boundary of the sector in which the reference phasor is located at that moment (completed with the zero-inverter states).

The difference is associated with the number of inverter states. When considering the two-level inverter, there are eight (2^3) inverter states and in a three-level there are 27 (3^3) inverter states. In a two-level inverter, each leg has two possible voltage levels and there are three legs. In a three-level inverter, each leg has three possible voltage levels and there are three legs. In a N-level inverter, each leg has N possible voltage levels and there are three legs implying N^3 inverter states.

The number of inverter states will increase the complexity, because some inverter states will produce the same load-voltage terminals v_{13} and v_{14} (Fig. 4.38..). The algorithm will have to deal with this kind of complexity by using a number of additional criteria. This complexity increases with the number of voltages levels and the additional benefits are not evident. Due to this additional complexity, the maximum number of levels used in practical applications equals 5. Using these 5 levels gives the best performance between complexity and the benefits when considering the resulting waveforms.

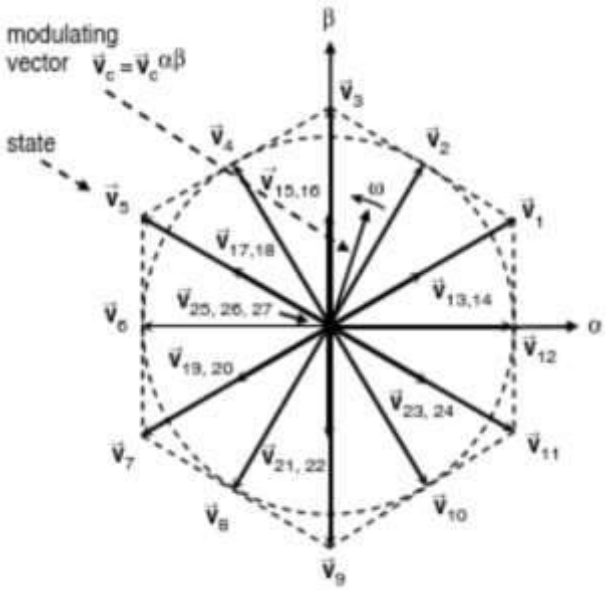


Fig. 4.38. Space vector modulation in a three-level VSI

References

M.H. Rashid, Power Electronics Handbook, Elsevier – Academic Press, 2011.

5. Matrix Converters

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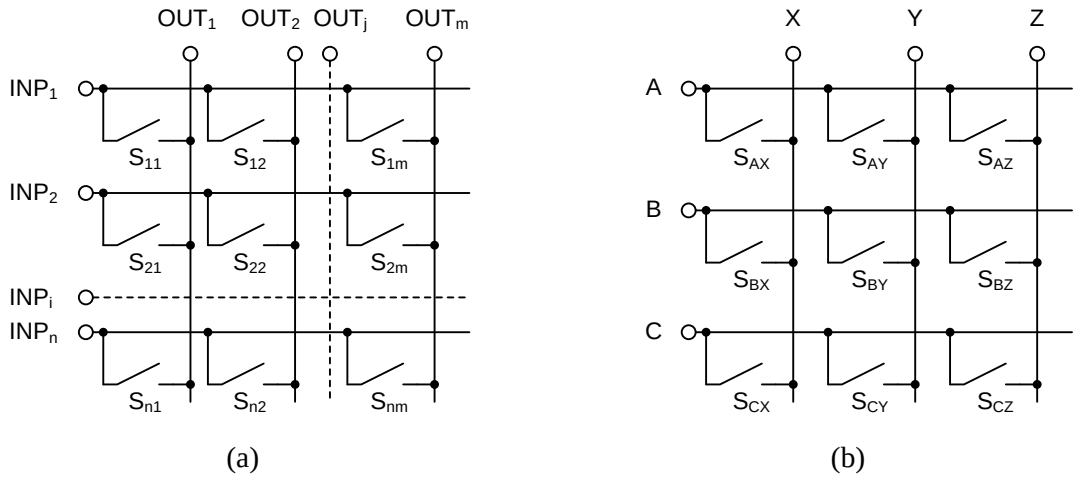
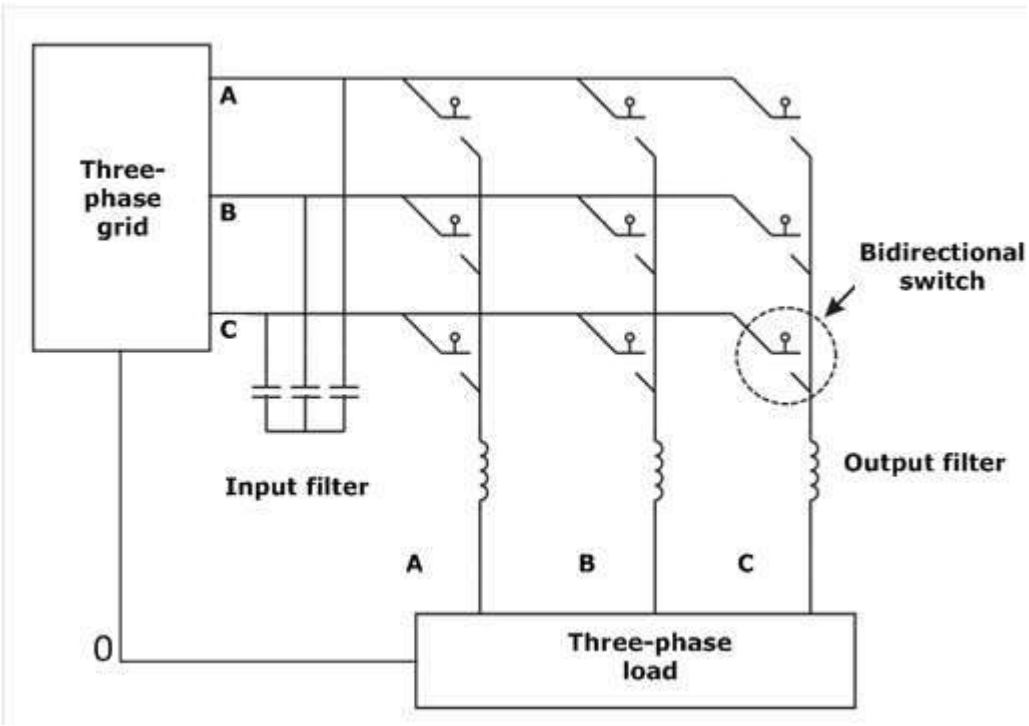
5.1. Configuration of Matrix Converters

Matrix converter is a kind of cycloconverters that is just an array of bidirectional electronic switches connecting each input of the converter to each output. If there are (m) outputs and (n) inputs, then they can be connected one to another, and matrix of connections can be formed. Each connection is made via electronic switch containing two transistors. The full matrix contains n×m switches.



(a) (b)



(c)

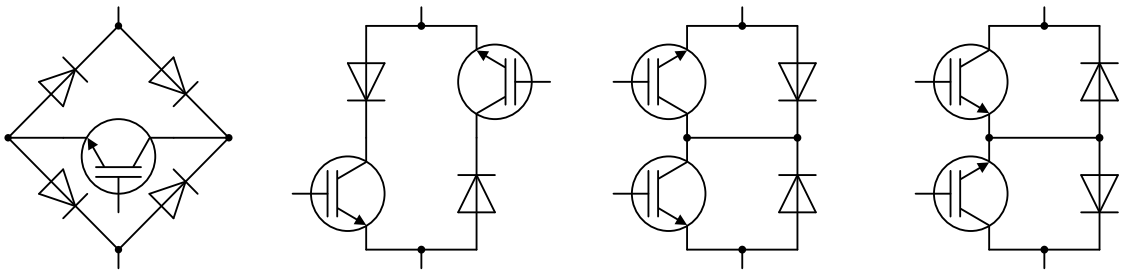
Fig. 5.1. Electrical diagram of the matrix converters: generalized diagram (a); converter with a 3-phase input and a 3-phase output (b); operation of the matrix converter (c)

Generalized matrix converter (MC) with m outputs and n inputs is given in Fig. 5.1.(a). Since usually load has three phases, but supply network has three lines, then the most useful MC has 3×3 structure and contains 9 switches, Fig. 5.1.(b). In reality MC operates with

voltage sources on one side and current sources on the other side. The first side is equipped with a voltage filter, but the other one – with current filter – Fig. 5.1.(c).

Some features of MCs are obvious from their topology. Since there are only three input curves in the 3×3 MC, then it is rather difficult to perform amplitude and phase synthesis as it common for other cycloconverters. However, these voltages give quite good basis for PWM. Since there are three voltages, then two or even three level PWM can be performed on MC, not one level like in the case of VSI. Since input phases can be almost arbitrary loaded, then MCs have also better input parameters. In other words, PWM of the input currents, based on the output currents can also be done in the MCs within the same modulation cycle. Besides that universal MCs are equivalent for both directions of energy flow.

5.2. Electronic Switches



(a) (b) (c) (d)

Fig. 5.2. Electronic switches: bridge (a); enhanced back-to-back (b); common collector (c); common emitter (d)

Choice of the control methods that are suitable for concrete MC and especially commutation technique depends on the construction of electronic switches (ESs) that are used in the power circuit. Since there are no completely developed fully controllable power semiconductor devices with symmetrical VA curve some combination of the components should used instead. The whole variety of different ESs is based on the two basic topologies of the circuit: ESs that are based on the diode bridge and counter parallel (back-to-back) connection.

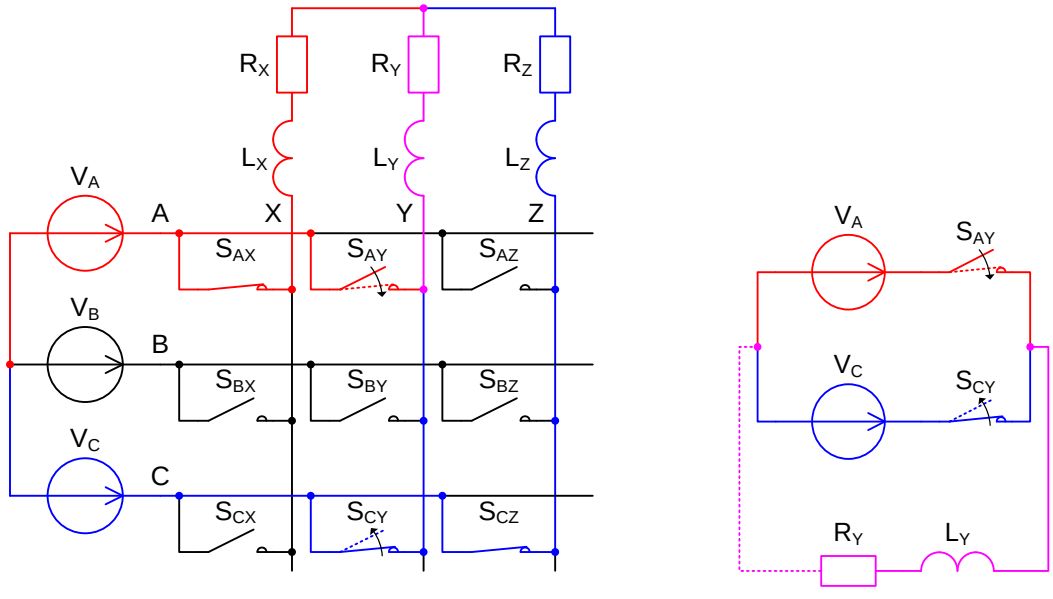
Switches of the first group are given in Fig. 5.2.(a). As it can be seen such ESs contain one phase diode bridge and switching element between “plus” and “minus” terminals of this bridge. ES is able to conduct current of any polarity between AC terminals while the switching element is “on”. Otherwise switch conducts no current. The switching is usually some transistor (for example MOSFET, BJT or IGBT). The most attractive feature of the bridge circuit is minimal number of controllable devices and, hence, smaller overall cost. Such switch is controlled by only one signal and it is another positive feature of this circuit. At the same time, since current flows through the three semiconductor elements – controllable device and two diodes, such circuit has higher on-state losses. Another disadvantage is the absence of the distinct back action component that makes safe commutation process less available.

Switches of the second group are shown in Fig. 5.2.(b), (c) and (d). Fig. 5.2.(b) shows back-to-back connection of the transistors the reverse capabilities of which are boosted by

auxiliary diodes. Two another circuits, Fig. 5.2.(c) and (d), are more realistic for implementation, since modern power semiconductor modules often contain both the transistor and reverse diode. Reverse voltage over the transistor in such circuit cannot be higher than few volts (voltage drop over the forward biased diode). Number of simultaneously conducting elements as well as power losses is also rather small (two elements – one transistor and one diode). The ES that is drawn in Fig. 5.2.(d) has an additional advantage of the common emitter. In the given case only one power supply is required for driver circuits of both transistors. Two controllable devices and, hence, two control signals are disadvantages of the given topology. However, each of these switches may act as forward device or as reverse element (depending on the voltage polarity), and thus makes safe commutation strategy possible.

5.3. Commutation of switches in MC

There are quite a large number of types of switching transients in MC. However, all this variety of switchings may be reduced to one type of the commutation: current in the output phase is being disconnected from one input voltage source and connected to another. For example, initial state of MC is XYZ=ACC, but the new state is XYZ=AAC. Hence, only output phase Y undergo switching from source VC to VA, Fig. 5.3.(a). Since two "static" phases (X and Z) composes the path for the current in the phase Y, then equivalent circuit of the switching can be drawn as in Fig. 5.3.(b). The practical circuit for further estimation by means of simulation and experimental investigation of the given type of the switching can be obtained if abstract switch is replaced by ES from Fig. 5.2.



(a) (b)

Fig. 5.3. Switching transient in the matrix converter: complete electrical diagram (a); equivalent diagram for the switching SCY-SAY (b)

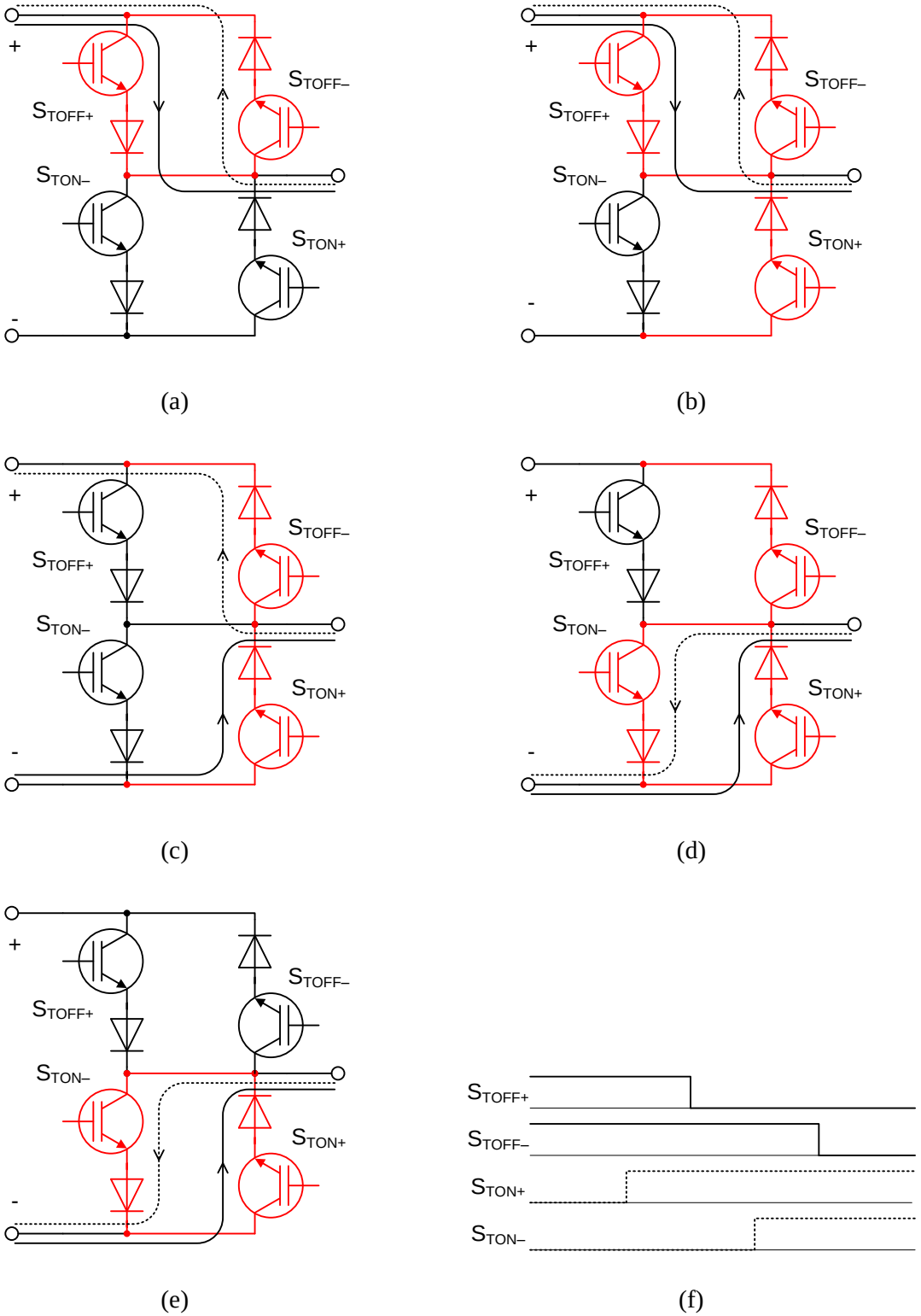


Fig. 5.4. Four step commutation sequence of MFC: output connected to the positive node (a); output voltage remains positive; an auxiliary switch between the load and the negative supply turned on by control, but accepts no current (b); voltage polarity depends on the current direction (c); voltage is negative; an extra switch between the positive supply and the load conducts no current (d); load connected to the negative supply. Activated devices - red, negative current – dotted (e); commutation diagram (f)

Switching strategy for MC may derived from those of VSI, if imitation of freewheeling diodes of VSI is done. It requires the polarity of input voltage to be known. The initial state of switched leg of MC is shown in Fig. 5.4.(a). Switching sequence in VSI starts when forward device of the leg (IGBT) goes off. After that, one of reverse diodes accepts load current. Since in MC all devices are controllable, then all reverse transistors must be in Fig. 5.4.(b) before outgoing forward device goes off Fig. 5.4.(c). Like in VSI, output voltage of MC is defined by load current, while only reverse devices are on. After certain time forward transistor of the incoming is leg turned in Fig. 5.4.(d). Since reverse device of outgoing leg conduct no current it can be switched off, Fig. 5.4.(e). Number of switchings is 4, and described process is assigned as four step commutation, Fig. 5.4.(f).

5.4. Control of MC

Control of MCs is PWM based. Since there are 9 switches in a typical MC it has 2^9=512 possible states, but only some of them are valid (Table 5-1), because the voltage sources on one side cannot be shortcircuited, but the current sources on the other – must have closed loops. This leads to 27 valid states of MC. Operation of MC is based on periodical switching between at least two of these states. In practice the number of MC states within 1 switching cycle is 3 or 5 (3 or 5 states of MC are utilized).

Table 5-1 : Valid states of the MC

N	**X=**	**Y=**	**Z=**	$\mathbf{V_{XY}}$	$\mathbf{V_{YZ}}$	$\mathbf{V_{ZX}}$
1	A	A	A	0	0	0
2	B	B	B	0	0	0
3	C	C	C	0	0	0
4	A	B	C	V_{AB}	V_{BC}	V_{CA}
5	A	C	B	$-V_{CA}$	$-V_{BC}$	$-V_{AB}$
6	B	A	C	$-V_{AB}$	$-V_{CA}$	$-V_{BC}$
7	B	C	A	V_{BC}	V_{CA}	V_{AB}
8	C	A	B	V_{CA}	V_{AB}	V_{BC}
9	C	B	A	$-V_{BC}$	$-V_{AB}$	$-V_{CA}$
10	A	B	B	V_{AB}	0	$-V_{AB}$
11	B	A	A	$-V_{AB}$	0	V_{AB}
12	B	C	C	V_{BC}	0	$-V_{BC}$
13	C	B	B	$-V_{BC}$	0	V_{BC}
14	C	A	A	V_{CA}	0	$-V_{CA}$
15	A	C	C	$-V_{CA}$	0	V_{CA}
16	B	A	B	$-V_{AB}$	V_{AB}	0
17	A	B	A	V_{AB}	$-V_{AB}$	0
18	C	B	C	$-V_{BC}$	V_{BC}	0
19	B	C	B	V_{BC}	$-V_{BC}$	0
20	A	C	A	$-V_{CA}$	V_{CA}	0
21	C	A	C	V_{CA}	$-V_{CA}$	0
22	B	B	A	0	$-V_{AB}$	V_{AB}
23	A	A	B	0	V_{AB}	$-V_{AB}$
24	C	C	B	0	$-V_{BC}$	V_{BC}
25	B	B	C	0	V_{BC}	$-V_{BC}$
26	A	A	C	0	$-V_{CA}$	V_{CA}
27	C	C	A	0	V_{CA}	$-V_{CA}$

For each switch it is possible to compose a switching function, defined as:

$$S_{Kj} = \begin{cases} 1, \textit{ switch } S_{Kj} \textit{ closed} \\ 0, \textit{ switch } S_{Kj} \textit{ open} \end{cases} \quad K = \{A, B, C\},\ j = \{a, b, c\}\ , \tag{5-1}$$

but taking into account state limitations it is possible to state

$$S_{Aj} + S_{Bj} + S_{Cj} = 1,\ \ j = \{a, b, c\}\ . \tag{5-2}$$

For MC analysis voltages are usually regarded as vectors:

$$\mathbf{v}_o = \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \text{ and } \mathbf{v_i} = \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix}. \tag{5-3}$$

Then the relationship of these voltages can be expressed as:

$$\mathbf{v_0} = \mathbf{T} \cdot \mathbf{v_i} = \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} S_{Aa}(t) & S_{Ba}(t) & S_{Ca}(t) \\ S_{Ab}(t) & S_{Bb}(t) & S_{Cb}(t) \\ S_{Ac}(t) & S_{Bc}(t) & S_{Cc}(t) \end{bmatrix} \times \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix}. \tag{5-4}$$

where T is a switching matrix, which is composed of switching states.

Currents can also be expressed as vectors

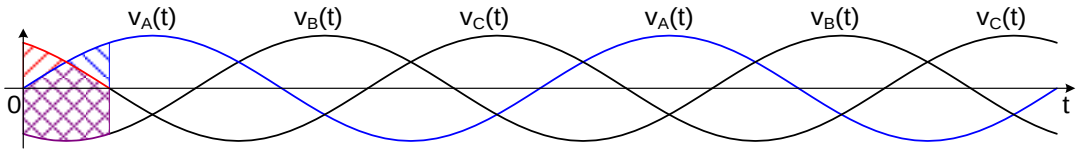
$$\mathbf{i_i} = \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \text{ and } \mathbf{i_o} = \begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix}. \tag{5-5}$$

Then their relationship is

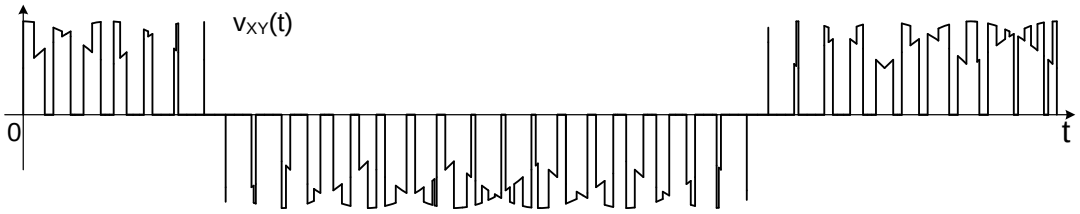
$$\mathbf{i_i} = \mathbf{T^T} \cdot \mathbf{i_o}\ , \tag{5-6}$$

where T^T is transposed T.

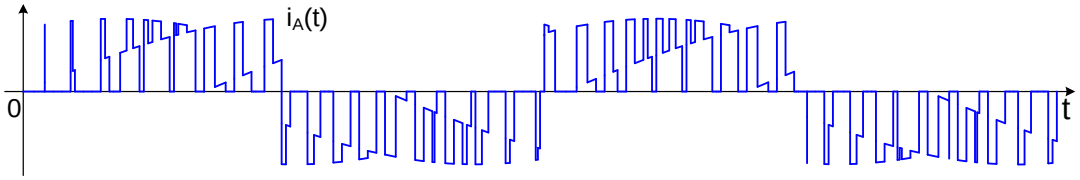
Equations (5-4) and (5-6) provide generalized instantaneous relationships between input and output parameters. Possible output voltage and input current that can be calculated with these equations are given in Fig. 5.5.



(a)



(b)



(c)

Fig. 5.5. Input and output variables of the MC: input voltage set (a);
output voltage $v_{XY}(t)$ (b); input current $i_A(t)$ (c)

6. Snubber Circuits and Soft-Switching Converters

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6.1. Switching Trajectory

6.1.1. The Really Operation Conditions of a Switch in Converter Scheme

Let us discuss operation of the transistor switch in the scheme Fig. 6.1 where the transistor VT is periodically connecting and disconnecting a resistive-inductive load to the DC supply source with voltage U_s . The load current is clamped with diode V and to the gate of transistor VT periodically control gate voltage turning-on the transistor is applied arising in such way a load current which is accepted as smoothed one I_{ld}.

When a control gate voltage u_{GE} is not applied the transistor is turned-off and the load current is passing through the clamp diode V. After rising of gate voltage and some turn-on process delay time $t_{d(on)}$ rising of a collector current i_c starts and simultaneously decreasing of current i_v of the clamp diode. Time interval in which transistor's collector current reaches the 90% level of load current is named as the « rise time » t_r and collector current in it changes as

$$i_{cr} = I_{ld}\frac{t}{t_r} \qquad 0 \le t \le t_r \ . \tag{6-1}$$

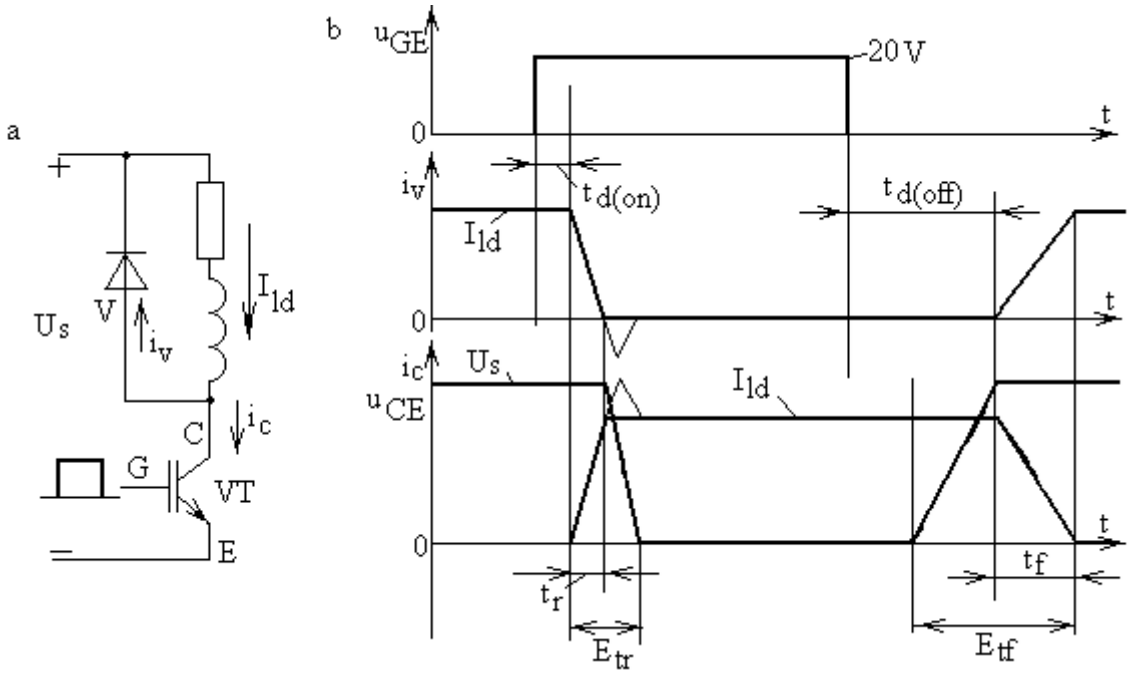

Fig. 6.1. Scheme (a) for description of the really switching process of transistor in DC circuit with load clamped with diode and according diagrams of processes (b)

In the interval the diode conducts current and its voltage drop is practically zero, i.e., collector-emitter voltage of the transistor $u_{CEr}=U_s$. When current of the diode becomes equal to zero then decreasing a voltage between the transistor's collector-emitter u_{CE} to zero level starts and this process practically lasts as long as the rise time (really this voltage decrease time interval in handbooks is not properly accounted):

$$u_{CEr} = U_s(1-\frac{t}{t_r}) \qquad 0 \le t \le t_r \ . \tag{6-2}$$

If the diode is accepted as an ideal device in respect to its dynamic process then energy losses for the turning-on process are

$$E_{tr} = U_s \int_0^{t_r} I_{ld} \frac{t}{t_r} dt + I_{ld} \int_0^{t_r} U_s(1-\frac{t}{t_r})dt = I_{ld}U_s t_r \, . \tag{6-3}$$

After nullification of the gate voltage of the transistor a rising of collector voltage of the transistor starts and length of this process is about interval t_f – current fall time – which really regards to the current decreasing interval to 10% level of the load current. When collector voltage is rising the current of the transistor is equal to I_{ld}. Again it can be noted that voltage rise time interval is not properly accounted in data-sheets. After turning-off delay time $t_{d(off)}$ the voltage across transistor becomes equal to the source U_s value and diode V starts to conduct rising current i_v but collector current i_c is decreasing and this process lasts for t_f. Totally energy losses in turning-off process are

$$E_{tf} = I_{ld}U_s t_f \ . \tag{6-4}$$

The summary switching transient energy losses in one switching cycle are

$$E_{tsw} = E_{tr} + E_{tf} = I_{ld}U_s(t_r + t_f) \ . \tag{6-5}$$

Power losses in switching transient processes – commutation losses - can be calculated as

$$\Delta P_{tsw} = E_{tsw} \cdot f \quad , \tag{6-6}$$

where f is switching frequency.

Calculation example.

The rise time for IGBT transistor is t_r=50ns, but its fall time is t_f=400ns. Load current in system with clamping diode is 50A, voltage of supply source – 600V. Obtain commutation power losses at switching frequency 4 kHz !

1 – commutation energy losses in one switching cycle

$$E_{tsw} = 50 \cdot 600(50+400) \cdot 10^{-9} = 13.5mJ.$$

2 – commutation power losses

$$\Delta P_{tsw} = E_{tsw} \cdot f = \frac{13.5}{10^3} \cdot 4 \cdot 10^3 = 54W \ .$$

All the above mentioned refers to the case when clamp diode is an ideal device. Really it is not so for at changing of voltage polarity across diode from according to conductivity situation to the reverse biasing one, due to storage of majority carrier's charges in the opposite conductivity layers of diode, at voltage polarity changing instant these carriers are returning to the original conductivity layers and for short time interval – recovery time t_{rec} -diode is conducting current in full extent in the reverse direction. This Recovery Charge has a certain

value which depends on quality of diode – the higher it is the lower is the recovery charge Q_{rec}.

Taking into account this dynamic property of the diode it is clear that transistor's collector current is rising in recovery time t_{rec} above the value of load current (Fig. 6.1.) and such situation increases the losses of transistor.

The really peak value of transistor current i_c depends on current rise speed in the rise time, i.e., on I_{ld}/t_r . Accepting the triangular shape of the reverse current of the clamp diode the rise time of the current will be

$$t_1 = \frac{Q_{rec}.2t_r}{I_{ld}.t_{rec}} \tag{6-7}$$

and the peak value of transistor's collector current

$$I_{VT\max} = I_{ld}\left(1+\frac{t_1}{t_r}\right) = I_{ld} + \frac{2Q_{rec}}{t_{rec}} \ . \tag{6-8}$$

Calculation example.

A clamp diode is with rather good indicators – Q_{rec}=1 μC, t_{rec}=0.1 μs. Load current is 50A, rise time of transistor t_r=50ns. Calculate the peak amplitude of collector current at turn-on process!

1 – the extra interval of current rise over I_{ld} level

$$t_1 = \frac{1\cdot 2\cdot 50\cdot 10^6}{10^6\cdot 10^9\cdot 50\cdot 0.1} = 20\cdot 10^{-9}s \quad ;$$

2 – anticipated the peak amplitude of the collector current

$$I_{VT\max} = 50 + \frac{2\cdot 1\cdot 10^6}{10^6\cdot 0.1} = 70A \ .$$

Summary turn-on energy losses have to rise for

$$\Delta E_{t(rec)} = 0.5(I_{ld} + I_{VT\max})U_s\cdot t_1 \ , \tag{6-9}$$

and if U_s=600V then $\Delta E_{t(rec)} = 0.72mJ$. Compare of it with the results of the previous calculation example gives an overview that the later loss is about half of energy losses for the rise time. It can be seen that quality of clamp diodes is of special significance.

The total power losses of transistor depend also on conductivity losses which can be calculated using collector current I_c for continuous conductivity interval and voltage drop across it between collector and emitter which is a function of I_c. Duty ratio D of switch – relation of on-duty cycle to the switching cycle - also have to be accounted and then

$$\Delta P_{tD} = I_c\cdot U_{CE}(I_c)\cdot D + E_{tsw}(I_c)\cdot f \ . \tag{6-10}$$

Calculation example.

Calculate power losses of transistor of the rated current 70A if its collector current is 50A collector voltage at it U_{CE}(50)=1.8V, switching frequency is f=4kHz, duty ratio D=0.5,

voltage of supply 800V but switching transient intervals are t_r=50ns, t_f=500ns! A clamp diode for load is an ideal one. Obtain also over-temperature of transistor's structure if thermal resistance between structure and heat sinker is $R_{th(js)}$=0.9 ^{0}C/W!

1 – the conductivity losses

$$\Delta P_{cD} = I_c \cdot U_{CE}(I_c) \cdot D = 50 \cdot 1.8 \cdot 0.5 = 45W \quad ;$$

2 – energy losses at switching transients

$$E_{tsw}(I_c) = U_s \cdot I_c \cdot (t_r + t_f) = 800 \cdot 50 \cdot 550 \cdot 10^{-9} = 22mJ \quad ;$$

3 – the summary power losses

$$\Delta P_{tD} = 45 + 22 \cdot 10^{-3} \cdot 4 \cdot 10^{3} = 133W \quad ;$$

4 – the over-temperature of the structure

$$\Delta\Theta = \Delta P_{tD}.R_{th(js)} = 119.7^0 C \quad .$$

That is rather high over-temperature and has to be applied measures for lowering of the losses. The described above switching process of the transistor switch regards to a so named "hard switching" one.

6.1.2. Safe Operating Area and switching process trajectory

On the base of the described switching processes they can be represented as it is shown in Fig. 6.2. In the first stage of turn-on process from point 1 to point 2 the process is ongoing at constant voltage and rising collector current. In the second stage of turn-on process from point 2 to point 3 a collector current is constant but collector voltage of transistor is decreasing practically to the zero value.

In the turn-off process the first stage of it is connected with rise of voltage to supply value U_s at constant collector current (from point 3 to point 2 of the Fig.6.2.). The second stage of the process proceeds with decreasing of collector current from point 2 to the point 1 at constant voltage U_s across collector-emitter terminals of transistor. Correspondingly the instantaneous power loss $u_{CE}.i_c$ is also changing in the structure of transistor reaching from zero values in the points 1 and 3 to the extreme maximum in the point 2 of the Fig. 6.2 when instantaneous power losses are $U_s.I_c$. If for instance U_s=800V but I_c=50A then in the point 2 power losses are 40kW. Such level of losses exists only for one instant and should not create large energy losses and essential heating of structure but nevertheless it should be desirable to move off of that trajectory in direction of smaller power losses (trajectory C in Fig. 6.2.).

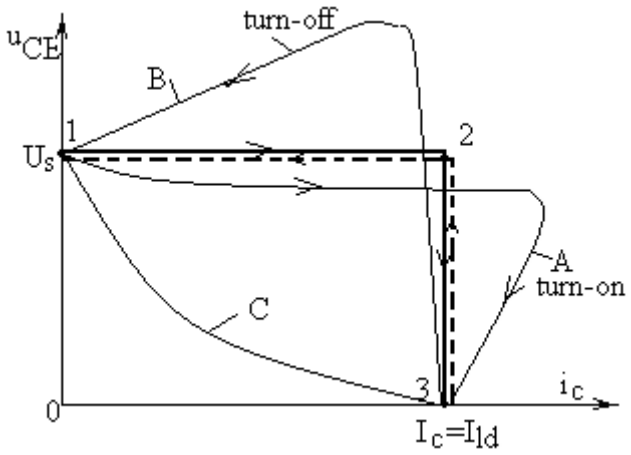

Fig.6.2. Representation of switching trajectories of transistor

Really switching trajectories differ from that represented in Fig. 6.2 and described above. In turn-on process some influence has a leakage inductance L_σ of circuit of transistor (each wire has its inductance) because at rising of current due to self-inductance voltage drop voltage across transistor is little under level of U_s but clamp diodes recovery process can cause considerable rise of collector current above I_{ld} level (curve A in Fig. 6.2.).

In the turn-off process when current is decreasing due to the change of polarity of the self-inductance voltage of L_σ voltage across transistor can be considerable higher as U_s (curve B in Fig. 6.2.).

Calculation example.

The summary leakage inductance of transistor circuit is 0.5μH but supply source voltage is 600V. Current of transistor at turn-off process decreases from 50A to zero in 200ns. How large will be a possible extreme maximum collector voltage and instantaneous power losses?

1 – decreasing speed of current

$$\frac{di_c}{dt} = \frac{-50 \cdot 10^9}{200} = -0.25 \cdot 10^9 \quad \text{A/s};$$

2 – extreme maximal voltage of transistor

$$U_{tm} = U_s - L_\sigma \frac{di_c}{dt} = 600 + \frac{0.5 \cdot 0.25 \cdot 10^9}{10^6} = 725V \ ;$$

3 – extreme maximally power losses

$$\Delta P_{tm} = I_c \cdot U_{tm} = 50 \cdot 725 = 36.25kW \ ;$$

4 – don't taking into account overvoltage

$$\Delta P_{t\max} = I_c \cdot U_s = 30.0kW \ .$$

Switching process trajectories have to comply with the Safe Operating Areas SOA of the applied transistor. For BJT, MOSFET and IGBT transistors SOA is defined as admissible to operate without a damage curves connecting collector voltage and collector current and is usually represented in datasheets of transistors with voltage on the abscissa axis and collector

current on the ordinate axis of the graph, at that data are presented in the logarithmic scale (Fig.6.3.). The SOA corresponds to the area under the curve and any combination of collector current and voltage outside of the curve is not admissible.

Decreasing part of SOA represents admissible power losses and approximately is calculated as $0.3I_{c\max} \cdot U_{CE\max}$, where I_{cmax} and U_{CEmax} are the maximal collector current and maximal collector-emitter voltage respectively. Transistor SOA of which is presented has I_{cmax}=75A and U_{Cemax}=800V. Therefore power loss limitation part of SOA corresponds to 18 kW. The trajectory shown with dashed lines corresponds to often accepted rule – use half of rated voltage and half of rated current of transistor and then point of trajectory with extreme maximum power losses every time will be inside the SOA.

The switching trajectories of transistors can be improved when moving part of the commutation losses to some passive elements forming some special circuits for dissipation of the losses and which is named as **snubber circuits**.

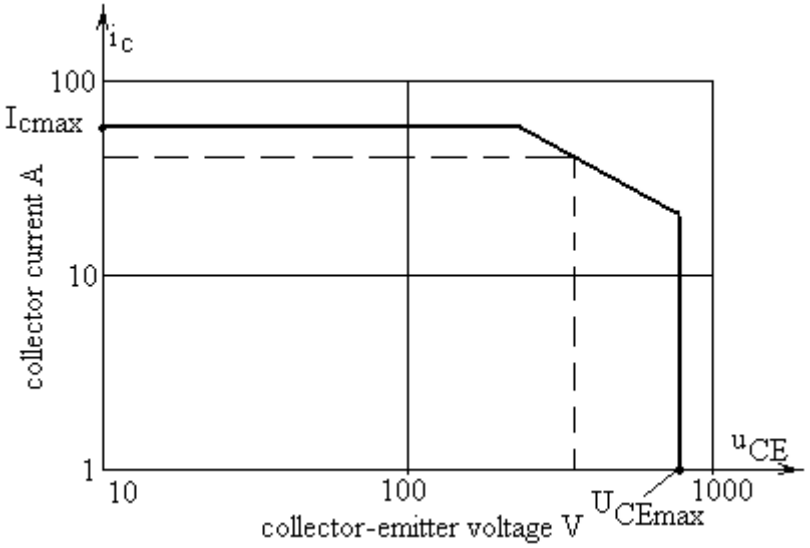

Fig. 6.3. Example of the Safe Operating Area of transistor

6.2. Snubber Circuits

6.2.1. Snubber circuits for improving a turn-off process of switching transistor

Snubber circuits for turn-off process have two main tasks:

1 – decrease power losses in turned-off transistor;

2 – restrict overvoltage possible at turn-off process.

Circuit with such C_s-R_s-V_s snubber circuit (named as RDC snubber) connected to a transistor in parallel is represented in Fig.6.4. Displayed diagrams of the turn-off process with the snubber circuit regard to the ideal case when capacitor is chosen so accurate that its end voltage at the end of current's fall interval exactly is U_s. Then voltage rise process of transistor can be described as

$$u_{vt} = \frac{1}{C_s}\int\left[I_{ld} - I_{ld}(1-\frac{t}{t_f})\right]dt + A = \frac{I_{ld}t^2}{2C_s t_f} + A \quad . \quad \text{A=0, } u_{vt}\text{=0 at t=0} \quad (6\text{-}11)$$

As end voltage is U_s for the case have to be chosen capacitor with capacitance

$$C_s = \frac{I_{ld}t_f}{2U_s} \quad . \qquad (6\text{-}12)$$

In this case (an ideal one) instantaneous turn-off power losses of transistor in way of t_f time can be calculated as

$$\Delta p_{tf} = i_c \cdot u_{vt} = I_{ld}^2\left(1-\frac{t}{t_f}\right)\cdot\frac{t^2}{2C_s t_f}. \ (0 \le t \le t_f) \qquad (6\text{-}13)$$

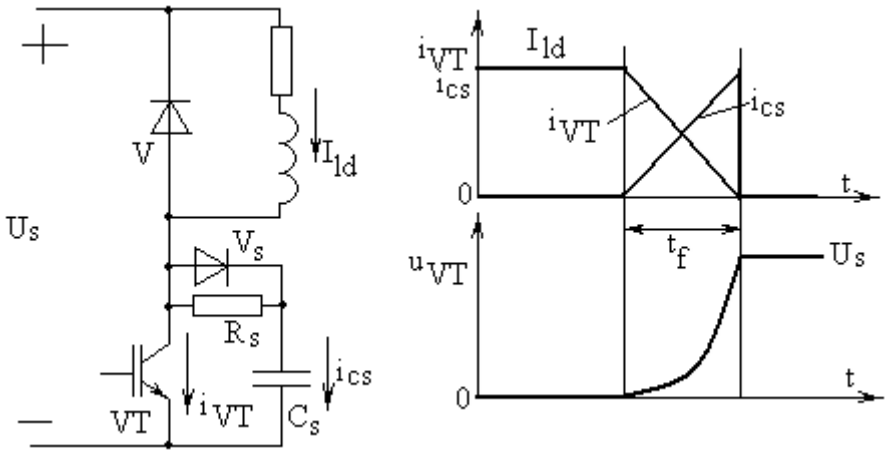

Fig. 6.4. Diagrams of turn-off process in the transistor circuit with RDC snubber

The extreme maximum instantaneous power in the transistor will be in time instant

$$t_{fm} = \frac{2}{3}t_f \qquad (6\text{-}14)$$

and the extreme maximal instantaneous power losses are

$$P_{tfm} = I_{ld}^2\frac{2t_f}{27C_s} = \frac{4I_{ld}U_s}{27} \qquad (6\text{-}15)$$

Transistor's energy losses in the all turn-off process are

$$\Delta E_{t(off)} = \int_0^{t_f} p_{tf}\,dt = \frac{I_{ld}^2 t_f^2}{24C_s} = \frac{I_{ld}U_s t_f}{12} \quad , \qquad (6\text{-}16)$$

i.e., they are in 12 times lesser as in turn-off process without snubber circuits.

The ideal trajectory of turn-off process is depicted in Fig.6.5 with curve 1. But really installed capacitance of snubber C_s should be too high or too low for a process taking place. In the first case at the end of interval t_f voltage across transistor $u_{VT}<U_s$ and then charging of C_s continues with load current I_{ld} until $u_{cs}=U_s$. Power losses in the extra charging interval in

transistor are zero but common energy losses in transistor will be lower than previously defined. The switching trajectory in the case is depicted as curve 2 in Fig.6.5.

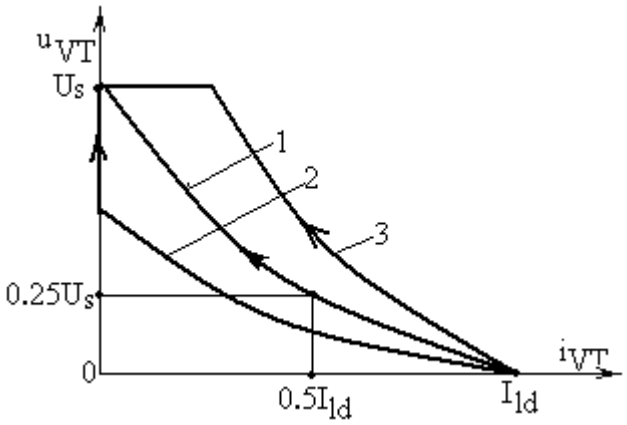

Fig.6.5. Switching process trajectories for different operation cases

In the second case voltage of capacitor C_s reaches value U_s before the end of the fall time interval t_f. In this moment current start conduct the load clamping diode V but current of the transistor decreases to zero at full voltage of supply U_s. Naturally those energy losses in the transistor will be higher than those for the ideal case. Process trajectory is depicted in Fig.6.5 with curve 3. Recharging of capacitor C_s until voltage U_s ends after time interval

$$t_{f1} = \sqrt{\frac{2U_s C_s t_f}{I_{ld}}} \tag{6-17}$$

but current of transistor in the instant is

$$I_{VT1} = I_{ld}(1 - \frac{t_{f1}}{t_f}) > 0 \ . \tag{6-18}$$

After interval t_{f1} current of the snubber capacitor is zero and transfer process of transistor's current to the clamp diode starts but collector-emitter voltage of transistor at it is equal to the supply one.

When transistor again is turned-on a snubber capacitor C_s is discharged in the loop through resistor R_s and averaged power losses of the resistor are

$$\Delta P_{RS} = 0.5 C_s U_s^2 \cdot f \ , \tag{6-19}$$

i.e., they do not depend on the resistance of the contour. The extreme minimal turned-on condition of transistor (the on-duty cycle) has to proceed enough long for discharge of snubber capacitor in the full extent, i.e., $t_{VT(on)} > 3C_sR_s$. In its turn the nominal of R_s for restricting of discharge current level must be higher than $U_s/(0.1I_{ld})$.

Calculation example.

Voltage of supply source is 600V but rated current of load is 50A. The fall time of transistor is t_f=400ns. Calculate necessary parameters of snubber circuit and power losses for turn-off process operating with the rated load current and increased until 75 A one if switching frequency is 4 kHz!

1 – necessary capacitance of snubber capacitor

$$C_s = \frac{I_{ld} t_f}{2U_s} = \frac{50 \cdot 400}{10^9 \cdot 1200} = 16.66nF \ ;$$

let us assume C_s=20nF.

2 – The nominal value of resistor

$$R_s \geq \frac{U_s}{0.1 I_{ld}} = \frac{600}{5} = 120\Omega \ ;$$

then power losses of the resistor

$$\Delta P_{RS} = 0.5 C_s U_s^2 \cdot f = \frac{10 \cdot 600^2 \cdot 4 \cdot 10^3}{10^9} = 14.4W \ ;$$ let's accept rated power of resistor as 20W.

3 – Energy losses in turn-off process at the rated current of load

$$\Delta E_{t(off)N} = \frac{I_{ld} U_s t_f}{12} = \frac{50 \cdot 60 \cdot 400}{10^9 \cdot 12} = 1mJ \ ;$$

power losses in turn-off process

$$\Delta P_{t(off)N} = \Delta E_{t(off)N} \cdot f = 4W \ .$$

4 – Length of the first interval at turn-off at higher load current

$$t_1 = \sqrt{\frac{2U_s C_s t_f}{I_{ld\,\max}}} = \sqrt{\frac{2 \cdot 20 \cdot 600 \cdot 400}{10^9 \cdot 10^9 \cdot 75}} = 375ns \ .$$

5 – Losses of energy in the first interval with increased load current

$$\Delta E_{t1(off)} = I_{ld}^2 \frac{t_{f1}^3}{24 C_s t_f} = 1.33mJ \ ;$$

6 – Energy losses in the second interval of turn-off process with the increased load current

$$\Delta E_{t2(off)} = 0.5 I_{ld} (1 - \frac{t_{f1}}{t_f}) U_s (t_f - t_{f1}) = 0.1mJ \ ;$$

7 – The common energy losses in the turn-off process with increased load

$$\Delta E_{t(off)} = 1.33 + 0.1 = 1.43mJ$$

and power losses

$$\Delta P_{t(off)} = 1.43 \cdot 10^{-3} \cdot f = 5.72W \ .$$

The second task for snubber circuit in turn-off process is to compensate influence of switched circuit leakage inductance L_σ on the extreme maximum voltage of transistor. When instantaneous meaning of the current at end of process is zero current of the leakage inductance and in series with it connected snubber capacitor is equal to the I_{ld} . Because voltage across the capacitor at the end of the process is U_s a current decreasing process in the circuit L_σ-C_s starts and at the same time – rise of current in clamp diode of load. Therefore to the all circuit voltage U_s is applied and process proceeds in accordance with differential equation

$$L_\sigma \frac{di}{dt} + \frac{1}{C_s}\int idt + U_s = U_s \tag{6-20}$$

with initial values at t=0 $i(0)=I_{ld}$ and $di/dt=(0)=0$. Therefore solution of the second-order differential equation

$$i = A\sin\omega t + B\cos\omega t \tag{6-21}$$

can be found as

$$i = I_{ld}\cos\omega t \ . \qquad i \geq 0 \tag{6-22}$$

Here $\omega = \sqrt{\frac{1}{L_\sigma C_s}}$ - resonant frequency of oscillations in the circuit L_σ-C_s . Voltage of the snubber capacitor changes as

$$u_{CS} = U_s + \frac{1}{C_s}\int idt = U_s + \frac{I_{ld}}{\omega C_s}\sin\omega t \tag{6-23}$$

reaching its maximum at $\omega t = 0.5\pi$ when i=0:

$$U_{cs\max} = U_s + I_{ld}\sqrt{\frac{L_\sigma}{C_s}} \ . \tag{6-24}$$

Calculation example.

Load current is 50A, voltage of the source is 600V. Capacitor of snubber circuit is accepted as 20nF but leakage inductance is $0.5\,\mu H$. Calculate the extreme maximal voltage peak across transistor!

1 - $$U_{cs\max} = U_s + I_{ld}\sqrt{\frac{L_\sigma}{C_s}} = 600 + 50\sqrt{\frac{0.5\cdot 10^9}{10^6\cdot 20}} = 850V \ .$$

As it can be seen, peak value of voltage is rather large, i.e., accepted capacitance of snubber capacitor is too small. If to increase capacitance to a 50nF value then U_{csmax}=758.1V.

For decreasing of overvoltage level at turn-off process a leakage inductance of switched circuit have to be decreased shortening a length of connection wires as well as optimizing displacement of elements in the schemes.

6.2.2. Improvement of turn-on process of switching transistor

Turn-on process is relatively short and power losses of it are much lower as for turn-off process but at working with high switching frequency these losses can rise essentially. Therefore sometimes snubber circuits for turn-on process also are applied and they usually comprise an extra inductance in circuit of the turned-on transistor or in circuit of the clamp diode (Fig. 6). At the first appliance in way of transistor's current rise a voltage drop across the snubber inductance L_s emerges and voltage of transistor is decreased to value

$$u_{t(on)} = U_s - L_s \frac{I_{VT\,\max}}{t_r + t_{rec}} \quad , \tag{6-25}$$

where $I_{Vtmax}=I_{ld}+\Delta I_{rec}$ and ΔI_{rec} are extreme magnitudes of transistor current taking into account rise of current in time duration of clamp diode recovery.

In the second case the current of transistor can rise slower as well as the extra current value in end instant of diode recovery time decreases too. At that a voltage at turning-on of the transistor can be decreased to very small levels.

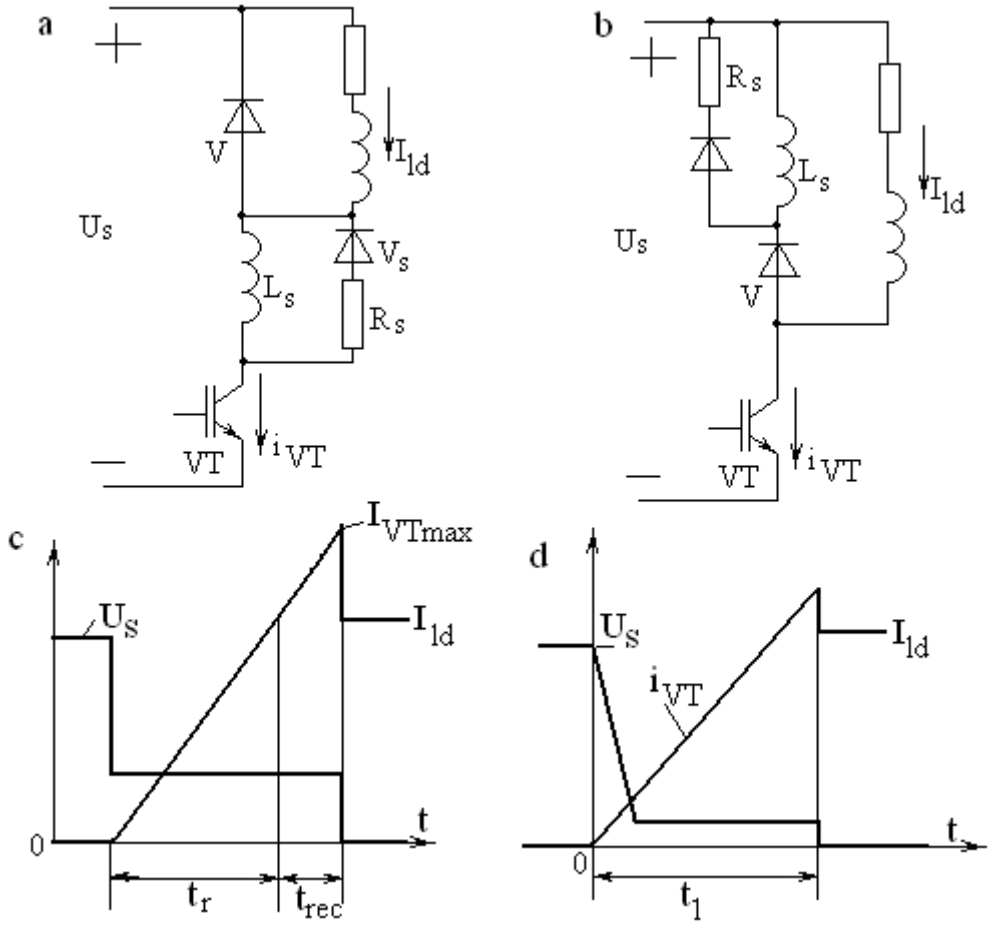

Fig.6.6. Turn-on process diagrams for transistor with series snubber inductance (a), with snubber inductance in clamp diode circuit (b) and corresponding diagrams (c) and (d)

In the first variant (Fig.6.6.(a)) inductance L_s for decreasing at the end of turn-on process voltage of the transistor to zero level have to be calculated as

$$L_{s\max} = \frac{U_s t_r}{I_{ld}} \quad . \tag{6-26}$$

In Fig.6.6.(a), is depicted case when $L_s < L_{smax}$.

In the second case (Fig.6.6.(b)) current of the transistor is increasing over turn-on transient process as

$$i_{VT} = \frac{U_s t}{L_s} \quad , \tag{6-27}$$

where $0 \le t \le L_s I_{ld} / U_s$. In the last variant an interval of current rise can be increased above the summary time interval $t_r + t_{rec}$.

For dissipation of energy stored over turn-on interval in inductance L_s to parallel to the inductance through a reverse connected diode a discharge resistance R_s is installed. Then at turned-off duty cycle of transistor which has to be longer as $3L_s/R_s$ a current of inductance decreases to practical zero value. But it can be accounted that such a resistive circuit arises extra voltage across transistor in turn-off process which can reach value $I_{ld}R_S$. Power losses in the resistor can be calculate as $\Delta P_{Rs} = 0.5 L_s I_{ld}^2 \cdot f$, where f is switching frequency.

Calculation example.

Calculate a necessary inductance of the turn-on process snubber if supply voltage is 600V, load current is 50A, the rise time of transistor is t_r=30ns but switching frequency – 50 kHz!. The extreme maximal duty ratio of transistor switch is D_{max}=0.9.

1 – necessary inductance introduced in series with transistor is

$$L_s = \frac{U_s t_r}{I_{ld}} = \frac{600 \cdot 30}{10^9 \cdot 50} = 0.36 \mu H \quad ;$$

2 – the time duration for turn-off position of the switch at the maximal duty ratio

$$t_{t(off)\min} = \frac{1 - D_{\max}}{f} = 2 \mu s \ ;$$

3 – the nominal value of discharging resistor

$$R_s = \frac{3L_s}{t_{t(off)}} = \frac{3 \cdot 0.36 \cdot 10^6}{10^6 \cdot 2} = 0.54 \Omega \ ;$$

4 – power losses of the resistor

$$\Delta P_{Rs} = 0.5 L_s I_{ld}^2 \cdot f = \frac{0.36 \cdot 0.5 \cdot 50^2 \cdot 50 \cdot 10^3}{10^6} = 22.5 W \quad .$$

As it can be seen from the calculation pattern power losses of the snubber resistor is rather large and therefore the selection of the proper parameters of the turn-on snubber circuit has to

be substantial. The inductive snubber circuit is very necessary for a bridge mode switch schemes when at turn-on of one transistor of one leg (Fig.6.7.) a charging process of capacitor of turn-off snubber of the other transistor of a leg proceeds. Usually between turn-off instant of one transistor of leg and turn-on instant of the other in leg is introduced a time gap – so named dead time – but anyway it is possible that turn-off process of transistor is yet not finished because it is much longer as turn-on one and its snubber capacitor is not charged in full extent. Then it is possible that sufficiently large charging current can flow through turned-on transistor and it can be a reason for its damage. Therefore introduction of snubber inductance for leg circuit should be advantageous (Fig.6.7.).

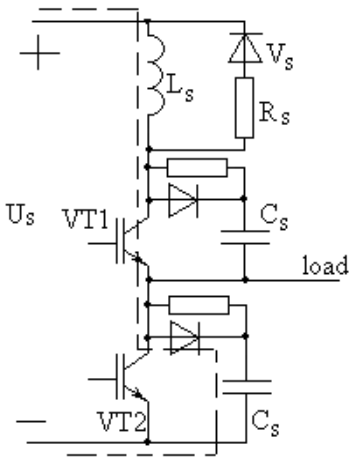

Fig. 6.7. Charging circuit of snubber capacitor through turned-on transistor in one leg of the bridge scheme

6.3. Soft-switching Converters

6.3.1. Zero Current (ZC) and Zero Voltage (ZC) Commutation

Best of all the conditions from view-point of minimum switching power losses should be if in turn-on and turn-off processes instantaneous current and voltage of switch transistor would be zero, i.e. switching power losses then will be at zero level and only conductivity losses will remain. For obtaining of the processes close to the mentioned case it is necessary to provide in switching instants a bidirectional oscillating character of current and voltage in switch circuit.

Such method have been applied already in thyristor based DC circuit switches where introducing of capacitor and coil in content of switch were necessary for providing of normally operation regimes. In Fig.6.8 a classical thyristor DC switch scheme is represented where two oscillating contours were introduced in the content of switch.

Operation of the scheme can be described as follows. Gating the main thyristor VS1 its current is at zero level for in the circuit is inserted a coil L and current from clamp diode V0 gradually pass to the thyristor-coil circuit until current of thyristor will be equal to a load current . At this instant an oscillating process of a previous charged capacitor C overcharging through diode V2, thyristor VS1 and coil L starts. Thr result of the process is in an opposite polarity of voltage on plates of capacitor in respect to the initial one. When the switch has to

be turned-off the thyristor VS2 is gated and current of capacitor in oscillating process is gradually rising above the level of load current but in the process current of VS1 is decreasing down to zero level when diode V1 starts to conduct, such providing also zero level of voltage across the turned-off thyristor VS1, i.e. thyristor VS1 is turned-on and turned-off with negligible small power losses.

On the basis of the thyristor system a switch system with zero current - zero voltage commutation facilities can be constructed, a scheme of which is presented in Fig. 6.9. With proper dimensioned parameters of an oscillating contours such switch can operate at rather high switching frequency in the regulated at constant switching frequency PWM system.

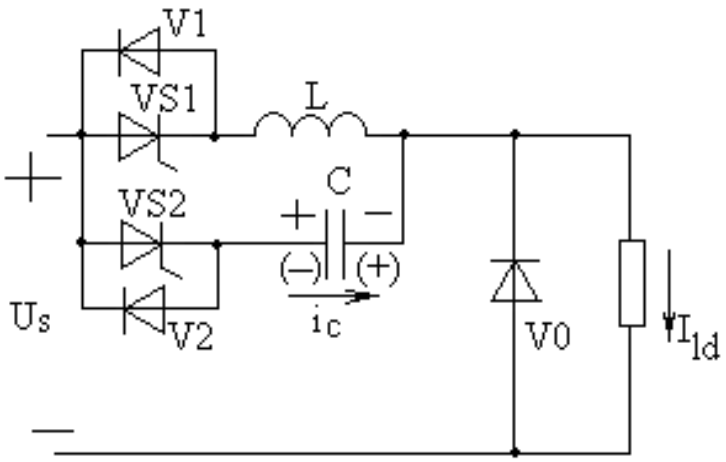

Fig. 6.8. Thyristor switch scheme with soft commutation

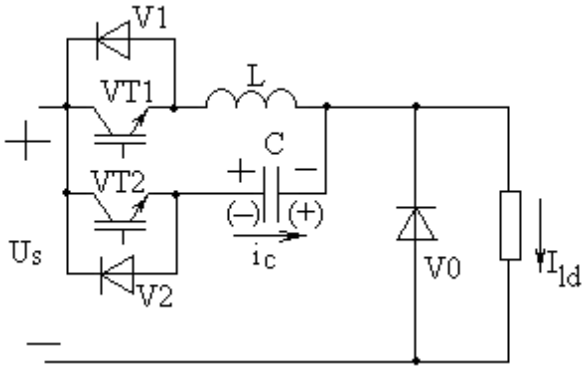

Fig. 6.9. Transistor switch scheme with soft commutation

The means applied in the thyristors schemes can be applied also in transistor schemes. Fig. 6.10 demonstrates 2 schemes of transistor switch where it is possible to turn-on and turn-off transistor with its zero current, i.e., they both are ZC switches. In the case *a* at turn-on of transistor its current due to the inserted in series coil L is at zero value. Capacitor C is charged in oscillating manner up to the two fold value of supply voltage U_1 (Fig.6.10.(a)) and then reverse resonance process takes place in which the current in the coil changes its direction and passes through the diode V, allowing in this time interval to turn-off transistor without current and practically without voltage, i.e. turn-off process can be ZC-ZV one.

In the case *b* coil L also is introduced in series with transistor (Fig.6.10.(b) and such a measure provides ZC turn-off process of the transistor. Capacitor C similarly as in the thyristors scheme changes its polarity overcharging through the transistor VT and coil L and

with its a negative half-wave voltage a decreasing of coil's current through the diode V to the zero value brings and in that interval the transistor can be turned-off without current and voltage too.

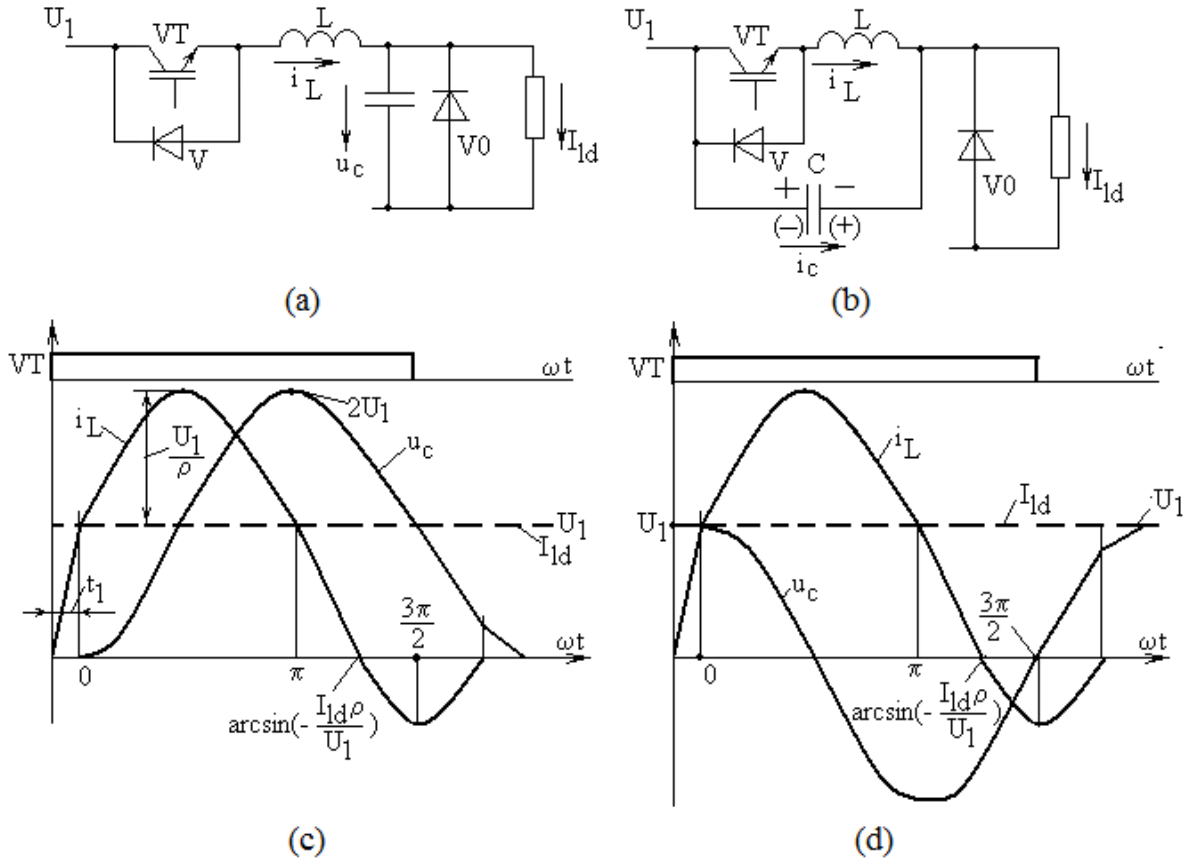

Fig. 6.10. Zero current switch realization and diagrams for scheme *a (c)* and *b (d)*

At gate voltage rising instant of the transistors VT in the both schemes due the coils L inserted in series with transistors their currents are equal to zero value. While current of the coils rise to the load value I_{ld} (intervals $t_1=L.I_{ld}/U_1$) voltage of capacitors are at its initial values: zero in the scheme *a* and U_1 in the scheme *b*. Then in the scheme a starts oscillating charging process of capacitor in accordance with differential equation

$$U_1 = L\frac{di_L}{dt} + \frac{1}{C}\int i_c dt \qquad (6\text{-}28)$$

at solving of which the following has to be accounted $i_L = i_c + I_{ld}$ and $di_L/dt=di_c/dt$.

The standard solution of the Second Order differential equation is

$$i_c = A\sin\omega t + B\cos\omega t \qquad (6\text{-}29)$$

where assuming that the start instant of the process is when $i_L=I_{ld}$, i.e. t=0, $i_c=0$ and the constant B=0. The constant A can be found using a derivative of i_C in initial point which from (6-28) is U_1/L. Then

$$i_C = \frac{U_1}{\omega L}\sin\omega t = \frac{U_1}{\rho}\sin\omega t \qquad (6\text{-}30)$$

where $\rho = \sqrt{\frac{L}{C}}$ is the resonant impedance, but $\omega = \sqrt{\frac{1}{LC}}$ - a resonant frequency.

As a result the current of the transistor circuit is rising above the load value:

$$i_L = I_{ld} + \frac{U_1}{\rho}\sin\omega t \tag{6-31}$$

reaching to its maximum extreme at $\omega t = 0.5\pi$ when

$$I_{Lm} = \frac{U_1}{\rho} + I_{ld} \quad . \tag{6-32}$$

Voltage of capacitor is changing as

$$u_c = \frac{1}{C}\int i_C \sin\omega t dt + K \tag{6-33}$$

where taking into account that at time instant t=0 voltage u_C=0, the constant K=0 and therefore voltage of capacitor changes as

$$u_C = U_1(1-\cos\omega t) \tag{6-34}$$

reaching to its extreme magnitude $2U_1$ at $\omega t = \pi.$

Current i_L in the oscillating process changes its polarity at angular instant

$$\omega t_1 = \arcsin(-\frac{I_{ld}\rho}{U_1}) \tag{6-35}$$

when voltage of capacitor is of the higher level than the supply voltage, i.e.

$$u_{C(0)} = U_1 + \sqrt{U_1^2 - I_{ld}^2\rho^2} \tag{6-36}$$

Therefore current i_L changes its polarity and passes through the diode V which bypasses the transistor in the reverse direction and reaches its negative extreme maximum I_{ld}-U_1/ρ at $\omega t = 1.5\pi$. At time instant $\omega t_2 = 3\pi - \arcsin(-\frac{I_{ld}\rho}{U_1})$ current i_L has its zero value and process is completed. Transistor can be turned off in time interval between ωt_2 and ωt_1 when its current is zero and its voltage too.

Processes in the second ZC switching scheme are quiet similar to the described except that capacitor is initially charged with voltage U_1 and in the resonant circuit C-L through transistor VT changes its polarity to the opposite and in the time instant ωt_1 when i_L=0, a voltage across the capacitor is of negative polarity $-\sqrt{U_1^2 - I_{ld}^2\rho^2}$ which effects a change of the coil current polarity to negative, when current i_L passes through the diode V which bypasses the transistor VT. Again in time interval between ωt_2 and ωt_1 transistor VT can be turned-off without current and voltage.

For achieving the positive effect the conductivity interval of transistors in the both schemes has to be rather fixed and therefore effect in changing of loading parameters can be achieved only changing a switching frequency of transistors, i.e. have to be applied the Pulse-Frequency Modulation PFM. It must be accented that for obtaining a proper resonant process a relation has to be $\frac{U_1}{\rho} > I_{ld}$.

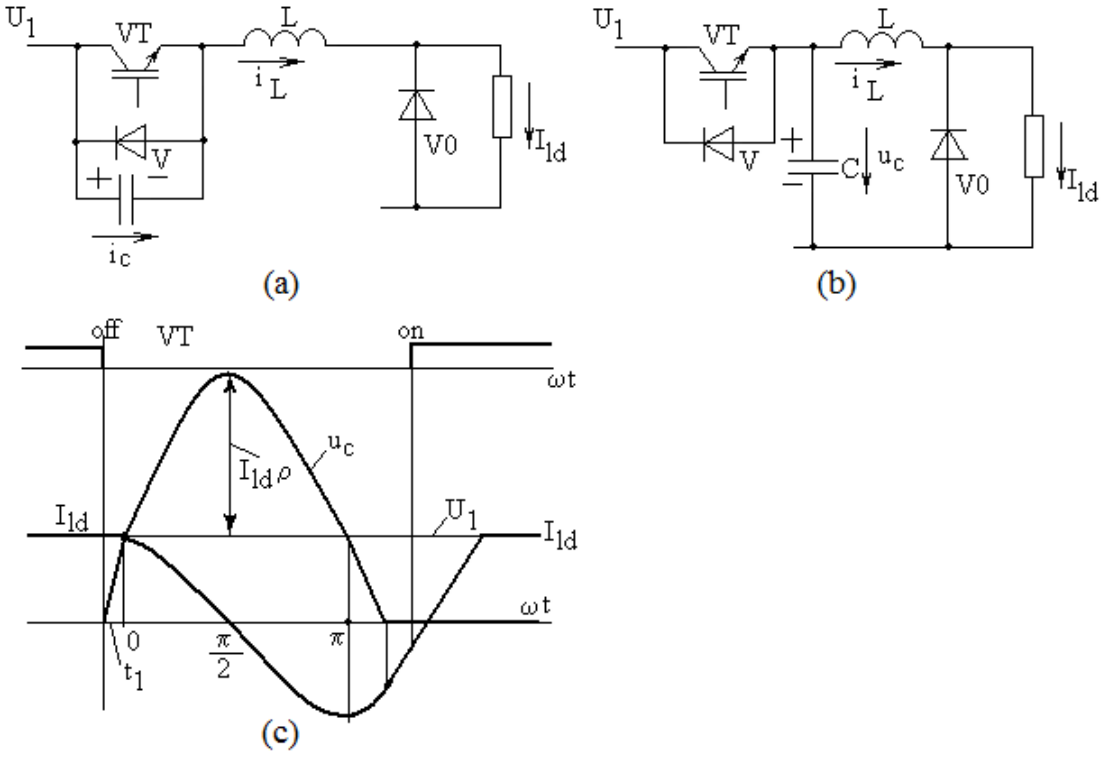

Fig. 6.11. Zero Voltage switch realization schemes and diagrams for the scheme *a (c)*

Similarly can be arranged the Zero-Voltage ZV switch. Transistor circuits are connected with L-C elements and transistor itself – with a clamp diode V (Fig. 6.11.).

In the case *a* when transistor is continuously conducting, its current is I_{ld} but voltage of the capacitor is at zero level. When switch is turned off, in the first stage of processes in interval $t_1=U_1C/I_{ld}$ voltage of capacitor is gradually rising up to the value of supply U_1. Then a resonant process starts in which current of the coil is changing as described with (6-29) and taking into account that at t=0 current $i_L=I_{ld}$ but derivative of i_L is zero, changes of the current can be described as

$$i_L = I_{ld}\cos\omega t \ . \qquad (6\text{-}37)$$

Voltage of capacitor in the process changes as

$$u_c = \frac{1}{C}\int i_c dt + K = \frac{1}{C}\int I_{ld}\cos\omega t dt + K = I_{ld}\rho\sin\omega t + K = U_1 + I_{ld}\rho\sin\omega t \ . (6\text{-}38)$$

In the process $i_L=i_C$ and initial voltage of the capacitor is U_1.

The extreme maximum voltage of capacitor is

$$U_{cm} = U_1 + I_{ld}\rho \tag{6-39}$$

and at that polarity of current i_L changes to the negative one. Voltage u_c will be at zero value at angular time instant

$$\omega t_2 = \arcsin(-\frac{U_1}{I_{ld}\rho}) > \pi \tag{6-40}$$

after which transistor is clamped with conducting current diode and then transistor VT can be turned-on without current and at zero voltage across it.

It has to be accounted that $(U_1 / \rho) > I_{ld}$. The turned-off condition is rather determined one by time lengths and it means that in the case regulation of processes can be obtained applying a variation of a length of turned-on condition of transistor switch using PFM method.

Calculation example.

Applying the **ZC** switch by version *a* an operation of the load with current 30A and supply voltage 300V with switching maximal frequency 20kHz at duty ratio of the switch transistor 0.9 have to be provided. Find necessary parameters of resonant circuit and check really conductivity interval complying with prescribed one duty ratio!

1 – applying relation of $U_1/\rho = 2I_{ld}$. Then $\rho = \frac{300}{60} = 5\Omega$;

2 – prescribed conductivity interval of the transistor

$$t_{con} = \frac{0.9}{f_{\max}} = \frac{0.9}{20 \cdot 10^3} = 45\mu s$$

3 – assuming arbitrary that conductivity interval is about 1.8π in length (proportionally to the duty ratio in full cycle), a resonant frequency is

$$\omega_r = \frac{1.8\pi}{t_{con}} = 125.59 \cdot 10^3 1/s \ ;$$

4 – from expression of resonant frequency

$$\omega_r = \sqrt{\frac{1}{C_r L_r}} = \sqrt{\frac{1}{C_r^2 \rho^2}}$$

the capacitance of resonant circuit is

$$C_r = \frac{1}{\omega_r \rho} = \frac{1}{125.59 \cdot 10^3 \cdot 5} = 1.59\mu F \ ;$$

5 – inductance of resonant circuit

$$L_r = C_r \cdot \rho^2 = 1.59 \cdot 10^{-6} \cdot 25 = 39.8\mu H \ ;$$

6 – current rising interval at turn-on

$$t_1 = \frac{I_{ld} L_r}{U_1} = 3.98 \mu s;$$

7 – angular time interval from resonant process start instant until current through the coil changes its polarity to the negative one

$$\omega_r t_{rev} = \arcsin(-\frac{I_{ld} \rho}{U_1}) = \arcsin(-0.5) = 3.66 rad$$

and corresponding t_{rev}=3.66/125.59x10^3=29 μs .

8 – angular time instant when current of the coil changes again its polarity to the positive one will be

$$\omega_r t_{\max} = \frac{2\pi}{3} + 3.66 = 5.75 rad$$ and t_{max}=45.8 μs .

It means that the prescribed turn-off instant will be at the end of the reverse current wave, i.e. off-switching will be safe without current and voltage across transistor.

6.3.2. Soft commutated converters

The above mentioned and described switch schemes can be efficiently applied in different versions of switching converters which are named as **Quasi-Resonant**. The main possible applications with ZC switches are presented in Fig.6.12.

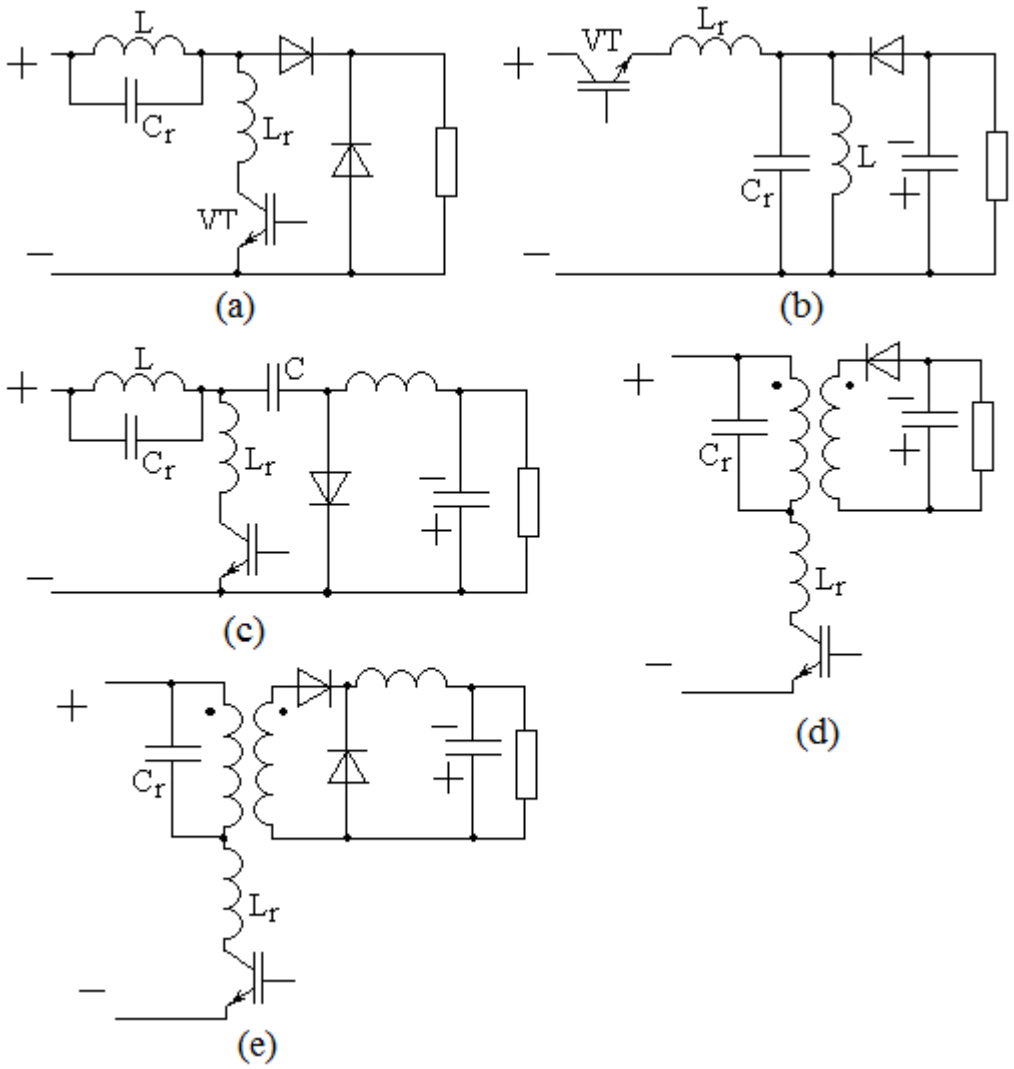

Fig. 6.12. Schemes of the Quasi-Resonant converters with ZC switches: Boost converter (a), Buck-Boost converter (b), Cuk Buck-Boost converter (c), Fly-back converter (d), Forward converter (e)

In the Boost converter scheme introduction of series inductance in the circuit of switch restricts also diode's recovery process reverse current influence on transistor operation but the resonant circuit softening switching transient processes of transistor. It has to be accounted that application of the ZC switches arise current stresses in transistors circuits which increase conduction losses of transistors.

Similarly, using resonant circuits, it is possible to arrange also QR converters with ZV switches when for instance in the Boost converter transistor is bypassed with a resonant capacitor but in series similarly as in the ZC case inductance has to be introduced. Here across resonant capacitor and transistor arise a voltage stresses.

In the common an application of soft commutated switches ask for converters realization on the base of PFM control principle when effect can be obtained at relative constant on-duty or off-duty cycles changing a switching frequency. Only in some special cases an auxiliary transistor switch with the soft commutation is introduced – as it is shown in Fig.6.9 – it is possible to provide PWM control with constant switching frequency and variation of length of on-duty or off-duty cycles in the constant switching cycle.

6.4. Resonant and Quasi-Resonant Converters

6.4.1. Quasi-Resonant QR converters

Quasi-resonant converters are possible evaluated on the base of their 4 possible Buck converters modifications – half-wave and full-wave, with ZC and with ZV switches. The half-wave version of Buck converter with ZC switch is represented in Fig. 6.13. There in series with transistor VT is introduced diode V such does not allow flowing a reverse current to the supply source. In the second part of the process voltage of capacitor C_r from the initial value at turn-off instant of the switch, equal to $\Delta U_{ld} = (U_1 + \sqrt{U_1^2 - I_{ld}^2 \rho^2})$, decreases to the zero value at influence of the load current I_{ld} . Therefore time interval of capacitor discharge length for

$$t_2 = \frac{\Delta U_{ld} \cdot C_r}{I_{ld}} \quad . \tag{6-41}$$

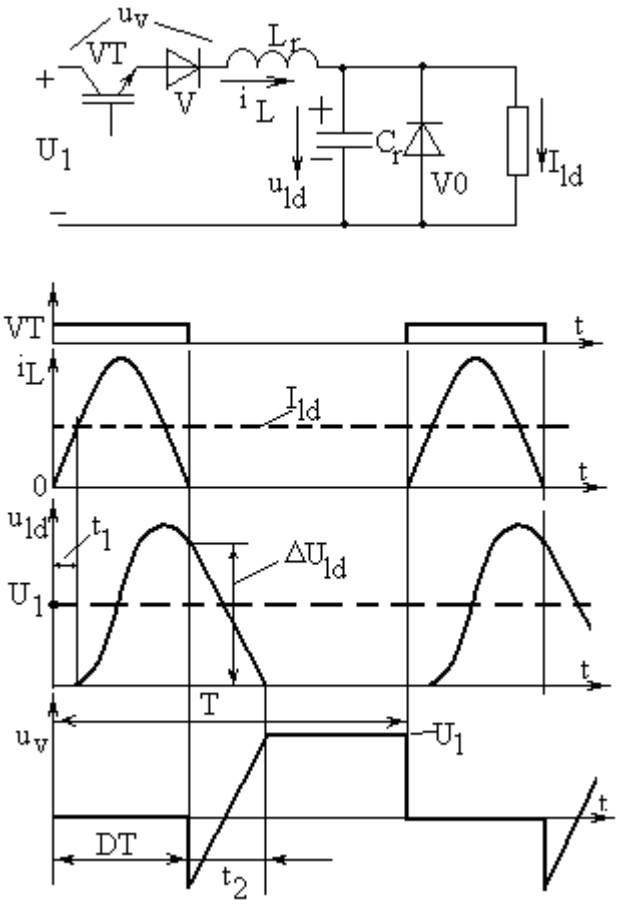

Fig. 6.13. Half-wave version of Buck converter with ZC switch

The averaged load voltage is equal to the difference between supply voltage U_1 and averaged voltage across circuit of transistor-diode U_{Vav}:

$$U_{ld} = U_1 - U_{Vav} = DU_1 + \frac{I_{ld} L_r f_{sw}}{2} = \frac{2DU_1}{2 + \frac{L_r}{R} f_{sw}} \quad , \tag{6-42}$$

where D is the ratio of time interval when transistor is turned-on to the switching cycle $1/f_{sw}$. It can be seen that at rising of switching frequency f_{sw} voltage of load is rising too because D rises proportional to the frequency. If at constant f_{sw} resistance of load is rising then discharging process prolongs and load voltage rises.

For proper operation of the system the time interval t_2 has to be lower than $(1-D)/f_{sw}$. Taking into account expression for the interval it can be stated that it is necessary that load current

$$I_{ld} \geq \frac{\Delta U_{ld}.C.f_{sw}}{1-D} \quad . \tag{6-43}$$

Calculation example.

Calculate a load voltage of the half-wave quasi-resonant ZC converter with U_1=100 V, switching frequency 5 kHz, capacitor C_r=1 μF and inductance L_r=60 μH at load resistance 5 Ω!

1 – resonant frequency $\omega_r = \sqrt{\frac{1}{L_r C_r}} = \frac{10^6}{7.75} = 129{,}032.3$ 1/s ;

2 – resonant half-cycle duration $t_r = \pi\sqrt{L_r C_r} = \frac{\pi \cdot 7.75}{10^6} = 24.34\mu s$;

3 – duration of current i_L initial rise to I_{ld} and end stage decrease from I_{ld} to zero

$$t_1 = \frac{L_r U_{ld}}{U_1 R} = \frac{2DL_r}{R(2+\frac{L_r}{R} f_{sw})}$$

and $(t_r + 2t_1) f_{sw} = D$. Here from at R=5 Ω D=0.109

4 – load voltage $U_{ld} = \frac{2DU_1 R}{2R + L_r f_{sw}} = \frac{0.218 \cdot 100 \cdot 5}{10 + 0.3} = 10.58V$

and load current is 2.117 A, which is bigger as $\frac{198 \cdot 0.5}{100 \cdot 0.891} = 1.1A$, where $\Delta U_{ld} = 198V$.

As it can be seen the scheme with half-wave ZC switch is very sensitive to the change of parameters of load. If for instance in the example above instead of load resistance 5 Ω would be installed one of 10 Ω then load current should be lower than it is required by (6-43) and scheme should not operate proper.

The full-wave scheme with ZC switch (Fig.6.14.) is characterized with almost rectangular shape of load voltage and also stable zero voltage duration across the switch. Therefore averaged meaning of load voltage is

$$U_{ld} = U_1 - U_{VTav} \approx DU_1 \, , \tag{6-44}$$

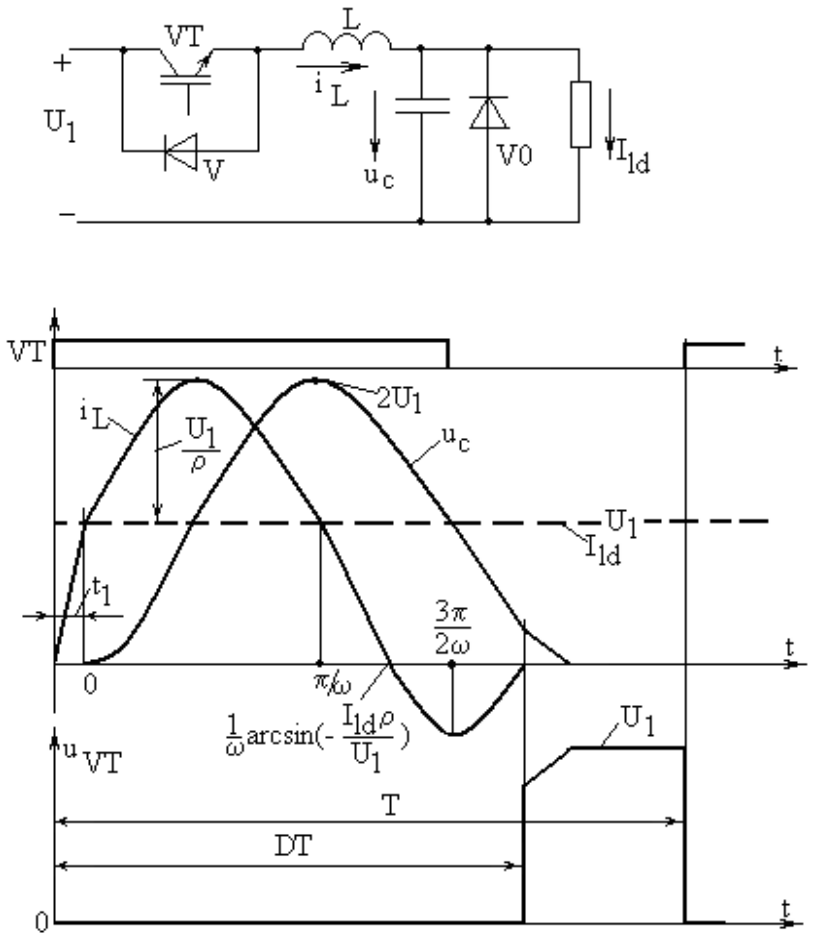

Fig. 6.14. Scheme and waveforms of signals for Full-wave QR converter with ZC switch

where duty ratio

$$D \approx [\frac{3\pi}{2\omega_r} + \left(\frac{1}{\omega_r}\arcsin(-\frac{I_{ld}\rho}{U_1}) - \frac{\pi}{\omega_r}\right)] \cdot f_{sw} = \left(\frac{\pi}{2\omega_r} + \frac{1}{\omega_r}\arcsin(-\frac{I_{ld}\rho}{U_1}\right) \cdot f_{sw} \quad (6\text{-}45)$$

If load current is constant then the load voltage changes almost linearly with frequency which can reach up to approximately $f_{swmax}=0.9/\left(\frac{\pi}{2\omega_r} + \frac{1}{\omega_r}\arcsin(-\frac{I_{ld}\rho}{U_1}\right)$. Similarly to that applied in other ZC switching schemes the product of $I_{ld}\rho/U_1$ must be lower than 1.

Calculation example.

Let us apply parameters of the previous calculation example and find switching frequency at duty ratio D=0.7 and 0.4.

1- load voltages at given values of D

$$U_{ld1} = 0.7 \cdot 100 = 70V \ ; \ U_{ld2} = 0.4 \cdot 100 = 40V \ ;$$

2 – load currents accordingly

$I_{ld1}=70/5=14A$; $I_{ld2}=40/5=8A$;

3 – the resonant impedance $\rho = \sqrt{\frac{L_r}{C_r}} = \sqrt{\frac{60}{1}} = 7.75\Omega$; as it can be seen at I_{ld1} a product $I_{ld}\rho/U_1$ will be bigger as 1, i.e., scheme can't operate in proper way. Let's increase volume of the resonant capacitor to $2\,\mu F$. Then $\rho = \sqrt{\frac{L_r}{C_r}} = \sqrt{\frac{60}{2}} = 5.48\Omega$ and operation of the scheme will be adequate.

4 – switching frequencies necessary

$$f_{sw1} = \frac{0.7}{\frac{\pi}{2\omega_r} + \frac{1}{\omega_r}\arcsin(-\frac{I_{ld1}\rho}{U_1})} = \frac{0.7}{\frac{\pi}{2\cdot 91{,}324.2} + \frac{1}{91{,}324.2}\arcsin(-\frac{14\cdot 5.48}{100})} = 11{,}448Hz$$

$$f_{sw2} = \frac{0.4}{\frac{\pi}{2\omega_r} + \frac{1}{\omega_r}\arcsin(-\frac{I_{ld2}\rho}{U_1})} = \frac{0.4}{\frac{\pi}{2\cdot 91{,}324.2} + \frac{1}{91{,}324.2}\arcsin(-\frac{8\cdot 5.48}{100})} = 7{,}516.5Hz$$

QR zero voltage ZV switch converters also can be realized in half-wave and full-wave versions. The scheme for the first is presented in Fig. 6.15. Here transistor switch is bypassed with resonant capacitor C_r and in reverse direction – with diode V which does not allow changing the polarity of the capacitor voltage.

In the scheme at turned-on transistor switch through it and the coil L_r flow load current I_{ld} but voltage across capacitor is at zero level. When transistor is turning-off the current of L_r passes through the capacitor rising its voltage to the level of the supply U_1 when the resonant process starts and load clamping diode V0 opens. In the way of the process current of the coil changes as

$$I_L = I_{ld}\sin\omega_r t \tag{6-46}$$

but voltage of capacitor as

$$u_c = u_v = U_1 + \rho I_{ld}\sin\omega_r t \ . \tag{6-47}$$

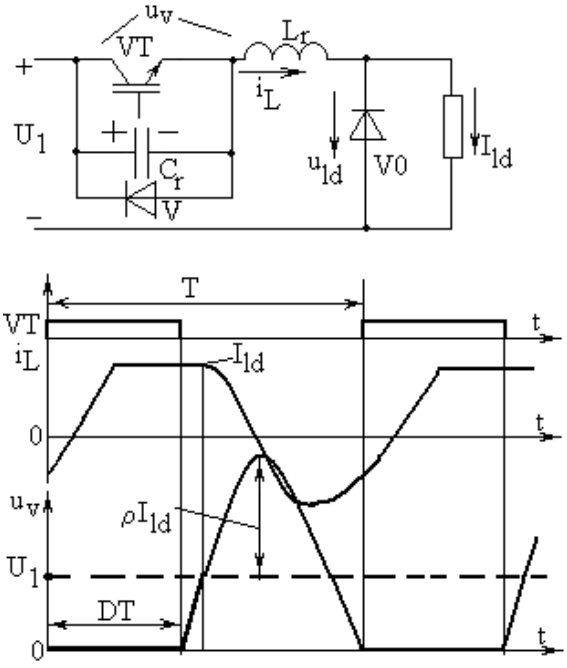

Fig. 6.15. Scheme and waveforms of signals for half-wave QR-ZV converter

The peak value of capacitor voltage is $(U_1 + \rho I_{ld})$. In the process voltage of capacitor decreases to U_1 and then to the zero level when current of L_r starts to flow through diode V, i.e. voltage across switch becomes equal to zero. Transistor can be activated at zero voltage across it. Time instant from beginning of the resonant process at which $u_c=0$ can be found from relation

$$\sin \omega_r t = -\frac{U_1}{\rho I_{ld}} \quad . \tag{6-48}$$

Expression (6-48) states that value ρI_{ld} has to be higher than U_1. Due to the fact that both of the diodes V and V0 are conducting current of the coil at initial part of transistor's conductivity when $u_c=0$ it rises in linear way up to the level of load current level when diode V0 becomes reverse biased.

Characteristic $U_{ld}=f(f_{sw})$ is rather sensitive to the level of load current and that is main drawback of the converter. Regulation $\rho I_{ld} > U_1$ restricts application of the scheme for the light loads.

Another version of the QR-ZV converter is at Full-wave operation (Fig.6.16.). Here when transistor VT is turned-off the capacitor C_r is discharged and voltage across the switch is of zero level. Then capacitor is charged in the first stage with load current but in the second one, when load clamping diode V0 is conducting current – in oscillating process through coil L_r up to voltage level above the supply one and then discharged in the same contour to the negative polarity with $i_L<0$, when it is possible to turn-on transistor VT, which starts to conduct current at instant when $u_c=0$. In this scheme length of the off-position of transistor depends in lesser extent on level of load voltage then it was in the first version of ZV system.

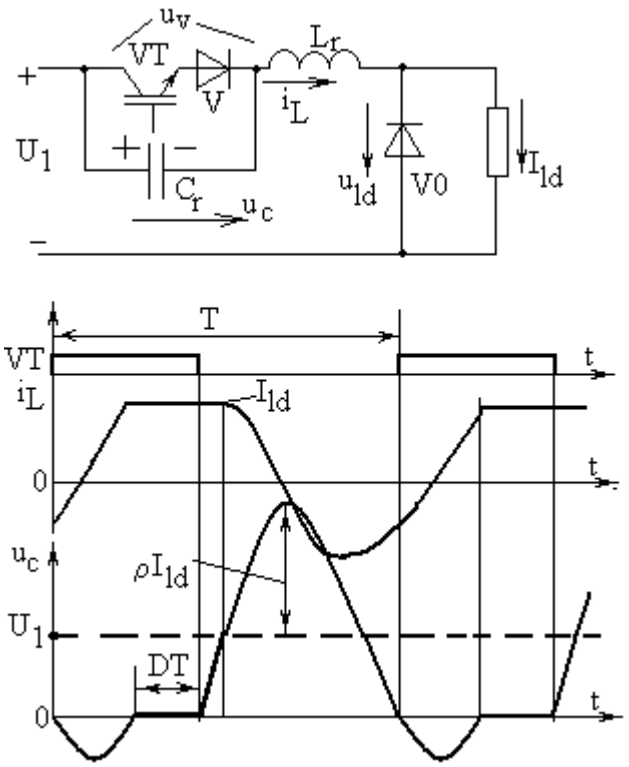

Fig. 6.16. Full wave quasi-resonant ZV Buck converter

6.4.2. Zero-Voltage transition converter

Regulation effect in the QR schemes discussed above can be obtained only applying different switching frequencies of transistor, i.e. using PFM control principle. That is certain disadvantage of converter. Ordinary PWM control can be obtained using in converter schemes with oscillating transition processes instead of one transistor switch two, one of which is the main but other an auxiliary. Such scheme of BUCK converter is presented in Fig. 6.17 where transistor VT1 is the main but VT2 – an auxiliary. The main transistor is bypassed with capacitor C1 and reverse diode V1 that both allow to obtain an oscillating turn-on and turn-off processes of the main transistor at zero voltage across the transistor. Auxiliary transistor also is turned-on at zero current of auxiliary circuit with coil L and turned-off at instant when diode V2 is conducting and transistor's VT2 voltage is zero.

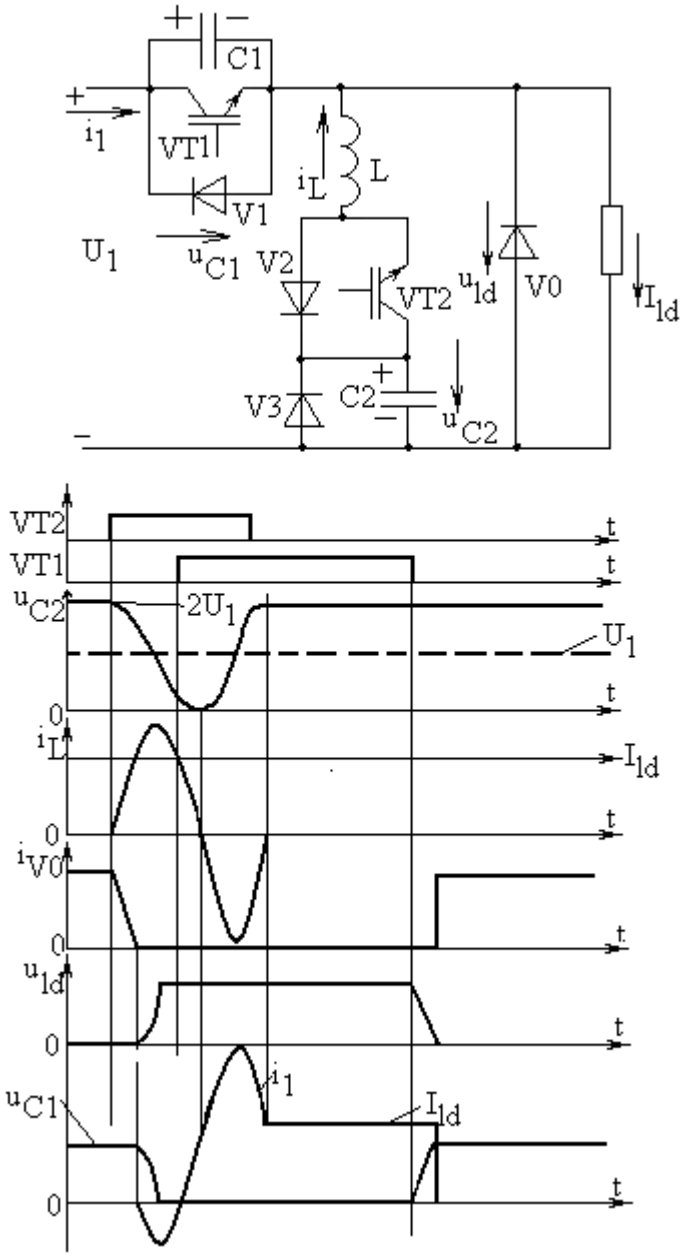

Fig. 6.17. Zero-voltage transition BUCK converter

Switching cycle starts with turn-on of transistor VT2 through which before capacitor C_2 was charged to the value $2U_1$. When current of coil L is equal to the load one the clamp diode stops conduct current and the oscillating process continues through previous charged to voltage U_1 capacitor C1 and supply circuit. Voltage of the both capacitors is decreasing and when $u_{c1}=0$ the process continues through the diode V1 when voltage across the transistor VT1 is zero and transistor can be activated for turn-on. When current of the coil L changes in oscillating process its polarity then diode V2 conducts and auxiliary transistor can be turned-off at zero voltage across it. Oscillating process is arising with turn-on of the both transistors finishes at charging of capacitor C2 up to $2U_1$ but the main transistor remains in turned-on condition on the all duty cycle, which finishes with turn-off of VT1, charging of capacitor C1 and transfer of load current to the load clamping diode V0.

Operation of the scheme can be provided in PWM mode at constant switching frequency of transistors, but the duration of oscillating processes has to be limited with the required minimal achieved load voltage.

6.4.3. Resonant Converters

Series load mode resonant converter scheme is presented in Fig. 6.18. Here resonant circuit comprises in series connected the resonant inductance L_r and resonant capacitor C_r. Introduction of resonant circuit in converter scheme provides possibility of soft switching of converter's transistors.

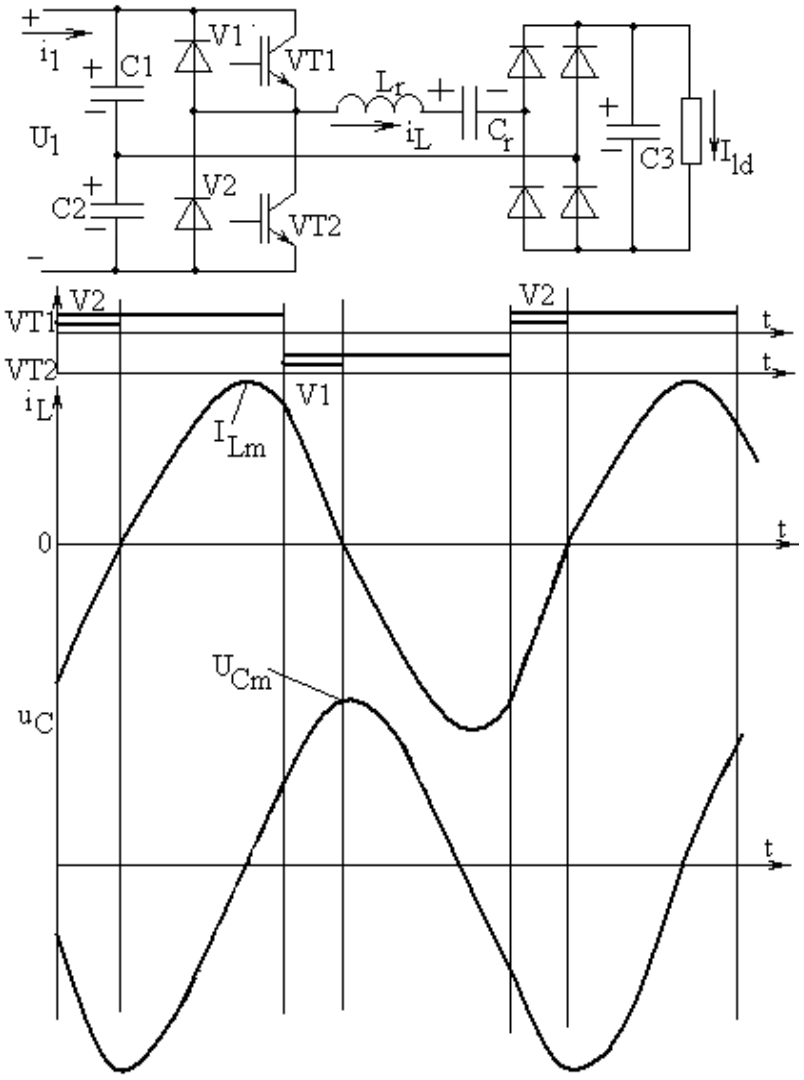

Fig. 6.18. Load mode series resonant converter scheme and waveforms at $\omega_{sw} \geq \omega_r$

In the scheme both transistors VT1 and VT2 are triggered alternatively. Let us assume that at instant when VT1 is triggered a current in the resonant circuit is with a negative sign and it means that in the first stage it is passed through the diode V1 and source capacitor C1. By influence of polarity of applied voltage current i_L is going to change its polarity and in instant when i_L=0 current starts its way through the transistor VT1. When transistor VT2 is turned-on in the first stage current i_L is with a positive sign and it means that it is really passing through

the diodeV2 and source capacitor C2 voltage of which operates against the current and it is going to the negative polarity. Again at instant when i_L=0 the transistor VT2 starts to conduct and so on.

Process presented is related to the case when control switching frequency is higher or equal to the resonant frequency. Then the load current is continuous and this case really is most applied. Transistors are turned-on at current transfer through zero level, i.e. loss-less but turn-off process takes place at current passing through transistor, i.e. with switching losses. That is disadvantage of the scheme.

Accurate calculation of the processes is difficult but in the case when $\omega_{sw} = \omega_r$ calculation is possible. For that it can be applied that a total voltage across all resonant circuit is zero, i.e. $0.5U_1 = U_{ld}$, where it is assumed that load voltage is smoothed one. Averaged meaning of load current depends on amplitude of current in resonant circuit:

$$I_{ld} = \frac{2I_{Lm}}{\pi} = \frac{U_{ld}}{R} \quad . \tag{6-49}$$

Therefore

$$I_{Lm} = \frac{0.5\pi U_1}{2R} \tag{6-50}$$

and amplitude of capacitor voltage is

$$U_{Cm} = \rho I_{Lm} \quad , \tag{6-51}$$

but DC supply source current can be calculated as

$$I_1 = 0.5I_{ld} = \frac{0.5U_1}{R} \quad . \tag{6-52}$$

Here $\rho = \sqrt{\frac{L_r}{C_r}}$ is resonant impedance, but resonant frequency is $\omega_r = \sqrt{\frac{1}{L_r C_r}}$.

Working in resonance case allows operating without power loss at switching of transistors but those are under stress of amplitudes of resonant circuit current. Due to very small switching losses in transistors it is possible to operate with very high (above 100 kHz) switching frequency which allows minimizing size of transformer in the load circuit at realizing very high values of power. Power depends on the value of supply voltage and load resistance attributed to the primary winding of transformer (in the scheme Fig.18 is presented a transformer-less version).

Calculation example.

DC supply voltage U_1=100V but load resistance in the scheme Fig.6.18. is 2Ω. Inductance of resonant circuit is 20μH but its capacitance is 5 μF. Calculate load voltage, amplitude of current in resonant circuit, amplitude of capacitor voltage and active power realized in the system!

1 – resonant frequency $\omega_r = \sqrt{\frac{1 \cdot 10^{12}}{20 \cdot 5}} = 10^5 rad/s$ which accords to frequency $f_r = \frac{10^5}{2\pi} = 15923.6Hz$;

2 – resonant impedance $\rho = \sqrt{\frac{L_r}{C_r}} = \sqrt{\frac{20}{5}} = 2\Omega$;

3 – load voltage $U_{ld} = 0.5U_1 = 50V$;

4 – amplitude of resonant circuit current $I_{Lm} = \frac{\pi U_1}{4R} = \frac{\pi \cdot 100}{4 \cdot 2} = 39.3A$;

5 – amplitude of resonant capacitor voltage

$$U_{Cm} = \rho I_{Lm} = 2 \cdot 39.3 = 78.6V ;$$

6 – DC supply current $I_1 = 0.5I_{ld} = 0.5 \cdot \frac{50}{2} = 12.5A$;

7 – power realized $P=I_1.U_1=1250$ W.

When switching frequency is above the resonant one a resonant half-cycle of current is shortened by closing of transistors before end of the resonant half-cycle when current is transferred to the diodes of scheme and it circulates through DC source capacitors (Fig.6.19.) decreasing an averaged meaning of supply current. It means that power realized in system as well as the load voltage are both decreasing. At circulation of current the voltage across the input of resonant circuit is changing its polarity and to the resonant circuit is applied a reverse polarity voltage $U_{ld}+0.5U_1$ to compare with transistors conductivity interval when applied voltage is $0.5U_1-U_{ld}$. It means that current in the resonant circuit in the reverse voltage intervals is decreasing very fast and shape of the current at this is not exactly of sinus wave.

Calculation of the processes at such operation is quite difficult and can be provided only in very simplified way.

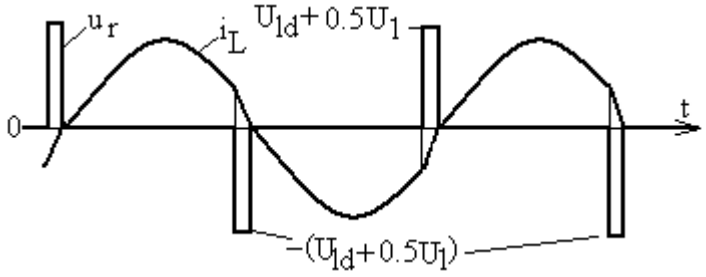

Fig. 6.19. Waveforms of current through resonant circuit and voltage across it at $\omega_s > \omega_r$

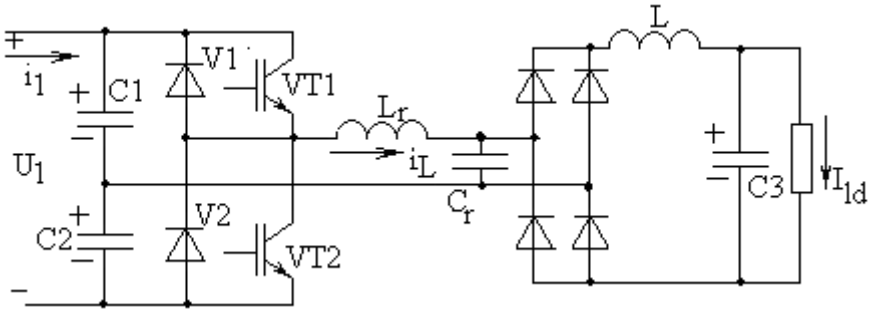

Fig. 6.20. Scheme of a parallel load mode resonant converter

It is possible to apply another version of load mode resonant converter when resonant capacitor is inserted in parallel to an input of rectifier bridge (Fig 6.20.). In the scheme voltage shape of the smoothing capacitor C3 of load current directly depends on the voltage shape of the resonant capacitor, i.e. capacitor C3 voltage has large scale ripples and therefore for their smoothing coil L has to be applied at the output of the rectifier.

If the load mode series resonant converter can be accepted more than the current source converter CSC because its load voltage depends on shape of resonant current then the parallel mode load resonant converter regards in large extent to the group of voltage source converters VSC because its load voltage does not depend on resonant coil current.

Waveforms of the main currents and voltages of the converter are presented in Fig 6.21. Input voltage of the resonant circuit u_{10} is of the AC square shape with amplitude $0.5U_1$ and changes in phase with the transistors triggering diagram. An averaged meaning of the resonant capacitor voltage per its half cycle is equal to the load voltage U_{ld} but averaged meaning of resonant coil current assuming its sinus shape in its half cycle is equal to the load current I_{ld} . When instantaneous meanings of the capacitor's AC mode voltage are equal to the u_{10} amplitude the current of the coil reaches its amplitude values I_{Lm} but when instantaneous meanings of coil's current are equal to the load current value a current of capacitor is zero and its voltage reaches its amplitudes U_{Cm} . Assuming a sine-form for capacitor voltage and coil current it can be stated that approximately

$$\frac{U_{Cm}}{I_{ld}} = \frac{\pi R}{2} \tag{6-53}$$

and

$$\frac{I_{Lm}}{I_{ld}} = \frac{\pi R}{2\rho} \ , \tag{6-54}$$

where ρ is resonant impedance.

In the supply circuit circulating current exists because the current of the coil is shifted in phase by angle φ in lagging direction and at turn-off for instance the transistor VT2 in the first stage of process current of coil is with negative sign and is passing through diode V1 back to the supply source. Connection between magnitude of coil current and averaged current of supply can be described as

$$I_1 = \frac{2I_{Lm}}{\pi}\cos\varphi \ . \tag{6-55}$$

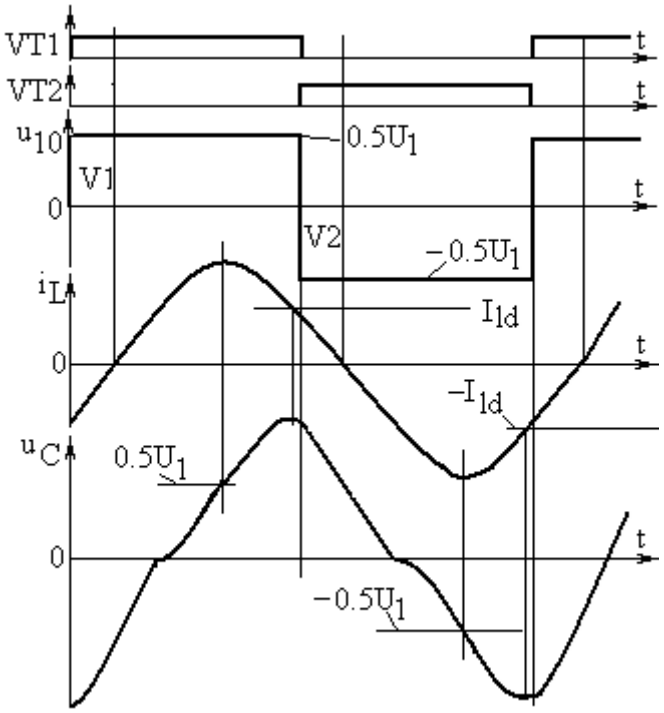

Fig. 6.21. Waveforms of input voltage of resonant circuit, its coil's current and capacitor's voltage

7. Selected Topics in Power Electronics

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7.1. Power Electronics in Energy Transmission

7.1.1. General construction of the system

A thyristor system consists of two blocks of controlled rectifiers and DC line (Fig.7.1.).

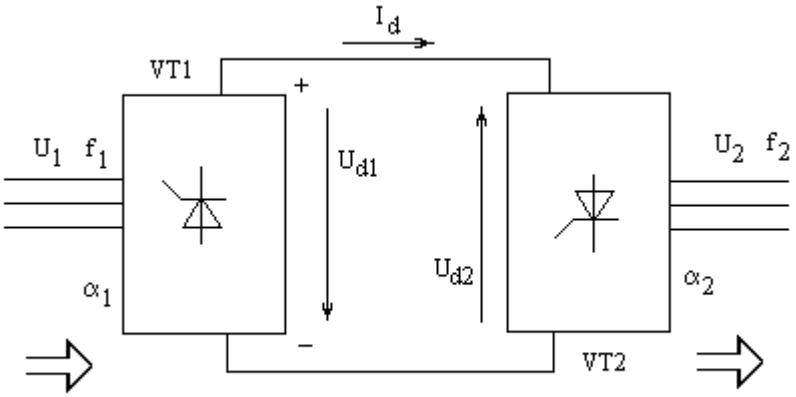

Fig. 7.1. Direct current power transmission with controlled rectifiers

The input of each rectifier can be supplied with different AC voltage and frequency. The current in the DC line I_d can flow in one direction only in accordance with the direction of the rectifier thyristors conductivity (clock-wise direction in the figure). If the energy from AC system with U_1, f_1 is transmitted to the system with U_2, f_2, then the rectifier VT1 is operating in the rectifier (generating) mode, when $U_{d1}>0$, but rectifier VT2 is operating as an inverter, through which DC power $P_d=U_dI_d$ is recuperated to the second AC system [1,2,3].

The operation regime of the controlled rectifier is changed with the changing of the control angle α. The output voltage of the rectifier is

$$U_d = U_{d0}\cos\alpha, \tag{7-1}$$

where α can change within the range from 0^o to 180^o. It means that operating in the rectifier regime VT1 has control angle in the range from 0^o to 90^o, but operation in the inverter regime – rectifier VT2 the control angle α_2 is within the range between 90^o and 180^o.

Value U_{d0} in expression (7-1) is an ideal output voltage of the controlled rectifier, if α=0, i.e. for the regime of diode rectifier. The value of U_{d0} depends on the topology of the rectifier scheme. For example, if the controlled rectifier is formed as a three-phase bridge scheme then

$$U_{d0} = 1{,}35U_l, \tag{7-2}$$

where U_l is the phase-to-phase voltage of AC system.

In a real rectifier the output voltage is lower than that defined in (7-1) because of the commutation processes, therefore

$$U_d = U_{d0}\cos\alpha - \Delta U_\gamma, \tag{7-3}$$

where ΔUγ is the voltage drop formed during the commutation process.

Similar commutation processes take place also in the rectifier operating in the inverter mode, however the real U_d absolute value of the controlled rectifier in this case is higher than that defined in (7-1). The simplified substitution scheme of DC transmission is in Fig.7.2.

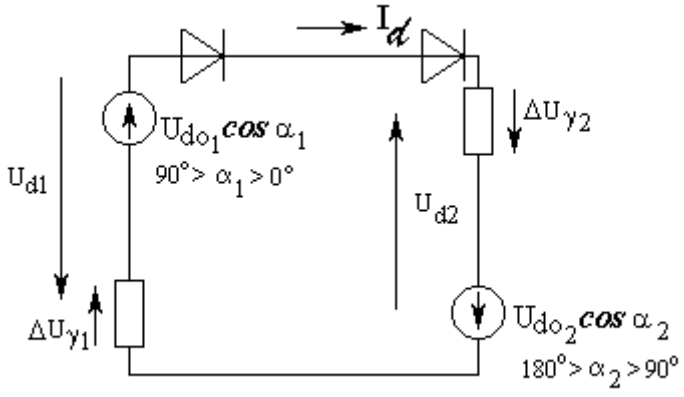

Fig. 7.2. Substitution scheme of DC transmission thyristor system

From this figure

$$U_{d01}\cos\alpha_1 - \Delta U_{\gamma 1} = -U_{d02}\cos\alpha_2 + \Delta U_{\gamma 2} \tag{7-4}$$

For three-phase bridge rectifier

$$\Delta U_{\gamma} = I_d \frac{6X_a}{2\pi}, \tag{7-5}$$

where X_a is an inductive resistance of AC system ($X_a=2\pi fL_a$).

For functioning of DC transmission system the generated DC voltage should be lower than (U_{d0}- ΔUγ). Expression (7-4) can be applied to determine the necessary control angles of the rectifiers.

Example. Calculate angles α_1 and α_2, if U_{l1}=30kV, U_{l2}=50kV, $f_1=f_2$=50Hz, L_{a1}=1mH, L_{a2}=1,5mH, U_{d1}=25kV, I_d=200A. The topology of the rectifier is three-phase bridge scheme. The flow of power is from system 1 to system2.

1. commutation voltage drops

$$\Delta U_{\gamma 1} = 200\frac{6\cdot 2\pi\cdot 50\cdot 0{,}01}{2\pi} = 600\text{V};$$

$$\Delta U_{\gamma 2} = 200\frac{6\cdot 2\pi\cdot 50\cdot 0{,}015}{2\pi} = 900V.$$

2. Calculated voltages of the rectifiers

$$U_{d01} = 1{,}35\cdot 30\cdot 10^3 = 40{,}5kV;$$

$$U_{d02} = 1{,}35\cdot 50\cdot 10^3 = 67{,}5kV.$$

3. Control angles

$$\alpha_1 = \arccos \frac{25600}{40500} = 50{,}79^\circ el\ .$$

$$\alpha_2 = \arccos \frac{-24102{,}66}{6700} = 110{,}0^\circ el\ .$$

7.1.2. Practical realization of the thyristor DC transmission system

The simplest DC transmission is realized by means of one wire (cable) using ground as the second. This system is called a monopolar and its simplified scheme is demonstrated in Fig.7.3.

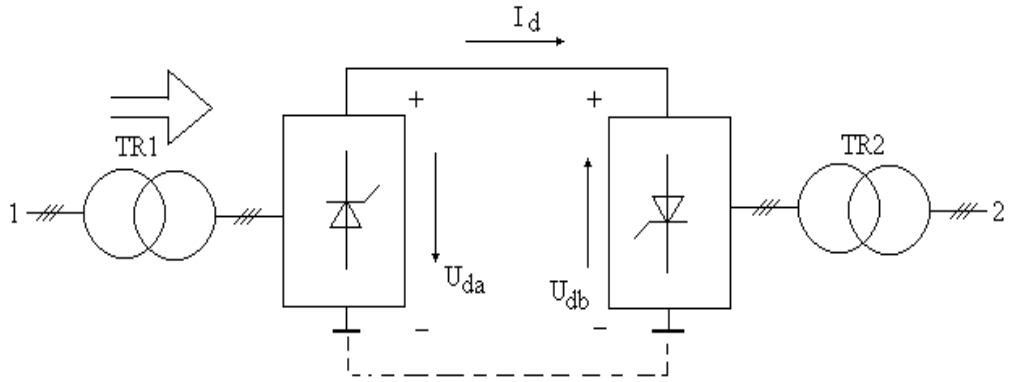

Fig. 7.3. Topology of monopolar DC transmission system

If the energy is transmitted from system 1 to system 2, then the polarity of the DC parts of the rectifiers is in accordance with that demonstrated in the figure. If the energy is transmitted from system 2 to system 1 then the polarity is opposite. However DC current flows in one direction only [3].

As the ground resistance is not determined the voltage drop in the ground circuit is also not defined. The second disadvantage is the influence of the ground current on the metal structures causing the corrosion. To avoid this special corrosion protection is applied.

Taking into account everything mentioned above the monopolar operation mode is usually applied for the relatively short-time operation (some hours or days) and mostly for emergency cases.

The basic transmission system is bipolar with two cables, when each AC system includes two blocks of thyristor rectifiers each with its own transformer (Fig.7.4).

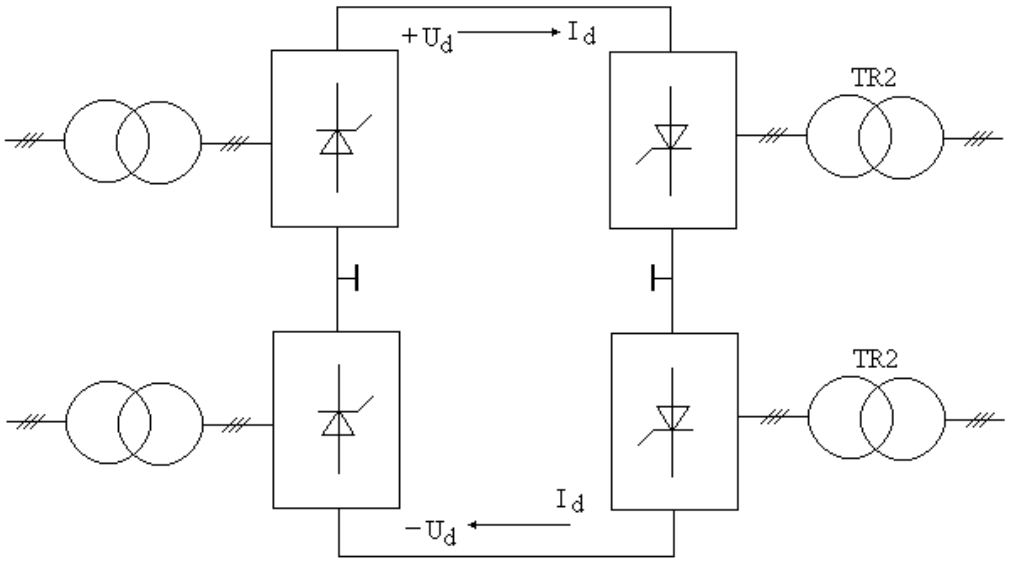

Fig.7.4. Bipolar system of transmission system

In this system the one wire to ground voltage is $+U_d$, the voltage of the second wire is $-U_d$, but if current is of the same value in both wires then the ground current is zero, i.e. the transmission system does not form the corrosion current in the metallic structures.

If to compare it with monopolar system with the same parameters of the rectifier groups bipolar system provides double higher power transmission: $P_d = 2U_d I_d$. If one of the blocks breaks its operation the scheme can operate in the regime of monopolar circuit [3].

The current transmitted by the bipolar DC line depends on the both AC voltages only, Fig.7.5.

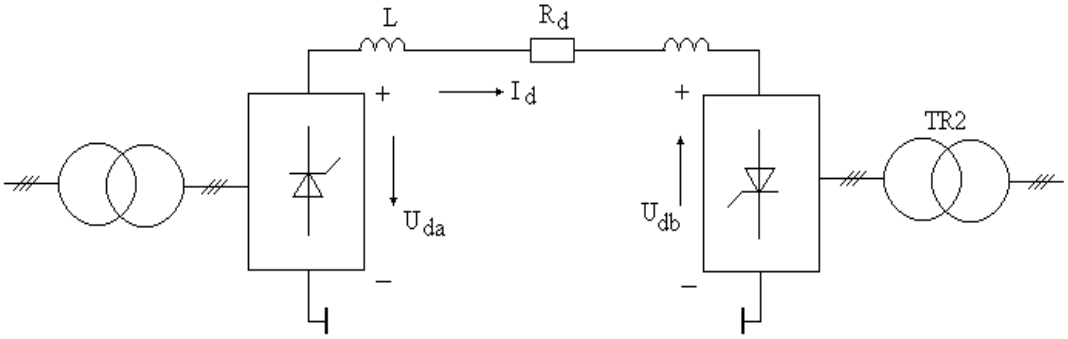

Fig. 7.5. Scheme for bipolar transmission current calculation

The value of the current is

$$I_d = \frac{U_{da} + U_{db}}{R_d}, \qquad (7\text{-}6)$$

where, if $U_{da}>0$, then $U_{db}<0$, but in their absolute values these voltages do not differ a lot;

R_d – total resistance of the transmission wire (cable) and current smoothing inductivity.

For example, if R_d=1Ω, the transmitted current is 500A, then, if U_{da}=100kV, then U_{db}= -99,5kV.

The active power generated at the output rectifier is

$$P_{dg} = U_{da} \cdot I_d ,$$

but the inverting input of the rectifier

$$P_{di} = -U_{db} \cdot I_d = -U_{db} \frac{U_{da} + U_{db}}{R_d} .$$

The circuit of the practical realization of the rectifier substation of the bipolar transmission corresponds to that given in Fig. 7.6. [3].

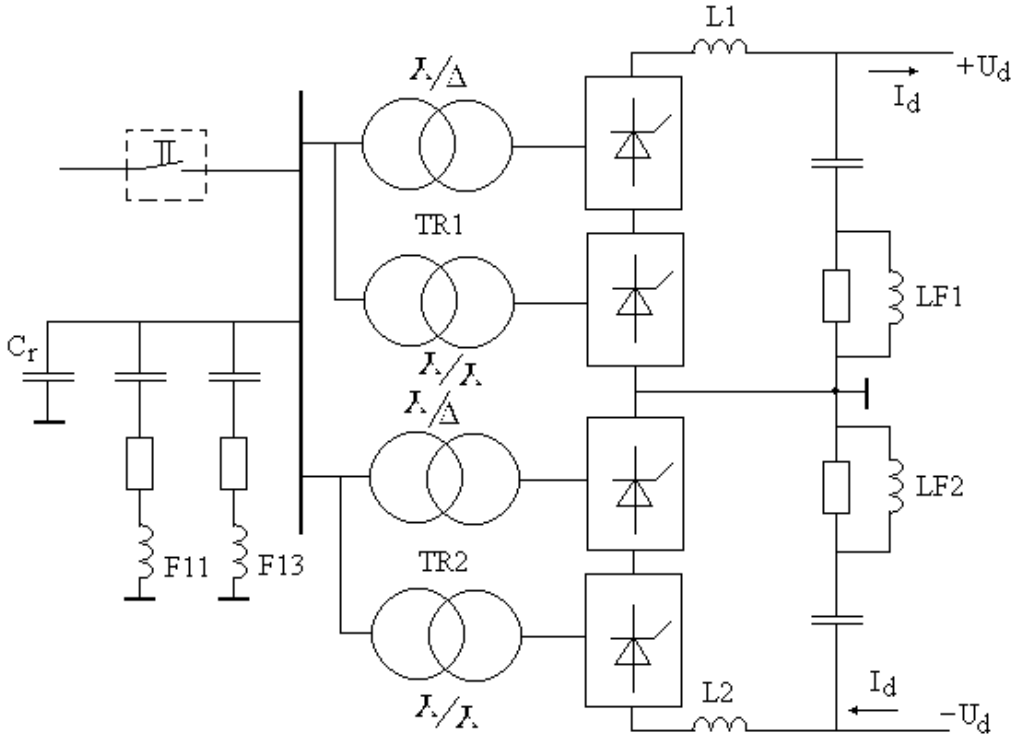

Fig. 7.6. Approximate scheme of the rectifier substation

AC transmission line is connected to the terminals of the station by means of protection switches. The substation also contains capacitors of the reactive power compensation C_r. This reactive power is calculated as the following:

$$Q = \frac{I_d \cdot U_{1l}}{k_{TRZ}} \sqrt{29{,}8 - 29{,}16 \cos^2 \alpha} , \qquad (7\text{-}7)$$

where U_{1l} is the phase-to-phase voltage of the AC network, k_{TRZ} – factor of transforming of Y-Y groups, I_d – transmitted current, α – rectifiers control angle.

In these systems the control angle of the generating rectifier (that operating in rectifying mode) usually is 10-15º. The transforming factor of the transformer is selected in accordance

with these angles and the voltage of AC line. For example, if U_{1l} =110kV, but U_d=100kV, then for Y-Y group of transformer of bipolar transmission system

$$k_{TRZ} = \frac{2{,}7U_{1l}|\cos\alpha|}{U_d} = 2{,}92\,.$$

If U_{1l} =110kV, α=10º, I_d=500A, U_d=100kV, then for the bipolar system

$$P_d = 2U_d I_d = 100MW;$$

$$S = \sqrt{3}U_{1l} \cdot 2I_d \frac{1{,}577}{k_{TRZ}} =$$

$$= \sqrt{3} \cdot 110 \cdot 2 \cdot 0{,}5 \cdot \frac{1{,}577}{2{,}92} 10^6 = 102{,}9MVA;$$

$$Q = \sqrt{S^2 - P_d^2} = 24{,}25M \text{ var}\,.$$

This power is also a reactive power of capacitors C_r .

Therefore the AC terminals supply the L-C-R filters of 11th and 13th harmonic components.

An important element of the substation is a thyristor block where each leg of the rectifier consists of some thyristor modules connected in series each containing 3-4 series connected thyritors.

As the transmitted voltages are high then the voltage of three-phase bridge operates with doubled reserve

$$U_{pl} \geq 1{,}05U_d\,.$$

At the same time the rated voltage of the thyristors does not exceed 10 kV. Therefore the rectifier's leg should contain more thyristors in series. Thus, if U_d=300kV, the rated voltage of the thyristor is 6kV, then the leg contains 53 thyristors in series, i.e. 14 modules with 4 thyristors in each.

7.1.3. DC transmission with transistor converters

Applying the thyristors at the rectifying and inverting substations causes some problems for the transmission system:

- the AC network current is not of sine-form that results in the necessity to apply complicated and expensive filter;
- reactive power is consumed from the AC network as the thyristor converters operate with current shift, therefore the reactive power compensation systems should be used;
- necessity to match the operation of both generating and inverting substations.

At the end of the 20th century powerful transistors with insulated gate were developed (IGBT). These transistors can operate with voltage 6,5kV and current 2000A, and their control is realized by means of voltage signals without current consumption in the stationary regimes. Development of these devices gave an opportunity to design new converters with improved characteristics [1,2].

One of the modern types of converters is an active reverse rectifier designed as a three-phase bridge topology with diode-transistor elements in each leg (Fig.7.7.). The diodes provide the flow of current from AC to DC circuit with capacitor C, the voltage of which can be with positive sign only and operated opposite to the diodes current.

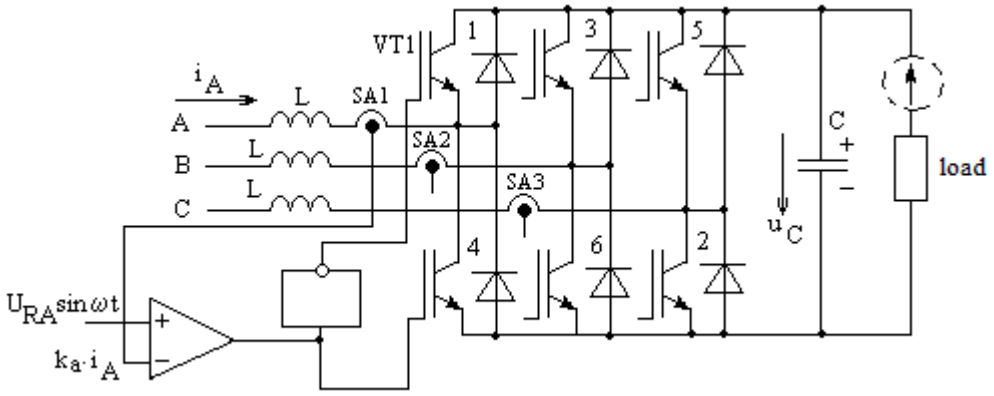

Fig. 7.7. Active reverse rectifier (control for A phase only)

The transistors in their turn provide the flow from DC to AC side of the circuit and the capacitor voltage u_C causes the increasing of the transistors current.

If the energy is transmitted from AC line to DC then the phase angle between phase voltage and current is zero. Figure 7.2.7 demonstrates possible solution for A phase with connected sensor SA1 with factor k_a and signal comparison with reference $U_{RA}\sin\omega t$.

When $i_A \cdot k_a > U_{RA}\sin\omega t$, the control signal is supplied to transistor VT1. If $i_A > 0$, current i_A flows through the diode and capacitor with opposite voltage, and instant value of the current is decreasing. If $i_A < 0$, the current is conducted through transistor VT1 and the operation of capacitor results in the negative instant value of throttle current.

When $i_A \cdot k_a < U_{RA}\sin\omega t$, the control signal is supplied to transistor 4. If $i_A > 0$, the current is conducted through capacitor with the coordinated voltage, and i_A is increasing. If $i_A < 0$, the current flow through the diode and the value of the current is positive.

The control of B and C phase transistors is organized in the similar way with correspondent shifting to 120^o each. B phase signal is fixed with sensor SA2, but the comparator controls transistors 3 and 6. C phase signal is fixed with sensor SA3, but the comparator controls transistors 5 and 2.

The switching results in the current close to sine-wave form in the circuit of throttle with amplitude $I_{Lm}=U_{RA} \cdot k_a$, with no shifting in phase of voltage and current at the generating substation. To provide the operation of the active rectifier in the inverting mode the DC load circuit is replaced with DC supply source (Fig.7.7.). The reference voltage of each phase of the inverting substation is out of phase with AC network voltage. It results in each phase current and voltage of the inverting station is out of phase as well (Fig. 7.8.).

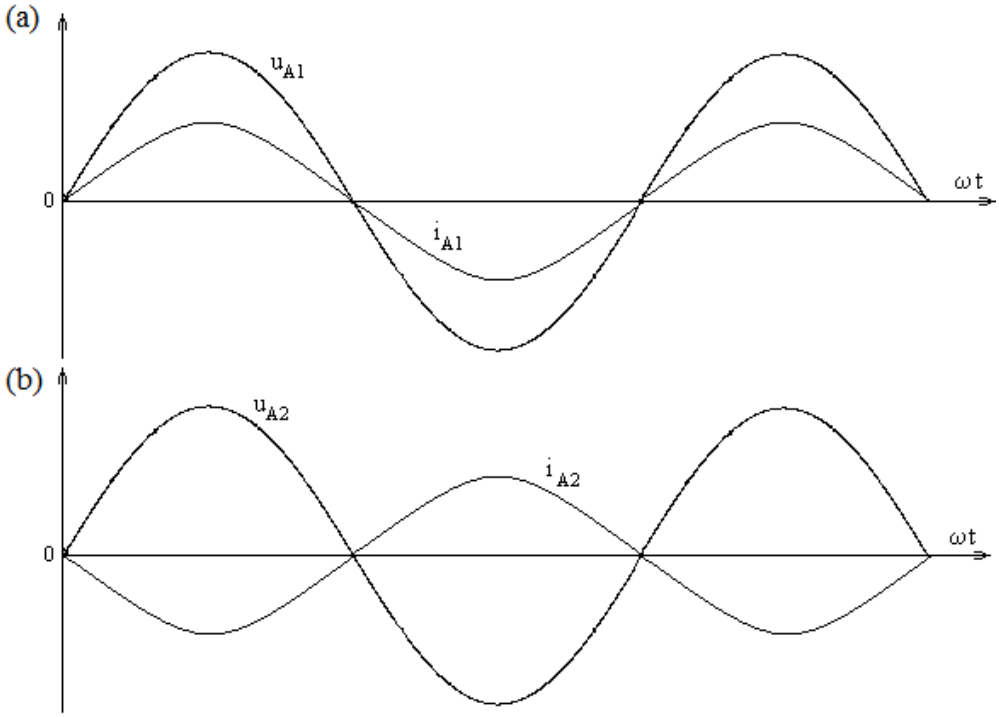

Fig. 7.8. Diagrams of phase current and voltage of generating (a) and inverting (b) substations with active convereters

The simplified scheme of the both converters is in Fig.7.9.

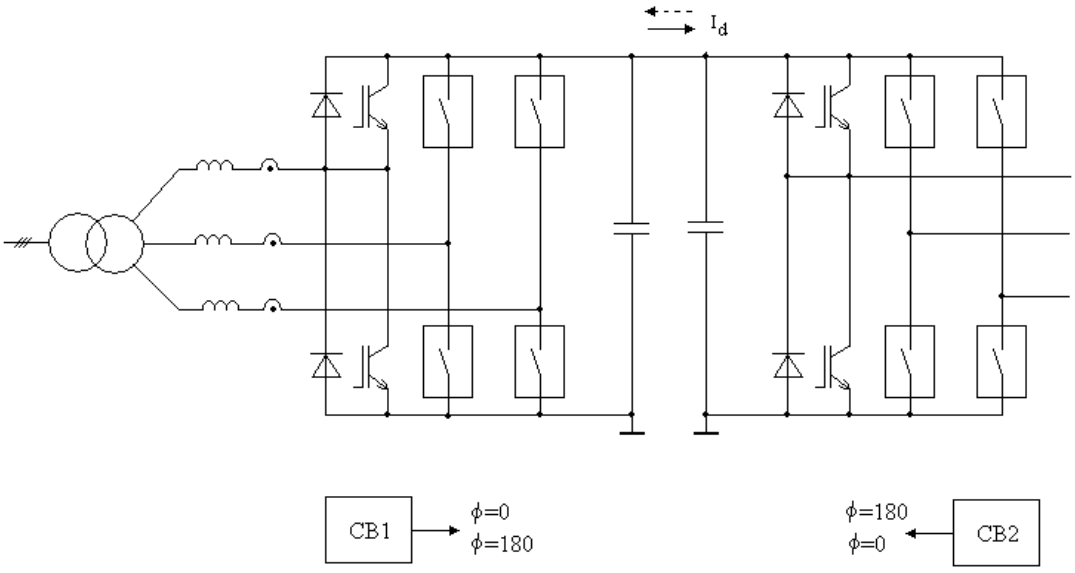

Fig.7.9. Simplified circuit of DC transmission line on the base of transistor converters

Both AC systems have the same active power and it means that each should be preset with the correspondent current amplitude of AC line. If the phase-to-phase voltages and frequencies of the both systems are the same then the amplitudes of the currents should be the same also. If the frequencies and voltages are not the same then taking into account the equality of the both systems capacitors voltages

$$U_{m1}^2 + (\omega_1 L_1 I_{m1})^2 = U_{m2}^2 + (\omega_2 L_2 I_{m2})^2 . \quad (7\text{-}8)$$

In this system if at both stations correspondent current amplitudes are set the network current is close to sine-wave form with low ripples. The form of this current is easy to improve by means of passive filters.

Example. Calculate necessary voltage and current of the AC system to provide DC transmission with voltage 150kV and power 100MW if total inductivity of one phase circuit (throttle and winding of transformer) is 5 mH, but that of the second 5 mH. Frequencies of the both systems are 50 Hz.

1.The transmitted power is related to the correspondent three-phase AC system phase voltage and current amplitude as

$$S = 3\frac{U_m . I_m}{2} = 1{,}5 U_m I_m . \quad (7\text{-}9)$$

2.The capacitor voltage can be expressed as

$$U_c = 2\sqrt{U_m^2 + (\omega L \frac{S}{1{,}5U_m})^2} . \quad (7\text{-}10)$$

3.The phase voltage amplitude of the first system with L=5 mH from this expression is U_{1m}=74,987 kV, but the phase current amplitude in accordance with power expression is I_{1m}=889 A. The rms values are 52,8 kV and 626 A.

4.For the second system with L=10 mH the amplitude of the phase voltage is U_{2m}=74,948 kV, but the current amplitude - I_{2m}=889,5 A.

7.1.4. Practical realization of the system

Similar system of DC transmission is realized between Estonia and Finland ESTLINK started its operation in January, 2007. The power of the system is 350 MW and the double direction transmission is with voltages ±150 kV.

The simplified scheme of this system is in Fig. 7.10. [4]

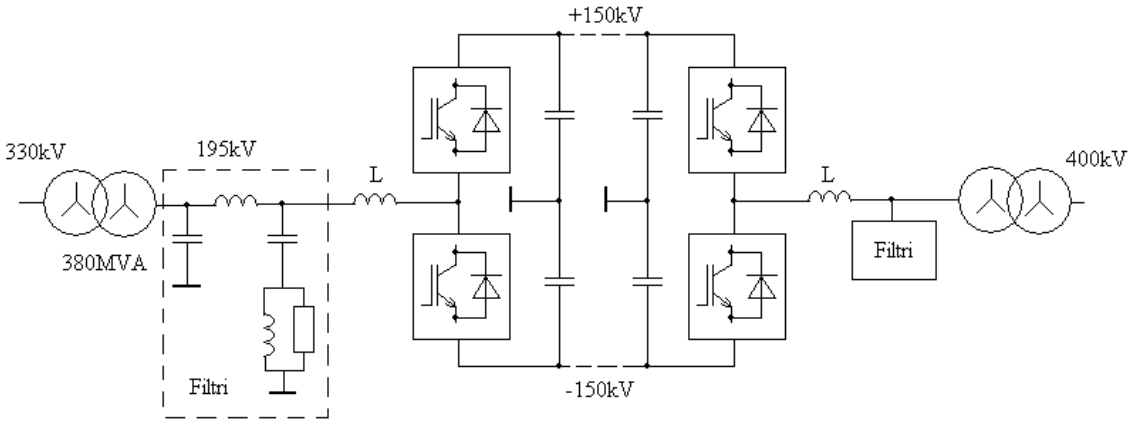

Fig.7.10. Simplified scheme of ESTLINK transmission line

Each leg of the three-phase bridge type converter consists of in series connected IGBT blocks. Each block contains 24 parallel transistors, shunted with diodes in opposite direction. The control is realized with constant switching frequency 1150 Hz and by means of pulse-width modulation method. The filters are tuned for frequencies of 1600 and 3000 Hz.

Under water cable between Estonia and Finland is made of copper conductors with total cross-section area of 1000 mm^2 and outside diameter about 80 mm. Mass of 1 m of the cable is 95 kg. 74 km of the cable is placed under the water.

References

1. Power Electronics. Handbook/ Muhammad H.Rashid, Editor in chief. Academic Press: NY,2001, 895 pp.
2. N. Mohan, T.Undeland, W. Robbins Power Electronics: Converters, Applications and Design, NY, 1989, 667 pp.
3. Oke Ekstrem High Power Electronics HVDC and SVC. – Stockholm:KTH, 1990, 600 pp.
4. Enerģija un pasaule, 2007.g. Nr1

7.2. Power Electronics in Renewable Energy Production

7.2.1. Renewable Energy Sources

Energy cannot be created or destroyed, it has always existed in different forms. On the Earth we are receiving solar energy from the Sun as radiation. The Sun is heating our planet and as a result we are getting wind, snow, rain, rivers, lakes, oceans, tidal flows, waves, growing plants and deserts.

Water, wind, light and biomass can be used in renewable electrical energy sources. After separation from other elements, hydrogen can be used in electricity production. Generally also production of methanol from waste and usage in electricity production can be classified as Renewable energy source.

7.2.2. Renewable Electrical Energy production plants and systems

Hydrolic power plants.

Histroically well known are the hydroelectric power plants. Water wheels and different types of turbines are converting potential energy to kinetic bringing to the rotation of electric generators.

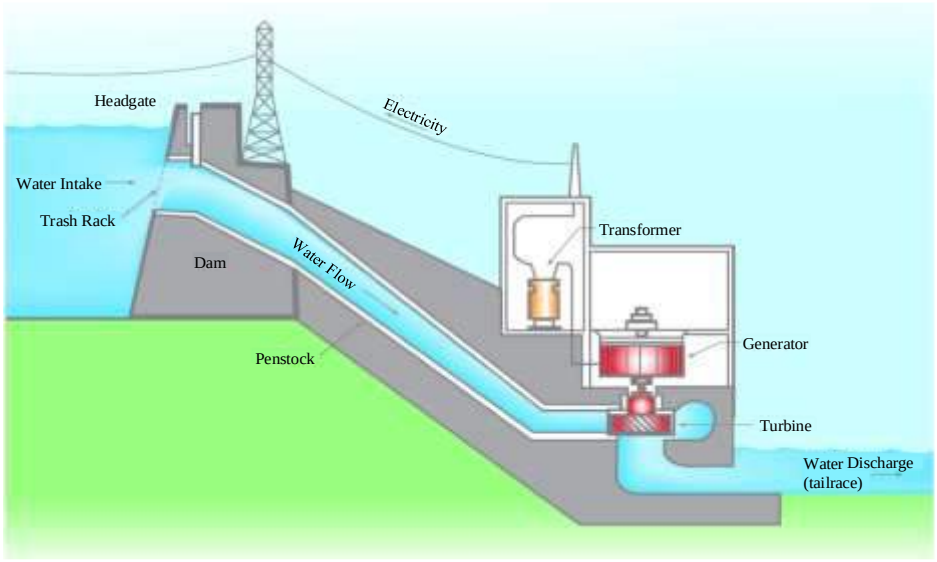

Fig. 7.11. Operating principle of the hydroelectric power station (source: Power Electrical & High Voltage Engineering web portal, 2009)

Fig.7.11 shows the connection of hydroturbine with electrical generator. Generated electrical energy through transformer is supplying high voltage grid.

The golden age of hydropower was the first half of the twentieth century, before oil took over as the dominant force in energy provision. Europe and North America built dams and hydropower stations at a rapid rate, exploiting up to 50 per cent of the technically available potential. The small hydro industry has been on the decline since the 1960s. Small hydro cannot compete with existing fossil fuel or nuclear power stations without environmental incentives to use non-polluting power sources. The arrival of the Renewables Obligation in April 2002 has greatly boosted the value of hydropower sold into the grid.

Hydropower has various degrees of ‘smallness’. There is still no internationally agreed definition of ‘small’ hydro; the upper limit varies between 2.5 and 25 MW.

Wind power plants.

Nowadays Wind is a very important alternative energy source. Wind energy was used in different forms centuries ago, but only in the second half of 20^{th} century the equipment for efficient electrical energy production was created.

a *b*

Fig. 7.12. Wind Power Plants: a) onshore (source: Creative Commons, Leaflet, 2004); b) offshore (source: IND Themes, GreenTechnology, 2013)

Most wind turbines have been installed in wind farms (Fig.7.12.), which are groups of turbines dedicated to supplying electricity into the local electricity distribution system. Wind farms are used effectively as small power stations, which give an output depending on the strength of the wind. Wind farm turbines, often known as utility-scale turbines, are generally very large structures of 50 metres or more in diameter with rated powers up to 12 MW and growing.

Wind turbines concentrate a low-energy density source, the wind, into a concentrated form of energy, electricity. They do this by intercepting a large volume of air passing through the rotor-swept area.

The rotor blades have an aerodynamic shape, which generates lift force. This lift produces torque in the rotor, causing the rotor to rotate.

Power output at high windspeeds is often limited to a rated value by changing the aerodynamic performance of the blade, either by actively changing the pitch angle or by employing passive aerodynamic stall.

The rotor is connected to an electrical generator. Most of the small turbine rotors are directly coupled to specially designed low-speed generators. In larger turbines, many employ gearboxes increase the rotational speed of the output shaft to that of more conventional electrical machines.

Small direct-drive turbines tend to use permanent magnet machines and generate at variable speed. Larger turbines tend to generate at a fixed speed using induction machines, but there is now a tendency towards full variable speed in the large utility-scale turbines.

The rotor shaft is supported in bearings housed in a structure at the top of a tower and the whole may be contained within a cover or nacelle.

Fig.7.13 shows the structure of the nacelle for wind turbine.

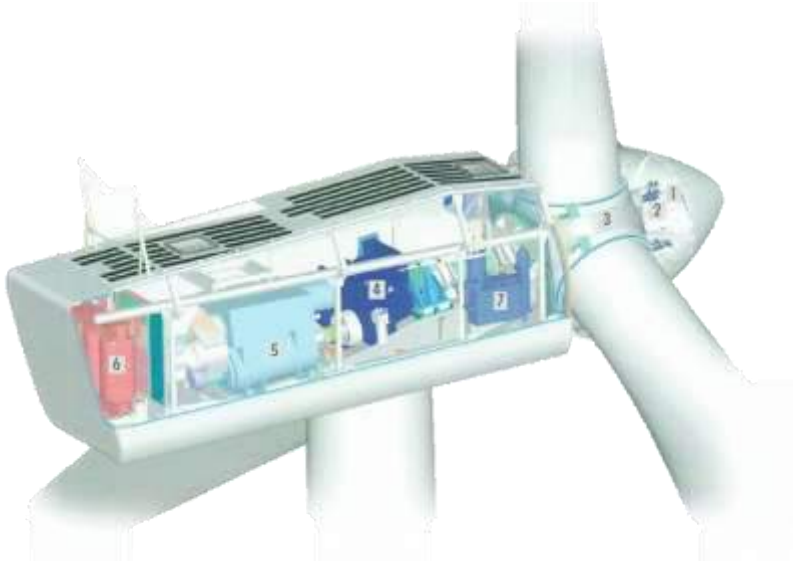

Fig. 7.13. Typical structure of the nacelle for a horizontal three-blade grid-connected wind turbine (1 - hub controller, 2 - “pitch” control cylinders, 3 - blade hub, 4 - gearbox, 5 - generator, 6 - high voltage transformer, 7 - hydraulic unit) (source: Vestas, 2009)

The tower is usually as high as economically possible to reach into the highest wind region.

Electricity generated by the turbine passes through cables down the tower to the point of use. Larger fixed-speed turbines tend to generate mains-quality ac power directly using induction machines; variable-speed turbines use the rectifier/inverter route.

Solar power plants.

Global solar radiation also includes thermal energy for either heating fluid or for transformation to another form of energy. The *photovoltaic effect* consists of the direct transformation of the radiation energy into electricity without the intermediate production of heat.

Solar light is converted directly into electricity with modules consisting of many photovoltaic solar cells. Such solar cells are usually manufactured from thin films or wafers. They are semiconductor devices capable of converting radiated solar energy into dc current, with efficiencies varying from 3 to 31 %, depending on the technology, the light spectrum, temperature, design, and the material of the solar cell.

A photovoltaic electric system consists of photovoltaic modules, an electronic converter, a controller, and a bank of batteries. Each module is made of photovoltaic cells connected in series, parallel, or series/parallel, as a part of a panel supported by a mechanical structure.

Fig.7.14 shows a photovoltaic panel for electricity supply of stand alone remote equipment.

Fig. 7.14. Pole-mounted AC module (source: SolarTown, 2012)

Solar modules are a group of cells that transform the radiant light in dc electric power, usually in standard connections of 12, 24, or 48 V. They are usually composed of mono crystalline silicon cells, protected by antireflexive glass and by a special synthetic material. The number of modules to be used in a system is determined by the electric power consumption needs.

Fig. 7.15. PV Power Plant (source: U.S. Air Force, 2007)

There are many panels installed in PV Power Plant shown in Fig.7.15.

Hydrogen power plants.

Very important renewable energy source is Hydrogen and it can be also produced from biomass.

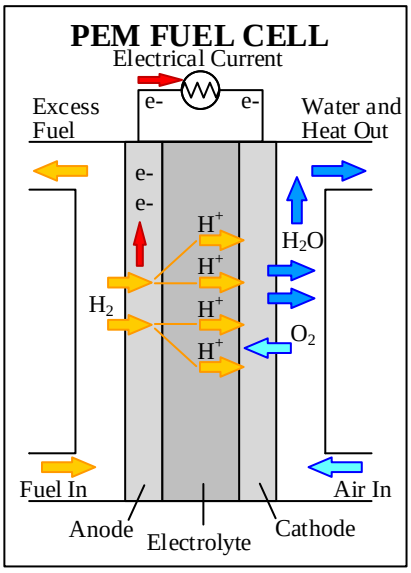

Figure 7.16. PEM Fuel Cell (source: U.S. Department of Energy, 2006)

Structure of Fuel cell is shown in Fig.7.16.

Fuel cells are electrochemical devices and in that fuel and oxidizer are supplied to fuel cells continually so that they can generate continuous electric power. Fuel cells are based purely on the electrochemical reaction. The hydrogen combines with the oxygen inside a combustion-free process, liberating electric power in a chemical reaction that is very sensitive to the operating temperature.

Fig. 7.17. In New York, U.S. the fuel cells from UTC Power generate 200 kilowatts each, providing a total of 1,4 megawatts of clean power (source: Image courtesy of UTC Power Corporation)

In Fig.7.17. is shown a large commercial application of Fuel Cell system for electric power generation.

There are different types of fuel cells classified according to their operation at low or high temperatures. Low-temperature PEM fuel cells (up to about 100^{o}C) are available and ready for mass production. The most compact systems are appropriate for powered electric vehicles and are available from 5 to 100 kW. High-temperature (about 1000^{o}C) SOFCs are typically used for industrial and large commercial applications and operate as decentralized stationary units of electric power generation.

In all described above Renewable Electrical Energy production plants are used advanced power electronic converters to connect generation units with consumers or electric grids.

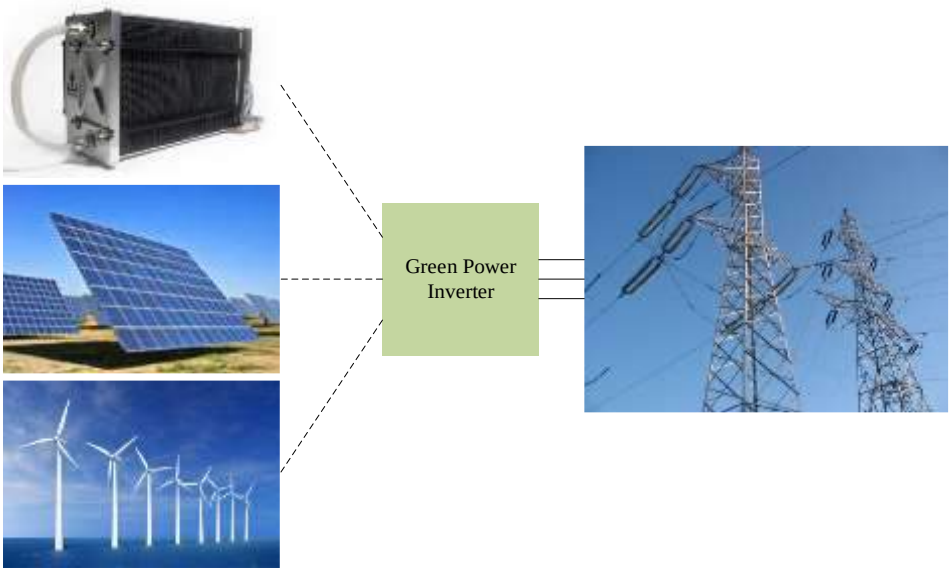

Fig. 7.18. Distributed power generation (source: ECPE)

In Fig.7.18. is schematically shown the role of power electronic "Green Inverter" in alternative electrical energy supply chain.

7.2.3. Power electronic converters for wind turbines

The wind turbine system is made of two parts: a mechanical part and an electrical one as a typical electric drive in generator mode. The first subsystem extracts the energy from the wind and makes the kinetic energy of the wind available to a rotating shaft; the second subsystem is responsible for the transformation of the electrical energy, making it suitable for the electric grid or consumer.

Controlling a wind turbine involves both fast and slow control dynamics. The two subsystems (electrical and mechanical) are characterized with different control goals but interact in view of the main aim: the control of the power injected into the grid or given to consumer separately. The electrical control is in charge of the interconnection with the grid (consumer) and active/reactive power control, and also of the overload protection. The mechanical subsystem is responsible for the power limitation, maximum energy capture, speed limitation and reduction of the acoustical noise. The two control loops have different bandwidths and therfore can be treated independently.

The unified scheme of the wind turbine control [2] is shown in Figure 7.19. The control of the generator-side converter is in charge of extracting the maximum power from the wind. The control of the grid-side converter is keeping the DC link voltage fixed. Internal current and voltage loops in both converters are used. The state variables of the LCL filter are controlled for stability purposes.

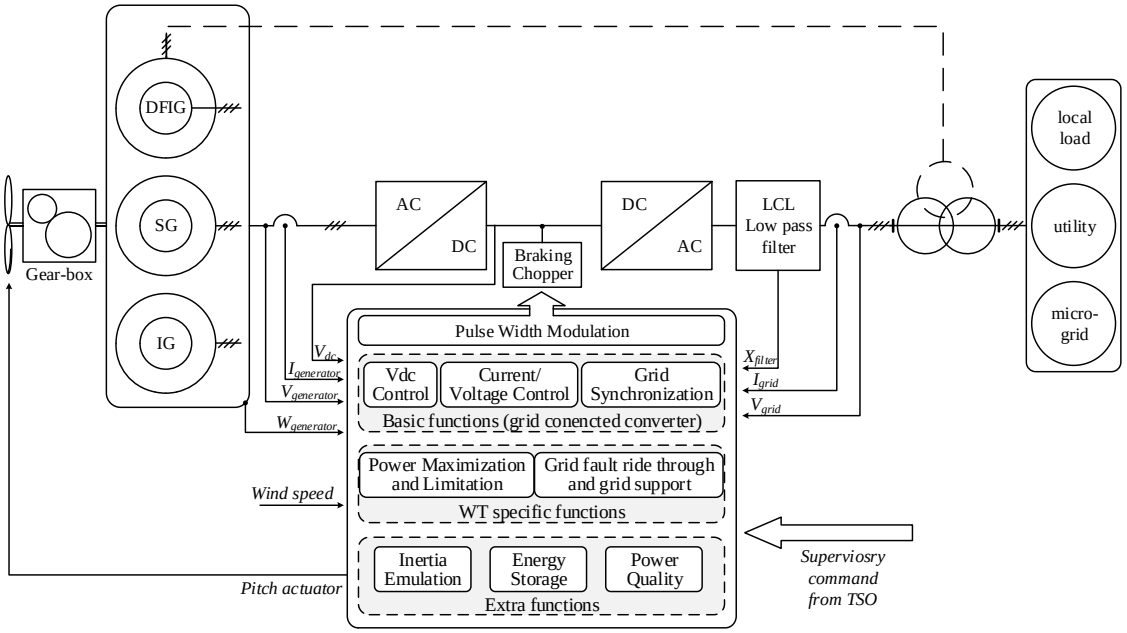

Fig. 7.19. Wind turbine control structure [2]

Wind turbine extra functions are: the inertia emulation that is a control function aiming at emulation the relation between active power and frequency normally present in generator with a large inertia. The energy storage refers to the possibility to store energy in the inertia of the generator, in the dc-link or to use additional storage to smooth the power output. The power quality refers to the possibility to use the grid converter of the WT to provide benefits in terms of grid power quality.

The squirrel cage induction generator (IG) with a full-power forced commutated back-to-back converter (Fig. 7.20.) was often chosen by wind turbine manufacturers for low-power stand-alone systems, but recently it has been used for high-power wind turbines as well. There is a possibility to upgrade the fixed-speed WT to a variable-speed WT with back-to-back converter of reduced power size (50%), which should only be used during low wind conditions to optimize the power transfer and when it is needed to compensate for the reactive power (only using the grid converter), but is bypassed during high-speed conditions [2].

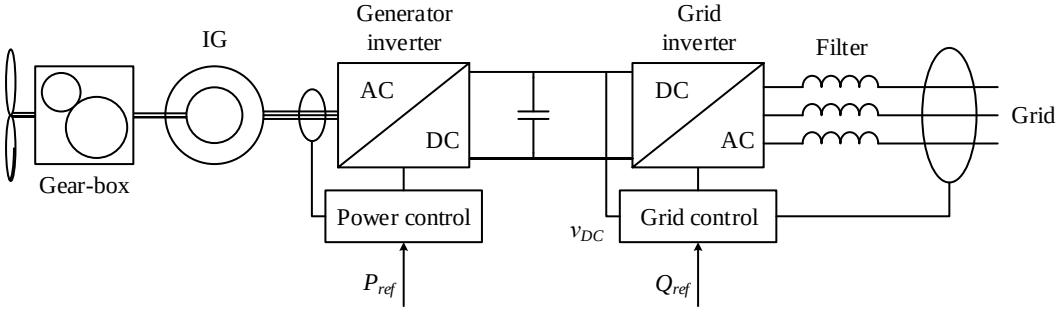

Figure 7.20. Induction generator with a full-scale back-to-back converter

The WT generator flux and rotor speed or electric torque is controlled using field oriented control (FOC) or direct torque control (DTC).

The first controller in the WT to adapt the rotor speed of an induction generator and try to achieve maximum power extraction and limitation of the mechanical stress on the drivetrain has been the slip control.

An evolution of over synchronous cascade control is the doubly fed induction generator equipped with back-to-back power converter allowing bidirectional power flow.

The doubly fed induction generator equipped with voltage source power converters connected to the grid side and to the rotor side (Fig. 7.21.) is one of the most adopted solutions in wind turbine systems.

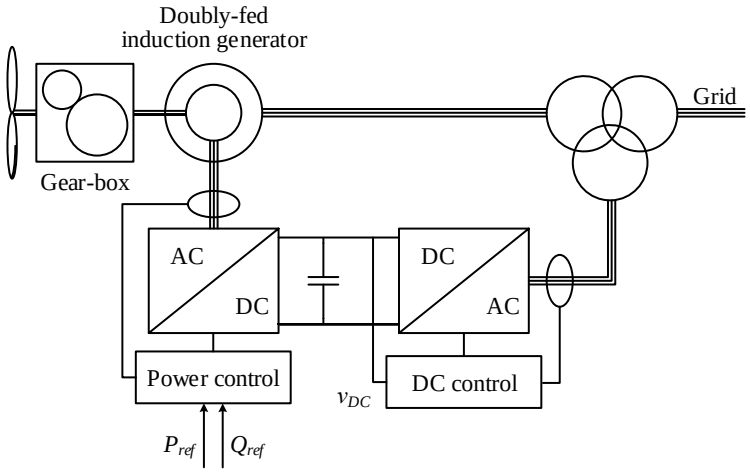

Fig. 7.21. Doubly fed induction generator control

The control of the WT is organized such that below maximum power production the wind turbine will typically vary the speed in proportion to the wind speed and keep the pitch angle fixed. At very low winds the speed of the turbine will be fixed at the maximum allowable slip in order not to have overvoltage. A pitch angle controller will limit the power when the turbine reaches nominal power. The generated electrical power is found by controlling the doubly fed generator through the rotor-side converter. The control of the grid-side converter simply keeps the DC link voltage fixed.

One of the most adopted wind turbine solutions employing a synchronous generator includes a passive rectifier and a boost converter to boost the voltage at low speed. But in this way it is not possible to control selectively the harmonics in the current and the phase of the fundamental current with respect to the generator electromotive force. This solution is one of the most adopted industrial solutions, especially in the case of direct-driven gearless multiphase wind turbine systems.

Fig.7.22 shows WT with synchronous generator and full-power back-to-back converter. In this case the generator control is usually a standard FOC where the current component that controls the flux can be adapted to minimize the core losses and the reference speed is adapted to optimize the power injection into the grid [2].

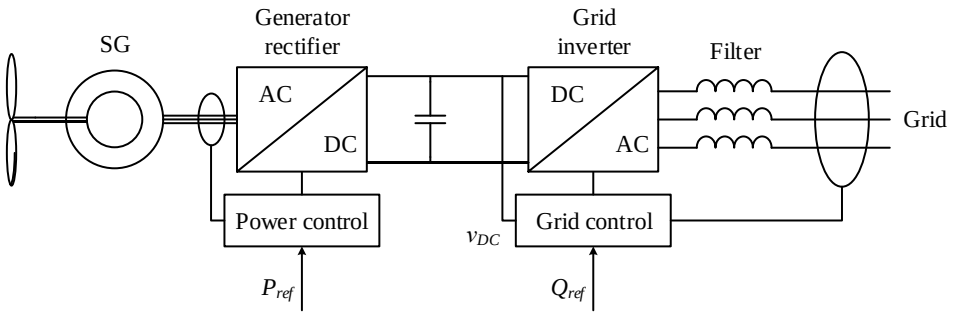

Fig. 7.22. Synchronous generator with: back-to-back converter

There are many demands on power converter topologies in wind turbine systems. The main are: reliability, minimum maintenance, limited physical size/weight and low power losses. The AC/AC conversion can be direct or indirect. In the indirect case there is a DC link that connects two converters performing AC/DC and DC/AC conversions, while in the direct case the DC link is not present. The advantage of the indirect conversion is the decoupling between the grid and generator (compensation for nonsymmetry and other power quality issues) while its major drawback is the need for major energy storage in the DC link.

The main advantage of the direct conversion, such as the matrix converter topology, is that it is a one-stage power conversion. It presents several advantages, but these advantages are balanced with many well-known disadvantages, such as the fact that this is not a proven technology requiring a higher number of components and a more complex control part, the grid filter design is more complex and there is not a unity voltage transfer ratio. There is a space for future technological developments.

The grid converter topologies can be classified into voltage-stiff (voltage-fed or voltage-source) and current-stiff (current-fed or current-source) ones respectively, indicated with the acronyms VSC and CSC. A third option is represented with the Z-source converter employing, on the DC side, an impedance network with capacitors and inductors [2].

Depending on the main power flow direction converters are named rectifiers or inverters, or in case they can work with both power flows they are bidirectional. Then they can be classified as phase-controlled or PWM using forced commutated devices.

The VSC is widely used. It has the following features:

- The AC output voltage cannot exceed the DC voltage. Therefore, the VSC is a buck (step-down) inverter for DC/AC power conversion and is a boost (step-up) rectifier (or boost converter) for AC/DC power conversion.
- The upper and lower devices of each phase leg cannot be gated on simultaneously either by purpose or by EMI noise. Otherwise, a shoot-through would occur and destroy the devices. This is a serious issue for the reliability of these converters. Dead-time to block both upper and lower devices has to be provided in the VSC which causes waveform distortion.
- An output high-order filter is needed for reducing the ripple in the current and complying with the harmonic requirements. This causes additional power loss and control complexity.

Operation of the current-source converters requires a constant current source, which could be maintained by either a generator-side or a grid-side converter.

The CSC has the following features:

- The AC output voltage has to be higher than the original DC voltage that feeds the DC inductor. Therefore, the CSC is a boost inverter for DC/AC power conversion and the CSC is a buck rectifier (or buck converter) for AC/DC power conversion. For grid converter applications this is a clear advantage.
- At least one of the upper devices and one of the lower devices has to be gated and maintained at any time. Otherwise, an open circuit of the DC inductor would occur and destroy the devices. The open-circuit problem of EMI noise is a major concern for the reliability of these converters.
- The main switches of the CSC have to block reverse voltage, which requires a series diode to be used in combination with high-speed and high-performance transistors such as IGBTs.

Medium-power wind turbine systems of 2 MW are still the best seller on the market and their power level can still allow a good design rade-off to be found using single-cell topologies with just six switches forming a bridge.

In all the cases forced commutated converters allow better control of the injected power and harmonics. Between the forced commutated converters the preferred solution is the VSC. Particularly in the case where the VSC is adopted, as usual, on the generator side, the resulting configuration is called back-to-back (Fig. 7.23.)

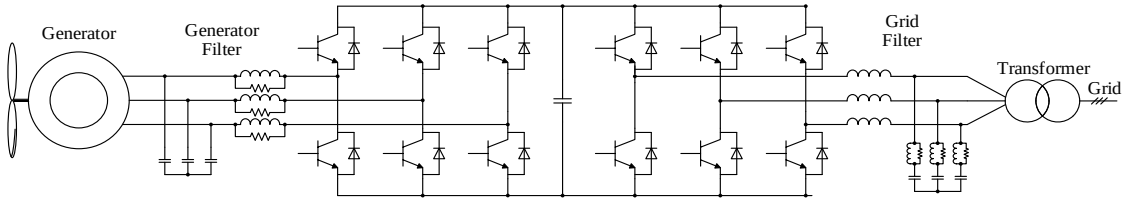

Fig. 7.23. Two-level back-to-back PWM-VSI

The two-level back-to-back VSI is a proven technology that employs standard power devices (integrated), but power losses (switching and conduction losses) may limit the use in higher power systems.

In case the power level increases over 2 MW a multilevel solution (Fig. 7.24.) such as the three-level voltage source converter is a known technology that allows lower rating for the semiconductor devices and lower harmonic distortion to the grid. However, the conduction losses are still high due to the number of devices in series through which the grid current flows and a more complex control is needed to balance the DC link capacitors.

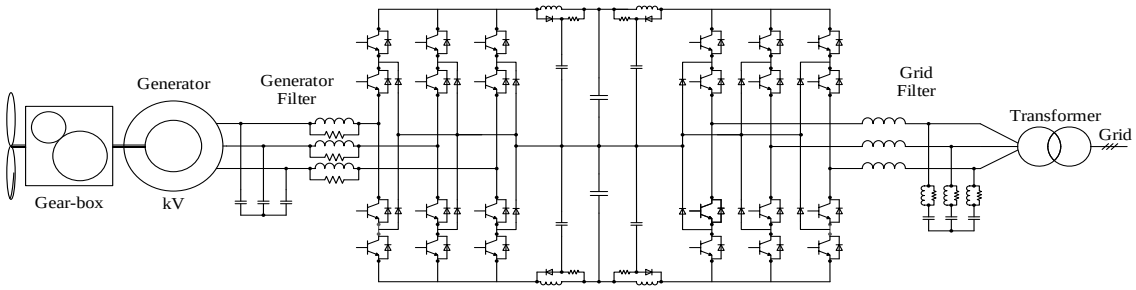

Fig. 7.24. Three-level back-to-back PWM VSI in Wind turbine

Another option to increase the overall power of the system is to use more power converter cells in parallel or in cascade. In both cases the power-handling capability increases while the reliability if computed in terms of the number of failures decreases and the number of system outages increases.

Typically the power cells are connected in parallel on the grid side to allow interleaving operation. The PWM patterns are shifted in order to cancel PWM side-band harmonics. In this way the size of the grid filter can be considerably reduced.

7.2.4. Power electronic converters for solar PV plants

The PV inverter is the key element of grid-connected PV power systems or stand alone consumer with AC appliances. The main function is to convert the DC power generated by PV panels into grid-synchronized AC power. Fig.7.25 shows the block circuit of PV power generation unit.

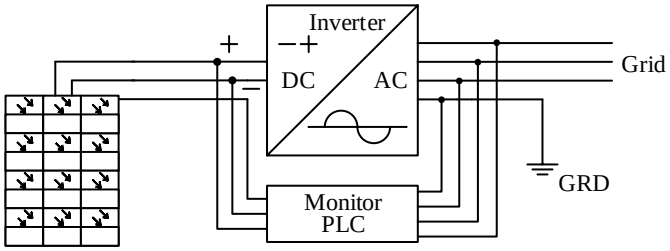

Figure 7.25. PV panel with inverter

Depending on the PV power plant configuration, the PV inverters can be classified as:

- Module integrated inverters, typically in the 50-400 W range for very small PV plants (one panel).
- String inverters, typically in the 0.4-2 kW range for small roof-top plants with panels connected in one string.
- Multistring inverters, typically in the 1.5-6 kW range for medium large roof-top plants.
- Mini central inverters, typically > 6 kW with three-phase topology and modular design for larger roof-tops or smaller power plants in the range of 100 kW.
- Central inverters, typically in the 100-1000 kW range with three-phase topology and modular design for large power plants ranging to tenths of a MW.

Historically the first grid-connected PV plants were introduced in the 1980s with thyristor based central inverters. Since the mid 1990s, IGBT and MOSFET technology has been extensively used.

In comparison with the motor drive inverters, the PV inverters are more complex in both hardware and functionality. Thus, the need to boost the input voltage, the grid connection filter, grid disconnection relay and DC switch are the most important aspects responsible for increased hardware complexity. Maximum power point tracking, anti-islanding, grid synchronization and data logger are typical functions required for the PV inverters.

New innovative topologies have recently been developed for PV inverters with the main purpose of increasing the efficiency and reducing the manufacturing cost.

The most popular PV inverter manufacturers in the market are SMA, Sunways, Conergy, Ingeteam, Danfoss Solar, Refu, etc., offering transformerless PV inverters with very high maximum efficiency of up to 98 %. The topology development for the transformerless PV inverters is in two directions:

- H-bridge.
- Neutral point clamped (NPC).

The half bridge (H-bridge) or full-bridge (FB) converter family, first developed by W.McMurray in 1965 (source: IEEE Std 1450-2010), has been an important reference in the power electronic converter technology development.

The H-bridge topology is very versatile, being able to be used for both DC-DC and DC-AC conversion and can also be implemented in FB form (with two switching legs) or in half-bridge form (with one switching leg). Fig.7.26 shows the Full Bridge inverter for PV electric power unit.

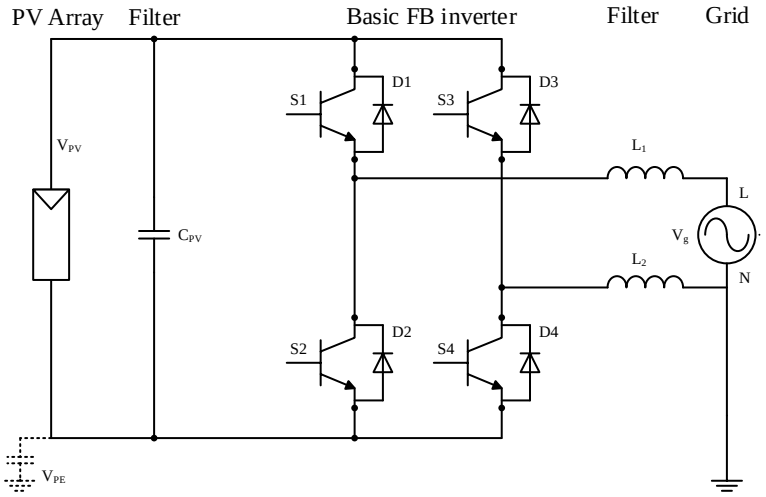

Fig. 7.26. Basic FB inverter

In the basic Full Bridge inverter circuit, three main modulation strategies can be used:

- Bipolar (BP) modulation.
- Unipolar (UP) modulation.
- Hybrid modulation.

FB inverter with all mentioned modulation strategies is not suitable for the use in transformless PV applications due to different reasons.

Therefore several new topologies of inverters for PV applications were invented and developed:

1) In 2005 SMA patented a new inverter topology called H5 (source: E.ON Netz GmbH “Requirements for Offshore Grid Connections in the E.ON Netz Network”, 2008). It is a classical H-bridge with an extra fifth switch in the positive bus of the DC link.
2) In 2006, Sunways patented a new topology also derived from the classical H-bridge called HERIC (highly efficient and reliable inverter concept) by adding a bypass leg in the AC side using two back-to-back IGBTs.
3) In 2007, Refu Solar patented a new topology also delivered from the classical H-bridge. The topology actually uses a half-bridge within the AC side bypass and a bypassable DC-DC converter.
4) Modified FB topology is the full-bridge with DC bypass as patented by Ingeteam (source: Akagi H., Kanazawa Y., Nabae A. Instantaneous Reactive Power Compensator Comprising Switching Devices without Energy Storage Components, 1984). This topology is a classical H-bridge with two extra switches in the DC link and also two extra diodes clamping the output to the grounded middle point of the DC bus.
5) Another “modified” FB topology is the full-bridge zero voltage rectifier (source: Peng F.Z., Ott Jr G.W., Adams D.J. Harmonic and Reactive Power Compensation Based on the Generalized Reactive Power Theory for Three-Phase Four-Wire Systems, 1996). This topology is derived from HERIC, where the bidirectional grid short-circuiting switch is implemented using a diode bridge and one switch and a diode clamp to the DC midpoint.

Those topologies convert the two-level FB inverter into a three-level one. This increases the efficiency as both the switches and the output inductor are subject to half of the input voltage stress.

Neutral Point Clamped (NPC) topology for Half-Bridge Inverter was introduced by Nabae, Magi and Takahashi in 1981. The main concept is that zero voltage can be achieved by ‘clamping’ the output to the grounded ‘middle point’ of the DC bus using D+ or D- depending on the sign of the current.

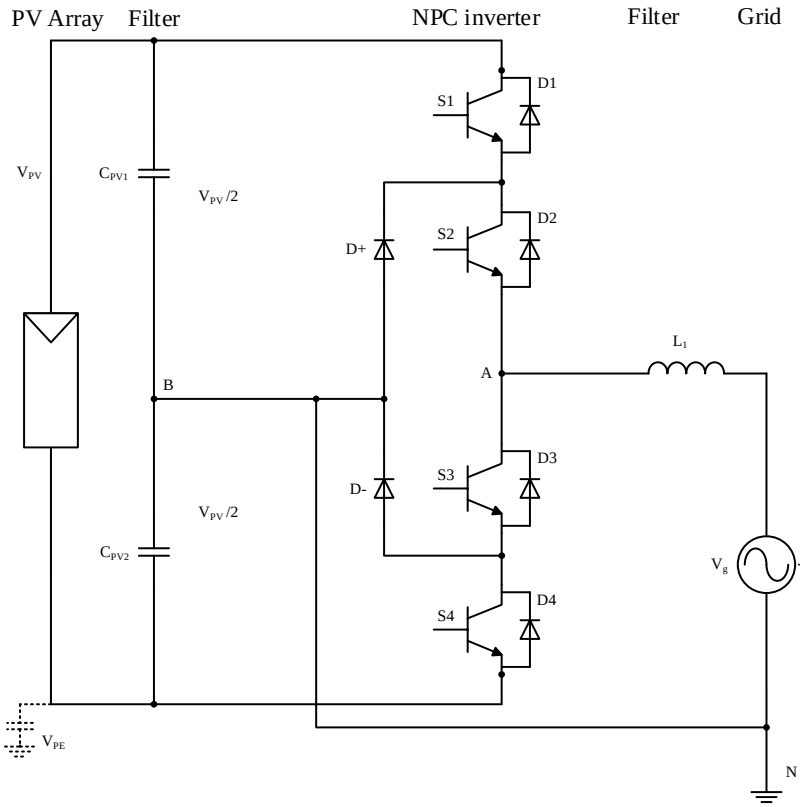

Fig. 7.27. Neutral clamped half-bridge

Fig.7.27 demonstrates NPC topology. Later different other NPC topologies were invented.

A ‘variant’ of the classical NPC is a half-bridge with the output clamped to the neutral using a bidirectional switch realized with two series back-to-back IGBTs as patented by Conergy (source: Kim H.S., Akagi H. The Instantaneous Power Theory on the Rotating *p-q-r* Reference Frames, 1999).

The classical NPC and its ‘variant’ Conergy NPC are both three-level topologies featuring the advantages of unipolar voltage across the filter, high efficiency due to clamping of PV panels during the zero voltage state and practically no leakage due to the grounded DC link midpoint. Due to higher complexity in comparison with FB-derived topologies, these structures are typically used in three-phase PV inverters with ratings over 10 kW. These topologies are also very attractive for high power in the range of hundreds of kW.

A typical structure of an H-bridge based boosting PV inverter is shown in Fig. 7.28. The FB DC-DC converter boost factor is controlled by shifting the switching phase between the two legs (source: Depenbrock M. Untersuchungen uber die Spannungs und Leistungsverhaltnisse bei Umrichtern ohne Energiespeicher, 1962).

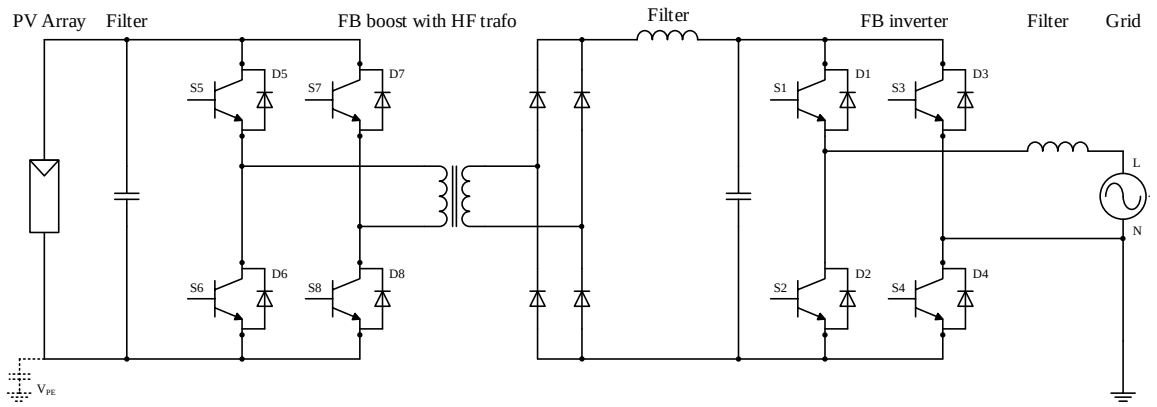

Fig. 7.28. Boosting inverter with a High Frequency (HF) transformer based on the H-bridge

Most of the three-phase PV inverters are not typically true three-phase three-wire inverters but rather three-phase four-wire ones. Actually they work as three independent single-phase inverters.

Due to the very large variety of transformerless PV inverter topologies, the control structures are also very different. An example of PV plant structure with micro-inverters and PLC monitoring system is shown in Fig.7.29.

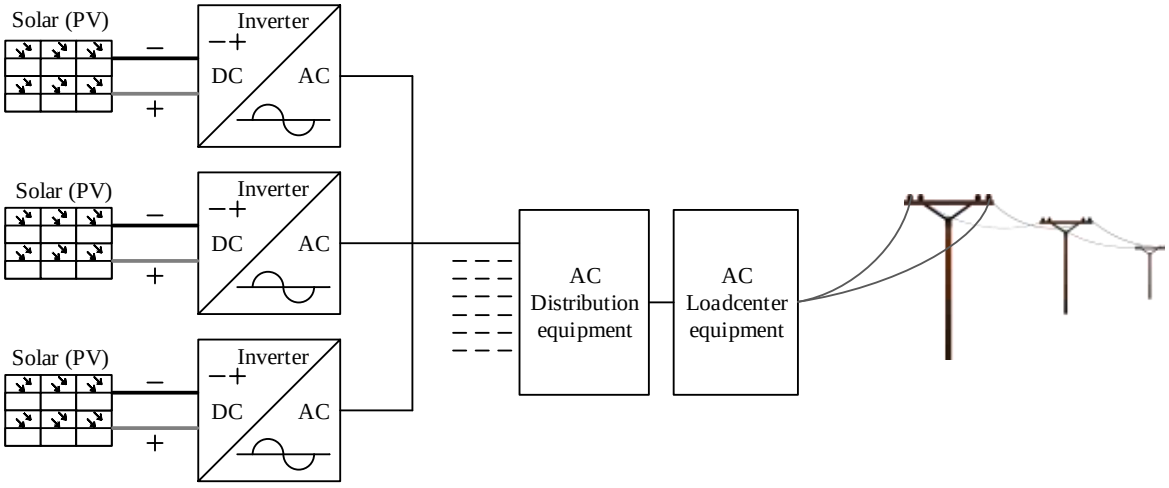

Fig. 7.29. Micro-inverter with PLC monitoring system

The modulation algorithm has to be specific for each topology. In the following a generic, topology invariant control structure will be presented for a typical transformerless topology with boost stage, as shown in Fig. 7.30.

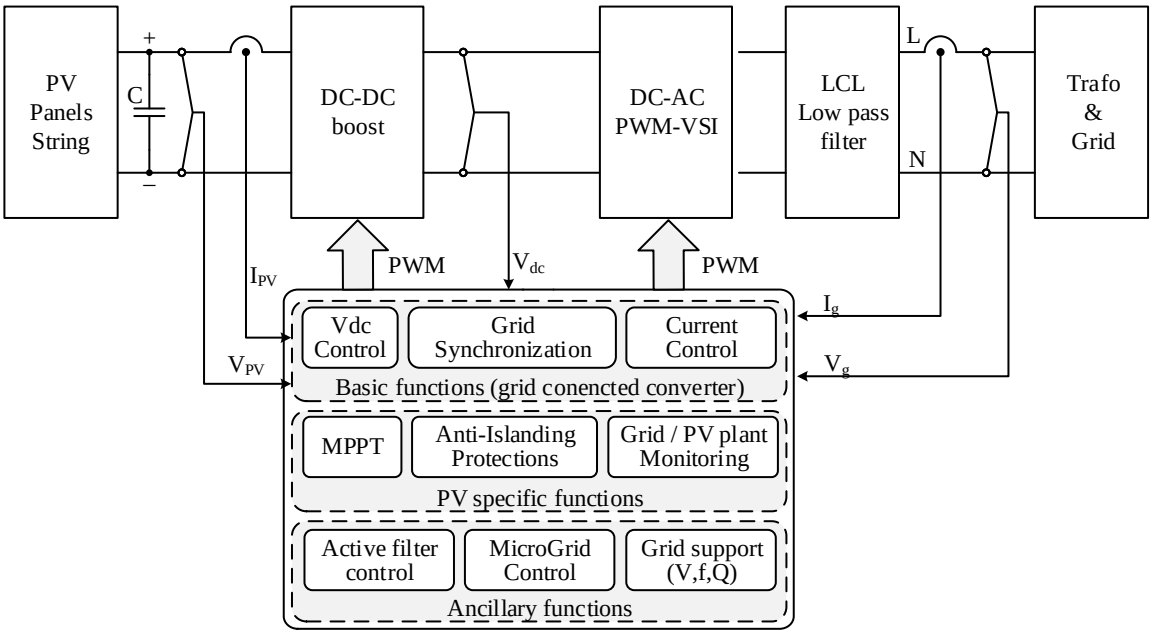

Fig. 7.30. Generic control structure for a PV inverter with boost stage

As can be seen, three different classes of control functions can be defined:

1. **Basic functions – common for all grid-connected inverters**
   - Grid current control
   - DC voltage control
   - Grid synchronization
2. **PV specific functions-common for all PV inverters**
   - Maximum power point tracking (MPPT)
   - Anti-islanding, as required by standards
   - Grid monitoring
   - Plant monitoring
3. **Ancillary functions**
   - Grid support
   - Active filter control
   - Micro grid control

PV inverter structures are evolving at a high pace. A high number of new patented transformerless topologies based on either H-bridge or NPC appeared on the market with very high efficiency, up to 98 %.

The obvious trend is more silicon for lower losses, as the number of switches has increased. The PV inverter market is driven by efficiency rather than cost, mainly due to the still very high price for PV energy. To increase even more the efficiency could be quite difficult using the current technology, but new research shows a real good potential in replacing the silicon switches by silicon-carbide ones.

Another trend in the design of PV inverters will be influenced by the grid requirements. In many countries it is required that eventual islanding should be quickly detected and the inverter should be disconnected from the grid immediately in order to avoid any personal safety issues, especially for residential PV systems. However, as the PV weight in the grid

integration is expected to grow very fast it is possible that grid requirements will change and will require fault ride-through capability in order to stabilize the power system. Just like the case for wind power systems, this requirement has been introduced after a long period when its share in the power generation became important. This will most probably apply for large PV plants connected to power distribution systems.

Integration of new power components is an important factor as it is known from the electric drives sector that this will reduce the costs in the long term.

7.2.5. Power electronics for power plants with Fuel Cells

Fuel cells (FC) can be used as commercial sources of electrical energy, but there is the need to consider the benefits and restrictions of a very complex market concerned with the following four points: Cost, Product availability, Fuel, Safety.

For a market, several fuel cell technologies are under development:

- Proton exchange membrane or solid polymer fuel cells (PEMFCs or SPFCs)
- Phosphoric acid fuel cells (PAFCs)
- Alkaline fuel cells (AFCs)
- Molten carbonate fuel cells (MCFCs)
- Solid oxide fuel cells (SOFCs)
- Direct methanol fuel cells (DMFCs)
- Reversible fuel cells (RFCs)

Common application ranges for these fuel cells are shown in Fig. 7.31.

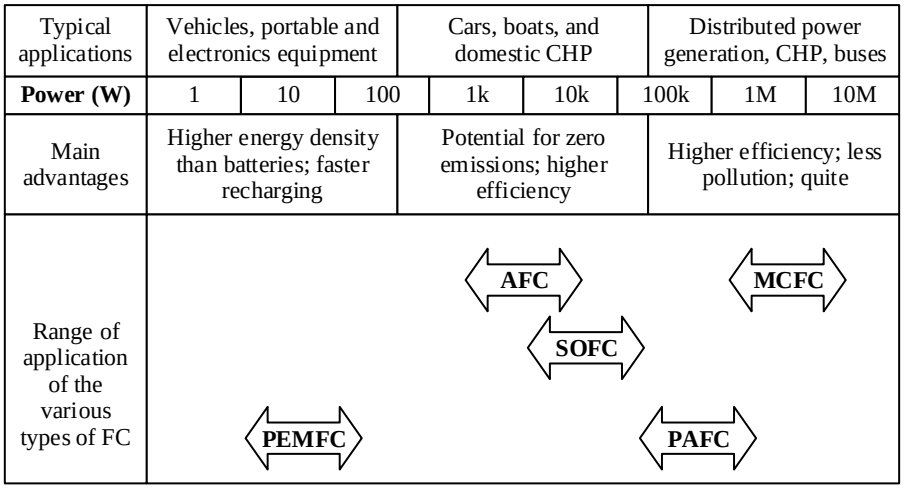

Fig. 7.31. Application areas of fuel cells [1]

Fuel Cell equipment development is very fast and today PEMFC output power is over 50 kW. SOFC, PAFC and MCFC are mostly used for large power plants.

SOFCs of size 200 kW are being widely considered for large combined heat and power generation units in shopping centres, hospitals, residential centres, public buildings, and stand-alone villages. Fig. 7.32 shows structure of COFC module with DC/AC converter.

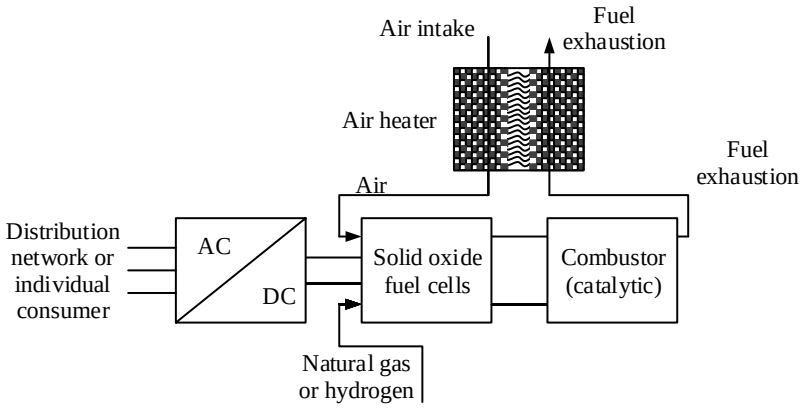

Fig. 7.32. Cogeneration system using Solide Oxide Fuel Cells [1]

The fuel cell is a unidirectional unregulated DC voltage source. To obtain the AC power requested by the variable loads a power electronic conditioning system is needed, which typically consists of:

- DC/DC converter to stabilize the FC DC voltage at the level required by the DC-AC converter;
- DC-AC converter;
- Accumulator element (battery or capacitor).

At present, there are widely used arrangements for PEMFC systems, which contain two and more FC modules for higher power and voltage levels:

- Central converter structure;
- DC bus distribution structure;
- High frequency AC (HFAC) distribution structure;
- Multilevel converter structure;
- Module integrated converter (MIC) structure.

In Fig.7.33 fuel cell modules powered inverter system with a central inverter are shown. Multiple FC modules are connected in series and in parallel connection to achieve the required power and DC voltage level and they power the DC/AC central inverter. In parallel connection a diodes (D1,D2 and D3) should be inserted to block any possible circulating currents between the FC modules series connections. Each FC module is connected parallel with diode (D4-D12) to ensure maximum power to the central inverter in cases, when some FC module cannot produce electrical energy or can work only with a half power. This technology is plant oriented and the power rating of the central converter is the highest if compared to other FC powered systems.

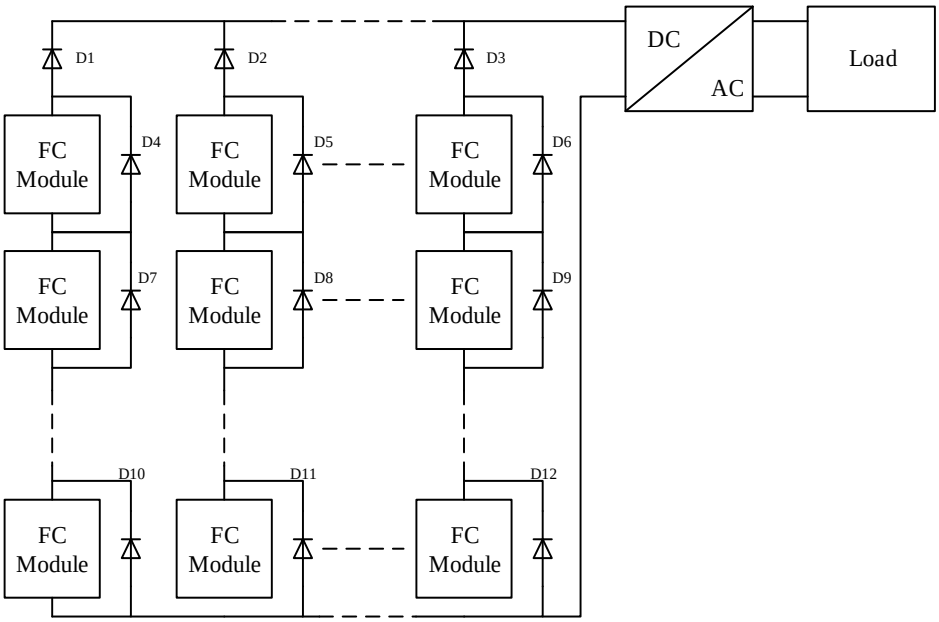

Fig. 7.33. Central inverter structure for FC power plant [9]

The advantages of the central converter technology:

- The number of devices is low, because of only one DC/AC converter;
- High DC/AC converter input voltage, equal to the sum of the FC modules output voltages in series connection;
- Less costs since it requires only a single inverter; from other side, specific inverter design can increase the costs of the system;
- Required only a basic control of the inverter.

The central converter technology has the following main disadvantages:

- The DC cabling design is complex;
- The central converter must be individually designed;
- FC module voltage and load are not controlled;
- The output power decreases due to module mismatching and partial shading conditions;
- The reliability of the FC plant is limited due to the dependence of one single converter [9].

To overcome the disadvantages of the central converter structure, a step-up DC/DC converter can be connected to each fuel cell module and the constant DC outputs of these converters can be connected in parallel making common DC distribution bus.

In this configuration, each FC module has its own power converter module. To increase reliability, a redundant number of FC powered DC/DC converters can be connected in this configuration. Additionally, the constant voltage DC bus can also be used to feed one or several inverters depending on the application [9].

Each fuel cell module can be connected to a DC/AC converter, which converts the FC DC output voltage to high frequency AC voltage (typically several tens of kHz) fed to the primary winding of a high frequency transformer. The secondary transformer winding (or windings) is connected to one or several converters, which convert the high frequency AC voltage to lower

frequency AC voltage (50Hz for industrial consumers). The transformer brings the advantages of electrical isolation, voltage boost, and the capability of adding other power sources and loads through a power converter. Several converters can be connected to the additional secondary transformer windings.

Fuel cell modules can be connected to one multilevel inverter as shown in Fig. 7.34. There are many types of multilevel inverters. One typical multilevel inverter, the diode clamped, is shown in Fig. 7.35 for four FC modules. The problem of this structure is the balancing of the DC sources in the DC link.

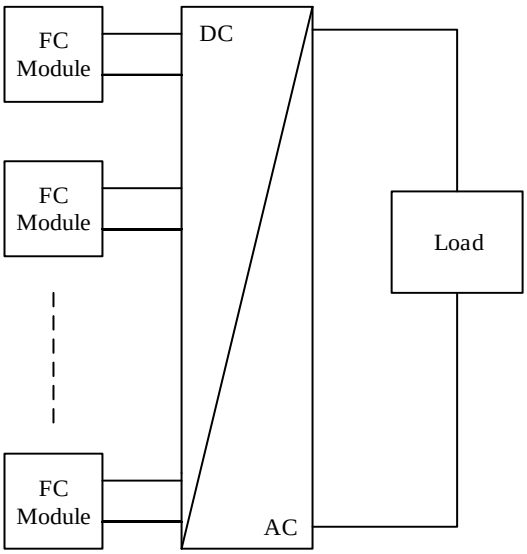

Fig. 7.34. Multilevel converter structure of FC power plant [9]

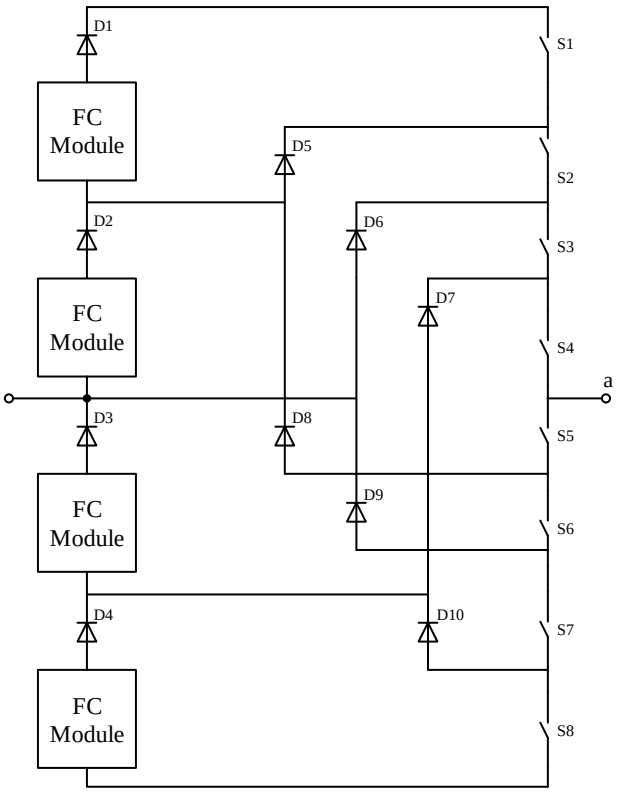

Fig. 7.35. One phase diode clamped five levels inverter of FC converter [9]

A cascaded multilevel converter is one of several multilevel structures. Its structure differs from other multilevel converters and is formed by connecting more than one FC powered converters in series. Input power sources of the cascade converters can be isolated each from other. This is the main distinctive property in comparision with other multilevel converters. Each converter generates a square wave AC voltage waveform with different duty ratios, which together form the output voltage waveform.

The advantages of multilevel converters are:

- Cascade multilevel converter input power sources can be isolated;
- Redundant levels can be added for increased reliability;
- For a fault occurring in the multilevel and cascaded multilevel structures the converter will continue to operate with a portion of the power circuit not working;
- Since each phase is built separate from others, the final converter can be easily connected to form different output waveforms;
- Other control strategies such as multilevel PWM, multilevel space vector PWM, etc. are possible;
- Low voltage type power switches;
- Structure can be divided into several subsystems; Cascaded multilevel structure into FC powered inverter subsystems and multilevel architecture into multilevel inverter subsystems [9].

The disadvantages of multilevel converters are:

- The number of power devices used in multilevel converters is high;
- Because of fundamental frequency switching, lower order harmonics are higher.

In Fig.7.36 the fuel cell module powered converter system with module integrated converter structure (MIC) is presented. There is only one FC module per DC/AC inverter.

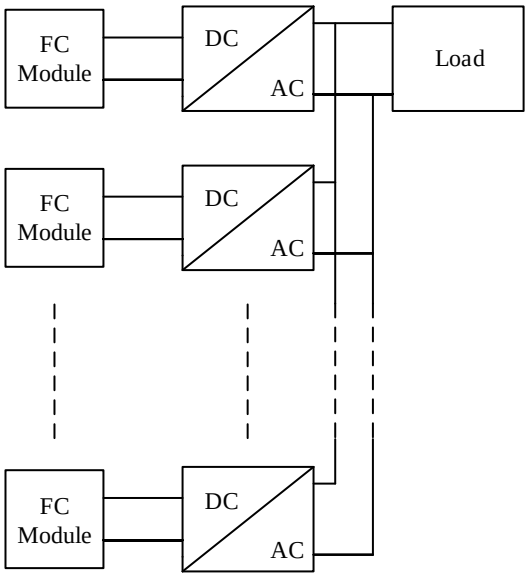

Fig. 7.36. Module integrated converter structure for FC power plant [9]

The MIC technology has the following main advantages:

- The system size can be minimized till one FC powered DC/DC subsystem;

- Each FC module voltage and load can be controlled;
- The FC system can be easily expanded;
- Increased reliability and fault tolerant operation can be achieved by adding redundant FC powered DC/AC converter subsystems;
- After a FC fault occurs the structure will continue providing power to the load from other subsystem.

The MIC technology main disadvantages:

- A higher device count than the central converter structure, because of the DC/AC converters for the each FC module;
- Additional involved control algorithms are required to prevent circulating currents between the DC/AC converters [9].

To provide transient and peak power in a FC powered systems and to ensure additional power for the FC module at the start up and shut down processes some energy storage elements must be included.

In a conventional FC one phase inverter system has two DC voltage levels – variable and low voltage at the FC module output and high, stabilized voltage in the DC/DC converter output commonly 360V or 400V, which value is easy to convert to the one phase industrial voltage 220V, 50Hz.

There are mainly three energy storage options available:

- High side batteries;
- Low side batteries;
- Double layer capacitors.

The high-side batteries option involves placing a large number of battery cells in series across the high voltage bus (commonly 360 or 400 VDC) .

Lower voltage batteries can be interfaced to the high voltage side through a bidirectional converter, which allows power flow from the batteries to the main power flow and ensures battery charging process [9].

An alternative to the batteries is the use of double layer capacitors (see Fig. 7.37.) which have a wider voltage range than the battery cell and can be directly paralleled to the FC module output. Double layer capacitors have a specific energy density less than that of a battery, but a specific power density greater than a battery, making them ideal for short pulses of power. Certain double layer capacitors can hold charge over extended periods of time, so as to act somewhat like a battery. However, unlike batteries, these double layer capacitors have a short charge time and a much longer lifetime.

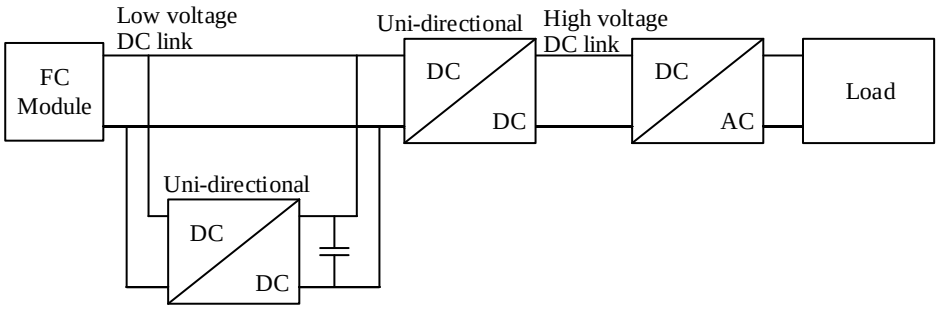

Fig. 7.37. FC powered invereter system with a double layer capacitor [9]

PEMFC system with double layer capacitor and battery contains power source – PEMFC, double layer capacitor C1, battery B1 and DC/AC power converter (see Fig. 7.38.). The distinctive properties of the novel proposed structure are defined by the FC connection to the DC/AC power converter with the first controllable switch S1 and to DC/DC power converter with the second controllable switch S2. To the output of the DC/DC power converter is wired series connection of the double layer capacitor C1 and the battery B1. With the thirs controllable switch S3 the double layer capacitor C1 is joined to the input of the DC/AC power converter.

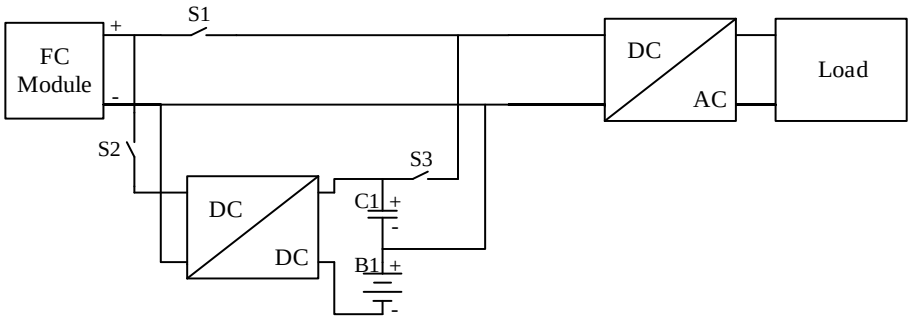

Fig. 7.38. PEMFC system with double layer capacitor and battery [9]

PEMFC system with double layer capacitor and battery operates as follows. The battery B1 supplies the FC at start-up and shutdown processes of the system and the double layer capacitor C1 provides necessary power at dynamic loads.

Controllable switches S1, S2 and S3 regulate energy flow in the system.

Improve efficiency of double layer capacitor and battery charging process is obtained with the battery and double layer capacitor series connection.

To increase the efficiency of a DC/DC power converter a topology with voltage fed push-pull (Fig. 7.39.) was created.

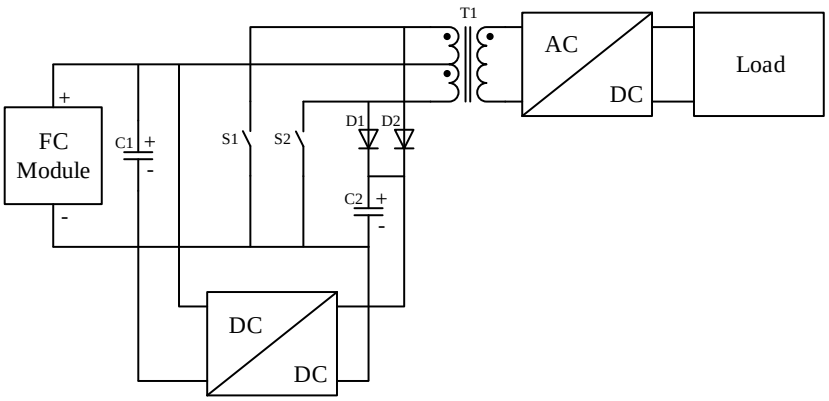

Fig. 7.39. High efficiency DC/DC power converter for PEMFC [9]

An improved DC/DC power converter for PEMFC contains FC, two controllable switches S1, S2, two diodes D1, D2, additional DC/DC power converter, one phase high frequency transformer T1, AC/DC power converter and the load (see Fig. 7.39.).

Higher efficiency is obtained by delivery of the demagnetization energy of the inductive elements directly to the input filter capacitor.

Comparing three topologies of direct-current high-frequency power converters, current-fed double inductor push-pull converter is considered to be the most appropriate (see Fig. 7.40.). This kind of topology allows decreasing the ripple of the input current and also eliminates divided primary winding of transformer. [8]

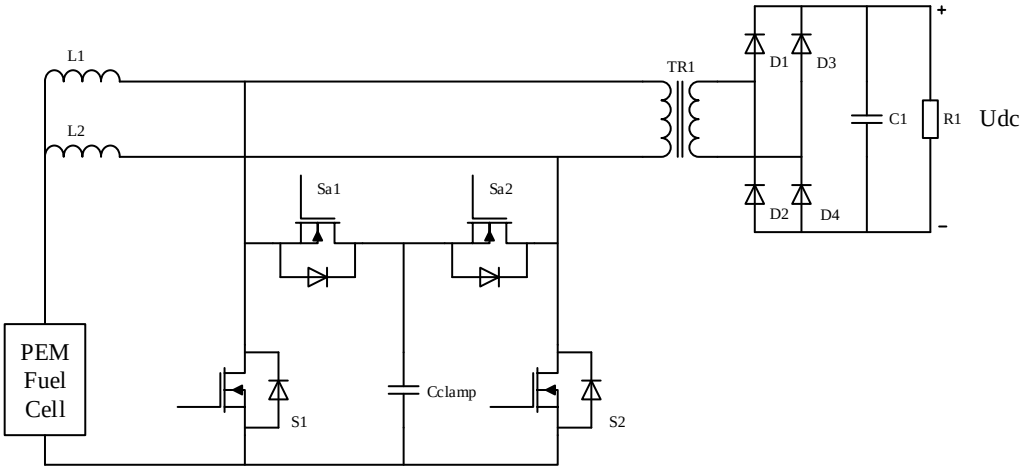

Fig. 7.40. Current-fed double inductor push-pull converter with active clamping for PEMFC

PEMFC are used for automotive applications too. Power electronics and microprocessor control systems are playing the main role in FC powered automobile equipment. Fig. 7.41 shows a structure and simplified topology of PEMFC powered electrical drive system for a car.

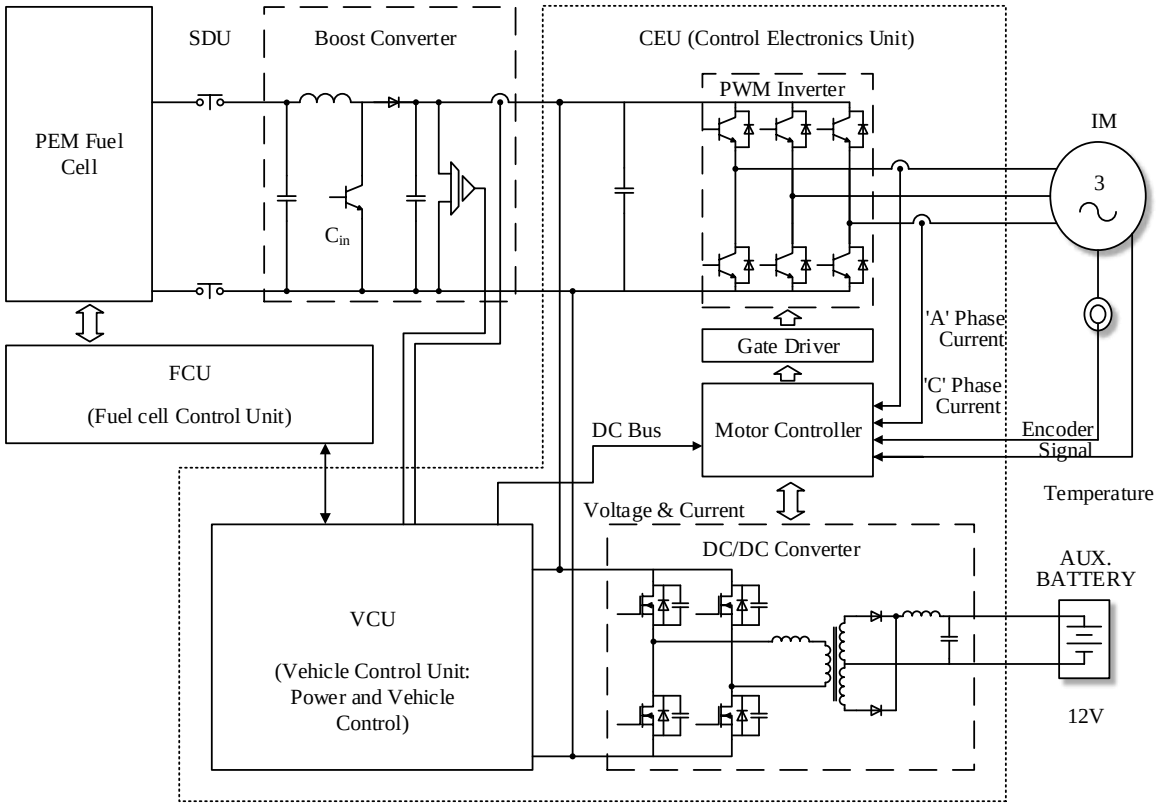

Figure 7.41. Typical configuration of a PEM fuel cell powered system for automotive applications (source: Song-Yul Choe, Jung-Gi Lee, Jong-Woo Ahn, Soo-Hyun Baek Integrated modelling and control of a PEM fuel cell power system with a PWM DC/DC converter, 2007)

The development of power electronic converters for fuel cell sources and plants is very fast and the usage of advanced semiconductor switches and passive elements is one of the state-of-art topics.

7.2.6. Power electronics in the integrated renewable sources of electrical energy

Distributed Generation technologies can improve power quality, boost system reliability, reduce energy costs, and defray utility capital investment.

Alternative sources of energy are either fossillfuel-based (systems that use diesel, gas, or hydrogen from reforming hydrocarbons) or renewable-based (systems that use solar, wind, hydro, tidal, geothermal energy or hydrogen produced from renewable sources.

The integration of renewable sources of electrical energy is a challenge because their output is variable and must be stored for use when there is a demand. If only one renewable energy source is considered, the electric power system is simple. The source can be connected to a storage system to deliver electricity for stand-alone use or interconnected with the grid. In the grid-connected application, the grid acts as energy storage. However, if multiple renewable energy sources are used, the electric power system can be rather complicated, and a microgrid will be formed.

Power electronics is the enabling technology that allows the conversion of energy and injection of power from renewable energy sources to the grid.

DG systems consist of small generators, typically 1 kW to 10 MW, scattered throughout the system to provide electrical and, sometimes, heat energy close to consumers. When interconnected with distribution systems, these small, modular generation technologies can form a new type of power system, the microgrid. Microgrids are illustrated in Fig. 7.42.

The microgrid concept assumes a cluster of loads and microsources operating as a single controllable system that can provide power and heat to the local area. The electrical connection of sources and loads can be realized with a dc link, an ac link, or an HFAC link. Converters are usually connected in parallel, although series arrangements of sources and loads are possible to allow better use of high voltages and currents.

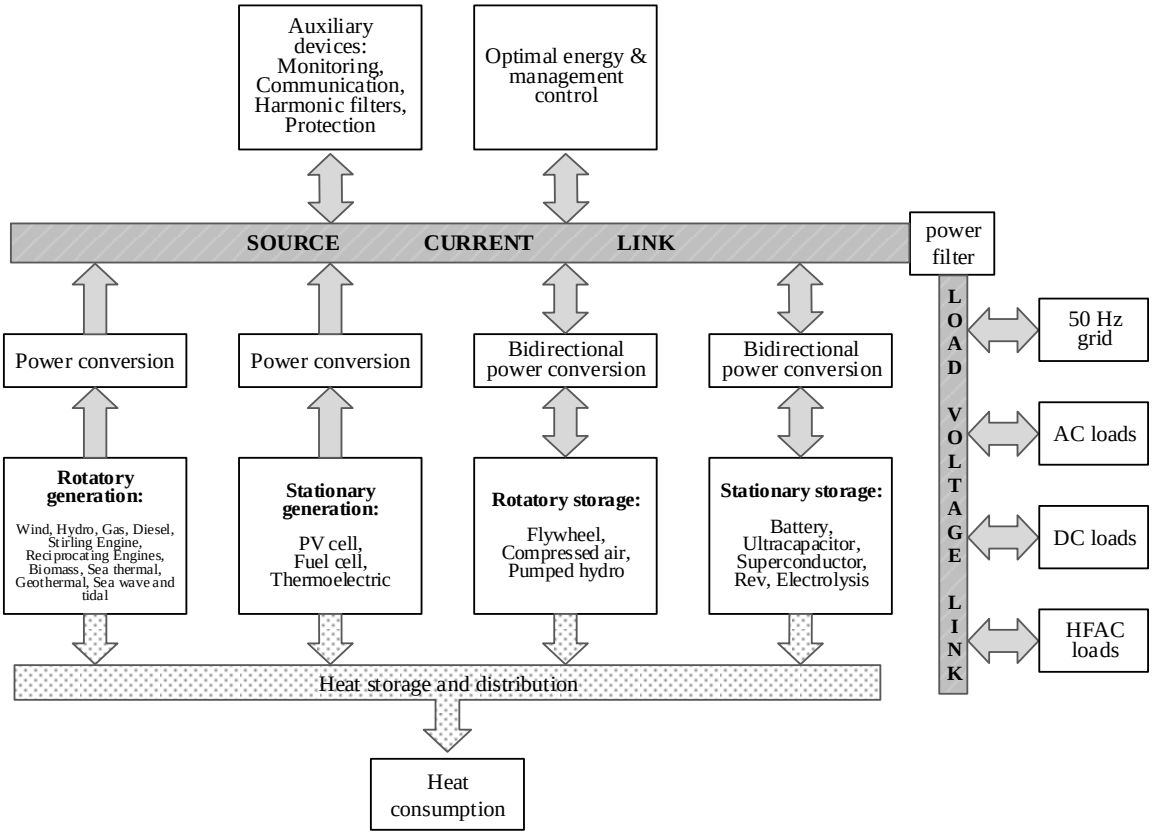

Fig. 7.42. General scheme for integration of alternative electrical sources and loads and thermal energy dissipation [1]

The simplest and oldest type of electrical energy integration is with a dc link (see Fig. 7.33.(a)). An example is the straightforward connection of a DC source to a battery and load scheme.

The advantages of dc-link integration include:

- Synchronism is not required;
- There are lower distribution and transmission losses than with ac-link;
- It has high reliability because of parallel sources;
- Although the terminal needs of a dc link are more complex, the dc transmission infrastructure per kilometre is simpler and cheaper than in ac links;
- Long-distance transmission (for high-voltage links) is possible, which enables integration of offshore wind turbines and other energies with inland networks;

- The converters required are easily available;
- Single-wired connections allow balanced terminal ac systems.

The disadvantages are:

- The need for careful compatibility of voltage levels to avoid current recirculation between the input sources;
- The need for robust forced commutation capabilities in circuits at high power levels;
- Corrosion concerns with the electrodes;
- A large number of components and controls;
- More complex galvanic isolation;
- Higher costs of terminal equipment;
- Difficulties with multiterminal or multi-voltage-level operation for transmission and distribution.

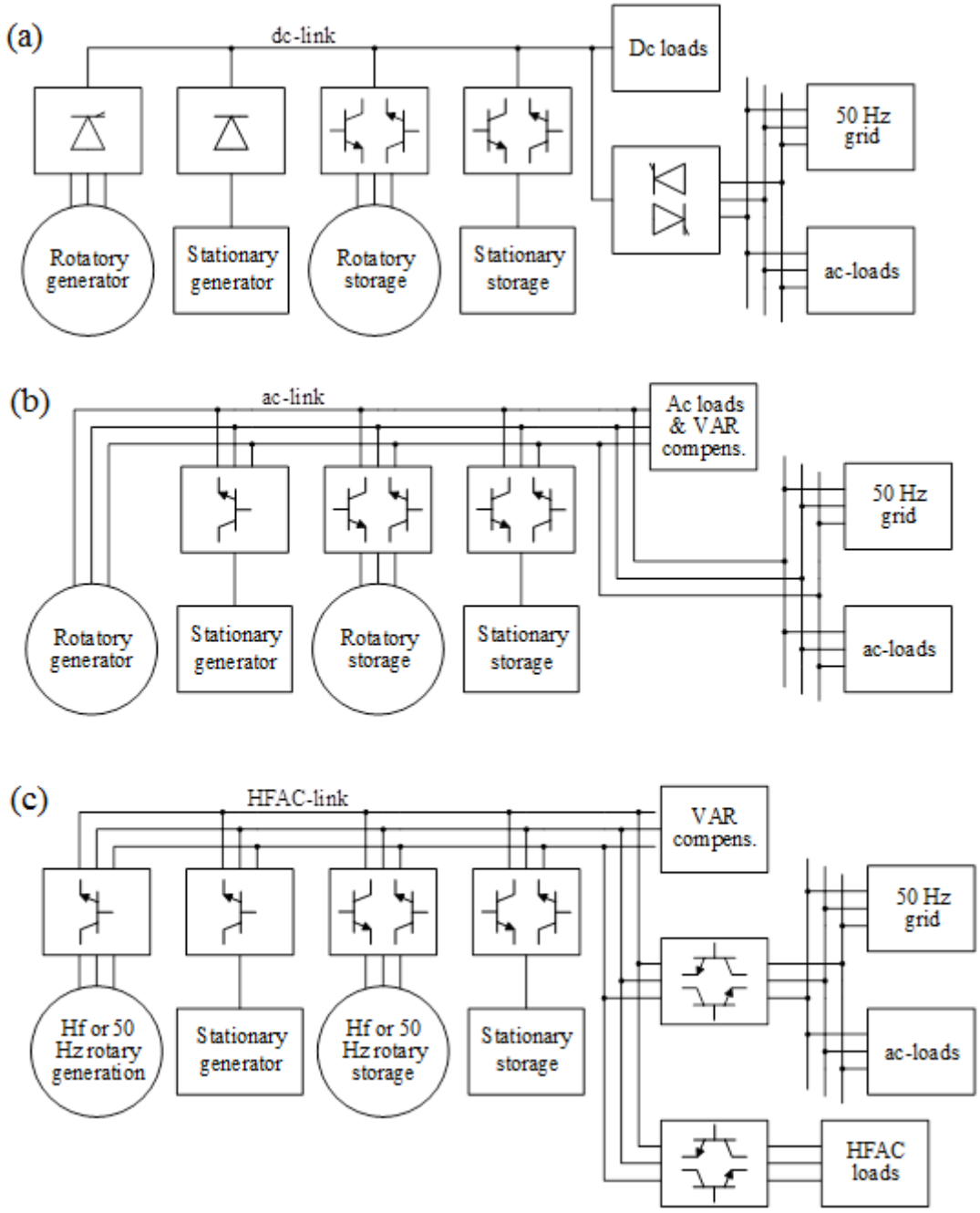

Figure 7.43. Methods of alternative energy sources integration: dc-link integration (a), ac-link integration (b), HFAC-link integration (c)

Another possibility for integrating renewable energy sources is the ac-link bus operating at 50 Hz, as indicated in Fig. 7.43.(b) This bus can be the public grid or a local grid for islanded operation. In this case, the interconnection of a local bus to the public bus must follow the standards and requirements for interconnection.

Positive features of this configuration include:

- Utility regulation and maintenance of the operational voltage, which makes it easier to inject power into the grid;
- The possibility, in some cases, of eliminating the electronic converters (e.g., by using synchronous generators or induction generators that establish their own operating point);

- Easy multivoltage and multiterminal matchings;
- Easy galvanic isolation;
- Well-established scale economy for consumers and existing utilities.

Negative points include:

- The need for rigorous synchronism, voltage-level matching, and correct phase sequence between sources during interconnection as well as during operation;
- Leakage inductances and capacitances in addition to the skin and proximity effects that cause losses in long distributions;
- Electromagnetic compatibility concerns;
- The possibility of current recirculation between sources;
- The need for power factor and harmonic distortion correction;
- Reduced limits for transmission and distribution.

An HFAC microgrid system is a power electronics solution that is promising as an interface for the utility grid and stand-alone operation. It provides embedded fault protection, small dimensions, and a configuration to serve various power quality functions. Frequencies in industrial use are 400 Hz, as is the case in spaceships, boats, buses, planes, submarines, and other loads of the kind.

Power electronic-based systems connected with the grid can be controlled and monitored remotely to allow real-time optimization of power generation and power flow, which allows aggregation of distributed power generation resources into a “virtual utility”. Several HFAC power distribution systems were implemented for aerospace applications, and NASA evaluated this scheme for space station applications. It has been proposed as a workable power distribution system for hybrid electronic vehicles as well as using traditional ac-ac conversion through semiconductor switches. This is performed in two stages, from ac-dc and then from dc-ac (dc-link converters), or directly by cycloconverters. A microgrid is illustrated in Fig. 7.43.(c). [1]

The matrix converter is another technology under development. First proposed in the early 1980s, it consists of a matrix of ac switches that connects the three input phases to the three output phases directly. This circuit allows any of the input phases to be connected to any output phase at any instant, depending on the control strategy. It is expected that new devices will accelerate the widespread use of matrix converters to convert HFAC into utility voltage and frequency.

Series resonant converters, using sero-voltage or zero-current switching, can be used with each of the sources to generate the HFAC link. In this way, the overall losses in the converters can be reduced. An HFAC microgrid system has the following inherent advantages:

- The harmonics are of higher orders and are easily filtered out;
- Fluorescent lighting will experience improvement because with higher frequency the luminous efficiency is improved, flicker is reduced, and dimming is accomplished directly. The ballast inductance is reduced proportionally to the frequency, with a corresponding reduction in size and weight;
- High-frequency induction motors can be used for compressors, high-pressure pumps, high-speed applications, and turbines. AC frequency changers based on

matrix converters can be used to soft start high-frequency induction motors. A safe operating area is not a restriction for soft switching, and therefore modern power electronic devices will be advantageous;

- Harmonic ripple current in electric machines will decrease, improving efficiency;
- High-frequency power transformers, harmonic filters for batteries, and other passive circuit components become smaller;
- Auxiliary power supply units are easily available by tapping the ac link. They would be smaller with higher efficiencies;
- Batteries have been the traditional energy storage source, but in HFAC microgrids, dynamic storage is an alternative.

The disadvantages are:

- The high cost of transformers;
- The large number of devices (because of the use of bipolar ac switches);
- Very complex control;
- The dependence on future advances of power electronic components;
- Concerns about electromagnetic compatibility;
- Extremely reduced limits and technological problems for transmission and distribution at high frequencies. [1]

An important issue related to microgrids is islanding. This condition occurs when the microgrid continues to energize a section of the main grid after that section has been isolated from the main utility. Unintentional islanding is a concern for the utility because sources connected to the system but not controlled by the utility pose a possibility of harm to utility personnel and damage from uncontrolled voltage and frequency excursion. It is therefore important that microgrid systems incorporate methods to prevent unintentional islanding.

References

1. Farret Felix A., Godoy Simoes M. Integration of alternative sources of energy // New Jersey: John Wiley & Sons, 2006 – 471 p.
2. Teodorescu R., Liserre M., Rodriguez P. Grid converters for photovoltaic and wind power systems // United Kingdom: John Wiley & Sons, 2011 – 398 p.
3. Mohan N., Undeland Tore M., Robbins William P. Power Electronics: Converters, Applications, and Design // USA: John Wiley & Sons, 1989 – 667 p.
4. Hart Daniel W. Power electronics // Singapore: McGraw-Hill, 2011 – 477 p.
5. De Doncker R.W. Lecture Notes: Power Electronics // Koln: Hundt Druck GmbH, 2009 – 206 p.
6. Ribickis L., Raņķis I. Electrical Drives: Static Characteristics and Methods of Speed Control // RTU Department of Automated Electrical Drive – Riga: RTU, 1996 – 107 p.
7. Raņķis I., Buņina I. Energoelektronika // Rīga: RTU Izdevniecība, 2007 – 186 lpp.
8. Steiks I. Development of Power Electric Converters for Hydrogen Energy Equipment: Doctoral Thesis // RTU Faculty of Power and Electrical Engineering. Inst. of Industrial Electronics and Electrical Engineering; scientific supervisor L.Ribickis – Riga: Riga Technical University, 2011. - 146 p.

9. Purviņš A. Dynamic Characteristics and Power Electronic Converters of the Hydrogen Fuel Cell Systems: Doctoral Thesis // RTU Faculty of Power and Electrical Engineering Inst. of Industrial Electronics and Electrical Engineering; scientific supervisor L.Ribickis; [rev. by K.Ketners [et al.]] – Riga, 2008 – 116 p.