GATE CS Topic wise Questions

Digital Logic

YEAR 2001

Question. 1

Given the following Karnaugh map, which one of the following represents the minimal sum-of-Products of the map ?

$yz \backslash wx$	00	01	11	10
00	0	×	0	×
01	×	1	×	1
11	0	×	1	0
10	0	1	1	×

(A) $xy + y'z$ (B) $wx'y' + xy + xz$

(C) $w'x + y'z + xy$ (D) $xz + y$

SOLUTION

$yz \backslash wx$	00	01	11	10
00	0	X	0	X
01	X	1	X	1
11	0	X	1	0
10	0	1	X	0

There are 2 quads.

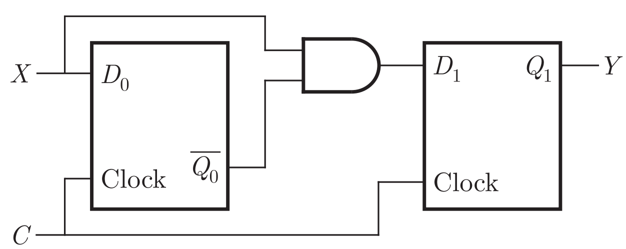
$y'z + yx$

So $xy + y'z$

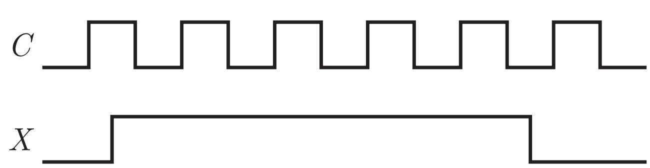
Hence (A) is correct option.

Question. 2

Consider the following circuit with initial state $Q_0 = Q_1 = 0$. The D flip-flops are positive edged triggered and have set up times 20 nanosecond and hold times 0.



Consider the following timing diagrams of X and C; the clock of $C \geq 40$ nanosecond. Which one is the correct plot of Y



(A) 

(B) 

(C) 

(D) 

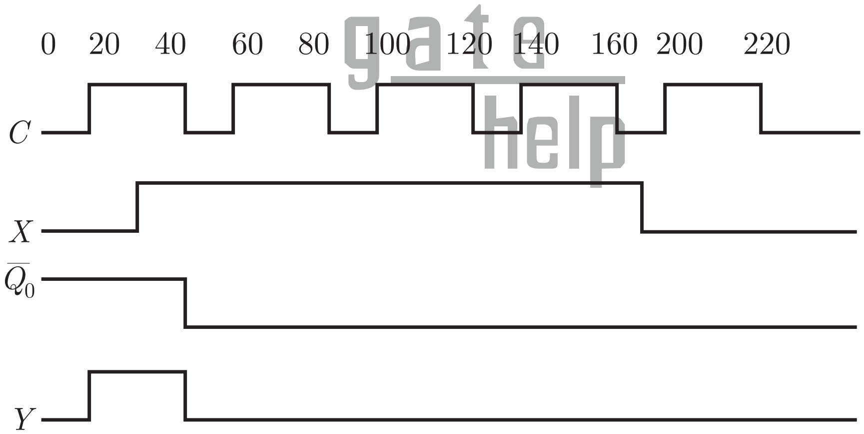
SOLUTION

Consider the following circuit with initial state $Q_0 = Q_1 = 0$. The D flip-flops are positive edged triggered and have set up times 20 nanosecond and hold times 0.

Figure

Consider the following timing diagrams of X and C; the clock period of $C \geq 40$ nanosecond. Which one is the correct plot of Y ?

Figure



Question. 3

The 2's complement representation of $(-539)_{10}$ is hexadecimal is

(A) ABE (B) DBC

(C) DE5 (D) 9E7

SOLUTION

Binary of 539 = 1000011011

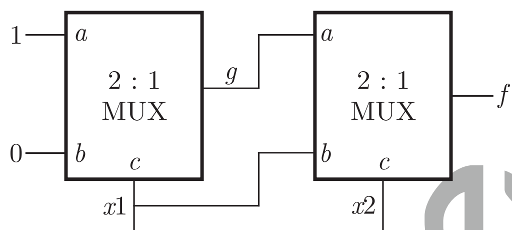
Binary	:0010	0001	1011
2's comp	:1101	1110	0101
Hexadecimal	D	E	5

$(DES)_{16}$

Hence (C) is correct option.

Question. 4

Consider the circuit shown below. The output of a 2:1 Mux is given by the function $(ac' + bc)$.



Which of the following is true ?

(A) $f = x1' + x2$

(B) $f = x1'x2 + x1x2'$

(C) $f = x1x2 + x1'x2'$

(D) $f = x1 + x2$

SOLUTION

Output of any 2:1 MUX $= ac' + bc$

Here output of MUX 1.

$$g = ax_1' + bx_1$$

Output of MVX 2

$$f = gx_2' + x_1x_2$$
$$f = (ax_1' + bx_1)x_2' + x_1x_2$$
$$f = ax_1'x_2' + bx_1x_2' + x_1x_2$$

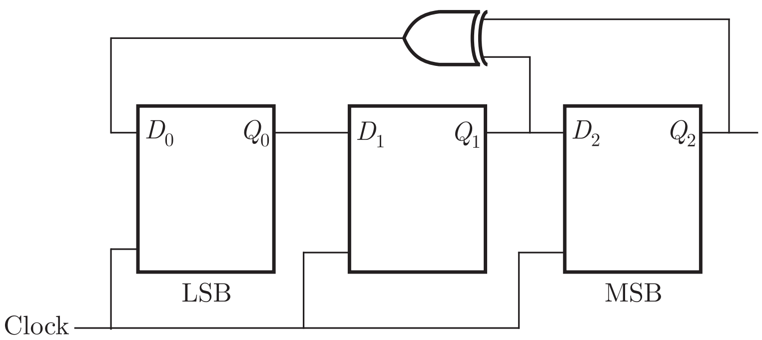
Given $a = 1,\ b = 0$

$$f = x_1'x_2' + x_1x_2$$

Hence (C) is correct option.

Question. 5

Consider the circuit given below the initial state $Q_0 = 1, Q_1 = Q_2 = 0$. The state of the circuit is given by the value $4Q_2 + 2Q_1 + Q_0$



Which one of the following is the correct state sequence of the circuit ?

(A) 1, 3, 4, 6, 7, 5, 2

(B) 1, 2, 5, 3, 7, 6, 4

(C) 1, 2, 7, 3, 5, 6, 4

(D) 1, 6, 5, 7, 2, 3, 5

SOLUTION

Initially	Q_0	Q_1	Q_2	Value $4Q_2 + 2Q_1 + Q_0$
Clk	1	0	0	1
1	0	1	0	2
2	1	0	1	5
3	1	1	0	3
4	1	1	1	7
5	0	1	1	6
6	0	0	1	4

Hence (B) is correct option.

YEAR 2002

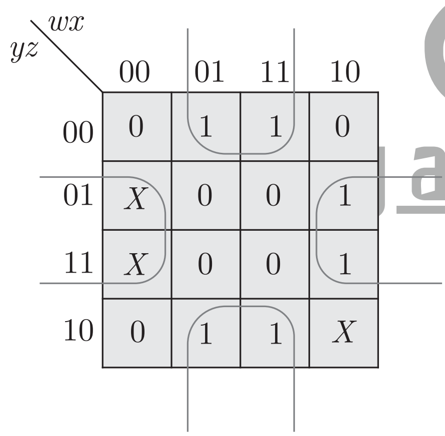
Question. 6

Minimum sum of product expression for $f(w, x, y, z)$ shown in Karnaugh-map below is

yz \ wx	00	01	11	10
00	0	1	1	0
01	×	0	0	1
11	×	0	0	1
10	0	1	1	×

(A) $xz + y'z$
(B) $xz' + zx'$
(C) $x'y + zx'$
(D) None of the above

SOLUTION



There are 2 quads possible

$xz' + x'z$

Hence (B) is correct option.

Question. 7

The decimal value of 0.25

(A) is equivalent to the binary value 0.1

(B) is equivalent to the binary value 0.01

(C) is equivalent to the binary value 0.00111.....

(D) cannot be represented precisely in binary.

SOLUTION

Given decimal no. 0.25

$$\text{Binary} = ?$$
$$.25 \times 2 = .5$$
$$.5 \times 2 = 1$$
$$(.01)_2$$

Hence (B) is correct option.

Question. 8

The 2's complement represent representation of the decimal value -15 is

(A) 1111
(B) 11111
(C) 111111
(D) 10001

SOLUTION

Given $(-15)_{10}$

Binary of 15 $= (01111)_2$

2's complement of 15 would represent (-15).

01111

$(10001)_2$

Hence (D) is correct option.

Question. 9

Sign extension is a step in

(A) floating point multiplication
(B) signed 16 bit integer addition
(C) arithmetic left shift
(D) converting a signed integer from one size to another.

SOLUTION

Sign extension is the operation in computer arithmetic of increasing no. of bits of a binary no., while preserving sign and value done by appending MSB's. In the floating point multiplication to bring the no. in desired no. of significant digits sign extension is done.

Hence (A) is correct option.

Question. 10

In 2's complement addition, overflow

(A) Relational algebra is more powerful than relational calculus

(B) Relational algebra has the same power as relational calculus.

(C) Relational algebra has the same power as safe relational calculus.

(D) None of the above.

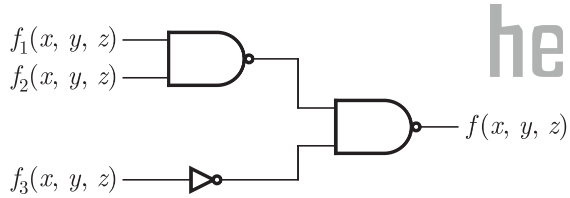
SOLUTION

In 2's complement addition, overflow occurs when the carries from sign bit & previous bit doesn't match. So overflow can't occur when a positive value is added to some negative value.

Hence (B) is correct option.

Question. 11

Consider the following logic circuit whose inputs are functions f_1, f_2, f_3 and output is f



Given that

$$f_1(x,y,z) = \Sigma(0,1,3,5)$$
$$f_2(x,y,z) = \Sigma(6,7), \text{ and}$$
$$f(x,y,z) = \Sigma(1,4,5)$$

f_3 is

(A) $\Sigma(1,4,5)$

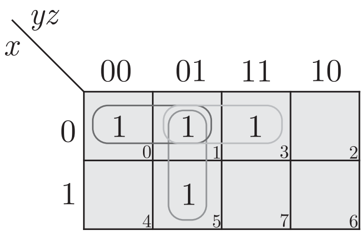
(B) $\Sigma(6,7)$

(C) $\Sigma(0,1,3,5)$

(D) None of the above

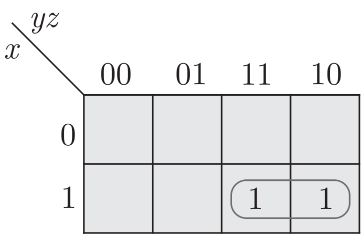
SOLUTION

$$f_1(x,y,z) = \Sigma(0,1,3,5)$$



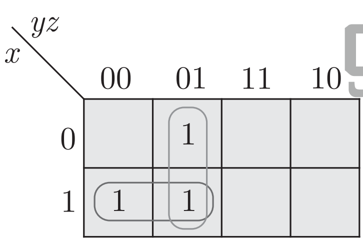
$$= x'y' + y'z + x'z$$

$$f_2(x, y, z) = \Sigma(6,7)$$



$$= xy$$

$$f(x, y, z) = \Sigma(1,4,5)$$



$$= xy' + y'z$$

$$f(x, y, z) = \overline{\overline{f_1 f_2} \cdot \overline{f_3}}$$

$$= f_1 \cdot f_2 + f_3$$

$$= xy(x'y' + y'z + x'z) + (xy' + y'z)$$

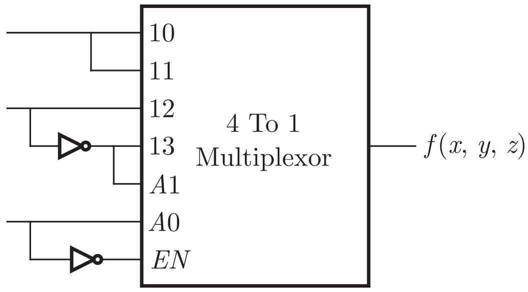
$$f_3 = xy'z + xy'z' + xy'z + x'y'z$$

$$f_3 = \Sigma(1,4,5)$$

Hence (A) is correct option.

Question. 12

Consider the following multiplexor where 10, 11, 12, 13 are four data input lines selected by two address line combinations $A1A0 = 00,01,10,11$ respectively and f is the output of the multiplexor. EN is the Enable input.



The function $f(x, y, z)$ implemented by the above circuit is

(A) xyz'

(B) $xy + z$

(C) $x + y$

(D) None of the above

SOLUTION

A_1	A_0	E_N	(MUX) work
0	0	1	do not
0	1	0	(MUX) Work
1	0	1	do not
1	1	0	

So MUX is ENABLED only if $A_0 = 0$

So output should have Z'.

Consider xyz' option (A)

$A, A_0 = 1 \quad 0$ gives correct answer.

Hence (A) is correct option.

Question. 13

Let $f(A, B) = A' + B$. Simplified expression for function $f(f(x + y, y), z)$ is

(A) $x' + z$

(B) xyz

(C) $xy' + z$

(D) None of the above

SOLUTION

$$f(x + y, y) = (x + y)' + y$$
$$\Rightarrow \overline{x + y} + y$$
$$f(f(x + y, y), z) = \overline{\overline{x + y} + y} + z$$
$$\Rightarrow (\overline{\overline{x + y}} \cdot \overline{y}) + z$$
$$[(x + y) \cdot \overline{y}] + z$$

$$[x\overline{y} + y\overline{y}] + z$$
$$x\overline{y} + z$$

Hence (C) is correct option.

Question. 14

What are the states of the Auxiliary Carry (AC) and Carry Flag (CY) after executing the following 8085 program ?

```
MIV   H,   5DH
MIV   L,   6BH
MOV   A,   H
ADD   L
```

(A) $AC = 0$ and $CY = 0$
(B) $AC = 1$ and $CY = 1$
(C) $AC = 1$ and $CY = 0$
(D) $AC = 0$ and $CY = 1$

SOLUTION

Program is to add 2 nos kept in H & L, result of addition is stored in A.

$(5D)_{16} + (6B)_{16} \Rightarrow$

```
       (1) 1 1 1
    0 1 0 1 1 1 0 1
  + 0 1 1 0 1 0 1 1
  -----------------
(0) 1 1 0 0 1 0 0 0
```

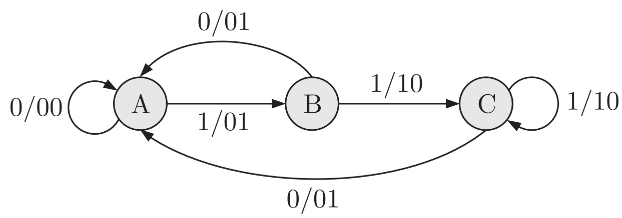
[0] is the carry so CY = 0

(1) is auxillary carry AC = 1

Hence (C) is correct option.

Question. 15

The finite state machine described by the following state diagram with A as starting state, where an arc label is $\frac{x}{y}$ and x stands for 1-bit input and y stands for 2-bit output.



(A) Outputs the sum of the present and the previous bits of the input.

(B) Outputs 01 whenever the input sequence contains 11

(C) Outputs 00 whenever the input sequence contains 10

(D) None of the above.

SOLUTION

Previous input	Present i/p	Output
0(A)	0(A)	00
0(A)	1(B)	01
1(B)	0(A)	01
1(B)	1(C)	10
1(C)	1(C)	10
1(C)	0(A)	01

So output is always sum of the present and previous bits of input.
Hence (A) is correct option.

YEAR 2003

Question. 16

Assuming all numbers are in 2's complement representation, which of the following number is divisible by 11111011?

(A) 11100111 (B) 11100100

(C) 11010111 (D) 11011011

SOLUTION

We can't judge the no's in 2's complement first we need to convert them in decimal

Given no. 11111011→00000101=5

(A) $11100111 \rightarrow 00011001 = 25$
(B) $11100100 \rightarrow 00011100 = 28$
(C) $11010111 \rightarrow 00101001 = 41$
(D) $11011011 \rightarrow 00100101 = 37$

From all only option (A) is divisible by 5.

Shortcut : To convert 2's complement no. directly into original binary, we should complement all the digits from MSB till the last one (1). Keep the last 1 from the LSB as it is. Observe in the example.

Question. 17

The following is a scheme for floating point number representation using 16 bits.

Bit Position	15	14... ... 9	8... 0
	s	e	m
	sign	exponent	Mantissa

Let s, c and m be the number represented in binary in the sign, exponent, and mantissa fields respectively. Then the flouting point number represented id

$$\begin{cases} (-1)^2(1 + m \times 2^{-9})2^{e-31}, \text{ if the exponent } 111111 \\ 0 \text{ otherwise} \end{cases}$$

What is the maximum difference between two successive real numbers representable in this system?

(A) 2^{-40}
(B) 2^{-9}
(C) 2^{22}
(D) 2^{31}

SOLUTION

e has 6 bits so max value can be

$$2^6 - 1 = 63 \text{ when } e = 111111$$

But given $e \neq 111111$

So max $e = 62 = 111110$

Two consecutive number will have same exponent but difference in mantissa by 1.

Difference would be

$$(-1)^2(1 + (m+1)2^{-9})2^{62-31} - (-1)^2(1 + m \times 2^{-9})2^{62-31}2^{31} \times 2^{-9}$$
$$= 2^{22}$$

Hence (C) is correct option.

Question. 18

A 1-input, 2-output synchronous sequential circuit behaves as follows.

Let z_k, n_k denote the number of 0's and 1's respectively in initial k bits of the input $(z_k + n_k = k)$. The circuit outputs 00 until one of the following conditions holds.

1. $n_k - n_k = 2$. In this case, the output at the k-th and all subsequency clock ticks is 10.

2. $n_k - z_k = 2$. In this case, the output at the k-th and all subsequent clock ticks is 01.

What in the minimum number of states required in the state transition graph of the above circuit?

(A) 5
(B) 6
(C) 7
(D) 8

SOLUTION

The sequential circuit has 3 variables to decide the state in which input & 2 inputs are present. Output for particular inputs decide states.

i/p	op 1	op 2	State
0	0	0	Intial
0	0	1	$n_K - z_K = 2$
0	1	0	$z_K - n_K = 2$
0	1	1	Not applicable
1	0	0	Initial
1	0	1	$n_K - z_K = 2$
1	1	0	$z_K - n_K = 2$
1	1	1	is correct

Using 3 bits we require
$2^3 - 1 = 7$ states here.
Hence (C) is correct option.

Question. 19

The literal count of a boolean expression is the sum of the number of times each literal appears in the expression. For example, the literal count of $(xy + xz)$ is 4. What are the minimum possible literal counts of the product-of-sum and sum-of-product representations respectively of the function given by the following karnaugh map?

Here, × denotes "don't care"

xy \ zw	00	01	11	10
00	×	1	0	1
01	0	1	×	0
11	1	×	×	0
10	×	0	0	×

(A) (11,9)

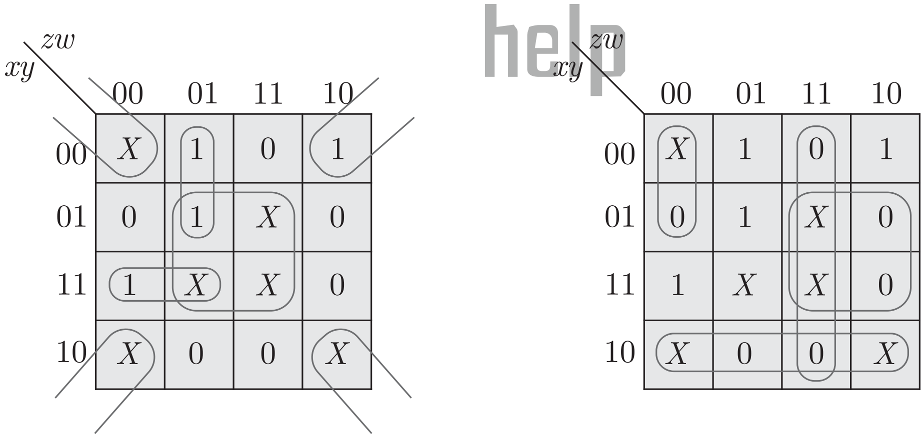
(B) (9,13)

(C) (9,10)

(D) (11,11)

SOLUTION

Considering product of sum & sum of product separately.



Sum of product

$= wy + w'y' + z'wx' + xyz'$

12 34 567 8910

Literal count =10

Product of sum

$= (y' + z')(z' + y)(w' + z')$

$(x + z + w)$

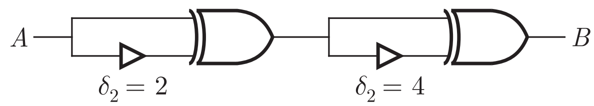
Lateral count =9

Hence (C) is correct option.

In SOP the K-map is solved for 1 & POS K-map solved for 0

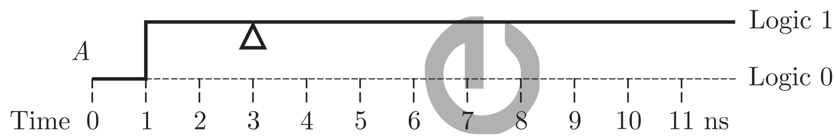
Question. 20

Consider the following circuit composed of XOR gates and non-inverting buffers.



The non-inverting buffers have delays $\delta_1 = 2ns$ and $\delta_2 = 4ns$ as shown

in the figure. both XOR gates and al wires have zero delay. Assume that all gate inputs, outputs and wires are stable at logic level 0. If the following waveform is applied at input. A, how many transition (s) (change of logic levels) occur (s) at B during the interval from 0 to 10 ns?



(A) 1
(B) 2
(C) 3
(D) 4

SOLUTION

Due to delays $S_1 = 2$ & $S_2 = 4$ the transitions would occur at time 1, 2 & 4.

	Time	Input (A)	Output (B)	
	0	1	0	
I	1	1	0	Transition
II	2	1	0	Transition
III	4	0	1	Transition

So total 3 transitions
Hence (C) is correct option.

YEAR 2004

Question. 21

The Boolean function $x'y' + xy + x'y$ is equivalent to

(A) $x' + y'$ (B) $x + y$

(C) $x + y'$ (D) $x' + y$

SOLUTION

$x'y' + xy + xy'$

$x'(y + y') + xy$ $(A + A') = 1$

$x' + xy$ $(A + AB) = (A + A) \cdot (A + B)$

$(x' + x) \cdot (x' + y)$

$1 \cdot (x' + y)$

$x' + y$

Hence (D) is correct option.

Question. 22

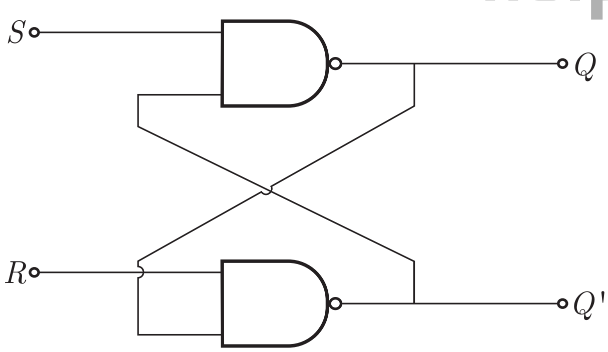
In an SR latch made by cross-coupling two NAND gates, if both S and R inputs are set to 0, then it will result in

(A) $Q = 0, Q' = 1$ (B) $Q = 1, Q' = 0$

(C) $Q = 1, Q' = 1$ (D) Indeterminate states

SOLUTION

SR latch both S and R when 0 leads to invalid state.



Transition table for SR flip flop.

S	R	Q(Next state)
0	0	Invalid so Q=Q'=1 change
0	1	1
1	0	0
1	1	previous state

For S=R=0 Q=Q'=1

Hence (C) is correct option.

Question. 23

If 73_x (in base-x number system) is equal to 54, (in base-y number system), the possible values of x and y are

(A) 8, 16 (B) 10, 12

(C) 9, 13 (D) 8, 11

SOLUTION

$$(73)_x = (54)_y$$
$$7x + 3 = 5y + 4$$

(x, y)	$7x+3$	$5y+4$
8, 16	59	84
10, 12	73	64
9, 13	64	69
8, 11	59	59

Hence (D) is correct option.

Question. 24

What is the result of evaluating the following two expressions using three-digit floating point arithmetic with rounding?

(113.+−111.)+7.51

113.+(−111.+7.51)

(A) 9.51 and 10.0 respectively (B) 10.0 and 9.51 respectively

(C) 9.51 and 9.51 respectively (D) 10.0 and 10.0 respectively

SOLUTION

Expression 1

$(113.0 + (-111.) + 7.51$

$(113.0 - 111.0) + 7.51$

$2.0 + 7.51$

9.51

10 rounded off

Expression 2

$113.0 + (-111.0 + 7.51)$

$113.0 + (-103.49)$

$113.0 - 103.00$

10.0 rounded off

Hence (D) is correct option

Question. 25

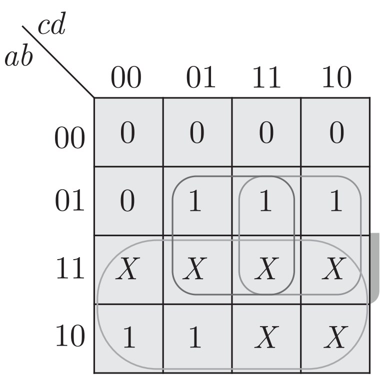
A circuit outputs a digit in the form of 4 bits. 0 is represented by 0000, 1 by 0001,...9 by 1001. A combinational circuit is to be diesigned which takes these 4 bits as input and outputs 1 if the digit ≥ 5, and 0 otherwise. If only AND, OR and NOT gates may be used, what is the minimum number of gates required?

(A) 2 (B) 3

(C) 4 (D) 5

SOLUTION

CKT takes 4 bits as the input so K-Map will have 4 variable so 16 options are available.



1 digit = 5
0 otherwise
Here for 0 to 4 we have 0 output, from 5 to 9 1 output & for 10 to 15 don't care. 1 octed & 2 pounds.
$a + bd + bc$
$a + b(d + c)$
Two OR gates
One AND gate
Total 3
Hence (B) is correct option.

Question. 26

Which are the essential prime implicates of the following Boolean function?

$$f(a, b, c) = a'c + ac' + b'c$$

(A) $a'c$ and ac' (B) $a'c$ and $b'c$

(C) $a'c$ only (D) ac' and bc'

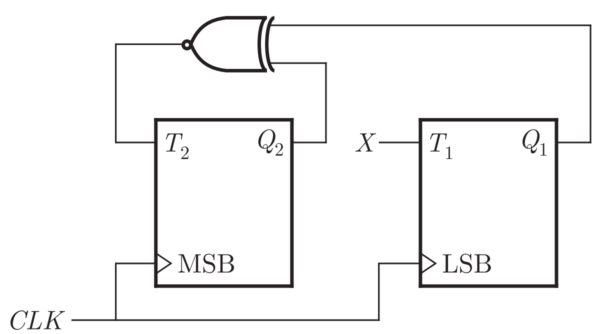
SOLUTION

$$f(a,b,c) = a'c + ac' + b'c$$

Making min terms $a'bc + a'b'c + abc' + ab'c' + a'b'c + ab'c$
Since $b'c$ gives no new term.
So $a'c$ & ac' are only essential prime implicants.
Solution detailed method
Tabulation method
Since $b'c$ gives no new term.
So $a'c$ & ac' are only essential prime implicants.
Solution detailed method
Tabulation method
$f(a,b,c) = \sum m(1,3,5,6,4)$
Figure
Figure
3 & 6 have only 1 cross they are in $a'c$ & ac'

Question. 27

Consider the partial implementation fo a 2-bit counter using T flip flops following the sequence 0-2-3-1-0, as shown below



To complete the circuit, the input X should be

(A) Q_2' (B) $Q_2 + Q_1$

(C) $(Q_1 \oplus Q_2)'$ (D) $Q_1 \oplus Q_2$

SOLUTION

Counter counts the no. of signal inversion change of states.
Sequence input is $0-2-3-1-0$

Binary $00-10-11-01-00$ to generate signals if we XOR gate then it outputs 1 if both are different.

So output sequence would be. $0-1-0-1-0$ & the sequence would be counted.

So. $X = Q_1 \oplus Q_2$

Hence (D) is correct option.

Question. 28

A 4-bit carry look ahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncompensated forms and the delay of each gate is one time unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND-OR logic.

(A) 4 time units
(B) 6 time units
(C) 10 time units
(D) 12 time units

SOLUTION

Carry of any higher order bit is dependent upon previous order bit addition generated carry.

$$\text{C out} = g_0 + p_0 \text{ C in}$$

$$P_3 P_2 P_1 P_0$$

$$\underline{g_3\ g_2\ g_1 g_0}$$

$$c_3\ c_2\ c_1\ c_0$$

$$c_3\ g_3 + P_3 g_2 + P_3 P_2 g_1 + |\ P_3 P_2 P_1 g_0 + P_3 P_2 P_2 P_0 \text{ C in}$$

This is 4 bit look ahead adder equation total gate delay

$$= 1 + 1 + 2 + 2$$

$$= 6$$

Hence (B) is correct option.

Question. 29

Let $A = 11111010$ and B 0000 1010 be two 8-bit 2's complement numbers. Their product in 2's complement is

(A) 1100 0100
(B) 1001 1100
(C) 1010 0101
(D) 1101 0101

SOLUTION

A and B are in 2's complement form.

$$A = 11111010$$

$$\text{Binary} = 00000110 = 6$$

2's complement represent $-ve$ number

So $\quad A = -6$

$$B = 00001010$$

MSB is 0 so $+ve$ no. decimal 10.

$$B = 10$$

$$A \times B = -6 \times 10$$

$$= -60$$

$$\text{Binary of } 60 = 00111100$$

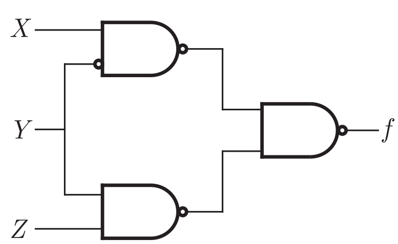
2's complement 11000100

Hence (A) is correct option.

YEAR 2005

Question. 30

Consider the following circuit.



Which one of the following is TRUE?

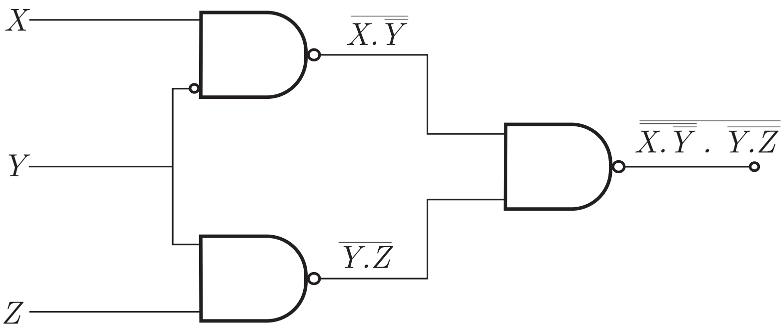
(A) f is independent of X

(B) f is independent of Y

(C) f is independent of Z

(D) None of X, Y, Z is redundant

SOLUTION

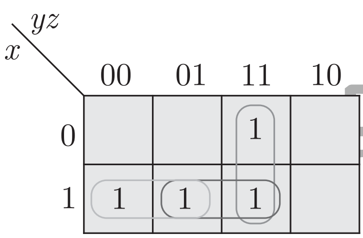


$$\begin{aligned} f &= \overline{\overline{X\cdot\overline{Y}}\cdot\overline{Y\cdot Z}} \\ &= \overline{\overline{X\cdot\overline{Y}}}+\overline{\overline{Y\cdot Z}} \\ &= X\cdot\overline{Y}+Y\cdot Z \end{aligned}$$

For redundant check we need to draw K map to min terms.

$X\overline{Y}(Z+\overline{Z})+(X+\overline{X})\cdot YZ$

$X\overline{Y}Z+X\overline{Y}\,\overline{Z}+XYZ+\overline{X}\,YZ$



$X\,\overline{Y}+YZ+XZ$

Hence (D) is correct option.

Question. 31

The range of integers that can be represented by an a bit 2's complement number system is

(A) -2^{n-1} to $(2^{n-1}-1)$

(B) $-(2^{n-1}-1)$ to $(2^{n-1}-1)$

(C) -2^{n-1} to 2^{n-1}

(D) $-(2^{n-1}+1)$ to $(2^{n-1}-1)$

SOLUTION

n bit 2's complement system must have corresponding bit binary system.

But to implement $+ve$ & $-ve$ nos.

Both we require MSB to be sign bit.

So maximum magnitude can be $2^{n-1}-1$ suppose we take $n=4$.

Using 4 bits.

1 1 1 1,. . . . . .0 0 0 0, ...01 1 1

-7 $\qquad\qquad\qquad\qquad\qquad$ $+7$

This would be the range.

So $-(2^{n-1}-1)$ to $+(2^{n-1}-1)$

Hence (B) is correct option.

Question. 32

The hexadecimal representation of 657_8 is

(A) 1AF $\qquad$ (B) D78

(C) D71 $\qquad$ (D) 32F

SOLUTION

$$(657)_8 = (?)_{16}$$

Making binary

$$\underbrace{0\,0\,0\,1}\,\underbrace{1\,0\,1\,0}\,\underbrace{1\,1\,1\,1} = (IAF)_{16}$$

Hence (A) is correct option.

Question. 33

The switching expression corresponding to

$$f(A,B,C,D) = \sum(1,4,5,9,11,12) \text{ is}$$

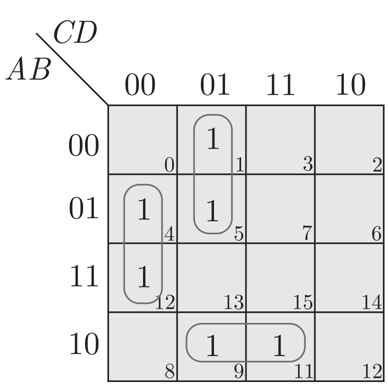
(A) $BC'D' + A'C'D + AB'D$ $\qquad$ (B) $ABC' + ACF + B'C'D$

(C) $ACD' + A'BC' + AC'D'$ $\qquad$ (D) $A'BD + ACD' + BCD'$

SOLUTION

$$f(A,B,C,D) = \sum(1,4,5,9,11,12)$$

Drawing K map for min terms.



$$B\overline{C}\,\overline{D}+\overline{A}\,\overline{C}\,\overline{D}+A\,\overline{B}\,D$$

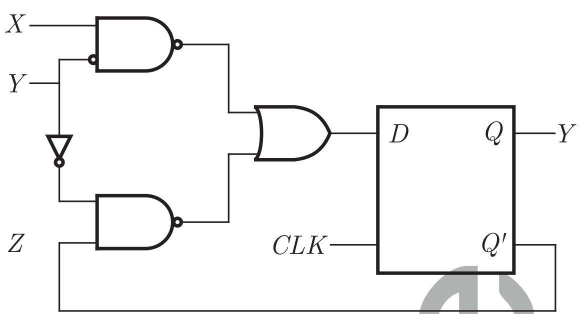
So min terms are

$$B\,\overline{C}\,\overline{D}+\overline{A}\,\overline{C}D+A\overline{B}\,D$$

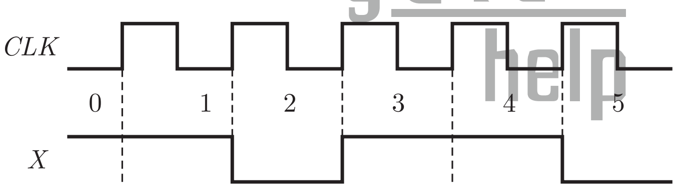
Hence (A) is correct option.

Question. 34

Consider the following circuit involving a positive edge triggered D -FF.



Consider the following timing diagram. Let Ai represent the logic level on the line A in the $i-th$ clock period.



Let A represent the complement of A. The correct output sequence on Y over the clock perids 1 through 5 is

(A) $A_0 A_1 A_1' A_3 A_4$

(B) $A_0 A_1 A_2' A_3 A_4$

(C) $A_1 A_2 A_2' A_3 A_4$

(D) $A_1 A_2' A_3 A_4 A_5$

SOLUTION

We need to calculate equation for D input.

$$D = (A_i X')' - (X'Q')'$$

$$= A_i + X + X + Q$$

$$D = A_i' + X + Q$$

Drawing truth table for ckt

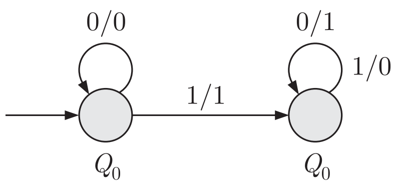
Clock	X	$Q_0 = 0$	$Q_1 = 1$	A_i	Y

0	1	0	1	A_0'	A_0'
1	1	0	1	A_1'	A_0'
2	0	0	1	A_2'	A_1'
3	1	0	1	A_3'	A_1'
4	1	0	1	A_4'	A_3'
5	0	0	1	A_5'	A_4'

Hence (A) is correct option.

Question. 35

The following diagram represents a finite state machine which takes as input a binary number from the least significant bit



Which one of the following is TRUE?

(A) It computes 1's complement of the input number

(B) It computes 2's complement of the input number

(C) It increments the input number

(D) It decrements the input number

SOLUTION

The transition table for the diagram

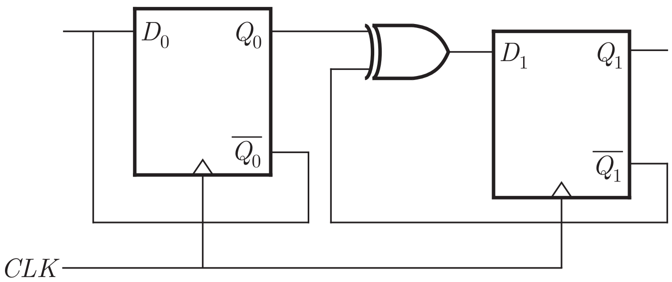
Present state	Input	Next state	Output
Q_0	0	Q_0	0
Q_0	1	Q_1	1
Q_1	0	Q_1	1
Q_1	1	Q_1	0

So the FSM takes input from LSB side it doesn't change state till the first 1 comes from LSB side, after that it complement all the bits. This is logic for 2's complement.

Hence (B) is correct option.

Question. 36

Consider the following circuit



The flip-flops are positive edge triggered $DFFs$. Each state is designated as a two bit string Q_0, Q_1. Let the initial state be 00. The state transition sequence is

(A) $00 \to 11 \to 01$

(B) $00 \to 11$

(C) $00 \to 10 \to 01 \to 11$

(D) $00 \to 11 \to 01 \to 10$

SOLUTION

Truth table for DFF

CP	D	Q_{n+1}	Action
0	X	Q_n	No change
1	0	0	Reset
1	1	1	Set

D here $AX + X'Q'$

Truth table for ckt

Q_1	Q_0	N	S
0	0	1	1
1	1	1	0
1	0	0	1
0	1	0	0
0	0	1	1

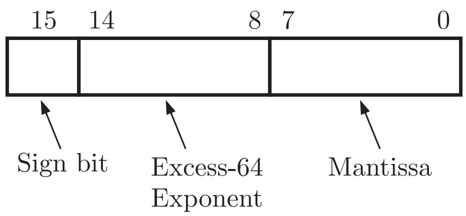
and so on.

Hence (D) is correct option.

Data for Q. 37 & 38 are given below.

Solve the problems and choose the correct answers.

Consider the following floating point format



Mantissa is a pure fraction is sign-magnitude form.

Question. 37

The decimal number 0.239×2^{13} has the following hexadecimal representation without normalization and rounding off

(A) $0D\ 24$ (B) $0D\ 4D$

(C) $4D\ 0D$ (D) $4D\ 3D$

SOLUTION

Sign bit 0

Exponent $= 13$

Excess $64 = 13 + 64 = 77 = 1001101$

Binary of 239

	carry
$.239 \times 2$	0
$.478 \times 2$	0
$.956 \times 2$	1
$.912 \times 2$	1
$.824 \times 2$	1
$.648 \times 2$	1
$.296 \times 2$	0
$.592 \times 2$	1
$.184$	

We have 8 bits for Mantissa 0 0 1 1 1 1 0 1

So the floating point format.

0	1 0 0 1 1 0 1	0 0 1 1 1 1 0 1	
0 1 0 0	1 1 0 1	0 0 1 1	1 1 0 1
4	D	3	D

Hence (D) is correct option.

Question. 38

The normalized representation for the above format is specified as follows. The mantissa has an implicit 1 preceding the binary (radix) point. Assume that only 0's are padded in while shifting a field. The normalized representation of the above number (0.239×2^{13}) is

(A) 0A 20
(B) 11 34
(C) 4D D0
(D) 4A E8

SOLUTION

Given no. $.239 \times 2^{13}$

Normalized form of binary.

Binary → $.239 = (00111101)_2$

Normalized $= 1.11101 \times 2^{10}$
↑

Proceeding implicit 1

So 8 bit mantissa

11101000 (000 = padding)

Excess 64 exponent

1 0 0 1 0 1 0 = 74

Sign bit = 0

Floating	Point	Format	
0	1001010	11101000	
0100	1010	1110	1000
4	A	E	8

GAE8

Hence (D) is correct option.

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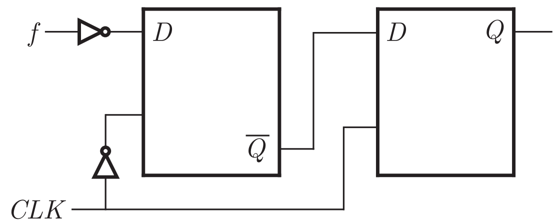
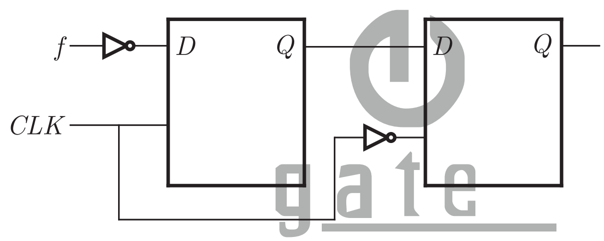
Question. 39

You are given a free running clock with a duty cycle of 50% and a digital waveform f which changes only at the negative edge of the clock. Which one of the following circuits (using clocked D flip flops) will delay the phase of f by 180° ?

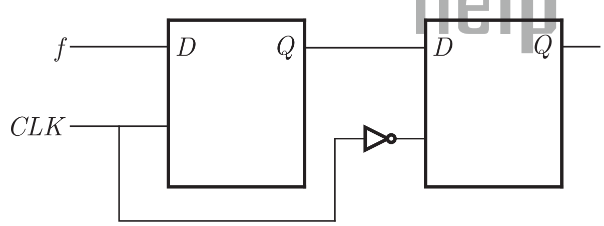
(A)



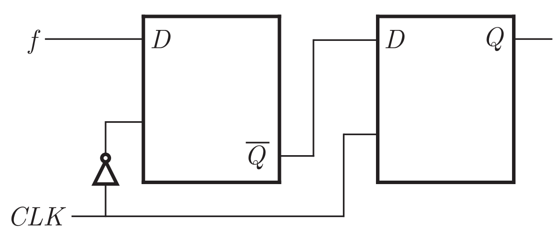
(B)



(C)

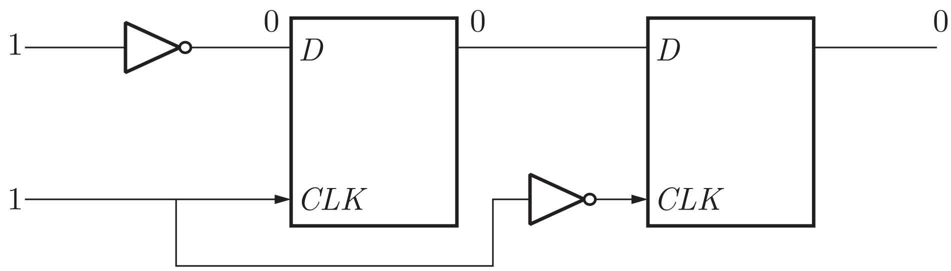


(D)



SOLUTION

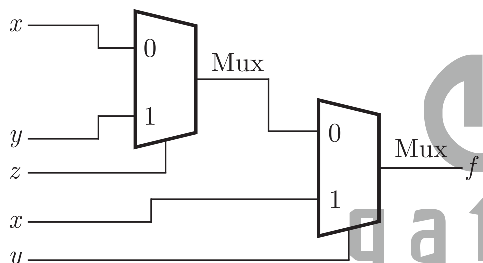
We require phase shift of 180 in f In ckt (B) the negation of signal f & clock delays signal f by 180.



So phase shift occurs.
Hence (B) is correct option.

Question. 40

Consider the circuit below. Which one of the following options correctly represents $f(x, y, z)$?



(A) $x\bar{z} + xy + \bar{y}z$ (B) $x\bar{z} + xy + y\bar{z}$

(C) $xz + xy + \bar{y}\bar{z}$ (D) $xz + x\bar{y} + \bar{y}z$

SOLUTION

MVXI
Selects X when Z = 0
Y' when Z = 0
MVX II
Selects $(XZ' + Y'Z)$ when $y = 0$
X when $y = 0$ so $(XZ' + YZ)\,Y' + XY$

$$\begin{aligned}\text{Simplifying} &= xz'y' + zy'y' + xy\\ &= xz'y' + xy(z + z') + zy'\\ &= xz'y' + xyz + xyz' + zy'(x + x')\\ &= xz'y' + xyz + xyz' + xy'z + x'y'z\\ &= y'z + xy'z + xyz' + xyz + xyz'\,[a + a = a]\\ &= y'z + xz'(y + y') + xy(z + z')\\ &= y'z + xz' + xy\end{aligned}$$

Hence (A) is correct option.

Question. 41

Given two three bit numbers $a_2 a_1 a_0$ and $b_2 b_1 b_0$ and c, the carry in, the function that represents the carry generate function when these two numbers are added is

(A) $a_2 b_2 + a_1 a_1 b_1 + a_2 a_1 a_0 b_0 + a_2 a_0 b_1 b_0 + a_1 b_2 b_1 + a_1 a_0 b_2 b_0 + a_0 b_2 b_1 b_0$

(B) $a_2 b_2 + a_2 b_1 b_0 + a_2 a_1 b_1 b_0 + a_1 a_0 b_{21} b_1 + a_1 a_0 b_2 + a_1 a_0 b_2 b_0 + a_2 a_0 b_1 b_0$

(C) $a_2 + b_2 + (a_2 \oplus b_2)[a_1 + b_1 + (a_1 \oplus b_1)(a_0 + b_0)]$

(D) $a_2 b_2 + \overline{a_2} a_1 b_1 + \overline{a_2 a_1} a_0 b_0 + \overline{a_2} a_0 \overline{b_1} b_0 + a_1 \overline{b}_2 b_1 \overline{a_1} a_0 \overline{b}_2 b_0 + a_0 \overline{b_2 b_1} b_0$

SOLUTION

a_2	a_1	a_0	b_2	b_1	b_0	C
0	0	0	0	0	0	0
0	0	1	0	0	1	1
0	1	0	0	1	0	
0	1	0	0	1	1	
1	0	1	1	0	0	
1	0	0	1	0	1	
1	1	1	1	1	0	
1	1	0	1	1	1	

Case I These are the possible value of $a_2 a_1 a_0$ & $b_2 b_1 b_0$ when $a_2 = 1$ $c = 1$

Case II $b_2 = 1$ $c = 1$ so $a_2 + b_2$

Case III If any 1 of a_2 or b_2 is 1 $a_2 \oplus b_2$
then if $a_1 = 1$ $c = 1$
$b_1 = 1$ $c = 1$ so $a_2 \oplus b_2 [a_1 + b_1]$

Case IV If any of a_2 or b_2 is 1 & any of a_2 or b_1 is 1
then if $a_0 = 1$ $c = 1$ or if $b_0 = 1$ then $c = 1$ so overall.
$a_2 + b_2 + [(a_2 \oplus b_2)\{a_1 + b_1 + (a_1 \oplus b_1)(a_0 + b_0)\}]$

Hence (C) is correct option.

Question. 42

Consider a boolean function $f(w, x, y, z)$. Suppose that exactly one of its inputs is allowed to change at a time. If the function happens to be true for two input vectors $i_1 + < w_1, x_1, y_1, x_1 >$ and $i_2 + < w_2, x_2, y_2, z_2 >$

, we would like the function to remain true as the input changes from i_1 to i_2(i_1 and i_2 differ in exactly one bit position), without becoming false momentarily. Let $f(w,x,y,z) = \sum(5,,711,12,13,15)$. Which of the following cube covers of f will ensure that the required property is satisfied?

(A) $\overline{w}xz, wx\overline{y}, x\overline{y}z, xyz, wyz$

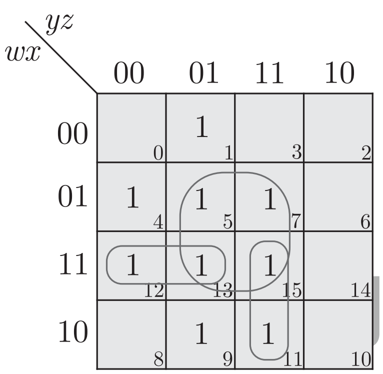
(B) $wxy, \overline{w}xz, wyz$

(C) $wx\overline{yz}, xz, w\overline{x}yz$

(D) $wzy, wyz, wxz, \overline{ww}xz, x\overline{y}z, xyz$

SOLUTION

Given function $f(w,x,y,z) \;= \Sigma(5,7,11,12,13,15)$ draw K-map of the above function.



1 quad $= xz = xz(y + y') = xzy + xy'z$

2 pairs $= wxy' + wyz$

$xyz + xy'z + wxy' + wyz$

Hence (A) is correct option.

Question. 43

We consider addition of two 2's complement numbers $b_{n-1}b_{n-2}.....b_0$ and $a_{n-1}a_{n-2}....a_0$. A binary adder for adding unsigned binary numbers is used to add the two numbers. The sum is denoted by $c_{n-1}c_{n-2}....c_0$ and the carryout by c_{out}. Which one of the following options correctly identifies the overflow condition?

(A) $c_{out}\overline{(a_{n-1} \oplus b_{n-1})}$

(B) $a_{n-1}b_{n-1}\overline{c_{n-1}} + \overline{a_{n-1}b_{n-1}c_{n-1}}$

(C) $c_{out} \oplus c_{n-1}$

(D) $a_{n-1} \oplus b_{n-1} \oplus c_{n-1}$

SOLUTION

Binary adder generates C out only if

1	C in	1	0	1
0	a	1	1	1
1	b	0	1	1
1	C out	1	1	1

C out in this case is C_{n-1} generated carry.

C in is C_{n-2}

So

$$b'_{n-1}a'_{n-1}c_{n-2} + b_{n-1}a_{n-1}c'_{n-2}$$

$$f = C_{out} \oplus C_{n-1}$$

Hence (C) is correct option.

Question. 44

Consider number represented in 4-bit gray code. Let $h_3h_2h_1h_0$ be the gray code representation of a number n and let $g_3g_2g_1g_0$ be the gray code of $(n+1)$ (modulo 16) value of the number. Which one of the following functions is correct?

(A) $g_0(h_1h_2h_1h_0) = \sum(1,2,3,6,10,13,14,15)$

(B) $g_1(h_1h_2h_1h_0) = \sum(4,9,10,11,12,,13,14,15)$

(C) $g_2(h_1h_2h_1h_0) = \sum(2,4,5,6,7,12,,13,15)$

(D) $g_3(h_1h_2h_1h_0) = \sum(0,1,6,7,10,11,12,,13,)$

SOLUTION

Binary	h	$h_3h_2h_1h_0$	$(n+1)$ mod 16	$g_3g_2g_1g_0$
0000	0	0000	1	0001
0001	1	0001	2	0011
0010	2	0011	3	0010
0011	3	0010	4	0110
0100	4	0110	5	0111
0101	5	0111	6	0101
0110	6	0101	7	0100
0111	7	0100	8	1100
1000	8	1100	9	1101

1001	9	1101	10	1111
1010	10	1111	11	1110
1011	11	1110	12	1010
1100	12	1010	13	1011
1101	13	1011	14	1001
1110	14	1001	15	1000
1111	15	1000	0	0000

This gives the solution option (B)

$$g_1(h_3, h_2, h_1, h_0) = \sum(4, 9, 10, 11, 12, 13, 14, 15)$$

YEAR 2007

Question. 45

What is the maximum number of different Boolean functions involving n Boolean variables?

(A) n^2
(B) 2^n
(C) 2^{2^n}
(D) 2^{n^2}

SOLUTION

Each boolean variable can have values 0 or 1, so for expression involving n boolean variables will have terms 2^n. These 2^n terms need to be arranged in different manner and nos., suppose $2^n = \text{M}$. So this arrangement would take 2^M ways or 2^{2^n} ways.
Hence (C) is correct option.

Question. 46

How many 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates?

(A) 7
(B) 8
(C) 9
(D) 10

SOLUTION

Total output lines required = 64
We need to use 3 to 8 decoders.
So decoders required $\frac{64}{8} = 8$ decoders for output.

But we need one more decoder i.e for combining result.

$$8 + 1 = 9 \text{ decoders.}$$

Hence (C) is correct option.

Question. 47

Consider the following Boolean function of four variables

$f(w, x,, y, z) = \sum(1,3,4,6,9,11,12,14)$

The function is

(A) independent of one variable

(B) independent of two variables

(C) independent of three variables

(D) dependent on all the variables

SOLUTION

$$f(w, x, y, z) = \sum m(1,3,4,6,9,11,12,14)$$

wx \ yz	00	01	11	10
00	(0)	1 (1)	1 (3)	(2)
01	1 (4)	(5)	(7)	1 (6)
11	1 (12)	(13)	(15)	1 (14)
10	(8)	1 (9)	1 (11)	(10)

2 qlead

1^{st} qlead $\quad xz'$

2^{nd} qlead $\quad x'z$

$$xz' + x'z\,xz' + x'z$$

So independent of 2 variables.

Hence (B) is correct option.

Question. 48

Let $f(w, x, y, z) = \sum(0,4,5,7,8,9,13,15)$. Which of the following expressions are NOT equivalent to f?

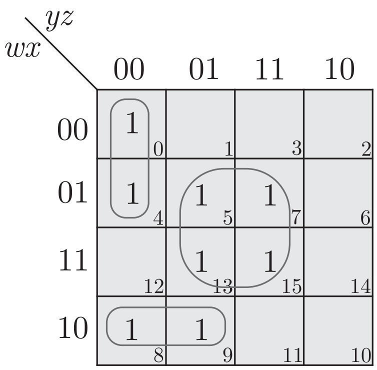
(A) $x'y'z + w'xy' + wy'z + xz$ (B) $w'y'x' + wx'y' + xz$

(C) $w'y'z' + wx'y' + xyz + xy'z$ (D) $x'y'z + wx'y' + w'y$

SOLUTION

$$f(w,x,y,z) = \sum m(0,4,5,7,8,9,13,15)$$

Drawing K-map.



$$xz + w'y'z' + wx'y'$$

Hence (B) is correct option.

Question. 49

Define the connective* for the boolean variable X and Y as: $X * Y = XY + X'Y'$

Let $Z = X * Z$

Consider the following expression P, Q and R.

$P: X = Y * Z Q: Y = X * Z$

$R: X * Y * Z = 1$

Which of the following is TRUE?

(A) only P and Q are valid

(B) Only Q and R are valid

(C) Only P and R are valid

(D) All P, Q, R are valid

SOLUTION

Given $Z = X * Z \quad \Rightarrow XZ + X'Z'$

$$\begin{aligned} P: X &= Y * Z \\ &= YZ + Y'Z' \\ &= Y(XZ + X'Z') + Y'Z' \\ &= XYZ + X'YZ' + Y'Z' \\ &= XYZ + X'YZ' + XY'Z' + X'Y'Z' \text{ valid.} \\ Q: Y &= X * Z \\ &= XZ + X'Z' \\ &= X(XZ + X'Z') + X'Z' \end{aligned}$$

$$\begin{aligned} &= XZ + X'Z' \\ &= X(Y + Y')Z + X'(Y + Y')Z' \\ &= XYZ + XY'Z + X'YZ' + X'Y'Z' \text{ valid} \\ R: X * Y * Z &= 1 \\ (XY + X'Y') * Z &\Rightarrow (XZ + X'Y')Z + (XY + X'Y')Z' \\ &\Rightarrow XYZ + X'Y'Z + [(\overline{XY} \cdot \overline{X'Y'})Z'] \\ &\Rightarrow XYZ + X'Y'Z + [(\overline{X} + \overline{Y}) \cdot (X + Y)]Z' \\ &\Rightarrow XYZ + X'Y'Z + X'YZ' + XY'Z' \neq 1 \end{aligned}$$

So invalid
Hence (A) is correct option.

Question. 50

Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of $n$variables. What is the minimum size of the multiplexer needed?

(A) 2^n line to 1 line
(B) 2^{n+1} line to 1 line
(C) 2^{n-1} line to 1 line
(D) 2^{n-2} line to 1 line

SOLUTION

To select 2^n lines we need a select function with n bits.
Here with n variables we have $(n-1)$ select bits thus 2^{n-1} data lines.
So MUX has 2^{n-1} lines to 1.
Hence (C) is correct option.

Question. 51

In a look-ahead carry generator, the carry generate function G_i and the carry propagate function P_i for inputs, A_i and B_i are given by $P_i = A_i \oplus B_i$ and $G_i = A_i B_i$

The expressions for the sum bit S and carry bit C_{i+1} of the look ahead carry adder are given by

$S_i + P_i \oplus C_i$ and $C_{i+1} G_i + P_i C_i$, Where C_0 is the input carry.

Consider a two-level logic implementation of the look-ahead carry generator.. Assume that all P_i and G_i are available for the carry generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with S_3, S_2, S_1, S_0 and C_4 as its outputs are respectively

(A) 6,3 (B) 10,4

(C) 6,4 (D) 10,5

SOLUTION

The equation for 4 bit carry look ahead adder is

$$C_{out}\ \ g_3 + p_3 g_2 + p_3 p_2 g_1 + p_3 p_2 p_1 g_0 + p_3 p_2 p_1 p_0 C_{in}$$

Here

no. of AND gates = 10

OR gates = 4

Hence (B) is correct option.

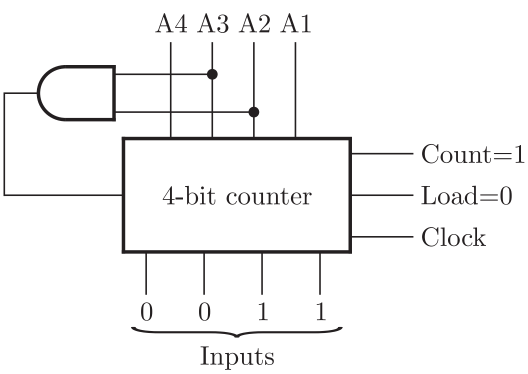
Question. 52

The control signal functions of 4-bit binary counter are given below

(where X is "don't care")

Clear	Clock	Load	Count	Function
1	X	X	X	Clear to 0
0	X	0	0	No change
0	↑	1	X	Load input
0	↑	0	1	Count next

The counter is connected as follows



Assume that the counter and gate delays are negligible. If the counter starts at 0, then it cycles through the following sequence

(A) 0,3,4 (B) 0,3,4,5

(C) 0,1,2,3,4 (D) 0,1,2,3,4,5

SOLUTION

From the truth table for the counter ckt we can see that when counter $= 1$. & load $= 0$, count next is the function.
So it would count from 0 to 4 & then clear to 0 & again start if clock input is increasing.
Hence (C) is correct option.

YEAR 2008

Question. 53

In the IEEE floating point representation the hexadecimal value $0x00000000$ corresponds to

(A) the normalized value 2^{-127} (B) the normalized value 2^{-126}

(C) the normalized value $+0$ (D) the special value $+0$

SOLUTION

This $0X00000000$ hexadecimal value can be converted into 32 bit binary.
0000 0000 0000 0000 0000 0000 0000 0000
$0 \times 2^{\circ}$
This is representation in IEEE floating point format.
Case for special $+0$.
Hence (D) is correct option.

Question. 54

In the karnaugh map shown below, X denoted a don't care term. What is the nominal form of the function represented by the karnaugh map

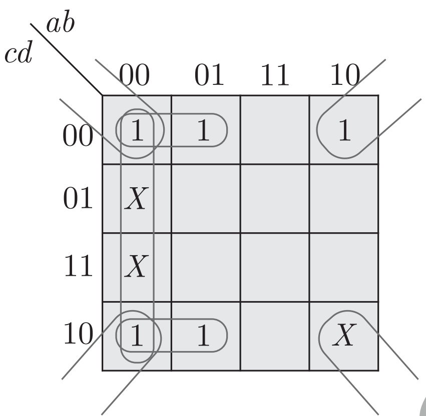
cd \ ab	00	01	11	10
00	I	I		I
01	×			
11	×			
10	I	I		×

(A) $\bar{b}.\bar{d} + \bar{a}.\bar{d}$ (B) $\bar{a}.\bar{b} + \bar{b}.\bar{d} + \bar{a}.\bar{b}.\bar{d}$

(C) $\bar{b}.\bar{d} + \bar{a}.\bar{b}.\bar{d}$ (D) $\bar{a}.\bar{b} + \bar{b}.\bar{d} + \bar{a}.\bar{d}$

SOLUTION

Given K-map is



$$\begin{aligned} \text{quad } 1 &\rightarrow \bar{a}\,\bar{b} \\ \text{quad } 2 &\rightarrow \bar{b}\,\bar{d} \\ \text{pair } 1 &\rightarrow \bar{a}\,\bar{c}\,\bar{d} \end{aligned}$$

So $\bar{a}\,\bar{b} + \bar{b}\,\bar{d} + \bar{a}\,\bar{d}(c + \bar{c})$

$\bar{a}\,\bar{b} + \bar{b}\,\bar{d} + \bar{a}\,\bar{d}$

Hence (D) is correct option.

Question. 55

Let a denote number system radix. The only value(s) of r that satisfy the equation $\sqrt{121} + 11$, is/are

(A) decimal 10 (B) decimal 11

(C) decimal 10 and 11 (D) any value> 2

SOLUTION

$$\sqrt{(121)_r} = (11)_r$$

If $r = 10$ it is true it can't be 2 since bit value can't be 2 then. It is not true for $r = 11$

It is true for 3 to 10.

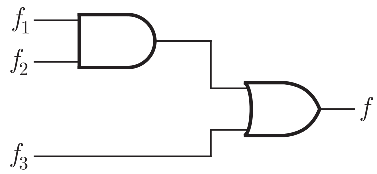
So it is true for

$r > 2$

Hence (D) is correct option.

Question. 56

Give f_1, f_3 and f in canonical sum of products form (in decimal) for the circuit



$$f_1 = \sum m(4,5,6,7,8)$$
$$f_3 = \sum m(1,6,15)$$
$$f = \sum m(1,6,8,15)$$

Then f_2 is

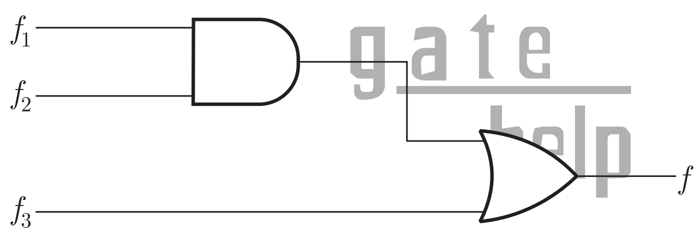
(A) $\sum m(4,6)$

(B) $\sum m(4,8)$

(C) $\sum m(6,8)$

(D) $\sum m(4,6,8)$

SOLUTION



Given $f = \Sigma m(1,6,8,15)$

$f_3 = \Sigma m(1,6,15)$

So output 1,6,8,15 here 1,6,15 can come form f_3.

Since the final gate is OR gate so from f_1 AND f_2 no minterm except 1,6,8,15 should come.

$f_1 = \Sigma m(4,5,6,7,8)$

So f_2 can be $\Sigma m(6,8)$

Since 4,5, & 7 should no 7 come here.

Hence (C) is correct option.

Question. 57

If P, Q, R are Boolean variables, $(P+\bar{Q})\ (P.\bar{Q}+P.R)\ (\bar{P}.\bar{R}+\bar{Q})$ simplifies to

(A) $P.\bar{Q}$

(B) $P.\bar{R}$

(C) $P.\bar{Q} + R$ (D) $P.\bar{R} + Q$

SOLUTION

$$\begin{aligned}
&= (P + \overline{Q}) \cdot (P\overline{Q} + PR) \cdot (\overline{P}\,\overline{R} + Q) \\
&= (PP\overline{Q} + PPR + P\overline{Q}\,\overline{Q} + PQR)(\overline{P}\,\overline{R} + \overline{Q}) \\
&= (P\overline{Q} + PR + P\overline{Q} + P\overline{Q}R)(\overline{P}\,\overline{R} + Q) \\
&= (P\overline{Q} + PR + P\overline{Q}R)(\overline{P}\,\overline{R} + \overline{Q}) \\
&= [P\overline{Q}(1 + R) + PR](\overline{P}\,\overline{R} + Q) \\
&= P(\overline{Q} + R)(\overline{P}\,\overline{R} + \overline{Q}) \\
&= (P\overline{P}\,\overline{R} + P\overline{Q})(\overline{Q} + R) \\
&= P\overline{Q} \cdot (\overline{Q} + R) \\
&= P\overline{Q} + P\overline{Q}R \\
&= P\overline{Q}(1 + R) \\
&= P\overline{Q}
\end{aligned}$$

Hence (A) is correct option.

YEAR 2009

Question. 58

$(1217)_8$ is equivalent to

(A) $(1217)_{16}$ (B) $(028F)_{16}$

(C) $(2297)_{10}$ (D) $(0B17)_{16}$

SOLUTION

$$\begin{aligned}
&= (1217)_8 \\
&= \underbrace{0010}\underbrace{1000}\underbrace{1111} \\
&= (028F)_{16}
\end{aligned}$$

Hence (B) is correct option.

Question. 59

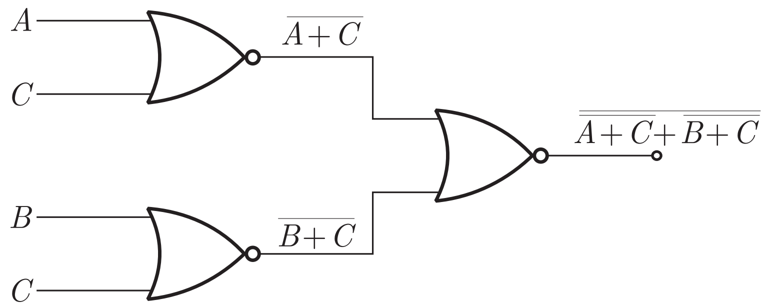
What is the minimum number of gates required to implement the Boolean function $(AB + C)$ if we have to use only 2-input NOR gates ?

(A) 2 (B) 3

(C) 4 (D) 5

SOLUTION

AB+C implementation through NOR gate ($\overline{X+Y}$)
We require one AND gate & 1 OR gate



AND gate & OR gate can be implemented by NOR gate.

$$= \overline{\overline{A+C}+\overline{B+C}}$$
$$= \overline{\overline{A+C}}\cdot\overline{\overline{B+C}}$$
$$= (A+C)\cdot(B+C)$$
$$= C+AB$$

So we require & NOR gates.
Hence (B) is correct option.

YEAR 2010

Question. 60

The minterm expansion of $f(P,Q,R) = PQ + Q\overline{R} + P\overline{R}$ is

(A) $m_2 + m_4 + m_6 + m_1$ (B) $m_0 + m_1 + m_3 + m_5$

(C) $m_0 + m_1 + m_6 + m_1$ (D) $m_2 + m_3 + m_4 + m_5$

SOLUTION

Given expression is

$$f(P,Q,R) = PQ + Q\overline{R} + P\overline{R}$$

For min term expansion we add the remaining variables in the expression.

$$= PQ(R+\overline{R}) + (P+\overline{P})\,Q\overline{R} + P(Q+\overline{Q})\,\overline{R}$$
$$= PQR + PQ\overline{R} + PQ\overline{R} + \overline{P}Q\overline{R} + PQ\overline{R} + P\overline{Q}R$$
$$= PQR + PQ\overline{R} + \overline{P}Q\overline{R} + P\overline{Q}\,\overline{R}$$
$$= m_7 + m_6 + m_2 + m_4$$
$$= 111 + 110 + 010 + 100$$
$$\text{So} = m_2 + m_4 + m_6 + m_7$$

Hence (A) is correct option.

Question. 61

P is a 16-bit signed integer. The 2's complement representation of P is $(F87B)_{16}$. The 2's complement representation of $8^{*}P$ is

(A) $(C3D8)_{16}$ (B) $(187B)_{16}$

(C) $(F878)_{16}$ (D) $(987B)_{16}$

SOLUTION

P's 2's complement.

$$= (F87B)_{16}$$

Is complement $= F87B - 1$

$$= (F87A)_{16}$$

In base 16 complement is done by subtracting from 15 i.e F.

$$P = (0785)_{16}$$
$$= (0000\,0111\,1000\,0101)_2$$
$$= 1 \times 2^{\circ} + 1 \times 2^{2} + 1 \times 2^{7} + 1 \times 2^{8} + 1 \times 2^{9} + 1 \times 2^{10}$$
$$P = 1925$$
$$8 \times P = 8 \times 1925 = 15400$$

Its binary 0011110000101000

For hexadecimal make pairs of 4 i.e. $(3C28)_{16}$

2's complement P = 1100 0011 1101 1000

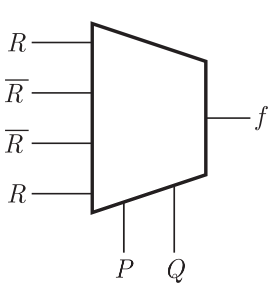
C 3 D 8

2's complement of P $= (C3D8)_{16}$

Hence (A) is correct option.

Question. 62

The Boolean expression for the output f of the multiplexer shown below is



(A) $\overline{P \oplus Q \oplus R}$ (B) $P \oplus Q \oplus R$

(C) $P + Q + R$ (D) $\overline{P + Q + R}$

SOLUTION

S_1 & so are the select bits which are used to select any 1 of the 4 inputs.
Selection table

$S_1(P)$	$S_0(Q)$	Input
0	0	0R
0	1	1$\overline{R}$
1	0	2$\overline{R}$
1	1	3R

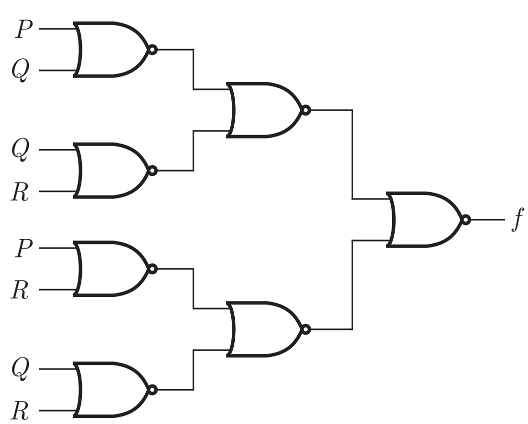
The expression has 3 variables
So K-map

P \ QR	00	01	11	10
0	0	1	0	1
1	1	0	1	0

This is K-map for $P \oplus Q \oplus R$
i.e $P\overline{Q}\,R + \overline{P}\,\overline{Q}\,\overline{R} + PQR + \overline{P}\,Q\overline{R}$
Hence (B) is correct option.

Question. 63

What is the boolean expression for the output f of the combinational logic circuit of NOR gates given below ?



(A) $\overline{Q+R}$ (B) $\overline{P+Q}$
(C) $\overline{P+R}$ (D) $\overline{P+Q+R}$

SOLUTION

After 1 stage

$\overline{P+Q}$ $\quad \overline{Q+R}$ $\quad \overline{P+R}$ $\quad \overline{Q+R}$

After 2 stage

$\overline{\overline{P+Q}+\overline{Q+R}}$ $\quad \overline{\overline{P+R}+\overline{Q+R}}$

After 3 stage

$$= \overline{\overline{\overline{P+Q}+\overline{Q+R}}+\overline{\overline{P+R}+Q+R}}$$

$\{\overline{A+B} = \overline{A}\cdot\overline{B}$

$$= (\overline{\overline{\overline{P+Q}+\overline{Q+R}}})\cdot(\overline{\overline{\overline{P+R}+\overline{Q+R}}})$$

$\{\overline{\overline{A}} = A$

$$= (\overline{P+Q}+\overline{Q+R})\cdot(\overline{P+R}+\overline{Q+R})$$

$\{\overline{A}+\overline{B} = \overline{A\cdot B}$

$$= \overline{(P+Q)\cdot(Q+R)}\cdot\overline{(P+R)\cdot(Q+R)}$$

$$= \overline{Q+PR}\cdot\overline{R+PQ}$$

$$= \overline{Q+PR+R+PQ}$$

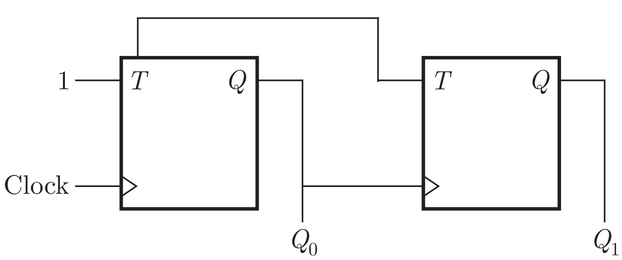
$$= \overline{R(P+1)+Q(P+1)}$$

$$= \overline{(Q+R)}$$

Hence (A) is correct option.

Question. 64

In the sequential circuit shown below, if the initial value of the output Q_1Q_0 is 00, what are the next four values of Q_1Q_0 ?



(A) 11, 10, 01, 00 (B) 10, 11, 01, 00
(C) 10, 00, 01, 11 (D) 11, 10, 00, 01

SOLUTION

There are 2 T-toggle flip flops in the ckt. Truth table for TFF.

CP	T	Q_{n+1}	
0	X	Q_n	Q_n previous state
1	0	Q_n	CP clock pulse
1	1	$\overline{Q_n}$	Q_{n+1} next state
			T toggle input

Since initially Q, $Q_0 = 00$, so during 1^{st} clock cycle both T & clock signals in ckt are 1. After $Q_0 = 1$ this fed to 2^{nd} TFF which invert previous state $Q_1 = 1$ so $Q_1 Q_0 = 11$

11 when fed to next cycle clock $= 1$ so $Q_0 = 0$ $Q_1 = 1$ since no inversion

Q, $Q_0 = 10$

In next cycle clock $= 1$ $Q_0 = 1$ inverse, $Q_1 = 0$ in the end $Q_1 Q_0 = 00$

So order 11, 10, 01, 00

Hence (A) is correct option.

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