

Code : T-03

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II Semester Diploma Examination, November 2010

E & C BOARD

DIGITAL ELECTRONICS – I

Time : 3 Hours ]

[Max. Marks : 100

- Instructions : (1) Section – I is compulsory.  
(2) Answer any six full questions choosing any two full questions from Section II, III & IV.

SECTION – I

1. (a) Fill in the blanks : 5 × 1 = 5
- (i) A max-term Boolean Expression is also called \_\_\_\_\_ form.
  - (ii) \_\_\_\_\_ two-input Nand gates must be used to produce two input NOR-function.
  - (iii) The excess 3 code number 10010011 equals in \_\_\_\_\_ in decimal.
  - (iv) The most important advantage of using CMOS is its Low power consp
  - (v) A \_\_\_\_\_ TTL input is equivalent to a HIGH Input.
- (b) Explain ASCII code. 5

SECTION – II

2. (a) List seven advantages of using Digital Systems. 7
- (b) Find the equivalent of
- (i)  $(3E6)_H = ( )_{10}$
  - (ii)  $(4095)_{10} = ( )_{16}$  4
- (c) Find the equivalent of
- (i)  $(156)_8 = ( )_{10}$
  - (ii)  $(391)_{10} = ( )_8$  4

[Turn over

3. (a) Draw the logic diagram and truth table for  
 (i) a two Input AND gate  
 (ii) a two Input OR gate  
 (b) Realize  
 (i) EX-NOR using NAND gates  
 (c) List three applications of EX-OR gate.

4. (a) Simplify  
 $XY + x(y + z) + y(y + z)$   
 using Boolean techniques.  
 (b) Apply De-morgans' theorem  
 (i)  $\overline{\overline{A + B} + \overline{C}}$   
 (ii)  $\overline{\overline{A + B} + \overline{CD}}$   
 (c) Subtract  $(11100)_2$  from  $(10011)_2$  using two's complement method.

### SECTION - III

5. (a) With block diagram explain the operation of a two-2 bit parallel adder.  
 (b) Differentiate between ENCODER and DECODER.  
 (c) Write logic symbol, truth table and logic diagram of full subtractor.
6. (a) Write the logic gate diagram of  $1 * 4$  Demultiplexer.  
 (b) List four applications of multiplexer.  
 (c) Draw the k-map for the following minterm and simplify  
 $Y = \Sigma 2, 3, 5, 6, 7, 9, 11, 13$ .  
 Consider the variables as A, B, C, & D.
7. (a) Differentiate between ENCODER and priority ENCODER.  
 (b) Explain  $1 : 8$  demultiplexer with circuit diagram and Truth Table.  
 (c) Explain the difference between MUX and DEMUX.

## SECTION - IV

- 8 (a) What do you mean by the following ? 12
- (i) LATCH
  - (ii) Level clocking
  - 4 (iii) Master-slave triggering
  - 3 (iv) Toggle
  - (v) Edge-Triggering
  - (vi) Race-condition
- (b) List three applications of a flip-flop. 3
- 7 9. (a) Define the terms : 8
- 4 (i) SSI
  - (ii) MSI
  - (iii) LSI
  - (iv) VLSI
- 4 (b) List five characteristics of ECL family of logic ckts. 5
- (c) What is fan-in ? 2
- 4 10. (a) With NAND gates logic diagram explain the operation of checked D-flip flop. 5
- 4 (b) What do you mean by the following ? 10
- 7 (i) Gate
  - (ii) truth-table
  - (iii) don't care
  - (iv) Redundant Group
  - (v) QUAD
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