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Use of A.C. Network Analyser and Digital Computer in Fault Calculations

Introduction — Problems on Network Analyzer — Description of A.C. Network Analyzer — Procedure of short circuit study on network analyzer — Digital Computer — Organization processes for solving engineering problem — Short circuit studies on digital computers

24.1. INTRODUCTION

Fault calculation of simple systems can be carried out with a calculator. Modern power systems are large and complex as they consist of generating stations, transmission lines, load centres etc. Fault calculations of such systems by direct means is laborious and time consuming. A.C. Network, Analyser, also called A.C. Calculating Board is being used for power system studies since 1929. A.C. Network Analyzer is in fact a small scale, single phase replica of the power system. It consists of component such as generators, transformers, load units impedance units, capacitors etc. which correspond to the components of the actual power system. The components of the network analyzed are connected such that it represents the power systems under study. For fault calculations, the fault is applied at different points of the analyzer and the fault currents and voltages are noted. The corresponding readings in actual values are obtained on multiplication by the scale factor. Besides fault calculations, the A.C. Network analyzer is used for stability studies, load flow studies, economic operation studies etc. But the use of Network Analyzer is restricted to the problem in power system alone. Digital computers are now being used for solving almost all the power system problems. No new Network Analyzers are installed any more. Digital computers are versatile computing devices, which can be used for solving a variety of technological, engineering, scientific, commercial and management problems. This chapter gives only an introduction the use of network analyzer and digital computer for fault calculations.

HVDC simulator is used for simulating various abnormal conditions in HVDC system and associated AC Networks.

24.2. A.C. NETWORK ANALYZER (A.C. CALCULATING BOARD)

(A) Problems that can be solved on an A.C. network analyzer.

1. Load studies.
2. Stability studies.
3. Special circuit problems.
4. Short circuit studies.

We will study the short circuit problems briefly. These include :

(*a*) Maximum short circuit current at different location for determining the short circuit duties of the circuit-breakers.

(*b*) Bus voltage during short circuits.

(*c*) Maximum and minimum fault currents and voltages for determining the relay settings.

(*d*) Effect of various types of neutral grounding on behaviour of power systems, etc.

(B) Description. Most A.C. network analyzer operate on 400 Hz or 480 Hz, though there are some, operating on 60 Hz or 10,000 Hz. Higher frequency permits smaller size of reactors.

An A.C. network analyzer consists of a number of independent single phase units such as generator units, variable resistors, reactors and capacitors, auto-transformers etc. The units can be arranged, adjusted and connected to have a circuit which represents the system under study. Sensitive measuring instruments ammeters, voltmeters, wattmeters, varmeters are provided for making electrical measurements at any point of system. For symmetrical fault calculations a single phase network is employed. For unsymmetrical fault the method of symmetrical components is used in which three sequence networks are involved. The nominal voltage or base voltage for a typical network analyzer is 50 volts and base current 50 milliamperes. Thereby base power is 2.5 watts and base impedance is 1000 ohms. All adjusting dials and instruments are marked in per unit of these base quantities. The 400 Hz supply is obtained from a motor generator set, or frequency converters.

Note. Figures in bracket give number of units in a particular network analyzer.

Generator Units (16). These represent the e.m.f. sources of actual power system. These are provided with independent phase shifter and voltage regulator. Each generator unit is equipped with voltmeter, varmeter. The output is single phase.

Line impedance Units (76). These consist of variable resistors and reactor connected in series and are used for representing transmission lines.

Load Impedance Units (50). These are adjustable resistors and reactors which are connected either in series or parallel to represent loads. The load impedance units have higher impedance rating than the line units.

Auto Transformer Units (32). Represent transformer.

Capacitor Units (48). Represent capacitances of cables, overhead transmission lines, capacitors, synchronous condensers.

Synchronous Impedance Units (16). Consist of adjustable resistors and reactors connected in series intended to represent synchronous impedances of machines.

Mutual Transformer Units (8). These are 1:1 ratio transformers which represent mutual reactance between parallel transmission lines which are not connected at the ends.

Master Instrument System. Consists of measuring instruments, metering selector panel, selector switches, etc.

(C) Procedure of fault calculation (Brief).

- To represent the power system by positive, negative and zero sequence network, chosen to common base MVA.
- To represent the network by network analyzer by choosing appropriate units mentioned in Sec. 23.3 (B) and connecting them such that the system is represented.
- The voltages and loads are adjusted to represent load condition.
- The fault is applied by plugging in the fault plug at desired point.
- The values of voltages and currents at various locations are measured.
- The multiplying factors are used to obtain the values corresponding to the represented system.

Three phase Faults. The network analyzer is arranged to represent the system under study. The voltages and loads are adjusted to obtain load balance for desired loading condition. Faults are applied by plugging the fault plug at a desired point of the system. The measurement of fault current is done by pressing the keys on the instrument panels.

Unsymmetrical Faults. The sequence networks (Refer Ch. 22) are arranged on the network analyzer. Very often the positive and negative sequence networks are further simplified with the assumption that they are identical. The study involving line to line faults do not require zero sequence network.

24.3. DIGITAL COMPUTERS

Digital computer may be defined as device which compute by arithmetic processes. The basic processes employed are addition and subtraction. These processes are also used in successive approximation or interaction to achieve function values, integration, solution of algebraic equations and linear and non-linear differential equations. Fundamental principles of the digital computer were set forth by the English Mathematician Charles Babbage in 1940. After the period 1944 several computers are built. High speed electronic computer such as IBM 7090, [International Business Machines Corporation] has the following execution speeds (including time required to take a number from or to put a number into core storage).

Addition	4.36μ sec.
Multiplication	25.3μ sec.
Division	31.0μ sec.

Digital computer is versatile computing device being increasingly used by power system engineers.

24.4. ORGANIZATION OF A DIGITAL COMPUTERS*

Fig. 24.1 illustrates the components of a digital computer, which are commonly known as input, control, memory, arithmetic and output. The operator supplies instructions (programme) to the input unit of the computer in the form of punched cards or type written instructions. The instructions are stored in 'memory'. The stored programme includes both 'instruction' words and 'data' words. The 'instruction' states the operation, to be performed such as multiplication, division, addition, printing or so. Each work of the instruction consists of two parts. Type of operation mentioned above and secondly 'address' *i.e.* the storage location in the memory for the data to be used. The instructions are in the binary form when they reach the control. The control separates the operation code and the addresses according to their position in the instruction word. The control unit issues orders (electrical pulses) to withdraw the data numbers from the memory and place them in appropriate perform registers. The control then activates the necessary circuits to operation the specified arithmetic operations. When the operation is completed, the next instruction word is taken up by the control from the memory and the specified operation is performed again. The operations are performed at a high speed until the instructions are carried out. The answer are printed or typed.

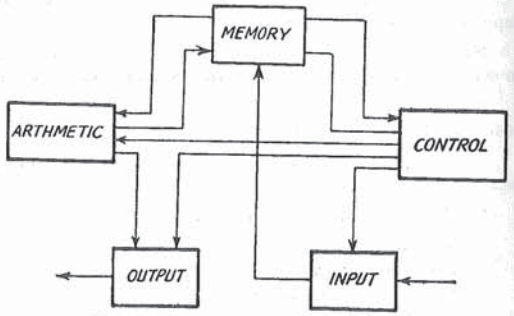

Fig. 24.1. Components of Digital Computer.

24.5. PROCESS OF SOLVING ENGINEERING PROBLEMS ON DIGITAL COMPUTERS

The process involves several steps, which include the following :

1. **Problems definition.** The problem to be solved is defined, its objectives are determined. Data required for input are acquired.

2. **Mathematical formulation.** The problem is developed into mathematical equations.

3. **Selection of solution technique.** The formulation of most of the engineering problems involves mathematical expressions, such as non-linear differential equations, trigonometric functions which cannot be directly evaluated by the computer since the computer can perform only four basic arithmetic operation namely addition, subtraction, multiplication and division. Numerical techniques are employed for solution of the problem.

* Ref. Ch. 46 for Microprocessors and Ref. Sec. 46.2 for Terms and Definitions.

4. **Programme Design.** The important aspects of programme design are :
(*a*) Sequence of logical steps by which particular problem is solved.
(*b*) Allocation of memory.
(*c*) Access of data.
(*d*) Assignment of inputs.
The objectives are primarily to develop a procedure which eliminates unnecessary repetitive calculations and remains within the capability of computer. The programme design is usually prepared in the form of a diagram called *Flow Chart.*

5. **Programming.** A digital computer is supplied a series of instructions consisting of operation codes and addresses which it is able to interpret and execute. In addition to the arithmetic input output instructions, logical instruction are available which are used in direct sequence of calculations. The programme can be developed by using computer instructions in actual and symbolic form or can by written in generalized programme language.

6. **Programme Verification.** There are chances of errors while developing a complete programme. Therefore, a systematic and series must be performed to ensure correctness of problem formulation, method of solution and operation of programme.

24.6. (I) SHORT CIRCUIT STUDIES ON DIGITAL COMPUTER

A typical short circuit programme which is designed to calculate fault currents needs positive sequence and zero sequence impedance matrices. The input data describing the system is specified using the names of the power stations, names of sub-stations, data of system components, voltage levels, reactances etc. The first programme assigns sequential bus number and then rearranges the network data to facilitate formation of positive sequence and zero sequence impedance matrices. During this phase, extensive data checks are performed. Next, the positive sequence bus impedance matrix is formed. This matrix is temporarily stored on an auxiliary storage device to provide space in memory for the next programme segment. Then zero sequence impedance matrix is formed and positive sequence matrix is retrieved for use in fault calculations. Since these matrices are symmetrical, only the diagonal elements and the upper of diagonal element need to be formed and stored. The sequences steps are shown in Fig. 24.2. The short-circuit MVA's are calculated for each bus and tabulated with corresponding station name. The following results are obtained :

1. Total 3-phase and line to ground fault current.
2. Contribution for the above from each line to connected to the fault bus.
3. Currents when the lines connected to fault bus are opened one by one.
4. Zero sequence driving point reactances for faulted bus.

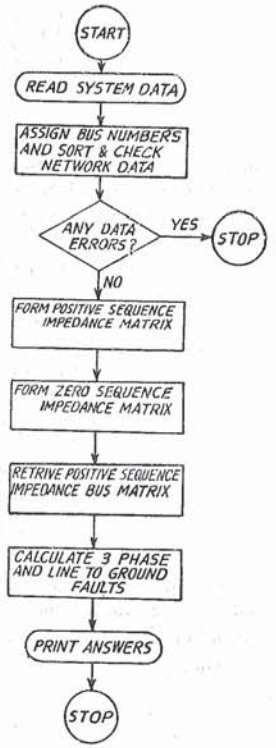

Fig. 24.2. Simplified flow chart for a short-circuit programme.

(II) Nodal Interactive Method

In this method, interaction of entire network are required for each fault condition. The basis of the node interactive method of briefly explained below :

The node equations are formulated by applying Kirchoff's current law. The node equations put in a systematic form provide an excellent method for computer solution. Consider a circuit Fig. 24.3. With certain simplification, this circuit is represented by Fig. 24.4. Series reactances have been combined. Capacitors are added at each high voltage bus of original system. The e.m.f. source with

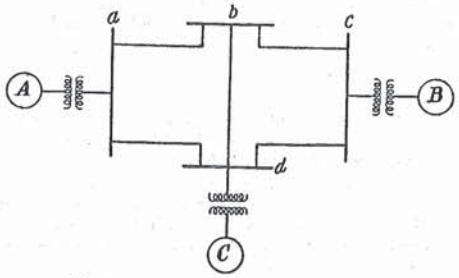

Fig. 24.3. System for one line diagram.

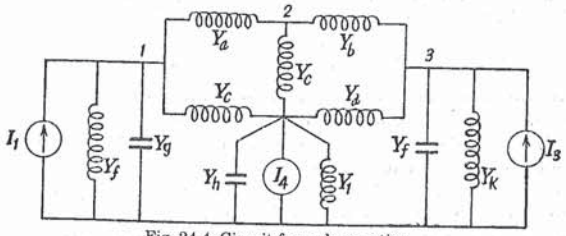

Fig. 24.4. Circuit for node equation.

their series impedance are replaced by their equivalent current sources and shunt impedances. Nodes are designated by numbers 1, 2, 3, 4. Applying Kirchhoff's current laws to the current at node 1, current entering into the node from the source is equal to current going away from the nodes, *i.e.*

$$V_1 (Y_f + Y_g) + (V_1 - V_2)\, Y_a + (V_1 - V_4)\, Y_c = I_1$$

For node 2,

$$0 = (V_2 - V_1)\, Y_a + (V_2 - V_3)\, Y_b + (V_2 - V_4)\, Y_c$$

rearranging,

$$V_1 (Y_f + Y_g + Y_a + Y_c) - V_2 Y_a - V_4 Y_c = I_1$$
$$- V_1 Y_a + V_2 (Y_a + Y_b - Y_c) - V_3 Y_b - V_4 Y_c = 0$$

Similar equations are obtained for nodes 3 and 4. The equations are put in the following standard form :

$$I_1 = Y_{11} V_1 + Y_{12} V_2 + Y_{13} V_3 + Y_{14} V_4$$
$$I_2 = Y_{21} V_1 + Y_{22} V_2 + Y_{23} V_3 + Y_{24} V_4$$
$$I_3 = Y_{31} V_1 + Y_{32} V_2 + Y_{33} V_3 + Y_{34} V_4$$
$$I_4 = Y_{41} V_1 + Y_{42} V_2 + Y_{43} V_3 + Y_{44} V_4$$

where Y_{11}, Y_{22}, Y_{33}, Y_{44} are called Self Admittances at the respective nodes which are sum of admittances terminating on the node. The other admittances such as Y_{12}, etc. are obtained by adding the admittances connected directly between the nodes 1, 2 and are given a negative sign.

Thus $Y_{12} = - Y_r$, $Y_{23} = - Y_r$, likewise. The equations given above are put in the form

$$I_k = \sum_{m=1}^{m=M} Y_{k_m} V_m$$

where M is the number of independent nodes (number of busses).

For solution on computer, one equation is written for each of buses at which the voltage is unknown. Load current is neglected and all internal voltages are assumed to be equal. If the voltage of faulty bus is zero, voltages are computed by load studies or assumed equal to V_f, the equations can be written as

$$Y_{kk} V_k + \sum_{m=1}^{m=M} Y_{km} V_m = 0$$

With $I_k = 0$, and $m \neq k$

A set of simultaneous equations is formed as equations are written for all the nodes where voltage is unknown. The equations are then solved by interactive process. Initial values are assumed for all unknown voltages. A correction value is found for the voltage at the first node based on unknown and assumed voltages at other nodes. This corrected value is used for subsequent buses. The computer repeats the computation until the correction at each bus is less than the required precision mark.

Another approach is by forming impedance-matrix. The matrix operations are formed on the impedances of branches that form loops of the network. After this a short-circuit matrix is obtained. The output information is obtained by means of arithmetic operations.

QUESTIONS

1. Describe a typical A.C. Network analyzer. How is it used for fault calculations ?
2. Describe the producer of fault calculations on an A.C. Network analyzer.
3. Describe the set-up of digital computer*.
4. Explain the procedure of fault calculation on digital computer.

* Ref. Sec. 46.2 for Terms and Definitions related with Digital Computers and Microprocessors.
Ref. Sec. 47.13 for 'HVDC Simulator' used for analysing HVDC Transmission System and associated AC Systems.