CS501-Advance Computer Architecture
MID TERM MCQS
Prepared by: JUNAID MALIK

AL-JUNAID TECH INSTITUTE

1) The multiplexer----------is used to decide which value is transferred to be written back to the register file.
   - MP2
   - MP3
   - MP4
   - MP5

2) Which of the following condition is evaluated when executing the branch instruction “brzr R2, R1”?
   - If(R2==0)
   - If(R1 >0)
   - If(R1==0)
   - If(R1 < 0)

3) In case of SRC processor, bits---------of IR (instruction register) are reserved for the opcode.
   - 0 to 4
   - 11 to 15
   - 27 to 31
   - 59 to 63

4) Which of the given RTL description is used to represent “load instruction register” (ldr) instruction?
   - (op<4..0>=6): R[ra] ⟵ rel
   - (op<4..0>=2): R[ra] ⟵ M [rel]
   - (op<4..0>=2): M[disp] ⟵ R [ra]
   - (op<4..0>=2): M[rel] ⟵ R [ra]

5) -------- Instruction is used to divide a register value by immediate value in FALCON-E processor.
   - div
   - idiv
   - divi
   - divim

6) Which field of machine language instruction is the “type of operation” that is to be performed.
   - Op-code(or the operation code)
   - CPU register
   - Memory Cells
   - I/O Location

7) Which of the following control signal is NOT activated during instruction fetch operation?
   - PCout
   - LC
   - LMAR
   - Cout

8) In case of FALCON-A---------- instruction are present which are not present in SRC processor.
   - create and destroy
   - in and out
   - open and close
   - read and write

9) ---------- provides a temporary storage for the address of memory location to be accessed.
   - MAR

- MBR
- PC
- LPC

10) Which of the following register is used to enable the tri-stable buffers with the MBR?

- MBRout
- MARout
- LMBR
- INC4

11) What functionality is performed by the instruction “str R8, 34” of SRC?

- It will load the register R8 with the contents of the memory location M[PC+34]
- It will load the register R8 with the contents of the memory location M[34]
- It will store the register R8 contents to the memory location M[PC+34]
- It will store the register R8 contents to the memory location M[34]

12) Program Counter(PC) holds the memory address of:

- Previous Instruction
- Current Instruction
- Next Instruction
- Previous and Current Instruction

13) What is the working of Processor Status Word (PSW)?

- To hold the current status of the processor
- To hold the current address of the process
- To hold the instruction that the computer is currently processing
- To hold the address of the next instruction in memory that is to be executed

14) mul is the example of a(n)---------- operation.

- Logic
- Shift
- Arithmetic
- Data transfer

15) Control Signal for RTL “IR< ---MBR” will be---------

- MBRout,LIR
- PC< --C
- PC< --MBR
- PC< --IR

16) What does the instruction”ldr R3, 58” of SRC do?

- It will load the register R3 with the contents of the memory location M[PC+58]
- It will load the register R3 with the relative address itself(PC+58)
- It will store register R3 contents to the memory location M[PC+58]
- It will store the value of register R3 at the relative address itself(PC+58)

17) The status register of the 68000 has -------- condition codes.

- 2
- 3
- 5
- 8

18) Which of the instruction is used to load register from memory using relative address?

- ld instruction
- ldr instruction

- lar instruction
- str instruction

19) For the ------ type instruction, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory.

- Jump
- Control
- L
- load/store
- Branch

20) In a processor, ---------- is responsible for the synchronization of internal as well external events.

- Memory Unit
- Data Unit
- Arithmetic & Logic Unit
- Control Unit

21) In CPU design, ---------- creates or forms the interface between the data path and control unit.

- Buses
- ALU
- Control signal
- cache

22) ---------- Control signal enables the input to the PC for receiving a value that is currently on the internal processor bus.

- LPC
- INC4
- LC
- Cout

23) In SRC, the effective address is computed a run-time by adding a constant to value of---------- register.

- FLAGS
- IR
- PC
- Ra

24) --------- control signal allow the content of the program counter register to be written onto the internal processo bus.

- INC4
- LPC
- PCout
- LC

25) In ---------- instruction format of EAGLE processor, there is no field reserved for the operands.

- Type V
- Type Y
- Type X
- Type Z

26) In Type C instruction of SRC, ---------- bits are allocated for constant values.

- 16
- 17
- 21
- 22

27) A general purpose digital computer has --------- main components.

- 2
- 3
- 4
- 5

28) The instruction ---------- will load the register R3 with the contents of the memory location M[PC+56].
- lar R3,M[56]
- ldr R3,M[56]
- ldr R3,56
- lr R3,[56]

29) In FALCON-A instruction format of Type-2 constants and variable should be in the range of.
- -132 to +131
- -164 to + 163
- -32 to + 31
- -128 to + 127

30) In a FALCON-A assembly program, labels are used to implement---------- jump.
- Direct
- Indirect
- Relative
- Displacement

31) In "Jump [8]" instruction, the size of the constant fields is -------- bits.
- 4
- 5
- 8
- 16

32) The multiplexer---------- is used to decide which value is transferred to be written back to the register file.
- MP2
- MP3
- MP3
- MP5

33) ---------- is a register which takes input from the ALSU as memory address to be accessed and transfer the memory contents on that location onto the memory sub-system.
- PC
- MBR
- MAR
- IR

34) In pipe-lined processor, there should be a--------- port register file so that if the register write and register read stages overlap they can be performed in parallel.
- Four
- Three
- Two
- One

35) Which of the following registers is used as an implicit operand in MUL/DIV instruction of FALCON-A?
- R0
- PC
- IR
- SP

36) Which one of the following control signals causes the data from the bus to be read into the register MAR.
- MARout
- MARin
- LMAR
- None of the given

37) To set the value of micro-PC from branch address, the value of 4 to 1 multiplexer is----------
- 00
- 01
- 10
- 11

38) The instruction “PUSH A” is an example of ----------
- 0-address instruction
- 1-address instruction
- 2-address instruction
- 3-address instruction

39) Which of the following branch instruction has a condition which is always executed?
- JZ
- JUMP
- JPL
- JMI

41) ---------- hazard occurs when attempting to access same resource in different ways at the same time.
- Branch
- Data
- Structural
- Instruction

42) ---------- is an example of Miscellaneous instruction.
- Shift
- Store
- Halt
- Call

43) Which type of instructions enables mathematical computations?
- Arithmetic
- Control
- Data transfer
- Numeric

44) VLIW Stands for----------
- Variable Length Instruction Word
- Very Long Instruction Word
- Very Long Instruction Width
- Variable Length Instruction Width

45) Which of the following is NOT related to the architecture of the computer?
- Instruction set
- Control signal
- I/O mechanism
- Memory addressing modules

46) In SRC, the general-purpose register file includes---------- registers, each 32 bit wide.
- 6 Registers R0 to R15
- 24 Registers R0 to R23

- 32 Registers R0 to R31
- 64 Registers R0 to R63

47) Which of the following RTL description is used for specifying the operation of an SRC instruction?

- IR<31..27>
- IR<22..26>
- IR<21..17>
- IR<21..0>

48) What is the size of the memory space that is available to FALCON-A processor?

- 2^8 bytes
- 2^16 bytes
- 2^32 bytes
- 2^64 bytes

49) How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL.

- IR<16..0>
- IR<15..0>
- IR<16..1>
- IR<15..1>

50) What is the working of Processor Status Word (PSW

- To hold the current status of the processor.
- To hold the address of the current process
- To hold the instruction that the computer is currently processing
- To hold the address of the next instruction in memory that is to be executed 51)

What does the instruction “ldr R3, 58” of SRC do?

- It will load the register R3 with the contents of the memory location M [PC+58]
- It will load the register R3 with the relative address itself (PC+58).
- It will store the register R3 contents to the memory location M [PC+58]
- No operation

52) What is the instruction length of the FALCON-E processor?

- 8 bits
- 16 bits
- 32 bits
- 64 bits

53) Which one of the following portions of an instruction represents the operation to be performed?

- Address
- Instruction code
- Opcode
- Operand

54) Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

- Processor-Memory-Switch level (PMS level)
- Instruction Set Level
- Register Transfer Level
- None of the given

55) Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register **B)** from the following example. ADD R1, R2, R3

- Opcode= R1, DR=ADD, SA=R2, SB=R3
- Opcode= ADD, DR=R1, SA=R2, SB=R3
- Opcode= R2, DR=ADD, SA=R1, SB=R3

- Opcode= ADD, DR=R3, SA=R2, SB=R1

56) Which one of the following circuit design levels is called the gate level?

- Logic Design Level
- Circuit Level
- Mask Level
- None of the given

57) The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?

- Jump and branch format instructions
- Immediate format instructions
- Register format instructions
- All of the above

58) P: R3 <- R5 MAR <- IR These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?

- Parentheses ()
- Arrow <-
- Colon :
- Comma ,

59) In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?

- Arithmetic/logic
- Load/store
- Test/branch
- None of the given

60) Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

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- Opcode= ADD, DR=R1, SA=R2, SB=R3
- Opcode= R2, DR=ADD, SA=R1, SB=R3
- Opcode= ADD, DR=R3, SA=R2, SB=R1

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- Immediate format instructions
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65) In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?

- Arithmetic/logic
- Load/store
- Test/branch
- None of the given

66) What does the word 'D' in the 'D-flip-Flop' stands for?

- Data
- Digital
- Dynamic
- Double

67) The instruction ----------will load the register R3 with the contents of the memory location M [PC+56]

- Add R3, 56
- lar R3, 56
- ldr R3, 56
- str R3, 56

68) What is the instruction length of the FALCON-E processor?

- 8 bits
- 16 bits
- 32 bits

69) Which one of the following are the code size and the Number of memory bytes respectively for a 2-address instruction?

- 4 bytes, 7 bytes
- 7 bytes, 16 bytes
- 10 bytes, 19 bytes
- 13 bytes, 22 bytes

70) Which one of the following portions of an instruction represents the operation to be performed?

- Address
- Instruction code
- Opcode
- Operand

71) Which operator is used to 'name' registers, or part of registers, in the Register Transfer Language?

- :=
- &
- %
- ©

72) What is the size of the memory space that is available to FALCON-A processor?

- 2^8 bytes
- 2^16 bytes
- 2^32 bytes
- 2^64 bytes

73) An "assembler" that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a ----------

- compiler
- cross assembler
- debugger
- linker

74) Which instruction is used to store register to memory using relative address.

- ld instruction
- ldr instruction
- lar instruction
- str instruction

75) Which of the following can be defined as an address of the operand in a computer type instruction or the target address in a branch type instruction?

- Base address
- Binary address
- Effective address
- All of the given

76) How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?

- IR<16..0>
- IR<15..0>
- IR<16..1>
- IR<15..1>

77) What functionality is performed by the instruction "str R8, 34" of SRC?

- It will load the register R8 with the contents of the memory location M [PC+34]
- It will load the register R8 with the relative address itself (PC+34).
- It will store the register R8 contents to the memory location M [PC+34]
- No operation

78) Which type of instructions help in changing the flow of the program as and when required?

- Arithmetic
- Control
- Data transfer
- Floating point

79) Which of the following statements is/are true about RISC processors' claimed advantages over CISC processors? (a) Keeping regularly accessed variables in registers as opposed to keeping them in memory facilitates faster execution. (b) RISC CPUs outperform CISC CPU's in procedural programming environments. (c) Instruction pipelining has helped RISC CPU's to attain a target of 1 cycle per instruction. (d) It is easier to maintain the "family concept" in RISC CPU.

- (a), (b) &(c)
- (b), (c) & (e)
- (c), (d) & (e)
- (a), (c) & (d)

80) Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

- Processor-Memory-Switch level (PMS level)
- Instruction Set Level

- Register Transfer Level
- None of the given

81) Which one of the following is/are the features of Register Transfer Language? a) It is a symbolic language b) It is describing the internal organization of digital computers c) It is an elementary operation performed (during one clock pulse), on the information stored in one or more registers d) It is high level language.

- (b) only
- & (b) only
- ,(b) & (d)
- (b),(c) & (d)

81) Motorola MC68000 is an example of ---------microprocessor.

- CISC
- RISC
- SRC
- FALCON

82) Which one of the following registers holds the instruction that is being executed?

- Accumulator
- Address Mask
- Instruction Register
- Program Counter

83) For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.

- Registers
- Control signals
- Memory
- None of the given

84) The external interface of FALCON-A consists of a _____ data bus.

- 8-bit
- 16-bit
- 24-bit
- 32-bit

85) In which one of the following techniques, the time a processor spends waiting for instructions to be fetched from memory is minimize

- Perfecting
- Pipelining
- Superscalar operation
- Speedup

86) _____ enable the input to the PC for receiving a value that is currently on the internal processor bus.

- LPC
- INC4
- LC
- Cout

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87) The processor must have a way of saving information about its state or context so that it can be restored upon return from the ----------

- Exception
- Function
- Thread
- Stack

88) ----------is the ability of application software to operate on models of equipment newer than the model for which it was originally developed.

- Backward compatibility
- Data migration
- Reverse engineering
- Upward compatibility

89) _____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.

- INC4
- LPC
- PCout
- LC

90) Which one of the following registers stores a previously calculated value or a value loaded from the main memory?

- Accumulator
- Address Mask
- Instruction Register
- Program Counter

91) Computer system performance is usually measured by the ----------

- Time to execute a program or program mix
- The speed with which it executes programs
- Processor's utilization in solving the problems
- Instructions that can be carried out simultaneously

92) The external interface of FALCON-A consists of a _____ address bus.

- 8-bit
- 16-bit
- 24-bit
- 32-bit

93) Which one of the following register(s) that is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?

- Instruction Register
- Memory address register
- Memory Buffer Register
- Registers A and C

94) The external interface of FALCON-A consists of a _____address bus and a _____ data bus.

- 8-bit , 8-bit
- 16-bit , 16-bit

- 16-bit , 24-bit
- 16-bit , 32-bit

95) ----------is the ability of application software to operate on models of equipment newer than the model for which it was originally developed.

- Backward compatibility
- Data migration
- Reverse engineering
- Upward compatibility

96) Which one of the following registers stores a previously calculated value or a value loaded from the main memory?

- Accumulator
- Address Mask
- Instruction Register
- Program Counter

97) Which one of the following register(s) contain(s) the address of the place the CPU wants to work with in the main memory and is/are directly connected to the RAM chips on the motherboard?

- Instruction Register
- Memory address register
- Memory Buffer Register
- Registers A and C

98) FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.

- 8-bits
- 16-bits
- 32-bits
- 64-bits

99) _____ enable the input to the PC for receiving a value that is currently on the internal processor bus.

- LPC
- INC4
- LC
- Cout

100) The external interface of FALCON-A consists of a _____ data bus.

- 8-bit
- 16-bit
- 24-bit
- 32-bit

101) For any of the instructions that are a part of the instruction set of the SRC, there are certain _____required; which may be used to select the appropriate function for the ALU to be performed, to select appropriate registers, or the appropriate memory location

- Registers
- Control signals
- Memory
- None of the given

102) Among the two approaches available to design a control unit, hardware approach is relatively---------- as compared to micro-programming.

- Slow

- Fast
- Average
- Better

103) The MAR is connected directly to the----------

- MBR
- CPU Internal bus
- CPU external bus
- LIC

104) Which of the following is not a part of processor state?

- IR
- PC
- Stacks
- Registers

105) ---------- form the branch control field in the micro instruction.

- C Bits
- M Bits
- B BITS
- M Bits

106) During the RESET operation of processor, control step counter is set to----------

- 1
- 0
- 2
- -1

107) An “assembler” that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a----------

- Compiler
- Cross assembler
- Debugger
- linker

108) In FALCON-A processor, the size of each I/O port is----------

- 16 bits
- 8 bits
- 8 bytes
- 256 bytes

109) ---------- is defined as the number of instructions processed per second.

- Memory access
- Throughput
- ALU operation
- Latency

110) In FALCON-A ISA, which of the following opcodes is used to perform “No Operation”?

- 20
- 21
- 22
- 23

111) ---------- is an example of Miscellaneous instruction:

- Shift
- Store

- Halt
- Cell

112) To apply two shifts to an input number using the barrel shifter, the control signals S1 and S0 of the shifter should be ----------.

- S1 = 1 and S0 = 1
- S1 = 0 and S0 = 1
- S1 = 1 and S0 = 0
- S1 = 2 and S0 = 0

113) Which one of the followings is the correct RTL description for sign extensions of an 8-bit constant:

- (8aIR<7>©IR<7..0>)
- (8aIR<5>©IR<8..0>
- (8aIR<7>©IR<6..0>
- (8aIR<8>©IR<7..0>

114) In MC68000, ---------- register is used as stack pointer:

- A0
- A7
- D0
- D7

115) In which of the following instructions, the data moves between a register in the processor and a memory location:

- Arithmetic
- Load/ Store
- Branch
- Logic

116) The size of data bus of mc68000 processor is:

- 8 bits
- 16 bits
- 20 bits
- 32 bits

117) Which one of the following operations is NOT performed by using miscellaneous instructions?

- Clearing all registers
- Stopping the processor
- NOP
- Returning from a procedure

118) In case of FALCON-A ---------- instructions are present which are not present in the SRC processor:

- Create and destroy
- In and out
- Open and close
- Read and write

119) In Type C instruction of SRC , ---------- bits are allocated for content value:

- 16
- 17
- 21
- 22

120) RISC stands for?

- Registers internal system cache
- Reduced instruction set computer
- Registers instruction set computer

- Reduced internal system computers

121) Which of the followings is not an example of super-scalar processors?

- PowerPC601
- IAPX88
- Intel P6
- DEC Alpha 21164

122) In EAGLE processor, which of the following notations is used to represent a memory word stored at address 8?

- M [8] <0..15>:= M[8]©M[9]
- M[8]<15..0>:=M[9] ©M[8]
- M[8]<15..0:=M[8] ©M[9]
- M[8]<0..15>:=M[9] ©M[8]

123) ---------- form the branch address field in the micro instruction:

- C bits
- M bits
- B bits
- A bits

124) What does the instruction “idr R3, 58” of SRC do?

- It will load register R3 with the contents of the memory location M[PC+58]
- It will load register R3 with the relative address itself (PC+58)
- It will store register R3 contents to the memory location M[PC+58]
- It will store the value of register R3 at the relative address itself (PC+58)

125) The SPARC architecture defines a ---------- that allows for multiple address spaces.

- Memory Location Unit(MLU)
- Memory Mapping Unit(MMU)
- Memory Shifting Unit (MSU)
- Memory Arithmetic Unit (MAU)

126) For a processor having 32 general purpose register, ---------- bits are required for each register field in the instruction:

- 32
- 3
- 8
- 5

127) Which of the following registers is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?

- Instruction register
- Memory address register
- Memory Buffer Register
- Registers A and C

128) In SRC which of the following is a notation which is used to repeat 32- bit memory word stored at address starting from 56?

- M[56]<31..0>:=M[56]M[57]M[58]M[59]
- M[56]<0..31>:=M[56]M[57]M[58]M[59]
- M[56]<0..31>:=M[59]M[58]M[57]M[56]
- M[56]<0..31>:=M[59]M[58]M[57]M[56]
-

129) Which of the following branch instruction has a condition which is always executed?

- JZ

- JUMP
- JPL
- JMI

130) Which of the following EAGLE instruction is used to initialize all the registers by setting them to 0?

- NOP
- HALT
- INIT
- RESET

131) Which notation do we use to name different fields of a register in RTL?

- 0
- <=
- +
- :=

132) Which of the following instruction is considered most important in pipelined EAGLE architecture?

- HALT
- NOP
- INIT
- RESET

132) SPARC uses a simple set of---------- instruction format.

- 64-bit
- 12-bit
- 16-bit
- 32-bit

- The ALSU function “INC2” increments the ---------- by 2 and the output is stored in the buffer register.PC,A
- IR,A
- PC,C
- IR,C

134) Which temporary register is loaded with either a register value from the register file or a constant from the instruction?

- Y3
- X3
- Z4
- Z5

135) “Finite-state machine” concepts are usually used to represent the control unit where every state corresponds to---------- clock cycles(s).

- 1
- 2
- 4
- 16

136) Total number of data registers in Motorola 68000 processor are----------

- 8
- 12
- 24
- 32

137) ---------- instruction is used to load a register with an immediate value.

- la
- lar
- ld
- ldr

138) A computer belongs to which of the following subset of the systems?

- Mechanical system
- Electrical system
- Optical system
- Magnetic system

139) In FALCON-A processor , the size of each I/O port is----------

- 16 bit
- 8 bit
- 8 bytes
- 256 bytes

140) Type A of SRC has which of the following instruction?

a) andi, instruction
b) No operation or nop instruction
c) lar instruction
d) ldr instruction
e) Stop operation or stop instruction

- (a)&(b)
- (b)&(c)
- (a)&(e)
- (b)&(e)

141) In which of the following technique, the time a processor spends waiting for instruction to be fetche from memory is minimized?

- Perfecting
- Pipelining
- Super-scalar operation
- Speed up

142) ---------- is the ability of application software to operate on models of equipment near than the model for which it originally developed.

- Backward compatibility
- Data migration
- Reverse engineering
- Upward compatibility

143) Which of the following register stores a previously calculated value or a value loaded from the main memory?

- Accumulator
- Address Mask
- Program counter

144) Computer system performance is usually measured by the ----------

- Time to execute a program or program mix
- The speed in which it executes programs
- Processor's utilization in solving the problems
- Instructions that can be carried out simultaneously

145) Which of the following code size and the number of memory bytes respectively for a 2-address instruction.
- 4 bytes, 7 bytes
- 7 bytes ,16 bytes
- 10 bytes , 19 bytes
- 13 bytes, 19 bytes

146) Which of the the given below measures is/are used for comparison of performance of various machine?
- Execution time
- MFLOPS
- MIPS
- All of the given

147) There are ---------- type of RESET operation in SRC.
- Three
- Four
- Two
- five

148) Type checking allows the ---------- to determine memory for variables.
- Compiler
- Debugger
- Linker
- loader

149) In FALCON-A processor, memory word size is----------
- 1 byte
- 4 bytes
- 8 bytes
- 2 bytes

150) What functionality is performed by the by the instruction “lar R3, 36” performed.
- It will load the register R3 with the contents of memory location M[PC+36]
- It will load the register R3 with the relative address itself (PC+36)
- It will store the register R3 contents of memory location M[PC+36]
- It will left rotate the value of R3 36 times and will store the value in R3

151) To connect together five (5) m-bit registers in a point-to-point scheme, _____ connections are required.
- 25
- 30
- 20
- 24

1. For the _____ type instructions, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory.
   - JUMP
   - LOAD/Store
   - Control
   - None of the Given
2. Almost every commercial computer has its own particular _____ language.
   a. 3 GL
   b. English Language
   c. High Level Language
   d. Asseembly Language
3. In a register-based machine having 64 registers, a _____ field is required in instruction to identify a register.
   a. 4-bit
   b. 6-bit
   c. 8-bit
   d. 16-bit