



CS501-Advanced Computer Architecture

(Solved Subjective)
LECTURE FROM
(23 to 45)



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1. Briefly Describe Classification of Networks?

Answer

Classification of Networks

We can classify a network based on the following two parameters:

- The number and type of machines to be interconnected
- The distance between these machines

Based on these two parameters, we have the following type of networks:

SAN (System/Storage Area Network)

It refers to a cluster of machines where large disk arrays are present. Typical distances could be tens of meters.

LAN (Local Area Network)

It refers to the interconnection of machines in a building or a campus. Distances could be in Kilometers.

WAN (Wide Area Network)

It refers to the interconnection between LANs.

2. Write note on Pipelining?

Answer

Pipelining is a technique of overlapping multiple instructions in time. A pipelined processor issues a new instruction before the previous instruction completes. This results in a larger number of operations performed per unit of time. This approach also results in a more efficient usage of all the functional units present in the processor, hence leading to a higher overall throughput. As an example, many shorter integer instructions may be executed along with a longer floating point multiply instruction, thus employing the floating point unit simultaneously with the integer unit.

3. What is virtual memory?

Answer

Virtual memory acts as a cache between main memory and secondary memory. Data is fetched in advance from the secondary memory (hard disk) into the main memory so that data is already available in the main memory when needed. The benefit is that the large access delays in reading data from hard disk are avoided.

4. How does work Associative Mapping?

Answer

In this technique, block of data from main memory can be placed at any location in the cache memory. A given block in cache is identified uniquely by its main memory block number, referred to as a tag, which is stored inside a separate tag memory in the cache. To check the validity of the cache blocks, a valid bit is stored for each cache entry, to verify whether the information in the corresponding block is valid or not. Main memory address references have two fields. • The word field becomes a “cache address” which specifies where to find the word in the cache.

- The tag field which must be compared against every tag in the tag memory.

5. How overflow is represented in case of floating point?

Answer

e^{255} , denotes numbers with no numeric value including $+\infty$ and $-\infty$ and called Not-a-Number or NaN. In computers, a floating-point number ranges from $1.2 \times 10^{-38} \leq x \leq 3.4 \times 10^{38}$ can be represented. If a number does not lie in this range, then overflow can occur.

Overflow occurs when the exponent is too large and can not be represented in the exponent field.

6. What is DMA?

Answer

The disadvantage however, would be that an additional DMA controller would be required, that could make the system a bit more complex and expensive. Generally, the DMA requests have priority over all other bus activities including interrupts. No interrupts may be recognized during a DMA cycle.

7. Differentiate between throughput and latency?

Answer

Latency is defined as the time required to process a single instruction, while throughput is defined as the number of instructions processed per second. Pipelining cannot lower the latency of a single instruction; however, it does increase the throughput. With respect to the example discussed earlier, in a non-pipelined machine there would be one instruction processed after an average of 5 cycles, while in a pipelined machine, instructions are completed after each and every cycle (in the steady-state, of course!!!). Hence, the overall time required to execute the program is reduced.

8. Describe six attributes of SRC Processor?

Answer

- The SRC contains 32 General Purpose Registers: R0, R1, ..., R31; each register is of size 32-bits.
- Two special purpose registers are included: Program Counter (PC) and Instruction Register (IR)
- Memory word size is 32 bits
- Memory space size is 232 bytes
- Memory organization is 232 x 8 bits, this means that the memory is byte aligned
- Memory is accessed in 32 bit words (i.e., 4 byte chunks)
- Big-endian byte storage is used

9. Disadvantages of Software Poll and Daisy Chain

The software poll has a disadvantage is that it consumes a lot of time, while the daisy chain is more efficient. The daisy chain has the disadvantage that the device nearest to the CPU would have highest priority. So, usually those devices which require higher priority would be connected nearer to the CPU. Now in order to get a fair chance for other devices, other mechanisms could be initiated or we could say that we could start instead of device 0 from that device where the CPU finishes the last interrupt and could have a cyclic provision to different devices.

10. cache and it's management

Answer

To manage the working of the cache, cache control unit is implemented in hardware, which performs all the logic operations on the cache. As data is exchanged in blocks between main memory and cache, four important cache functions need to be defined. Block Placement Strategy Block Identification Block Replacement Write Strategy

11. Steps used for floating point addition and subtraction.

Answer

The following are the steps for floating-point addition and subtraction.

- Unpack sign , exponent and fraction fields
- Shift the significand
- Perform addition
- Normalize the sum
- Round off the result
- Check for overflow

12. Diff b/w distributed computing and computer Network and classifications of networks

Answer

Difference between Distributed Computing and Computer Networks

In distributed computing, all elements which are interconnected operate under one operating system. To a user, it appears as a virtual uni-processor system. In a computer network, the user has to specify and log in on a specific machine. Each machine on the network has a specific address. Different machines communicate by using the network which exists among them.

Classification of Networks

We can classify a network based on the following two parameters:

- The number and type of machines to be interconnected
- The distance between these machines

13. .software polling and drawbacks of software polling and daisy chain

Answer

Software Poll

CPU polls to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt. This identification is done using special commands or reading the device status register. Special command may be a test I/O. In this case, CPU raises test I/O and places the address of a particular I/O module on the address line. If I/O module sets the interrupt then it responds positively. In the case of an addressable status register, the CPU reads the status register of each I/O module to identify the interrupting module. Once the correct module is identified, the CPU branches to a device service routine which is specific to that particular device.

14. Similarities and diff. between RAID level 4 and 5

RAID Level 4

- Make use of independent access technique.
- Data striping is used.
- A bit-by-bit parity strip is calculated across corresponding strip on each data disk.
- Involves a write penalty when an I/O write request of small size is performed.
- To calculate the new parity, the array management software must read the old user parity strip.

RAID Level 5

- Organized in a similar fashion to RAID 4
- The only difference is that RAID 5 distributes the parity strips across all disks.

15. Which technique allows certain hardware subsystems within a computer to access system memory for read/write independently of the main CPU?

Answer

Direct Memory Access. Allows certain hardware subsystems within a computer to access system memory for reading and/or writing independently of the main CPU. Examples of systems that use DMA: Hard Disk Controller, Disk Drive Controller, Graphics Card, Sound Card.

16. define the type of error control

Answer

There are two main issues in error control:

1. Detection of Error
2. Correction of Error

For detection of error, we just need to know that there exists an error. When the error is detected then the next step is to ask the source to resend that information. This process is called automatic request for repeat. In some cases there is also possibility that redundancy is enough and we reconstruct and find out exactly which particular bits are in error. This is called error correction.

17. convert (390)₁₀ into base 16

Answer:- (Page 335)

According to the above algorithm

$$390/16 = 24(\text{rem}=6), x_0=6$$

$$24/16 = 1(\text{rem}=8), x_1=8, x_2=1$$

Thus $390_{10} = 186_{16}$

18. define pipelining

Answer

Pipelining is a technique of overlapping multiple instructions in time. A pipelined processor issues a new instruction before the previous instruction completes. These results in a larger number of operations performed per unit of time. This approach also results in a more efficient usage of all the functional units present in the processor, hence leading to a higher overall throughput. As an example, many shorter integer instructions may be executed along with a longer floating point multiply instruction, thus employing the floating point unit simultaneously with the integer unit.

19. difference between higher level language and assembler (3)

Answer

Higher-level languages may not be appropriate for programming special purpose or embedded processors that are now in common use in various appliances. This is because the functionality required in such applications is highly specialized. In such a case, assembly language programming is required to implement the required functionality.

20. what is program instruction control?

Answer

The program control instructions direct the flow of a program and allow the flow of the program to change. A change in flow often occurs when decisions, made with the CMP or TEST instruction, are followed by a conditional jump instruction.

21. Single detached DMA

When a particular I/O module needs to read or write large amounts contiguous data it requests the processor for direct memory access. If permission is granted by the processor, the I/O module sends the read or writes address and the size of data needed to be read or written to the DMA module. Once the DMA module acknowledges the request, the I/O module is free to read or write its contiguous block of data from or onto main memory. Even though in this situation the processor will not be able to execute while the transfer is going on (as there is a just a single bus to facilitate transfer of data), DMA transfer is much faster than having each word of memory being read by the processor and then being written to its location.

22. what do you know about " booth pair recording 3marks

Answer

The Booth Algorithm makes multiplication simple to implement at hardware level and speed up the procedure.

This procedure is as follows:

1. Start with LSB and for each 0 of the original number, place a 0 in the recorded number until a 1 is indicated.
2. Place a 1 for 1 in the recorded table and skip any succeeding 1's until a 0 is encountered.
3. Place a 0 with 1 and repeat the procedure.

23. assembler symbol table note.3-marks:

Answer:-

Symbol table contains information to locate and relocate symbolic definitions and references. The assembler creates the symbol table section for the object file. It makes an entry in the symbol table for each symbol that is defined or referenced in the input file and is needed during linking.

Symbol Table corresponds to the storage of all program variables, labels and data values in a data structure at the implementation level. The Symbol Table includes data members, data addresses and labels with their respective values.

24. convert the hexadecimal number B316 to base 10 5Marks

Answer

According to the above algorithm,

$$X=0$$

$$X= x+B (=11) =11$$

$$X=16*11+3= 179$$

$$\text{Hence } B316=17910$$

25. Define different level of RAID and What are the similarities at Level 2 and Level 3 of the RAID?

Answer

RAID Level 0

- Not a true member of the RAID family.
- Does not include redundancy to improve performance.
- In few applications, capacity and performance are primary concerns than improved reliability. So RAID level

0 is used in such applications.

- The user and system data are distributed across all the disks in the array

Two requests can be issued in parallel, reducing the I/O queuing time

Similarities between RAID Levels 2 and 3

- Make use of parallel access techniques.
- All member disks participate in execution of every request.
- Spindles of the individual drives are synchronized
- Data striping is used.
- Strips are as small as a single byte or word.

26. Define the different types of Instructions used in FALCON-E

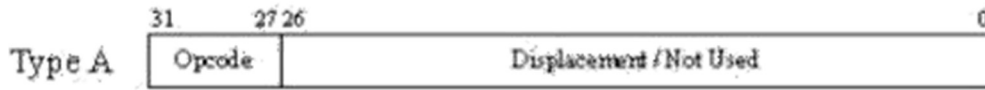
Answer

Four different instruction formats are supported by the FALCON-E. These are

Type A instructions

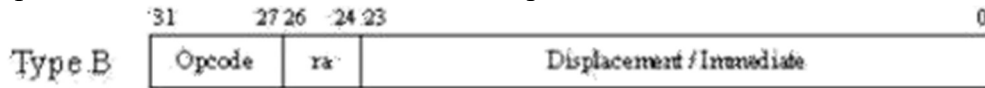
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The type A instructions have 5 bits reserved for the operation code (abbreviated op-code), and the rest of the bits are either not used or specify a displacement.



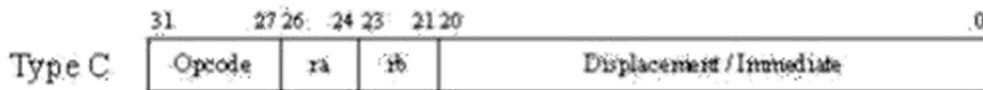
Type B instructions

The type B instructions also have 5 bits (27 through 31) reserved for the op-code. There is a register operand field, ra, and an immediate or displacement field in addition to the op-code field.



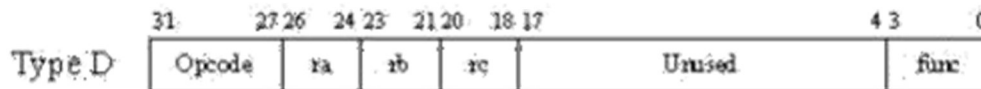
Type C instructions

Type C instructions have the 5-bit op-code field, two 3-bit operand registers (rb is the source register, ra is the destination register), a 17-bit immediate or displacement field, as well as a 3-bit function field. The function field is used to differentiate between instructions that may have the same op-code, but different operations.



Type D instructions

Type D instructions have the 5-bit op-code field, three 3-bit operand registers, 14 bits are unused, and a 3-bit function field.

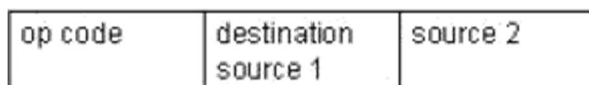


**27. How to
right
RTL**

Answer

RTL stands for Register Transfer Language. The Register Transfer Language provides a formal way for the description of the behavior and structure of a computer. The RTL facilitates the design process of the computer as it provides a precise, mathematical representation of its functionality. In this section, a Register Transfer Language is presented and introduced, for the SRC (Simple „RISC“ Computer), described in the previous discussion.

28. What is format of 2-address instruction set?



29. Write structural RTL of ret ra.

Step	RTL
T0-T2	Instruction Fetch
T3	$C \leftarrow R[ra];$
T4	$PC \leftarrow C;$

30. What are functions of valid bit in Associative mapping strategy for cache?

A given block in cache is identified uniquely by its main memory block number, referred to as a tag, which is stored inside a separate tag memory in the cache. To check the validity of the cache blocks, a valid bit is stored for each cache entry, to verify whether the information in the corresponding block is valid or not.

31 An IO system with single disk gets 100 IO requests/sec. Assume the average time for a disk to service an IO request is 6ms. What is utilization of the IO system?

Answer:- (Page 382)

Time for an I/O request = 6ms

=0.006sec

Server utilization = 100×0.006

= 0.6

32. What are characteristics of D-flip-flop? Draw truth table.

A flip-flop is a bi-stable device, capable of storing one bit of Information. Therefore, flip-flops are used as the building blocks of a computer's memory as well as CPU registers.

There are various types of flip-flops; most common type, the D flip-flop is shown in the figure given. The given truth table for this positive-edge triggered D flip-flop shows that the flip-flop is set (i.e. stores a 1) when the data input is high on the leading (also called the positive) edge of the clock; it is reset (i.e., the flip-flop stores a

0) when the data input is 0 on the leading edge of the clock. The clear input will reset the flip-flop on a low input.

33. Give all steps of Integer division algorithm to divide 45 by 5 in 10 base systems.

Answer

There are steps of integer division present on page number 343 of course handouts. But none the less I am going to explain its working.

Divide 47 decimal with 5 decimal.

The result is again negative so we append “0” as the quotient

$$\begin{array}{r}
 D = \quad 000111 \ 000000 \\
 d \ = \quad 000101 \\
 \hline
 = \quad 000010 \qquad \qquad \qquad q = 001001
 \end{array}$$

The result is negative so we append “0” to the quotient

The result is positive so we append “1” to the quotient.

Remainder = 000010 = 2 decimal

Quotient = 001001 = 9 decimal

34. Write about single server model and give example.

Answer

Consider a black box. Suppose it represents an I/O controller. At the input, we have arrival of different tasks. As one task is done, we have a departure at the output. So in the black box, we have a server. Now if we expand and open-up the black box, we could see that incoming calls are coming into the buffer and the output of the buffer is connected to the server. This is an example of “single server model”.

35. Write structural RTL Call ra

,rb.

Answer

Step	RTL
T0-T2	Instruction Fetch
T3	C ← PC;
T4	R[ra] ← C;
T5	C ← R[rb];
T6	PC ← C;

36. What are the advantages of RAID ?

Answer

The main advantage of having an array of disks is that we could have a simultaneous I/O request. Latency could also be reduced..

37. What is EPROM

Answer

Erasable Programmable Read-only Memory or EPROM chips have quartz windows and by applying ultraviolet light erase the data can be erased from the EPROM. Data can be restored in an EPROM after erasure. EPROMs are more expensive than PROMs and are generally used for prototyping or small-quantity, special purpose work.

38. What is difference between comma and semi-colon

Answer

Comma „,“ indicates that these two instructions are concurrent and only one of them would execute at a time.

Comments are indicated by a semicolon (;) and can be placed anywhere in the source file. The FALSIM assembler ignores any text after the semicolon.

39. What is Cache? How does it works?

Answer

Cache by definition is a place for safe storage and provides the fastest possible storage after the registers. The cache contains a copy of portions of the main memory. When the CPU attempts to read a word from memory, a check is made to determine if the word is in the cache. If so, the word is delivered to the CPU. If not, a block of the main memory, consisting of some fixed number of words, is read into the cache and then the word is delivered to the CPU.

40. Comparisons of FALCON-A and SRC

Answer

Comparisons of the SRC and FALCON-A Examples

The FALCON-A and SRC programmed I/O examples discussed are similar with some differences. In the first example discussed for the SRC (i.e. Character output), the control signal responsible for data transfer by the CPU is the ready signal while for FALCON-A Busy (active low) signal is checked. In the second example for the SRC, the instruction set, address width and no. of lines on address is different. Although different techniques have been used to increase the efficiency of the programmed I/O, overheads due to polling can not be completely eliminated.

41. S assembly program for the following expiration.

$Z = 13(A+B)$ -

32(c-58)

Answer

```
ld R1, c ; c is a label used for a memory location
```

```
subi R3, R1, 58 ; R3 contains (c-58)
```

```
shl R7, R3, 5 ; R7 contains 32(c-58)
```

```
ld R4, A
```

```
ld R5, B
```

```
add R6, R4, R5 ; R6 contains (A+B)
```

Notice that the SRC does not have a multiply instruction. We will make use of the fact that multiplication with powers of 2 can be achieved by repeated shift left operations. But in the given example 13 is not directly is a

power of 2. So you need to make it power of 2.

$$13(A+B) = 8(A+B) + 4(A+B) + (A+B)$$

Suppose we place A+B in some register say R6.

```
Shl R7, R6, 3;      ;8 (A+B)
Shl R8, R6, 2;      ;4 (A+B)
Add R10, R8, R7;    ;8 (A+B) + 4 (A+B)
Add R11, R6, R10;   ;8 (A+B) + 4 (A+B) + (A+B) that is equal to 13((A+B))
sub R12, R7, R11
st R12, z ; store the result in memory location z
```

42. What attributes should have a device to qualify in order to be master device

Answer

A Master must have the capability to place addresses on the address bus and direct the bus activity during a bus cycle.

43. What is ISA explain

Answer

This set of instructions or operations and the resources together form the instruction set architecture (ISA). It is the ISA, which serves as an interface between the program and the functional units of a computer, i.e., through which, the computer's resources, are accessed and controlled.

44. Explain the relation ship between the Hard disk tracks, cylinders and sectors

Answer

A hard disk is the most frequently used peripheral device. It consists of a set of platters. Each platter is divided into tracks. The track is subdivided into sectors. To identify each sector, we need to have an address. So, before the actual data, there is a header and this header consisting of few bytes like 10 bytes. Along with header there is a trailer. Every sector has three parts: a header, data section and a trailer.

45. Explain 1bit half adder function

Answer:- (Page 339)

It takes two

1-bit inputs x and y and as a result, we get a 1-bit sum and a 1-bit carry. This circuit is called a half adder because it does not take care of input carry. In order to take into account the effect of the input carry, a 1-bit full

adder is used which is also shown in the figure. We can add two m-bit numbers by using a circuit which is made by cascading m 1-bit full adders.

46. hard disk with 5 platters has 1024 tracks per platter,512 sectors per track and 512 bytes/sector.

What is the total capacity of the disk?

Answer

512 bytes x 512

sectors=0.2MB/track

0.2MB x 1024 tracks=0.2GB/platter

Therefore the hard disk has the total capacity of 5 x 0.2=1GB

47. What is the difference between control unit n data path?

Answer

The data path design involves decisions like the placement and interconnection of various registers, the type of flip-flops to be used and the number and kind of the interconnection buses.

The control unit design is a rather tricky process as it involves timing and synchronization issues besides the usual combinational logic used in the data path design.

48. What is the working of DMA controller?

Answer

A DMA controller could be a CPU in itself and it could control the total activity and synchronize the transfer of data". DMA could be considered as a technique of transferring data from I/O to memory and from memory to I/O without the intervention of the CPU. The CPU just sets up an I/O module or a memory subsystem, so that it passes control and the data could be passed on from I/O to memory or from memory to I/O or within the memory from one subsystem to another subsystem without interaction of the CPU. After this data transfer is complete, the control is passed from I/O back to the CPU.

49. Define 64K x 1 static RAM chip?

Answer

A 64k×1 Static RAM Chip

The cell array is indicated as 256 × 256. So, there would be 256 rows and 256 columns.

A 64k × 1 cell array requires 16 address lines, a read/write line, R/\overline{W} , a chip select line, CS, and only a single data line. The lower order 8-address lines select one of the 256 rows using an 8-to-256 line row decoder. Thus the selected row contains 256 bits. The higher order 8-address lines select one of those 256 bits. The 256 bits in the row selected flow through a 256-to-1 line multiplexer on a read. On a memory write, the incoming bit flows through a 1-to-256 line demultiplexer that selects the correct column of the 256 possible columns.

50. Differentiate b/w RISC n CISC according to their instruction size and hardware, software? 5 marks.

Answer

CISC	RISC
Emphasis on hardware	Emphasis on Software
Include multi-clock	Include Single-clock
complex instructions	Reduced instructions only
memory to memory:	Registers to Register:
"LOAD" and "STORE" incorporated in instructions	"LOAD" and "STORE" are independent instructions
Small code sizes	Large code sizes
high cycles per second	Low cycles per second
Transistors used for storing	Spend more transistors on memory registers

RISC	CISC
Multiple register sets, often consisting of more than 256 registers	Single register set, typically 6 to 16 registers total
Three register operands allowed per instruction (e.g., add R1, R2, R3)	One or two register operands allowed per instruction (e.g., add R1, R2)
Parameter passing through efficient on-chip register windows	Parameter passing through inefficient off-chip memory
Single-cycle instructions (except for load and store)	Multiple-cycle instructions
Hardwired control	Microprogrammed control
Highly pipelined	Less pipelined
Simple instructions that are few in number	Many complex instructions
Fixed length instructions	Variable length instructions
Complexity in compiler	Complexity in microcode
Only load and store instructions can access memory	Many instructions can access memory
Few addressing modes	Many addressing modes

51. Compare 1D AND 2D

Answer

1×8 Memory Cell Array (1D)

In this arrangement, each block is connected through a bi-directional data bus implemented with 2 tri-state buffers. R/\overline{W} and Select signals are common to all these cells. This 1-dimensional memory array could not be very efficient, if we need to have a very large memory.

4×8 Memory Cell Array (2D)

In this arrangement, 4×8 memory cell array is arranged in 2-dimensions. At the input, we have a 2×4 decoder. Two address bits at the input A0 and A1 would be decoded into 4 select lines. The decoder selects one of four rows of cells and then R/\overline{W} signal specifies whether the row will be read or written.

52. Write RTL for five instructions movi R3,45 In R3,57 OUT R6 15 RET R3 ANDI R5, R4. 5

Answer

movi R3,45

$R[3] \leftarrow 56$

In R3,57

$R[3] \leftarrow IO[57]$

OUT R6 15

$IO[16] \leftarrow R[6]$

RET R3

PC ← R[3]

ANDI R5, R4, 5
R[5] ← R[4]&5

53. Differ b/w serial and parallel transfer

Answer

Serial Transfer, or serial communication of data between the CPU and the I/O devices, refers to the situation when all the data bits in a "piece of information", (which is a byte or word mostly), are transferred one bit at a time, over a single pair of wires.

Parallel Transfer, or parallel communication of data between the CPU and the I/O devices, refers to the situation when all the bits of data (8 or 16 usually), are transferred over separate lines simultaneously, or in parallel.

54. configuration of 1x8 memory

Answer

1×8 Memory Cell Array (1D)

In this arrangement, each block is connected through a bi-directional data bus implemented with 2 tri-state buffers. R/\overline{W} and Select signals are common to all these cells. This 1-dimensional memory array could not be very efficient, if we need to have a very large memory.

55. difference bw connection oriented and connection less

Answer

Connection Oriented Communication

- In this method, same path is always taken for the transfer of messages.
- It reserves the bandwidth until the transfer is complete. So no other server could use that path until it becomes free.
- Telephone exchange and circuit switching is the example of connection oriented communication.

Connection less Communication

- Here message is divided into packets with each packet having destination address.
- Each packet can take different path and reach the destination from any route by looking at its address.
- Postal system and packet switching are examples of connection less communication.

56. where TCP/IP Used??

Answer

Internet uses TCP/IP protocol. In the TCP/IP model, session and presentation layers are not present, so Store-Forward routing is used.

57. STAGes in pipelined SRC

Answer

The SRC uses a five-stage pipeline. Those five stages are given below:

1. Instruction Fetch
2. Instruction decode/operand fetch
3. ALU operation

4. Memory access

5. Register write

58. What does the RTL expression M [1234] means 2

Answer _____

The RTL expression [M(1234)] means the contents of memory whose location (i.e., address) is 1234. Or, sometimes expressed as 0x1234 to denote hex.

59. What are the sectors of the hard disk?

Answer

A hard disk is the most frequently used peripheral device. It consists of a set of platters. Each platter is divided into tracks. The track is subdivided into sectors. To identify each sector, we need to have an address.

60. Why MIPS is not very accurate basis for comparison of different processes. Write formula of MIPS. 3

Answer

$$\text{MIPS} = \text{IC} / (\text{ET} \times 106)$$

This measure is not a very accurate basis for comparison of different processors. This is because of the architectural differences of the machines; some machines will require more instructions to perform the same job as compared to other machines. For example, RISC machines have simpler instructions, so the same job will require more instructions. This measure of performance was popular in the late 70s and early 80s when the VAX 11/780 was treated as a reference.

61. Record the integer 485 according to the BOOTH procedure

Answer

Solution

Original number:

$$00111100101 = 256 + 128 + 64 + 32 + 4 + 1 = 485$$

Recoded Number:

$$01000\bar{1}0\bar{1}\bar{1}\bar{1}\bar{1} = +512 - 32 + 8 - 4 + 2 - 1 = 485$$

62. Find out sign, significand and exponent of -7×10^{-4} .

Answer:-

Sign = -1

Significand = 7

Exponent = -4

Base = 10

63. Define virtual memory

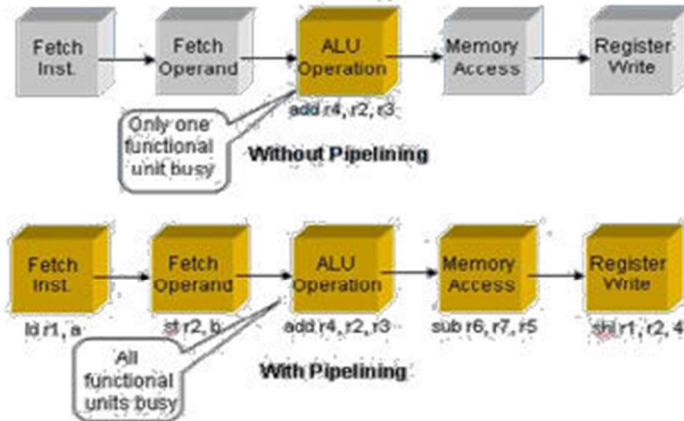
Virtual memory acts as a cache between main memory and secondary memory. Data is fetched in advance from the secondary memory (hard disk) into the main memory so that data is already available in the main memory when needed. The benefit is that the large access delays in reading data from hard disk are avoided.

64. what is difference of instruction in machine with and without Pipeline?

Answer: Comparing machine instructions with and without pipelining

We start by assuming that a given processor can be split in to five different stages as shown in the diagram below,

and as explained later in this section. Each stage receives its input from the previous stage and provides its result to the next stage. It can be easily seen from the diagram that in case of a non-pipelined machine there is a single instruction `add r4, r2, r3` being processed at a given time, while in a pipelined machine, five different



instructions are being processed simultaneously. An implied assumption in this case is that at the end of each stage, we have some sort of a storage place (like temporary registers) to hold the results of the present stage till they are used by the next stage.

65. Find the average access time of a level of memory hierarchy if the hit rate is 80%. The memory access takes 12ns on a hit and 100ns on a miss.

Answer:

Hit rate =80%

Miss rate=20%

$T_{hit}=12\text{ ns}$

$T_{miss}=100\text{ns}$

$$\begin{aligned} \text{Average } T_{\text{access}} &= (\text{hit rate} * T_{\text{hit}}) + (\text{miss rate} * T_{\text{miss}}) \\ &= (0.8 * 12\text{ns}) + (0.2 * 100\text{ns}) \\ &= 29.6\text{ns} \end{aligned}$$

66. Difference between virtual address and physical address

Answer

Virtual Address:

Virtual address is generated by the logical by the memory management unit for translation.

Physical Address:

Physical address is the address in the memory.

67. Why Transaction Lockside Buffer is used? How it is implemented inside CPU?

Answer

Identifying a particular page in the virtual memory requires page tables (might be very large) resulting in large memory space to implement these page tables. To speed up the process of virtual address translation, translation Lookaside buffer (TLB) is implemented as a small cache inside the CPU, which stores the most recent page table entry reference made in the MMU. Its contents include

- A mapping from virtual to physical address
 - Status bits i.e. valid bit, dirty bit, protection bit
- It may be implemented using a fully associative organization

68. What is sender overhead and receiver overhead in computer networks?

Answer

Sender overhead

It is the time for the processor to inject message in to the network.

Receiver overhead

It is the time for the processor to pull the message from the network.

69. How can overflow occur in floating point?

Answer

Overflow occurs when the exponent is too large and can not be represented in the exponent field

70. Difference between Eagle and modified Eagle

Answer

The modified EAGLE is an improved version of the processor EAGLE. As we have already discussed, there were several limitations in EAGLE, and these have been remedied in the modified EAGLE processor.

71. Why we represent sometime some numbers in sign magnitude form.

Answer

- This is the simplest form for representing a signed number
- A symbol representing the sign of the number is appended to the left of the Number
- This representation complicates the arithmetic operations

72. What is 4-address instruction set and when it use?

ANSWER:

Discussion 4-address instruction

- The code size is 13 bytes (1+3+3+3+3 = 13 bytes)
- Number of bytes

op code	destination	source 1	source 2	next address
1 byte	3 bytes	3 bytes	3 bytes	3 bytes

accessed from memory is 22 (13 bytes for instruction fetch + 6 bytes for source operand fetch + 3 bytes for storing destination operand = 22 bytes)

Note that there is no need for an additional memory access for the operand corresponding to the next instruction, as it has already been brought into the CPU during instruction fetch.

73. Which name convention will you use to name each of these eight general purpose registers? What is the available memory space size knowing that memory word is 16 bits? 5 marks

Answer

- a) As the length of register is 16-bit so we use Little-endian name convention
b) memory word is 16-bit so the available memory space size is 2^{16} bytes

74. What are the functions of memory cell?

Answer

A memory cell provides four functions: Select, DataIn, DataOut, and Read/Write. DataIn means input and DataOut means output. The select signal would be enabled to get an operation of Read/Write from this cell.

75. How we can specify registers in RTL? Give an example?

Answer

Specifying Registers

The format used to specify registers is Register Name<register bits>

Name<register bits>

For example, IR<31..0> means bits numbered 31 to 0 of a 32-bit register named "IR" (Instruction Register).

76. What is seek time of hard disk? 3 marks

Answer

When it is required to read data from a particular location of the disk, the head moves towards the selected track and this process is called seek. The disk is constantly rotating at a fixed speed. After a short time, the selected sector moved under the head. This interval is called the rotational delay. On the average, the data may be available after half a revolution. Therefore, the rotational latency is half revolution.

The time required to seek a particular track is defined by the manufacturer. Maximum, minimum and average seek times are specified. Seek time depends upon the present position of the head and the position of the required sector. For the sake of calculations, we will use the average value of the seek time.

77. Differences between RAID2 and RAID 3?

Answer

- In RAID 2, error-correcting code is calculated across corresponding bits on each data disk.
- RAID 3 requires only a single redundant disk.
- Instead of an error-correcting code, a simple parity bit is computed for the set of individual bits in RAID 3

78. What are three main functions of control Unit? 3marks

Answer

It directs the entire computer system to carry out stored program instructions.

It must communicate with both the arithmetic logic unit (ALU) and the main memory.

It instructs the ALU on arithmetic operations to be performed.

79. Consider a 64KB direct-mapped cache with a line length of 32 bytes. (5 marks)

- a. Determine the number of bits in the address that refer to the byte within a cache line. b. Determine the number of bits in the address required to select the cache line**

Answer

Address breakdown

$n = \log_2$ of number of bytes in line

$m = \log_2$ of number of lines in cache

- a. For the given cache, the number of bits in the address to determine the byte within the line = $n = \log_2 32 = 5$

b. There are $64K/32 = 2048$ lines in the given cache. The number of bits required to select the required line = m

$$= \log_2 2048 = 11$$

Hence $n=5$ and $m=11$

80. If a DRAM has 512 rows and its refresh time is 9ms .What should be the frequency of row refresh operation on the average?

Answer

Refresh time =9ms

Number of rows =512

Therefore we have to do 512 row refresh operations in a 9 ms interval, in other words one row refresh operation every $(9 \times 10^{-3})/512 = 1.76 \times 10^{-5}$ second

81.

Structural RTL for not instruction not ra ,rb

Answer

Step	RTL
T0-T2	Instruction fetch
T3	$C \leftarrow I(R[rb]);$
T4	$R[ra] \leftarrow C;$

82. why we use matrix in decoder

Answer

A typical one level decoder has n inputs and 2^n output, using one level of gates, each with a fan-in of n. Two level decoders are limited in size because of high gate fan-in. In order to reduce the gate fan-in to a value of 8 or 6, tree and matrix decoders are utilized.

83. Convert $(0.23)_{10}$ to the base 2 address

Answer

$$0.23 \times 2 = 0.46, f_1 = 0$$

$$0.46 \times 2 = 0.92, f_2 = 0$$

$$0.92 \times 2 = 1.84, f_3 = 1$$

$$0.84 \times 2 = 1.68, f_4 = 1$$

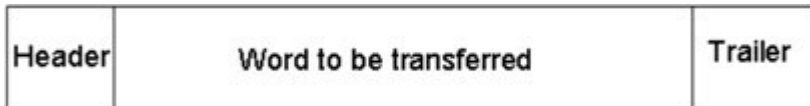
$$0.68 \times 2 = 1.36, f_5 = 1, \dots$$

$$\text{Thus } 0.2410 = (0.00111)_2$$

84. What is meant by Packet switching

Answer

A block (an appropriate number of bits) of data is called a packet. Transfer of data in the form packets through different paths in a network is called packet switching. Additional bits are usually associated with each packet. These bits contain information about the packet. These additional bits are of two types: header and trailer. As an example, a packet may have the form shown below:



If we use a 1-bit header, we may have the following protocol:

Header = 0, it means it is a request

Header = 1, Reply

By reading these header bits, a machine becomes able to receive data or supply data. To transfer data by using packets through hardware is very difficult. So all the transfer is done by using software. By using more number of bits, in a header, we can send more messages. For example if n bits are used as header then 2^n is the number of messages that can be transmitted over a network by using a single header. For a 2 bit header: we may have 4 types of messages:

00= Request

01= Reply

10= Acknowledge request

11= Acknowledge reply

85. What function is performed by the reset operation of a processor? What are the two types of reset operations?

Answer

The two essential features of a reset instruction are clearing the control step counter and reloading the PC to a predefined value.

Hard Reset

The SRC should perform a hard reset upon receiving a start (Strt) signal. This initializes the PC and the general registers.

Soft Reset

The SRC should perform a soft reset upon receiving a reset (rst) signal. The soft reset results in initialization of PC only.

The reset signal in SRC is assumed to be external and asynchronous.

86. What do you know about Hard disk.

Answer

Peripheral devices connect the outside world with the central processing unit through the I/O modules. One important feature of these peripheral devices is the variable data rate. Peripheral devices are important because of the function they perform.

A hard disk is the most frequently used peripheral device. It consists of a set of platters. Each platter is divided into tracks. The track is subdivided into sectors. To identify each sector, we need to have an address. So, before the actual data, there is a header and this header consisting of few bytes like 10 bytes. Along with header there is a trailer. Every sector has three parts: a header, data section and a trailer.

87. How many drives do you need a minimum to form RAID 0?

0

Only 1

Minimum 2

Maximum 2

Answer

Minimum 2

To establish a RAID 0 volume, a minimum of at least 2 hard disk drives are required. Unlike RAID 1, the number of drives used in the array can be an odd or even number.

88. Define PROM?

Answer

The PROM stands for Programmable Read only Memory. It is also nonvolatile and may be written into only once. For PROM, the writing process is performed electrically in the field. PROMs provide flexibility and convenience.

89. How we refer the register to the RTL? Give an example?

Answer

Specifying Registers

The format used to specify registers is

Register Name<register bits>

For example, IR<31..0> means bits numbered 31 to 0 of a 32-bit register named "IR" (Instruction Register).

90. What is the use of modem?

Answer

To interconnect different computers by using twisted pair copper wire, an interface is used which is called modem. Modem stands for modulation/demodulation. Modems are very useful to utilize the telephone network (i.e. 4 KHz bandwidth) for data and voice transmission.

91. What is the advantage of RAID level 0?

Answer

- The user and system data are distributed across all the disks in the array.
- Notable advantage over the use of a single large disk.

92. Encode the register into binary? R0 TO R7

Answer

Encoding of the General Purpose Registers.

R0	00000
R1	00001
R2	00010
R3	00011
R4	00100
R5	00101
R6	00110
R7	00111

93. What is the difference multimode fiber and mono fiber which are used as a physical medium of the network?

Answer

Multimode fiber

This fiber has large diameter. When light is injected, it disperses, so the effective data rate

decreases. Multimode fiber is used as a physical medium of the network

Mono mode Fiber

Its diameter is very small. So dispersion is small and data rate is very high.

94. What is meant by cycle stealing in the DMA?

Answer

The DMA module takes control of the bus to transfer data to and from memory by forcing the CPU to temporarily suspend its operation. This approach is called Cycle Stealing because in this approach DMA steals a bus cycle.

95. Write the radix conversion algorithm to convert 392_{10} to the base 16?

Answer

According to the above algorithm $390/16 = 24$ (rem=6), $x_0=6$ $24/16 = 1$ (rem=8), $x_1=8$, $x_2=1$ Thus
 $390_{10} = 186_{16}$

96. What is the difference between internal segmentation and external segmentation relevant to the computer storage ?

Answer:

In fixed partitioning the pages are of fixed size and some space is wasted in the last page. For example if we have page size equal to 2 K and the program size is of 9 K then we have to use 5 pages each of size 2 k. In this case 4 pages fully consumed but the last page has 1 k free memory and it can not be utilized, so this type of fragmentation is called internal fragmentation. It is basically the wastage of space of within the partition.

In variable partitioning the page size is not fixed. In this type of partitioning the page size is variable. So pages are allocated accordingly. If say program A is of size 5 k then 5 k page size is reserved and say another program B comes in having size 3 k so now page size of 3 k is reserved. Now if A program exits and the new program C having size 4 k comes in, it will replace the 5 k partition of program A but the space of 1 K is wasted between program C and program B. This wastage of space is called external fragmentation. It is basically the wastage of space between the partitions.

97. Write the SRC assembly program for the following expression?

$$Z = 16(a+b) - 32(c-58)$$

Answer

```
ld R1, c ; c is a label used for a memory location
subi R3, R1, 58 ; R3 contains (c-58)
shl R7, R3, 5 ; R7 contains 32(c-58)
ld R4, a
ld R5, b
add R6, R4, R5 ; R6 contains (a+b)
shl R8, R6, 4 ; R8 contains 16(a+b)
sub R9, R7, R8 ; the result is in R9
st R9, z ; store the result in memory location z
```

98. Write two lines on connection oriented

communication?

Answer

In this method, same path is always taken for the transfer of messages. It reserves the bandwidth until the transfer is complete. So no other server could use that path until it becomes free.

99. What is the advantage of direct cache memory?

Answer

Advantage is Simplicity.

100.

Write the drawbacks of DMA?

Answer

The disadvantage however, would be that an additional DMA controller would be required, that could make the system a bit more complex and expensive. Generally, the DMA requests have priority over all other bus activities including interrupts. No interrupts may be recognized during a DMA cycle.

101. What is the difference between selection channel and multiple channels?

Answer

Selector Channel

It is the DMA controller that can do block transfers for several devices but only one at a time.

Multiplexer Channel

It is the DMA controller that can do block transfers for several devices at once.

102. What is the advantage of linker in assembly language program?

Answer

When developing large programs, different people working at the same time can develop separate modules of functionality. These modules can then be „linked“ to form a single module that can be loaded and executed. The modularity of programs, that the linking step in assembly language makes possible, provides the same convenience as it does in higher-level languages; namely abstraction and separation of concerns. Once the functionality of a module has been verified for correctness, it can be re-used in any number of other modules. The programmer can focus on other parts of the program. This is the so-called “modular” approach, or the “top-down” approach.

103. What do you understand by the assembler of the assembly language?

Answer

Programs written in assembly language require translation to the machine language, and an assembler performs this translation. This conversion process is termed as the assembly process.

104. Consider a LAN using bus topology if we replace the bus with a switch, what change occurs in such a configuration.

Answer

If we replace the bus with a switch, the speed of the data transfer will be improved to a great extent.

105. Name the two classes of instruction set architecture

Answer

- Accumulator based machines

- Stack based machines

106. Find the average rotational latency if the disk rotates 15000rpm.

Answer

The average latency to the desired data is halfway round the disk so Average rotational latency = $(1 / (\text{RPM} / 60)) * 0.5 * 1000$
 $= 30000 / \text{RPM} = 30000 / 15000 = 2\text{ms}$

107. How shift instructions are useful? When do we use them? (3 marks)

Answer

Using shift instructions (shifl, asr, etc.) is faster than **mul** and **div**, if the multiplier or divisor is a power of 2. Shift and logical instructions are used to implement logical expressions and bitwise logical operators in high level languages. Shift instructions for arithmetic operations are more efficient than the corresponding arithmetic instruction.

108. How the exception may be generated? Difference between external and internal exception.

Answer

Exceptions may be generated by an external or internal event such as a mouse click or an attempt to divide by zero etc.

External exceptions or interrupts are generally asynchronous (do not depend on the system clock) while internal exceptions are synchronous (paced by internal clock)

109. Find out the sign, significant and exponent from the above example

Answer

Sign = -1

Significand= 6

Exponent= -3

Base = 10= fixed for given type of representation

110. Does DMA affect the relationship between the memory system and the CPU? Explain

Answer

DMA and memory system

DMA disturbs the relationship between the memory system and CPU.

Direct memory access and the memory system

Without DMA, all memory accesses are handled by the CPU, using address translation and cache mechanism. When DMA is implemented into an I/O system memory accesses can be made without intervening the CPU for address translation and cache access. The problems created by the DMA in virtual memory and cache systems can be solved using hardware and software techniques.

111. Suppose the I/O system with a single disk get an average of 200 I/O request/second assume that the average time for a disk to service and I/O request is 4ms. What is the utilization of I/O system? (5marks) Answer:- (Page 382)

Time for an I/O request = 4ms

=0.004sec

Server utilization = 200×0.004

= 0.8

- 112. Consider a 4 way set-associative cache with 256KB capacity and 32 byte lines**
a) How many sets are there in the cache?
b) How many bits of address are required to select a set in cache?

Answer:-

(a)

$256 \times 1024 \div 32 = 8192$ lines of data

$8192 / 4 = 2048$ sets in the cache

A 256KB cache with 32 byte lines contains 8192 lines of data. In a 4-way set associative cache, each set contains 4 lines, so there are 2048 sets in the cache.

(b)

$\text{Log}_2(2048) = 11$. Hence 11 bits of the address are required to select the set.

- 113. The following table shows a partial summary of the ISA for the SRC. Write an assembly language program using the SRC assembly language to evaluate the expression:**

$$Z = (7 + 16a) - (8b - c)$$

Answer:-

ld R1, c ; c is a label used for a memory location

ld R2, b

shl R3, R2, 3

sub R4, R3, R1

ld R5, a

shl R5, 4

addi R6, R5, 7

sub R7, R6, R4

st R7, z ; store the result in memory location z

- 114. Find the bandwidth of a memory system that has a latency of 30ns, a pre charge time of 10ns and transfers 3 bytes of data per access.**

Answer:-

Time between two memory reference

= latency + pre charge time

= 30ns + 10ns

= 40ns

Throughput = $1/40\text{ns}$

= 2.5×10^7 operation/sec

Bandwidth = $3 \times 2.5 \times 10^7$

= 7.5×10^7 byets/sec

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