Proude To Be Virtulian MOAAZ SIDDIQ	**CS302- Digital Logic Design** **LATEST SOLVED MCQS FROM MIDTERM PAPERS**	**May 07,2011** **Latest Mcqs**
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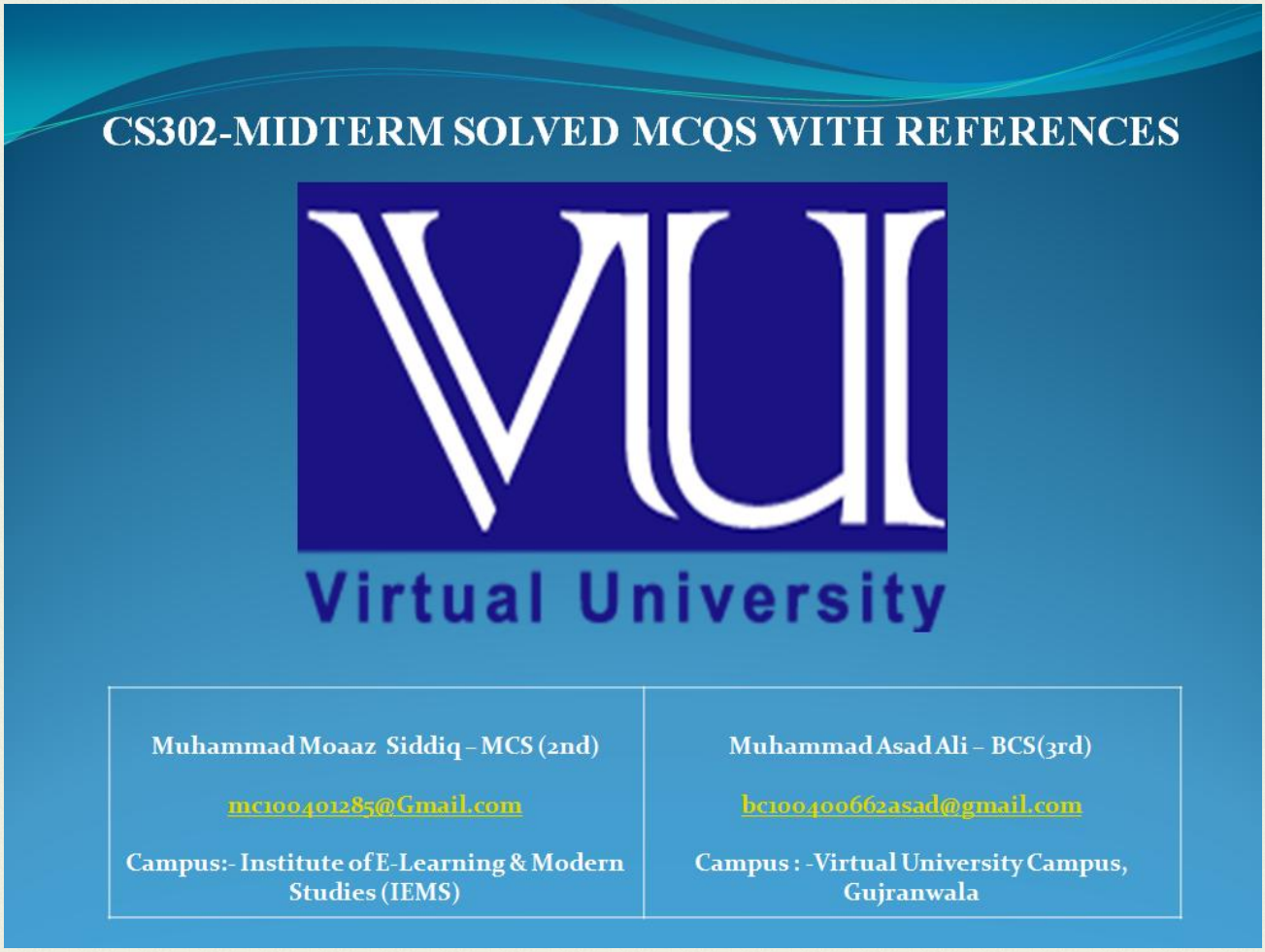

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MIDTERM EXAMINATION
Spring 2010

Question No: 1 (Marks: 1) - Please choose one
A SOP expression is equal to 1 _____

► All the variables in domain of expression are present
► At least one variable in domain of expression is present.
► When one or more product terms in the expression are equal to 0.
► When one or more product terms in the expression are equal to 1. (Page 86)

Question No: 2 (Marks: 1) - Please choose one
The output A < B is set to 1 when the input combinations is _____

► A=10, B=01
► A=11, B=01
► A=01, B=01
► A=01, B=10 (Page 109)

Question No: 3 (Marks: 1) - Please choose one
Two 2-bit comparator circuits can be connected to form single 4-bit comparator

► True (Page 154)
► False

Question No: 4 (Marks: 1) - Please choose one
High level Noise Margins (V_{NH}) of CMOS 5 volt series circuits is _____

► 0.3 V
► 0.5 V
► 0.9 V (Page 65)
► 3.3 V

Question No: 5 (Marks: 1) - Please choose one
If we multiply "723" and "34" by representing them in floating point notation i.e. by first, converting them in floating point representation and then multiplying them, the value of mantissa of result will be _____

► 24.582 (But not sure)
► 2.4582
► 24582

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► 0.24582

Question No: 6 (Marks: 1) - Please choose one
The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol'+' here represents OR Gate.

► Undefined
► One
► Zero
► 10 (binary)

Question No: 7 (Marks: 1) - Please choose one
If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

► SET (page 220)
► RESET
► Clear
► Invalid

Question No: 8 (Marks: 1) - Please choose one
3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series.

► Low switching speeds, high power dissipation
► Fast switching speeds, high power dissipation
► Fast switching speeds, very low power dissipation (page61)
► Low switching speeds, very low power dissipation

Question No: 9 (Marks: 1) - Please choose one
The binary value "1010110" is equivalent to decimal _____

► 86 (According to Formula)
► 87
► 88
► 89

Question No: 10 (Marks: 1) - Please choose one
The _____ Encoder is used as a keypad encoder.

► 2-to-8 encoder
► 4-to-16 encoder
► BCD-to-Decimal

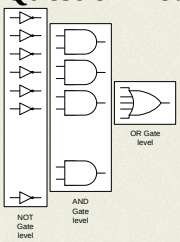
► **Decimal-to-BCD Priority (Page 166)**

Question No: 11 (Marks: 1) - Please choose one

How many data select lines are required for selecting eight inputs?

► 1
► 2
► **3 click here for detail**
► 4

Question No: 12 (Marks: 1) - Please choose one



the diagram above shows the general implementation of _____ form

► boolean
► arbitrary
► POS
► **SOP**

Question No: 13 (Marks: 1) - Please choose one

The Quad Multiplexer has _____ outputs

► **4 (Page 217)**
► 8
► 12
► 16

Question No: 14 (Marks: 1) - Please choose one

Demultiplexer has

► Single input and single outputs.
► Multiple inputs and multiple outputs.
► **Single input and multiple outputs. (Page 178)**
► Multiple inputs and single output.

Question No: 15 (Marks: 1) - Please choose one

The expression _____ is an example of Commutative Law for Multiplication.

► AB+C = A+BC
► A(B+C) = B(A+C)
► **AB=BA (Page 72)**
► A+B=B+A

Question No: 16 (Marks: 1) - Please choose one
"Sum-of-Weights" method is used _____
► **to convert from one number system to other (Page 14)**
► to encode data
► to decode data
► to convert from serial to parralel data

MIDTERM EXAMINATION
Spring 2010

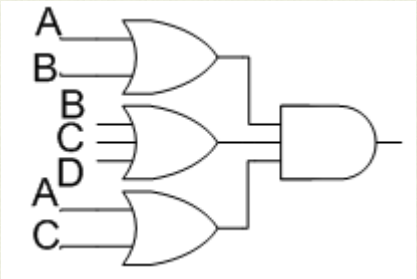
Question No: 1 (Marks: 1) - Please choose one
The maximum number that can be represented using unsigned octal system is _____

► 1
► **7 (Page 31)**
► 9
► 16

Question No: 2 (Marks: 1) - Please choose one
If we add "723" and "134" by representing them in floating point notation i.e. by first, converting them in floating point representation and then adding them, the value of exponent of result will be _____

► 0
► 1
► **2 (Page 26)**
► 3

Question No: 3 (Marks: 1) - Please choose one
The diagram given below represents _____



► Demorgans law

► Associative law
► **Product of sum form (According to rule of theorem)**
► Sum of product form

Question No: 4 (Marks: 1) - Please choose one
The range of Excess-8 code is from _____ to _____
► **+7 to -8 (Page 34)**
► +8 to -7
► +9 to -8
► -9 to +8

Question No: 5 (Marks: 1) - Please choose one
A non-standard POS is converted into a standard POS by using the rule _____
► $A+\overline{A}=1$
► $A\overline{A} = 0$ **(Page 85)**
► $1+A=1$
► A+B = B+A

Question No: 6 (Marks: 1) - Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms
► 4
► **8 (Page 89)**
► 12
► 16

Question No: 7 (Marks: 1) - Please choose one
The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?
► **A > B = 1, A < B = 0, A < B = 1**
► A > B = 0, A < B = 1, A = B = 0
► **A > B = 1, A < B = 0, A = B = 0 (Page 109)**
► A > B = 0, A < B = 1, A = B = 1

Question No: 8 (Marks: 1) - Please choose one
A particular Full Adder has
► **3 inputs and 2 output (Page 135)**
► 3 inputs and 3 output
► 2 inputs and 3 output
► 2 inputs and 2 output

Question No: 9 (Marks: 1) - Please choose one
The function to be performed by the processor is selected by set of inputs known as _____

► **Function Select Inputs (Page 147)**
► MicroOperation selectors
► OPCODE Selectors
► None of given option

Question No: 10 (Marks: 1) - Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

► **2 (Page 160)**
► 1
► 3
► 4

Question No: 11 (Marks: 1) - Please choose one
GAL is an acronym for _____.

► Giant Array Logic
► **General Array Logic (Page 183)**
► Generic Array Logic
► Generic Analysis Logic

Question No: 12 (Marks: 1) - Please choose one
The Quad Multiplexer has _____ outputs

► **4 (Page 216)**
► 8
► 12
► 16

Question No: 13 (Marks: 1) - Please choose one
A.(B.C) = (A.B).C is an expression of _____

► Demorgan's Law
► Distributive Law
► Commutative Law
► **Associative Law (Page 72)**

Question No: 14 (Marks: 1) - Please choose one
2's complement of any binary number can be calculated by
► adding 1's complement twice
► **adding 1 to 1's complement (Page 144)**

► subtracting 1 from 1's complement.
► calculating 1's complement and inverting Most significant bit

Question No: 15 (Marks: 1) - Please choose one
The binary value "1010110" is equivalent to decimal _____

► **86 (According to formula)**
► 87
► 88
► 89

Question No: 16 (Marks: 1) - Please choose one
Tri-State Buffer is basically a/an _____ gate.

► AND
► OR
► NOT
► **XOR (Page 186)**

MIDTERM EXAMINATION 2010

1. **The binary value "11011" is equivalent to _____**

►**1B (According to rule)**
►1C
►1D
►1E

2. **An important application of AND Gate is its use in counter circuit**

►**True (Page 281)**
►False

3. **The OR Gate performs a Boolean _____ function**

►**Addition (Page 42)**
►Subtraction
►Multiplication
►Division

4. **TTL based devices work with a dc supply of ____ Volts**

►+10
►**+5 (Page 61)**
►+3

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►3.3

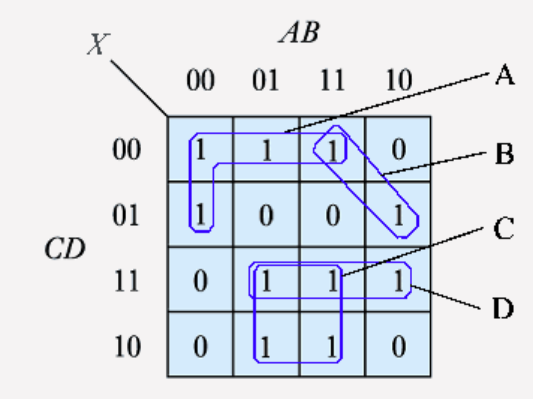
5. A standard POS form has _____ terms that have all the variables in the domain of the expression.

►**Sum (Page 85)**
►Product
►Min
►Composite

6. A SOP expression having a domain of 3 variables will have a truth table having ____ combinations of inputs and corresponding output values.

►2
►4
►**8 (According to rule)**
►16

7. A BCD to 7-Segment decoder has
►3 inputs and 7 outputs
►**4 inputs and 7 outputs (Page 103)**
►7 inputs and 3 outputs
► inputs and 4 outputs



8. In the Karnaugh map shown above, which of the loops shown represents a legal grouping?

►A
►
►**C click here for detail**
►D

9. The binary value of 1010 is converted to the product term $\bar{A}B\bar{C}D$

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►True
►**False**

10. The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

►A > B = 1, A < B = 0, A < B = 1
►A > B = 0, A < B = 1, A = B = 0
►**A > B = 1, A < B = 0, A = B = 0 (Page 109)**
►A > B = 0, A < B = 1, A = B = 1

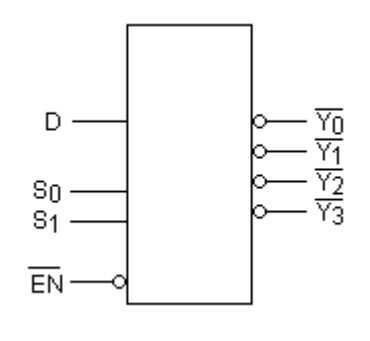
11. $C_{out1} + S_3(S_2 + S_1)$ **is boolean expression for**

►Half Adder
►Full Adder
►**The Invalid BCD Detector Circuit (page 142)**
►Parity Checker

12. 3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

►**True (Page 160)**
►False

13. The device shown here is most likely a _____



►Comparator
►Multiplexer
►**Demultiplexer click here for detail**
►Parity generator

14. The GAL22V10 has ____ inputs

►**22 (Page 195)**
►10
►44
►20

15. A latch retains the state unless

►Power is turned off
►**Input is changed (page 218)**
►Output is changed
►Clock pulse is changed

16. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

►**SET (Page 220)**
►RESET
►Clear
►Invalid

17. Consider a circuit consisting of two consecutive NOT gates, the entire circuit belongs to a CMOS 5 Volt series, if certain voltage is applied on the input, the output voltage of Logic high signal (V_{oH}) will be in the range of _____ volts.

►4 to 4.5
►**4.5 to 5**
►0 to 4.5
►0 to 3.5

18. A.(B.C) = (A.B).C is an expression of _____

►Demorgan's Law
►Distributive Law
►Commutative Law
►**Associative Law (Page 72)**

19. The 4-bit 2's complement representation of "+5" is _____

►1010
►1110
►**1011**
►0101

20. Which of the number is not a representative of hexadecimal system

►1234
►ABCD
►1001
►DEHF Hexa does not have H as remainder

MIDTERM EXAMINATION
Spring 2010

Question No: 1 (Marks: 1) - Please choose one

► 1
► **7**
► 9
► 16

Question No: 2 (Marks: 1) - Please choose one
If we add "723" and "134" by representing them in floating point notation i.e. by first, converting them in floating point representation and then adding them, the value of exponent of result will be _____

► 0
► 1
► 2 (Page 26)
► 3

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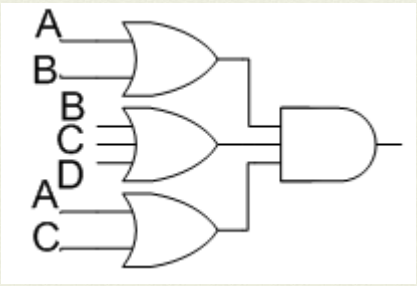
The diagram given below represents _____



► Demorgans law
► Associative law
► Product of sum form (According to rule)
► Sum of product form

Question No: 4 (Marks: 1) - Please choose one

The range of Excess-8 code is from _____ to _____

► **+7 to -8 (Page 34)**
► +8 to -7
► +9 to -8
► -9 to +8

Question No: 5 (Marks: 1) - Please choose one
A non-standard POS is converted into a standard POS by using the rule _____

► $A+\overline{A}=1$
► $A\overline{A}=0$ **(Page 85)**
► $1+A=1$
► A+B = B+A

Question No: 6 (Marks: 1) - Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► **8 (Page 89)**
► 12
► 16

Question No: 7 (Marks: 1) - Please choose one
The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

► A > B = 1, A < B = 0, A < B = 1
► A > B = 0, A < B = 1, A = B = 0
► **A > B = 1, A < B = 0, A = B = 0 (Page 109)**
► A > B = 0, A < B = 1, A = B = 1

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A particular Full Adder has

► **3 inputs and 2 output (Page 135)**
► 3 inputs and 3 output
► 2 inputs and 3 output
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Question No: 9 (Marks: 1) - Please choose one
The function to be performed by the processor is selected by set of inputs known as ____

► **Function Select Inputs (Page 147)**

► MicroOperation selectors
► OPCODE Selectors
► None of given option

Question No: 10 (Marks: 1) - Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

► **2 (Page 160)**
► 1
► 3
► 4

Question No: 11 (Marks: 1) - Please choose one
GAL is an acronym for _____.

► Giant Array Logic
► **General Array Logic (Page 183)**
► Generic Array Logic
► Generic Analysis Logic

Question No: 12 (Marks: 1) - Please choose one
The Quad Multiplexer has _____ outputs

► **4 (Page 216)**
► 8
► 12
► **16**

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A.(B.C) = (A.B).C is an expression of _____

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► Distributive Law
► Commutative Law
► **Associative Law (Page 72)**

Question No: 14 (Marks: 1) - Please choose one
2's complement of any binary number can be calculated by
► adding 1's complement twice
► **adding 1 to 1's complement (Page 144)**
► subtracting 1 from 1's complement.
► calculating 1's complement and inverting Most significant bit

Question No: 15 (Marks: 1) - Please choose one

The binary value “1010110” is equivalent to decimal _____

► **86 (According to formula)**
► 87
► 88
► 89

Question No: 16 (Marks: 1) - Please choose one
Tri-State Buffer is basically a/an _____ gate.

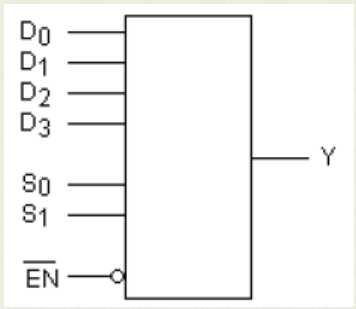
► AND
► OR
► **NOT (page 196)**
► **XOR**

MIDTERM EXAMINATION
Spring 2009
CS302- Digital Logic Design (Session - 1)

Question No: 1 (Marks: 1) - Please choose one
GALcan be reprogrammed because instead of fuses _____logic is used in it

► **E^2CMOS (Page 191)**
► TTL
► CMOS+
► **None of the given options**

Question No: 2 (Marks: 1) - Please choose one
The device shown here is most likely a



► Comparator
► **Multiplexer** **click here for detail**
► Demultiplexer
► Parity generator

Question No: 3 (Marks: 1) - Please choose one
If“1110” is applied at the input of BCD-to-Decimal decoder which output pin will be activated:

► 2^{nd}
► 4^{th}

► 14^{th}

► **No output wire will be activated (Page 163)**

Question No: 4 (Marks: 1) - Please choose one

Half-Adder Logic circuit contains 2 XOR Gates

► True

► **False (Page 135)**

Question No: 5 (Marks: 1) - Please choose one

A particular Full Adder has

► **3 inputs and 2 output (Page 135)**

► 3 inputs and 3 output

► 2 inputs and 3 output

► **2 inputs and 2 output**

Question No: 6 (Marks: 1) - Please choose one

$Sum = A \oplus B \oplus C$

$CarryOut = C(A \oplus B) + AB$

are the Sum and CarryOut expression of

► Half Adder

► **Full Adder (Page 135)**

► 3-bit parralel adder

► MSI adder cicuit

Question No: 7 (Marks: 1) - Please choose one

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

► **True** click here for detail

► **False**

Question No: 8 (Marks: 1) - Please choose one

The output A < B is set to 1 when the input combinations is _____

► A=10, B=01

► A=11, B=01

► A=01, B=01

► **A=01, B=10 (Page 109)**

Question No: 9 (Marks: 1) - Please choose one

The 4-variable Karnaugh Map (K-Map) has _____cells for min or max terms

► 4

► 8

► 12

► 16 (Page 90)

Question No: 10 (Marks: 1) - Please choose one

Generally, the Power dissipation of _____devices remains constant throughout their operation.

► TTL (Page 65)
► CMOS 3.5 series
► CMOS 5 Series
► **Power dissipation of all circuits increases with time.**

Question No: 11 (Marks: 1) - Please choose one
The ecimal "8" is represented as _____using Gray-Code.

► 0011
► 1100 (page 36)
► 1000
► 1010

Question No: 12 (Marks: 1) - Please choose one

(A+B).(A+C) = _____
► B+C
► A+BC (According to rule)
► AB+C
► AC+B

Question No: 13 (Marks: 1) - Please choose one
A.(B+ C) = A.B + A.C is the expression of _____

► Demorgan's Law
► Commutative Law
► Distributive Law (Page 73)
► Associative Law

Question No: 14 (Marks: 1) - Please choose one
NOR Gate can be used to perform the operation of AND, OR and NOT Gate

► **FALSE**
► TRUE (Page 50)

Question No: 15 (Marks: 1) - Please choose one
In ANSI/IEEE Standard 754 "Mantissa" is represented by _____32-bits_____bits

► 8-bits
► 16-bits
► 32-bits (Page 24)

► 64-bits

Question No: 16 (Marks: 1) - Please choose one
Caveman number system is Base _5_____number system

► 2
► 5 (Page 11)
► 10
► 16

MIDTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
According to Demorgan's theorem:
$\overline{A + B + C}$ = _____

► A.B.C
► $A + \overline{B.C}$
► $\overline{A}.\overline{B}.\overline{C}$ (Page 74)
► $\overline{A.B} + C$

Question No: 2 (Marks: 1) - Please choose one
The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

► 2-bit
► 7-bit
► 8-bit (Page 38)
► 16-bit

Question No: 3 (Marks: 1) - Please choose one
The AND Gate performs a logical _____function

► Addition
► Subtraction
► Multiplication (Page 40)
► Division

Question No: 4 (Marks: 1) - Please choose one
NOR gate is formed by connecting _____

► OR Gate and then NOT Gate (Page 47)
► NOT Gate and then OR Gate
► AND Gate and then OR Gate

► OR Gate and then AND Gate

Question No: 5 (Marks: 1) - Please choose one
Generally, the Power dissipation of _____ devices remains constant throughout their operation.

► **TTL (Page 65)**
► CMOS 3.5 series
► CMOS 5 Series
► Power dissipation of all circuits increases with time.

Question No: 6 (Marks: 1) - Please choose one
Two 2-bit comparator circuits can be connected to form single 4-bit comparator

► **True (Page 154)**
► False

Question No: 7 (Marks: 1) - Please choose one
When the control line in tri-state buffer is high the buffer operates like a _____ gate

► AND
► OR
► **NOT (Page196)**
► XOR

Question No: 8 (Marks: 1) - Please choose one
The GAL22V10 has ____ inputs

► **22 (Page 195)**
► 10
► 44
► 20

Question No: 9 (Marks: 1) - Please choose one
The ABEL symbol for "OR" operation is

► !
► &
► **# (Page 201)**
► $

Question No: 10 (Marks: 1) - Please choose one
The OLMC of the GAL16V8 is _____ to the OLMC of the GAL22V10

► Similar
► Different
► **Similar with some enhancements (Page 207)**
► Depends on the type of PALs input size

Question No: 11 (Marks: 1) - Please choose one
All the ABEL equations must end with _____

► " . " (a dot)
► " $ " (a dollar symbol)
► **" ; " (a semicolon) (Page 201)**
► " endl " (keyword "endl")

Question No: 12 (Marks: 1) - Please choose one
The Quad Multiplexer has _____ outputs

► **4 (Page 216) rep**
► 8
► 12
► 16

Question No: 13 (Marks: 1) - Please choose one
"Sum-of-Weights" method is used _____
► **to convert from one number system to other (Page 14)**
► to encode data
► to decode data
► to convert from serial to parralel data

Question No: 14 (Marks: 1) - Please choose one
Circuits having a bubble at their outputs are considered to have an active-low output.

► **True (Page 128)**
► False

Question No: 15 (Marks: 1) - Please choose one
$(A+B)(A+\overline{B}+C)(\overline{A}+C)$ is an example of _____

► **Product of sum form (According to rule)**
► Sum of product form
► Demorgans law
► Associative law

Question No: 16 (Marks: 1) - Please choose one
Which one is true:

► **Power consumption of TTL is higher than of CMOS (Page 61)**
► Power consumption of CMOS is higher than of TTL
► Both TTL and CMOS have same power consumption
► Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

MIDTERM EXAMINATION
Spring 2009

Question No: 1 (Marks: 1) - Please choose one
In the binary number "10011" the weight of the most significant digit is ____

► **2^4 (2 raise to power 4) (Page 13)**
► 2^3 (2 raise to power 3)
► 2^0 (2 raise to power 0)
► 2^1 (2 raise to power 1)

Question No: 2 (Marks: 1) - Please choose one
An S-R latch can be implemented by using _____ gates

► AND, OR
► **NAND, NOR (Page 218-220)**
► NAND, XOR
► NOT, XOR

Question No: 3 (Marks: 1) - Please choose one
A latch has _____ stable states

► One
► **Two (Page 218)**
► Three
► Four

Question No: 4 (Marks: 1) - Please choose one
Sequential circuits have storage elements

► **True (Page 8)**
► False

Question No: 5 (Marks: 1) - Please choose one
The ABEL symbol for "XOR" operation is

► **$ (Page 210)**
► #
► !

► &

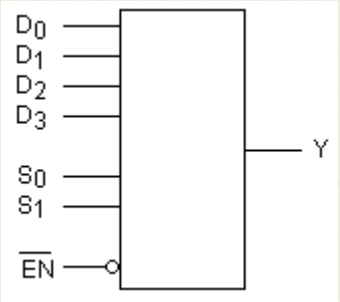
Question No: 6 (Marks: 1) - Please choose one
A Demultiplexer is not available commercially.

► **True (Page 178)**
► False

Question No: 7 (Marks: 1) - Please choose one
Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer

► **A parallel to serial converter circuit (Page 244)**
► A counter circuit
► A BCD to Decimal decoder
► A 2-to-8 bit decoder

Question No: 8 (Marks: 1) - Please choose one
The device shown here is most likely a



► Comparator
► **Multiplexer click here for detail**
► Demultiplexer
► Parity generator

Question No: 9 (Marks: 1) - Please choose one
The main use of the Multiplexer is to

► **Select data from multiple sources and to route it to a single Destination (Page 167)**
► Select data from Single source and to route it to a multiple Destinations
► Select data from Single source and to route to single destination
► Select data from multiple sources and to route to multiple destinations

Question No: 10 (Marks: 1) - Please choose one

A logic circuit with an output $X = \overline{A}\,B\,C + A\,\overline{B}$ consists of _____.

► two AND gates, two OR gates, two inverters
► three AND gates, two OR gates, one inverter
► two AND gates, one OR gate, two inverters
► two AND gates, one OR gate

Question No: 11 (Marks: 1) - Please choose one
The binary value of 1010 is converted to the product term $\overline{A}B\overline{C}D$

► True
► False

Question No: 12 (Marks: 1) - Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► 8 (Page 89)
► 12
► 16

Question No: 13 (Marks: 1) - Please choose one
Following is standard POS expression
$(A+\overline{B}+C+\overline{D})(A+\overline{B}+C+D)(A+B+\overline{C}+\overline{D})(A+B+C+\overline{D})(A+\overline{B}+\overline{C}+D)$

► True (According to logic)
► False

Question No: 14 (Marks: 1) - Please choose one
The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol'+' here represents OR Gate.

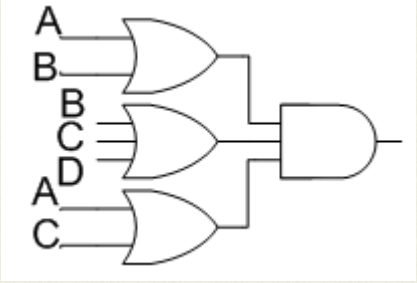
► Undefined
► One
► Zero
► 10 (binary)

Question No: 15 (Marks: 1) - Please choose one
The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

► 2-bit
► 7-bit

► **8-bit (Page 38)**
► 16-bit

Question No: 16 (Marks: 1) - Please choose one
The diagram given below represents _____



► Demorgans law
► Associative law
► **Product of sum form (According to rule)**
► Sum of product form

MIDTERM EXAMINATION
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Question No: 1 (Marks: 1) - Please choose one
Which of the number is not a representative of hexadecimal system

► 1234
► ABCD
► 1001
► **DEFH Hexa does not have H as remainder**

Question No: 2 (Marks: 1) - Please choose one
The Unsigned Binary representation can only represent positive binary numbers

► **True (Page 21)**
► False

Question No: 3 (Marks: 1) - Please choose one
The values that exceed the specified range can not be correctly represented and are considered as _____

► **Overflow (Page 23)**
► Carry
► Parity
► Sign value

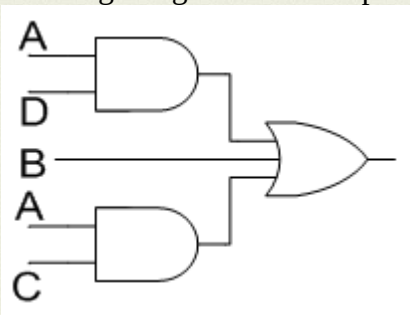
Question No: 4 (Marks: 1) - Please choose one
The 4-bit 2's complement representation of "-7" is _____

► 0111
► 1111
► **1001 (Page 21)**
► 0110

Question No: 5 (Marks: 1) - Please choose one
$\overline{A}B + \overline{A}B\overline{C} + AC$ is an example of _____

► Product of sum form
► **Sum of product form (Page 77)**
► Demorgans law
► Associative law

Question No: 6 (Marks: 1) - Please choose one
The diagram given below represents _____



► Demorgans law
► Associative law
► Product of sum form
► **Sum of product form**

Question No: 7 (Marks: 1) - Please choose one
The output of an AND gate is one when _____

► **All of the inputs are one**
► Any of the input is one
► Any of the input is zero
► All the inputs are zero

Question No: 8 (Marks: 1) - Please choose one
The 4-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► 8
► 12
► **16 (Page 90)**

Question No: 9 (Marks: 1) - Please choose one
A BCD to 7-Segment decoder has

► 3 inputs and 7 outputs
► **4 inputs and 7 outputs (Page 103)**
► 7 inputs and 3 outputs
► 7 inputs and 4 outputs

Question No: 10 (Marks: 1) - Please choose one
Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a ____ multiplexer.

► 4-input, 8-bit
► 4-input, 16-bit
► 2-input, 8-bit
► **2-input, 4-bit (Page 169)**

Question No: 11 (Marks: 1) - Please choose one
The PROM
consists of a fixed non-programmable _____ Gate array configured as a decoder.

► **AND (Page 182)**
► OR
► NOT
► XOR

Question No: 12 (Marks: 1) - Please choose one
In ABEL the variable 'A' is treated separately from variable 'a'

►

► **True (Page 201)**

► False

Question No: 13 (Marks: 1) - Please choose one

The ABEL notation equivalent to Boolean expression A+B is:

► A & B

► A ! B

► **A # B (Page 201)**

► A $ B

L-21

Question No: 14 (Marks: 1) - Please choose one

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

► **SET (Page 220)**

► RESET

► Clear

► Invalid

Question No: 15 (Marks: 1) - Please choose one

Demultiplexer has

► Single input and single outputs.

► Multiple inputs and multiple outputs.

► **Single input and multiple outputs. (Page 178)**

► Multiple inputs and single output.

Question No: 16 (Marks: 1) - Please choose one

Which one is true:

► **Power consumption of TTL is higher than of CMOS (Page 61)**

► Power consumption of CMOS is higher than of TTL

► Both TTL and CMOS have same power consumption

► Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

MIDTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one

The first Least Significant digit in decimal number system has

position 0 and weight equal to 1

position 1 and weight equal to 0

position 1 and weight equal to 10
position 0 and weight equal to 10

Question No: 2 (Marks: 1) - Please choose one
The decimal equivalent of the binary number "10011" is

19 (According to rule)
99
29
None of given options

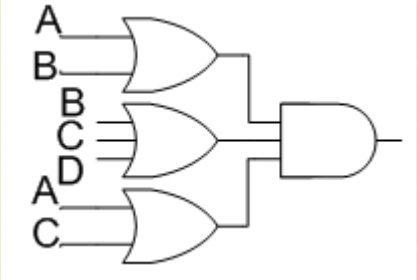
Question No: 3 (Marks: 1) - Please choose one
In ANSI/IEEE Standard 754 "Mantissa" is represented by ____32-bits_____bits

► 8-bits
► 16-bits
► 32-bits (Page 24)
► 64-bits

Question No: 4 (Marks: 1) - Please choose one
The binary value "11011" is equivalent to

1B (According to rule)
1C
1D
1E

Question No: 6 (Marks: 1) - Please choose one
The diagram given below represents



Demorgans law
Associative law
Product of sum form (According to rule)
Sum of product form

Question No: 7 (Marks: 1) - Please choose one
NOR gate is formed by connecting

OR Gate and then NOT Gate (Page 47)
NOT Gate and then OR Gate

AND Gate and then OR Gate
OR Gate and then AND Gate

Question No: 8 (Marks: 1) - Please choose one
"74ALS" stands for

Advanced Low-frequency Schottky TTL
Advanced Low-dissipation Schottky TTL
Advanced Low-Power Schottky TTL (Page 61)
Advanced Low-propagation Schottky TTL

Question No: 9 (Marks: 1) - Please choose one
An adder circuit can be used to perform subtraction operation

True (Page 146)
False

Question No: 10 (Marks: 1) - Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

2 (Page 160)
3
4
1

Question No: 11 (Marks: 1) - Please choose one
3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

True Page 161
False

Question No: 12 (Marks: 1) - Please choose one
Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a multiplexer.

2-input, 4-bit
4-input, 8-bit
4-input, 16-bit
2-input, 8-bit (Page 171)

Question No: 13 (Marks: 1) - Please choose one
The four outputs of two 4-input multiplexers, connected to form a 16-input multiplexer, are connected together through a 4-input gate

AND
OR (Page 171-172)
NAND
XOR

Question No: 14 (Marks: 1) - Please choose one
The Programmable Array Logic (PAL) has AND array and a OR array

Fixed, programmable
Programmable, fixed (Page 182)
Fixed, fixed
Programmable, programmable

Question No: 15 (Marks: 1) - Please choose one
Sequential circuits have storage elements

True (Page 218)
False

Question No: 16 (Marks: 1) - Please choose one
Demultiplexer has

Single input and single outputs.
Multiple inputs and multiple outputs.
Single input and multiple outputs. (Page 178)
Multiple inputs and single output.