CS302- DLD
(SOLVED MCQs)
FROM MIDTERM PAPERS
LECTURE (1-22)

BC190202640@vu.edu.pk
Junaidfazal08@gmail.com

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JUNAID MALIK
(0304-1659294)

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1. Which of the following is a volatile memory?

a. PROM
b. DRAM
c. EPROM
d. EEPROM

2. _____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

a. Combinational Input/output
b. Combinational Output
c. Combinational Input AL-JUNAID INSTITUTE OF GROUP
d. Programmable polarity

3. The AND Gate performs a logical _____ function.

a. Addition
b. Subtraction
c. Multiplication
d. Division AL-JUNAID INSTITUTE OF GROUP

4. The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacent 1s are detected in the input, the output is set to high.

a. 2
b. 4
c. 1 Not answer
d. 0

5. In the keyboard encoder, how many times per second does the ring counter scan the key board?

a. 600 scans/second
b. 625 scans/second
c. 650 scans/second
d. 700 scans/second

6. The FAST Model Page Access allows _____ memory read and access times when reading successive data values stored in consecutive locations on the same row.

a. Slow
b. Faster
c. Medium
d. Modern

7. GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.

a. column, row
b. row, column
c. column, column
d. row, row

8. Which of the following Output Equations determines the output of the State Machine?

a. MIN = Q0Q1
b. MAX = Q0Q1EN
c. MIN = Q0Q1EN
d. MAX = Q1EN

9. The maximum value, represented by a single hexadecimal digit is _____.

a. "E"
b. "F"
c. "G"
d. "H"

10. If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.

a. 0
b. 1

11. The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information.

a. Low
b. High
c. Medium
d. Hot

12. DE Morgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.

a. Negative-OR, Negative-AND
b. Negative-AND, Positive-OR
c. Positive-OR, Negative-AND
d. Positive-OR, Positive-AND

13. Two signals _____ and _____ provide the timing inputs to the State Machine.

a. NSSR and EWSR
b. LTIME and STIME
c. PTIME and QTIME
d. NSGrn and NSYel

14. The 74HC163 is a 4-bit Synchronous counter, it has _____ data output pins.

a. 2
b. 4
c. 6
d. 8

15. PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.

a. PLAs
b. PALs
c. PLDs AL-JUNAID INSTITUTE OF GROUP
d. EPROM

16. The CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.

a. CONSTATE
b. FLOOR
c. MOTION
d. OPEN

17. Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using _____.

a. Shift Registers
b. Circular Buffers
c. Ring Buffers
d. Reduce Registers

18. The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.

a. Sequential
b. Asynchronous
c. Synchronous AL-JUNAID INSTITUTE OF GROUP
d. Combinational

19. For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____.

a. 111
b. 110
c. 010
d. None of the given

20. The _____ gate and _____ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.

a. AND, NOR
b. AND, NOT
c. AND, OR

d. XOR, NAND

21. The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to _____ location(s) using a single address.

a. One
b. Two
c. Three
d. Four

22. In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.

a. NOR, NAND
b. NAND, NOR
c. NOR, NOR
d. NAND, NAND

23. Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms (minterms) with an 8-input OR gate.

a. 8 OR
b. 8 AND
c. 8 XOR
d. 8 NOR

24. 8-bit parallel data can be converted into serial data by using _____ multiplexer.

a. 4-to-2

b. 8-to-1
c. 4-to-4
d. 8-to-4

25. The _____ input overrides the _____ input.

1. Asynchronous, synchronous
2. Synchronous, asynchronous
3. Preset input (PRE), Clear input (CLR)
4. Clear input (CLR), Preset input (PRE)

26. A SOP expression can be implemented by an _____ combination of gates.

1. OR-XOR
2. AND-NAND
3. AND-OR
4. XOR-NOR

27. The 64-cell array organized as 8 x 8 cell array is considered

1. as an 64 byte memory
2. as a 16 byte memory
3. as an 8 byte memory
4. as an 4 byte memory

28. The terminal count of a 4-bit binary counter in the UP mode is _____.

1. 1100
2. 0011
3. 1111
4. 0000

29. A 3-variable karnaugh map has

1. eight cells
2. three cells
3. sixteen cells
4. four cells

30. An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting _____.

1. Q output of all flip-flops to clock input of next flip-flops
2. Q' output of all flip-flops to clock input of next flip-flops
3. Q output of all flip-flops to J input of next flip-flops
4. Q' output of all flip-flops to K input of next flip-flops

31. Memory is arranged in _____.

1. linear fashion
2. two-dimensional manner
3. three-dimensional manner
4. random fashion

32. If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result.

1. 1001 AL-JUNAID INSTITUTE OF GROUP
2. 0110
3. 1111
4. 1100

33. Subtractors also have output to check if 1 has been _____.

1. Primed
2. Shifted
3. Complemented
4. Borrowed

34. The Test Vector definition defines the test vectors for all the three counter inputs and _____ counter output/outputs.

1. One
2. Two
3. Three
4. Four

35. A multiplexer with a register circuit converts

1. Serial data to parallel
2. Parallel data to serial
3. Serial data to serial
4. Parallel data to parallel

36. A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

1. True
2. False

37. The n flip-flops store _____ states.

1. 1
2. 2^n
3. 0
4. 2^(n+1)

38. The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.

1. two
2. four
3. eight
4. sixteen

39. Why demultiplexer is called a data distributor?

1. The input will be distributed to one of the outputs
2. The input will be selected for the output
3. The output will be distributed to one of the inputs
4. Single input to Single Output

40. When the transmission line is idle in an asynchronous transmission

1. It is set to logic low
2. It is set to logic high
3. It remains in previous state
4. State of transmission line is not used to start transmission

41. UVERPROM is stands for

1. Ultra-Variant
2. Ultra-Vibrant
3. Ultra-Voilet
4. Ultra-Visible

42. In memory write cycle, the time for which the WE signal remains active is known as the _____.

1. Write address setup
2. Write pulse width AL-JUNAID INSTITUTE OF GROUP
3. Write delay width
4. Write data time

43. The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.

1. NOT

2. AND
3. OR
4. XOR

44. PALs tend to execute _____ logic.

1. SPD
2. SOP
3. SAC
4. SAP

45. The ROM used by a computer is relatively _____ as it stores few byres of code used to Boot the Computer system on power up.

1. Small
2. Large
3. Heavy
4. High

46. Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?

1. $\overline{CS}$
2. $\overline{WE}$
3. W
4. OE

47. You have to choose suitable option when your timer will reset by considering this given code:
TRSTATE.CLK = clk;
TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);

1. NSY2 or EWY2
2. NSSR or TMRST

3. EWSR or NSRED
4. EWRed or EWYel

48. A NOR based S-R latch is implemented using _____ gates instead of _____ gates.

1. XOR, NAND
2. NOR, XOR
3. NOR, NAND
4. OR, XOR

49. Implementation of Latch is required almost _____ transistor.

1. Two
2. Four
3. Six
4. Eight

50. In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in _____ when Distributed refresh is used.

1. 4.8 microsec
2. 5.9 microsec
3. 7.8 microsec
4. 5.5 microsec

51. The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.

1. AND
2. NAND
3. OR

4. NOT

52. For a Standard SOP expression, a _____ is placed in the cell corresponding to the product term (Minterm) present in the expression.

1. 0
2. 1
3. x (don't care condition)
4. Any of given option depending on SOP term

53. Select the mode of programming in which GAL16V8 can be programmed:

1. Simple Mode
2. Complex Mode
3. Registered Mode
4. All of the given

54. Divide-by-32 counter can be achieved by using

1. Flip-Flop and DIV 10
2. Flip-Flop and DIV 16
3. Flip-Flop and DIV 32
4. DIV 16 and DIV 32

55. The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.

1. REQ0
2. OPEN
3. REQ1 AL-JUNAID INSTITUTE OF GROUP
4. FLOOR1

56. Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be _____.

1. Zero
2. One
3. Undefined
4. No output as input is invalid

57. A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:

1. 0001
2. 1000
3. 1110
4. 1111

58. Adding two octal numbers "36" and "71" result in _____.

1. 213
2. 123
3. 127
4. 345

59. The ABEL Input file can use a _____ instead of the equation to specify the Boolean expressions.

1. Truth Table
2. State Diagram
3. Karnaugh Map
4. Logic Circuit

60. The domain of the expression AB'CD + AB' + C'D + B is

1. A and D

2. B only
3. A, B, C and D
4. None of the given

61. If the number of samples that are collected is reduced by half, the reconstructed signal will be _____ from/to the original.

1. Different
2. Same
3. Equal
4. Opposite

62. In DRAM read cycle R /W^- signal is activated to read data which is made available on the _____ data line.

1. D(IN)
2. D(OUT)
3. D(AB)
4. D(INT)

63. In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

1. True
2. False

64. Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.

1. RAMAL-JUNAID INSTITUTE OF GROUP
2. ROM
3. PPROM
4. Flash Memory

65. As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack _____.

1. Bottom
2. Top
3. Down
4. Vertex

66. Which one flip-flop has an invalid output state?

1. T
2. JK
3. SR
4. D

67. The output of a NAND gate is _____ when all the inputs are one.

1. Zero
2. One
3. Available
4. Not available

68. The Transition table is very similar to the _____ table.

1. Truth
2. State
3. Transition
4. None of the given

69. Consider the sum of weight method for converting decimal into binary value, _____ is the highest weight for 411.

1. 64

2. 128
3. 256
4. 512

70. Canonical form is a unique way of representing _____.

1. SOP
2. Minterm
3. Boolean Expression
4. POS

71. _____ Counters as the name indicates are not triggered simultaneously.

1. Asynchronous
2. Synchronous
3. Positive-Edge triggered
4. Negative-Edge triggered

72. Cin is part of _____ Adder.

1. Half
2. Full
3. Single
4. Double

73. Flash memory Operation are classified into _____ different operation.

1. Two
2. Three
3. Four
4. Five

1. A Product term is 0 when_____

a. Any one literal is 0

b. Any of the literals is 1

c. At least two literals are 1

d. All the literals are 1

2. In 8-inpit multiplexer, the two outputs are connected through a/an___gate.

a. AND

5. **OR** AL-JUNAID INSTITUTE OF GROUP

b. NOT

c. NOR

3. _____ Device dissipate varying amount of power depending upon the frequency of operation.

a. TTL

b. CMOS

c. Storage

d. Peripheral

4. Boolean Addition operation is performed by a(an)___ gate.

a. AND

b. OR

c. XOR

d. NAND

5. A SOP expression can be implemented by an_____ combination of gates.

a. OR-XOR

b. AND-AND

c. AND-OR

d. XOR-NOR

6. The maximum decimal number that can be represented using the 64-bit unsigned representation is _____.

a. 2^63

b. (2^64)-1

c. (2^64+

d. 2^64

7. In 16-bit ALU, The G output is activated if the 4-bi unit generate a Carry ____ irrespective of Carry___.

a. In,In

b. In,Out

c. Out,In

d. Out,Out

8. A standard POS from has ____ ters that have all the variables in the domain of the expression.

a. Sum

b. Product

c. Min

d. Composite

9. In Cascading Priority Encoders, the EO output is connected to the EI input of the encoder which handles_____.

a. Lower priority outputs

b. Higher priority outputs

c. Lower priority inputs

d. Higher priority inputs

10. Which of the following is the example of comparater?

a. OR

b. AND

c. XOR

d. XNOR

11. IN CMOS 5 Volt series, Input voltage of Logic high signal (VIH) with a ranges from ____ to ____ volts.

a. 4,5,5

b. 0 ,5

c. 0,3,5

d. 3,5,5

12. The Adjacent 1 S Detector accepts 4-bits input. If ____ adjacent 1S are detected in the input, the output is set to high.

a. 2

b. 4

c. 1

d. 0

13. DE Morgan's two theorems prove the equivalency of the NAND and

_____ gates and the NOR and _____ gates respectively.

a. Negative-OR, Negative-AND

b. Negative-AND, Negative-OR

c. positive-OR, Negative-AND

d. positive-AND, Negative-OR

14. Adding two octal numbers "36 and 71" result in ____.

a. 213

b. 123

c. 127

d. 345

15. Any of the _____ forms of the Karnaugh Map can be used to simplify Boolean expressions

a. Three

b. Four

c. Two

d. Five

16. Quine-McCuskey and K-Map methods are used for _____ of Boolean expression.

a. Multiplication

b. Addition

6. **Simplification** AL-JUNAID INSTITUTE OF GROUP

c. Subtraction

17. The number "1259" may belong to ____ number system.

a. Binary number system

b. Octal or Decimal system

c. Decimal or Hexadecimal system

d. Binary or Hexadecimal system

18. The series of TTL chips are characterized by their____.

a. Switching Speed only

b. Power Dissipation only

c. Both

d. None of these

19. All ABEL statements must end with_____.

a. :

b. ,

c. ;

d. “

20. In sequential circuit memory elements are connected with____.

a. Logical circuit

b. Clock

c. Feedback path

d. External Event

21. In the 32-bit Single Precision Floating Point format, the exponent value____ is reserved to represent infinity exponents.

a. 98

b. 99

c. 255

d. 256

22. The _____ output has the output of the OR gate connected through an XOR gate to the tri-state buffer.

a. Combinational

b. Combinational input/

c. PLA

d. None Programmed Polarity

23. The limitation in implementation of parallel binary address is known as_____.

a. Delay

b. Carry propagation

c. Carry input

d. Carry output

24. The Gray code is different form the unsigned binary code

because___.

a. Successive value of Gray code by only one bit

b. Gray code is positional code

c. Gray code not support negative values

d. Gray code ranges from “o” to “9”

25. Removing the NOT gate at the output of the NOR gate result in an____.

7. **OR gate** AL-JUNAID INSTITUTE OF GROUP

a. NAND gate

b. AND gate

c. NOT gate

26. Portable devices that run on batteries use___ circuit that have low power dissipation.

a. Series

b. Integrated

c. Parallel

d. Electric

27. The domain of the expression AB'CD+B is

a. A and D

b. A,B,C and D

c. C and D only

d. B only

28. _____ is a single input gate

a. AND

b. OR

c. NOT

d. XOR

29. To represent in digital value, the number of digit (0s and 1s) that represent a quantity is ____ to the range of values that are to be

represented.

a. Equal

b. Greater

c. Lesser

d. Not equal

30. BCD code of 16 is____.

a. 10001

b. 00010001

c. 00010111

d. 01110001

31. To determine the seven expressions for each of the seven outputs in 7-segment display, seven____ variable Karnaugh Maps are used.

8. **3** AL-JUNAID INSTITUTE OF GROUP

a. 4

b. 5

c. 2

32. In Odd parity generator circuit which gate is used to detect parity errors?

a. OR

b. NOR

c. XOR

d. AND

33. A 3-variable Karnaugh map has

a. Eight cells

b. Three cells

c. Sixteen cells

d. Four cells

34. The measurable values generally change over a

a. Specified period

b. Discrete range

c. Time

d. Continuous range

35. ____ uses E2CMOS technology which is Electrically Erasable CMOS

instead of Bipolar technology and fusible links.

a. PAL

b. GAL

c. PLA

d. PROM

36. When the number 29 is represent on 7-segment display, which BCD input is represented on LSD display unit?

a. 1000

b. 1001

c. 1010

d. 1100

37. How many of enable inputs is(are) active-low in 74xx138 3 to 8 Decorder?

a. One

b. Two

c. Three

d. Four

38. The simplified expression using either of the two K-maps are_____.

a. Similar

b. Different

c. Identical

d. None-identical

39. Which of the following expression in the product of sums form?

a. (A + B)(C+D)

b. (AB)(CD)

AL-JUNAID INSTITUTE OF GROUP

c. AB(CD)

d. AB+CD

40. CMOS technology is characterized by low power dissipation with____ switching speeds.

a. Slow

b. Fast

c. Average

d. Medium

41. GAL Two 2-bit comparator circuits can be connected to form single 4-bit comparator

a. True

b. False

42. High level Noise Margins (VNH) of CMOS 5 volt series circuits is

_____

a. 0.2 V

b. 0.5 V

c. 0.9 V

d. 3.3 V

43. The output of the expression F=A+B+C will be Logic _____

when A=0, B=1, C=1. the symbol"+" here represents OR Gate

b. One

a. Undefined

c. Zero

d. 10(binary)

44. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

a. SET

b. RESET

c. Clear

d. Invalid

45. 3.3 v CMOS series is characterized by _____ and

_____as compared to the 5 v CMOS series.

a. Low switching speeds, high power dissipation

b. Fast switching speeds, high power dissipation

c. Fast switching speeds, very low power dissipation (page61)

d. Low switching speeds, very low power dissipation

46. The binary value “1010110” is equivalent to decimal _____

a. 86

b. 87

c. 88

d. 89

47. The _____ Encoder is used as a keypad encoder.

a. 2-to-8 encoder

b. 4-to-16 encoder

c. BCD-to-Decimal

d. Decimal-to-BCD Priority

48. How many data select lines are required for selecting eight inputs?

a. 1

b. 2

c. 3

d. 4

49. The Quad Multiplexer has _____ outputs

a. 4

b. 8

c. 12

d. 16

50. Demultiplexer has

a. Single input and single outputs.
b. Multiple inputs and multiple outputs.
c. Single input and multiple outputs.
d. Multiple inputs and single output.

51. The expression _____ is an example of Commutative Law for Multiplication.

a. AB+C = A+BC

b. A(B+C) = B(A+C)

c. AB=BA

d. A+B=B+A

52. The look-ahead carry circuits_____

a. Add a 1 to complemented inputs

b. Reduce propagation delay

c. Increase ripple delay

d. Determine sign and magnitude

53. What is the output expression of segment 'b' implementation in BCD to 7-segment decoder?

a. B+C'D'+CD

b. B'+C'D'+CD

c. B+C'D'+C'D

d. B'+C'D'+CD'

54. 2-input, 8-bit Multiplexer, by setting the S input to logic_____

the____ inputs of both the multiplexers are selected.

a. Low

b. High, B

c. Low, C

d. Low, C

55. The maximum decimal number that can be represented using the

64-bit unsigned representation_____

a. 2^63

b. (2^64)-1

c. (2^64)+1

d. 2^64

56. When two or more products terms are assumed by Boolean addition, the result is a ____

a. POS

b. SOP

c. Boolean

d. Simplified

57. Tri-State Buffer is a ___ gate with a control line that disconnects the

a. OR

b. AND

c. NAND

d. NOT

58. The 4-bits 2's complement representation of "7" is _____

a. 0111
b. 1111
c. 1001
d. 0110

59. _____and _____ are the steps of the Quine-McCluskey.

a. Draw a table and make groups

b. Write binary codes and write SOP

c. Find prime implicants and select minimal set of the prime implicants.

d. None of the given

60. The binary number 1011,101 has an Integer part represented by_____ and a fraction part ___ separated by a decimal point.

a. 1011,101

b. 101,1011

c. 101,1101

d. 10111,11

61. Subtractors also have output to check if 1 has been _____

a. Primed

b. Shifted

c. Complemented

d. Borrowed

62.CMOS technology is characterized by low power dissipation with_____ switching speeds.

a. Slow

b. Fast

c. Average

d. Medium

63. The _____ description is used to simulate the logic circuit

and verify its operation.

a. Test file

b. Declaration

c. Logic

d. Test vector

64. How many outputs can an integrated circuit comparator have?

a. One

b. Two

c. Three

d. Four

65. Which of the following is not the correct method of grouping?

a. Along adjacent columns

b. On comers

c. Diagonally

d. Along adjacent rows

66. The output of the expression F=A.B.C will be logic _____

when A=1,B=0, C=1.

a. Undefined

b. One

c. Zero

d. No output as input is valid

67. The _____ gate and ___ gate implementation connected at the B

input of the 4-bit Adder is used to allow complemented or Un-Complemented B input to be connected to the Adder input.

a. AND,NOR

b. AND,NOT

c. AND,OR

d. XOR,NAND

68. In the 32-bit Single Precision Floating point format, the exponent value _____ is reserved infinity exponent.

a. 98

b. 99

c. 255

d. 256

69. The Boolean expression (AB'CS') is used

a. A sum term

b. A product term

c. A literal term

d. A max term

70. The product of an XOR gate is zero(0), when _____

I. All the inputs are zero

II. Any of the inputs is zero

III. An of the inputs is one IV. All the inputs are one

a. I only

b. IV only

c. I and IV only

d. II and III

71. _____ methods are used to Convert Decimal fractions to Binary.

a. 1
b. 2
c. 3
d. 4

72. To display the number___ the BCD number 0010 representing the MSD is applied at the inputs of the BCD to 7-segment display circuit connected to the MSD &-Segment Display digit

a. 19
b. 29
c. 39
d. 49

73. The look-ahead carry circuits_____

a. Add a 1 to complemented inputs
b. Reduce propagation delay
c. Increase ripple delay
d. Determine sign and magnitude.

74. If two numbers in BCD representation generate an invalid BCD number then the binary __ is added to the result

a. 1001

b. 0110

c. 1111

d. 1100

75. Both the multiplexers are selected simultaneously when _____

is set to logic _____ in 2-inputs, 8-bit Multiplexer.

a. G, Low

b. G, High

c. S, Slow

d. S, High

76. Function labels required to represent the input/output combinations for each segment in 7-segment display

a. 5

b. 7

c. 8

d. 10

77. Multiplexers are also known as _____

a. Date distributors

b. Data selectors

c. Data manipulators

d. Data setters

78. The PLA can be programmed to give and output of constant

_____ or _____

a. 0,1

b. 1,2

c. 2,3

d. 0,0

79. Cin is part of _____ Adder.

a. Half

b. Full

c. Single

d. Double

80. The look-ahead carry circuits_____

a. Add 1 to complemented inputs

b. Reduce propagation delay

c. Increase ripple delay

d. Determine sign and magnitude

81. Which of the following gates has the outputs 1 if and only if at last one input is 1?

a. AND

b. NOR

c. NAND

d. OR

82. A sop expression can be implemented by on ___ combination of gates.

a. OR-XOR

b. AND-NAND

c. AND-OR

d. XOR-NOR

83. The carry, instead of rippling through the 4-bits of the individual ALU circuit, has to propagate through ___ ALU units in 16-bit ALU.

a. Two

b. Four

d. 9

91. Digital circuits operates with_____ voltage value(s)

a. 1

b. 2

c. 3

d. 4

92. Which of the following is the octal equivalent of 28 decimal numbers?

a. 31

b. 32

c. 33

d. 34

93. In cascading Priority Encoders, the EO output is connected to the EI of the encoder which handles_____

a. Lower priority outputs

b. Higher priority outputs

c. Lower priority inputs

d. Higher priority inputs

94. To determine the seven expressions for each of the seven outputs in

7-segment display, seven _____ variable Karnaugh maps are used.

a. 3

b. 4

c. 5

d. 2

95. The output of a NAND Gate is ____ when all the inputs are one.

a. Zero

b. One

c. Available

d. Not available

96. The _____ is the slowest and consumes more power.

a. Standard TTL

b. Schottky TTL

c. Advanced Schokottky TTL

d. Low-Power Schottky TTL

97. The between expression X-AB+CD represents

a. Two Ors ANDed together

b. A 4-input AND gate

c. Two ANDs ORed together

d. An eclusive-OR

98. The expression F-A+B+C describes the operation of three bits___ Gate.

a. OR

b. AND

c. NOT

d. NAND

99. Which one of the following is NOT a valid rule of Boolean Algebra?

a. A+1=1

b. A=A'

c. AA=A

d. A+0=A

100. A 5-Variable Karnaugh map has

a. Sixteen cells

b. Thirty two cells

c. Sixty four cells

d. None of these

101. _____ is invalid number of cells in a single group formed by the adjacent cells K-map

a. 2

b. 8

c. 12

d. 16

102. In 32-bit Single –Precision floating point format representation the range of exponent value is from _____to _____

a. +127 to -126

b. +127 to -254

c. +128 to -254

d. +256 to -255

103. _____ has the fastest switching speed and low power requirements

a. Advanced low power schottky

b. Fast TTL

c. Standard TTL

d. Schottky TTL

104. A standard sum term is equal to zero for only one combination of _____ values.

a. Literal
b. Maximum
c. Variable
d. None

105. NOR gate is form by connecting _____

a. OR Gate and then NOT Gate
b. NOT Gate and then OR Gate
c. AND Gate and then OR Gate
d. OR Gate and then AND Gate

106. The output of an AND gate with three inputs, A, B, and C, is HIGH when _____.

a. A=1, B=1,C=0
b. A=1, B=1, C=1
c. A=1, B=0, C=1
d. A=0, B=1, C=1

107. The output of an exclusive-OR gate is HIGH if _____.

a. All Input or Unequal
b. All inputs are DON'T care
c. All inputs are HIGH
d. All inputs are low

108. On a Karnaugh map, grouping the 0s produces____

a. A POS expression
b. A SOP expression
c. AND-OR Logic
d. NAND-NOR Logic

109. The simplified expression is presented in a _____ format.

a. Function Table
b. Logic Table
c. Truth Table
d. Data Table

110. The boolean expression X = AB + CD represents.

a. two ors anded together
b. a 4-input and gate
c. two ands ored together
d. an exclusive- or

111. Which of the following is the example of comparator?

a. SPD
b. SOP
c. SAC
d. SAP

112. The 4-variable K-Map has _____ rows and _____ columns of cells.

a. 4,4
b. 2,2
c. 3,3
d. 6,6

113. The switching speed of CMOS is now _____.

a. competitive with TTL
b. three times that of TTL
c. slower than TTL
d. twice that of TTL

114. Gray code of 8 is:

a. 1100
b. 1000
c. 0100
d. 0000

115. The 4-variable Karnaugh Map (K-Map) has _____ cells for min or max terms.
a. 12
b. 16
c. 8
d. 4

116. Which circuit is used in 7-segments display?
a. BCD Code
b. Excess Code
c. Binary code
d. Gray code

117. The 4-bit 2's complement representation of "-7" is ___
a. 0111
b. 1111
c. 1001
d. 0110

118. _____ integrated circuit technology can easily be damaged due to accumulated static charge.

119. Don't care conditions are marked as _____ in the output column of the function table

a. A

b. 1
c. X
d. 0

120. The digital circuits operate with which combination of values given below?
a. 0 volts, 0 volts
b. +5 volts, 0 volts
c. -5 volts, 0 volts
d. -5 volts, 0 volts

121. In 15 digit decimal floating point format, the biased exponent value _____ can be used to represent the number zero whatever the value of the mantissa.
a. 00
b. 000
c. 0
d. 0000

122. The ANSI/IEEE Standard 754 defines a _____Single-Precision Floating Point format for binary numbers.
a. 16-bit
b. 32-bit
c. 64-bit
d. 8-bit

123. A function represented by an expression in _____ form can be readily programmed.
a. Boolean
b. Standard POS
c. Standard SOP

d. Non-standard SOP

124. _____ is an essential part of sequential circuit.
   a. Clock
   b. Memory element
   c. JK flip flop
   d. Multiplexer

125. The OR Gate performs a Boolean _____ function
   a. Multiplication
   b. Addition
   c. Subtraction
   d. Division

126. The values that exceed the specified range can not be correctly represented and are considered as _____
   a. Carry
   b. Parity
   c. Overflow
   d. Sign Value

127. which of the following is the hexadecimal equivalent of 28?
   a. 1A
   b. 1C
   c. 1B
   d. 1D

128. To implement the decoder circuit, having _____ inputs and _____outputs, function tables have to be drawn which represent the output status of each output line for all combinations of inputs.

a. 3 and 8
b. 4 and 7
c. 1 and 9
d. 5 and 6

129. The _____ Gate is used in applications where the output signal is a 1 when any one input is a 1.
a. OR
b. XOR
c. NOT
d. AND

130. "1101" in signed representation is equivalent to _____
a. 13
b. -5
c. 10
d. -10

131. The three fundamental gates are _____
a. NOT, OR, AND
b. AND, NANAD, XOR
c. NOT, NOR, XOR
d. OR, AND, NAND

132. In a 4-variable K-map, a 2-variable product term is produced by
a. A 4-cell group of 0s
b. A 8-cell group of 1s
c. A 4-cell group of 1s
d. a 2-cell group of 1s

133. _____ function tables are required to represent the input/output combinations for each segment in 7-segment display.
   a. 5
   b. 7
   c. 10
   d. 8

134. Suppose we want to transmit the data “10001101”, and an “Even-Parity” bit scheme is used to detect errors, the parity bit added to this data will be ____
   a. “0”
   b. “1”
   c. Both “0” and “1”
   d. Parity bit is not needed in this case

135. A variable can have a _____ value.
   a. 0
   b. 0 or 1
   c. 0 and 1
   d. 1

136. Which one is true?
   a. Power consumption of both CMOS and TTL depends on no. of gates in circuit.
   b. Power consumption of CMOS is higher than TTL
   c. Power consumption of TTL is higher than CMOS
   d. Both TTL and CMOS have same power consumption

137. XOR is an abbreviation of_____.
   a. Inclusive-OR
   b. Extended-OR

c. Extendable-NOR
d. Exclusive-OR

138.

Inputs		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

This function table represents _____ Gate.

a. NANAD
b. AND
c. OR
d. XOR

139. Which of the following is the example of comparator?

a. AND
b. XOR
c. OR
d. XNOR

140. The output of an AND gate is one when _____.

a. Both inputs are 1

141. The decimal value “20” is equivalent to binary value _____.

a. 10011
b. 11001

c. 00101
d. 10100

142. Boolean algebra is the _____ of Digital Systems.
a. Science
b. Equation
c. Expression
d. Mathematics

143. In 15 digit decimal floating point format, the biased exponent value _____ can be used to represent the number infinity whatever the value of mantissa.
a. 99
b. 98
c. 256
d. 255

144. The digital circuits operate with which combination of values given below?
a. A=0, B=0, C=1, D=1
b. A=1, B=0, C=0, D=1
c. A=0, B=1, C=1, D=0
d. A=1, B=1, C=,0, D=0

145. A___is converted into a standard POS by using the rule AA=0.
a. No-standard SOP
b. Non-standard POS
c. Simplified POS
d. Simplified SOP

146. (A+B).(A+C)=_____
a. A+BC

b. B+C
c. AC+B
d. AB+C

147. The PLDs are implemented having a general purpose structure based on____arrays
a. AND+NANAD
b. AND-OR
c. XOR-NOR
d. OR-XOR

148. Each octal Number didgit can represent a___binary Number.
a. 2-bit
b. 3-bit
c. 4-bit
d. 7-bit

149. The output of any CMOS___series logic gate can be at logic high “1” or logic low “0”.
a. 3.3 and 5 volt
b. 5+ volt
c. 4.5 volt
d. 5 volt

150. A standard SOP from has___terms that have all the variables in the domain of the expression.
a. Sum
b. Max
c. Composite
d. Product

151. In caveman number system the value “2” is represented by Symbol____.

a. “>”
b. “!”
c. “^”
d. “&”

152. The expression F=A.B.C describes the Operating of three bits___Gate.

a. NAND
b. NOT
c. OR
d. AND

153. In CMOS 5 volts series, input voltage of logic high signal (VH) with a range from___to__volts.

a. 0, 3.5
b. 4.5,5
c. 0,5
d. 3.5,5

154. TTL based devices work with a DC supply of___volts.

a. +5
b. 3.3
c. +10
d. +3

155. A function represented by an expression in___ from can be readily programmed.

a. Non-standard SOP

b. Standard SOP
c. Boolean
d. Standard POS

156. Sum term (Max term) is implemented using___gates.
a. NOT
b. AND
c. NOR
d. OR

157. A SOP expression is equal to 1 _____
a. All the variables in domain of expression are present
b. At least one variable in domain of expression is present. ►
c. When one or more product terms in the expression are equal to 0.
d. **When one or more product terms in the expression are equal to 1. (Page 86)**

158. The output A < B is set to 1 when the input combinations is _____
a. A=10, B=01
b. A=11, B=01
c. A=01, B=01
d. **A=01, B=10 (Page 109**

159. If we multiply “723” and “34” by representing them in floating point notation i.e. by first, converting them in floating point representation and then multiplying them, the value of mantissa of result will be _____
a. **24.582**
b. 2.4582

c. 24582

160. "Sum-of-Weights" method is used _____

a. **to convert from one number system to other (Page 14)**

b. to encode data

c. to decode data

d. to convert from serial to parralel data

161. The maximum number that can be represented using unsigned octal system is _____

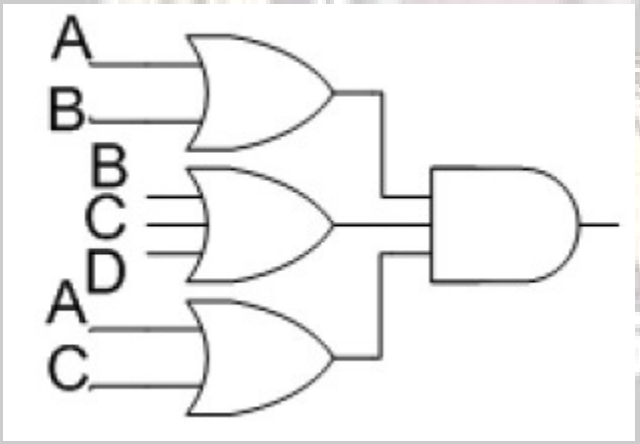
a. 1

b. **7 (Page 31)**

c. 9

d. 16

162. The diagram given below represents _____



a. Demorgans law

b. Associative law

c. **Product of sum form (According to rule of theorem)**

d. Sum of product form

163. The range of Excess-8 code is from _____ to _____
   a. **+7 to -8 (Page 34)**
   b. +8 to -7
   c. +9 to -8
   d. -9 to +8

164. A non-standard POS is converted into a standard POS by using the rule _____
   a. $A+\bar{A}=1$
   b. $A\bar{A}=0$
   c. $1+A=1$ **(Page 85)**
   d. A+B = B+A

165. The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms
   a. 4
   b. **8 (Page 89)**
   c. 12
   d. 16

166. The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?
   a. **A > B = 1, A < B = 0, A < B = 1**
   b. A > B = 0, A < B = 1, A = B = 0
   c. **A > B = 1, A < B = 0, A = B = 0 (Page 109)**
   d. A > B = 0, A < B = 1, A = B = 1

167. A particular Full Adder has
   a. **3 inputs and 2 output (Page 135)**
   b. 3 inputs and 3 output
   c. 2 inputs and 3 output
   d. 2 inputs and 2 output 0

168. The function to be performed by the processor is selected by set of inputs known as _____
   a. **Function Select Inputs (Page 147)**
   b. MicroOperation selectors
   c. OPCODE Selectors

d. None of given option

169. For a 3-to-8 decoder how many 2-to-4 decoders will be required?
   a. **2 (Page 160)**
   b. 1
   c. 3
   d. 4

170. GAL is an acronym for _____.
   a. Giant Array Logic
   b. **General Array Logic (Page 183)**
   c. Generic Array Logic
   d. Generic Analysis Logic

171. A.(B.C) = (A.B).C is an expression of _____
   a. Demorgan"s Law
   b. Distributive Law
   c. Commutative Law
   d. **Associative Law (Page 72)**

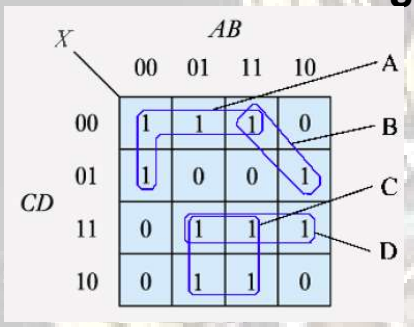
172. 2's complement of any binary number can be calculated by
   a. adding 1's complement twice
   b. **adding 1 to 1's complement (Page 144)**
   c. subtracting 1 from 1's complement.
   d. calculating 1's complement and inverting Most significant bit

173. Tri-State Buffer is basically a/an _____ gate.
   a. AND
   b. OR
   c. NOT
   d. **XOR (Page 186)**

174. **An important application of AND Gate is its use in counter circuit**
   a. **True (Page 281)**
   b. False

175. **A SOP expression having a domain of 3 variables will have a truth table having ____ combinations of inputs and corresponding output values.**
   a. 2
   b. 4
   c. **8 (According to rule)**
   d. 16

176. **A BCD to 7-Segment decoder has**

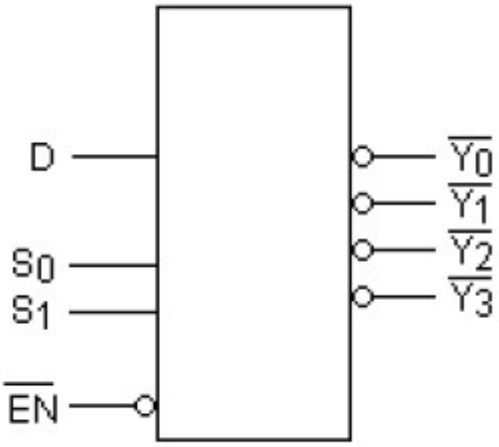


   a. 3 inputs and 7 outputs
   b. **4 inputs and 7 outputs (Page 103)**
   c. 7 inputs and 3 outputs
   d. inputs and 4 outputs

177. In the Karnaugh map shown above, which of the loops shown represents a legal grouping?
   a. A
   b. B
   c. C
   d. D

178. 3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions
   a. **True (Page 160)**
   b. False

179. **The device shown here is most likely a _____**



a. Comparator
b. Multiplexer
c. **Demultiplexer**
d. Parity generator

180. **The GAL22V10 has ____**
a. **22 (Page 195)**
b. 10
c. 44
d. 20

181. A latch retains the state unless
a. Power is turned off
b. **Input is changed (page 218)**
c. Output is changed
d. Clock pulse is changed

182. **Consider a circuit consisting of two consecutive NOT gates, the entire circuit belongs to a CMOS 5 Volt series, if certain voltage is applied on the input, the output voltage of Logic high signal (VoH) will be in the range of _____ volts.**
a. 4 to 4.5
b. **4.5 to 5**
c. 0 to 4.5

d. 0 to 3.5

183. Which of the number is not a representative of hexadecimal system
   a. 1234
   b. ABCD
   c. 1001
   d. **DEHF Hexa does not have H as remainder**

184. GALcan be reprogrammed because instead of fuses _____logic is used in it
   a. **E2CMOS (Page 191)**
   b. TTL
   c. CMOS+
   d. **None of the given option**

185. If"1110" is applied at the input of BCD-to-Decimal decoder which output pin will be activated:
   a. 2nd
   b. 4th
   c. 14th
   d. **No output wire will be activated (Page 163)**

186. Half-Adder Logic circuit contains 2 XOR Gates
   a. True
   b. **False (Page 135)**

187. A particular Full Adder has
   a. **3 inputs and 2 output (Page 135)**
   b. 3 inputs and 3 output
   c. 2 inputs and 3 output
   d. **2 inputs and 2 output**

188. A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.
   a. **True**
   b. **False**

189. Generally, the Power dissipation of devices remains constant throughout their operation.
   a. **TTL (Page 65)**
   b. CMOS 3.5 series
   c. CMOS 5 Series
   d. **Power dissipation of all circuits increases with time.**

190. The ecimal “8” is represented as using Gray-Code.
   a. 0011
   b. **1100 (page 36)**
   c. 1000
   d. 1010

191. NOR Gate can be used to perform the operation of AND, OR and NOT Gate
   a. **FALSE**
   b. **TRUE (Page 50)**

192. The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code
   a. 2-bit
   b. 7-bit
   c. **8-bit (Page 38)**
   d. 16-bit

193. NOR gate is formed by connecting _____
   a. **OR Gate and then NOT Gate (Page 47)**
   b. NOT Gate and then OR Gate
   c. AND Gate and then OR Gate
   d. OR Gate and then AND Gate

194. The OLMC of the GAL16V8 is _____ to the OLMC of the GAL22V10
   a. Similar
   b. Different
   c. **Similar with some enhancements (Page 207)**

d. Depends on the type of PALs input size

195. All the ABEL equations must end with _____
   a. " . " (a dot)
   b. " $ " (a dollar symbol)
   c. **" ; " (a semicolon) (Page 201)**
   d. " endl " (keyword "endl")

196. Circuits having a bubble at their outputs are considered to have an active-low output.
   a. **True (Page 128)**
   b. False

197. Which one is true:
   a. **Power consumption of TTL is higher than of CMOS (Page 61)**
   b. Power consumption of CMOS is higher than of TTL
   c. Both TTL and CMOS have same power consumption
   d. Power consumption of both CMOS and TTL depends on no. of gates in the circuit

198. An S-R latch can be implemented by using _____ gates
   a. AND, OR
   b. **NAND, NOR (Page 218-220)**
   c. NAND, XOR
   d. NOT, XOR

199. A latch has _____ stable states
   a. One
   b. **Two (Page 218)**
   c. Three
   d. Four

200. Sequential circuits have storage elements
   a. **True (Page 8)**
   b. False

201. The ABEL symbol for "XOR" operation is
   a. **$ (Page 210)**

b. #
c. !
d. &

202. A Demultiplexer is not available commercially.
a. **True (Page 178)**
b. False

203. Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer
a. **A parallel to serial converter circuit (Page 244)**
b. A counter circuit
c. A BCD to Decimal decoder
d. A 2-to-8 bit decoder

204. The device shown here is most likely a
a. Comparator
b. Multiplexer
c. Demultiplexer
d. Parity generator

205. The main use of the Multiplexer is to
a. Select data from multiple sources and to route it to a single Destination (Page 167)
b. Select data from Single source and to route it to a multiple Destinations
c. Select data from Single source and to route to single destination
d. Select data from multiple sources and to route to multiple destinations

206. A logic circuit with an output $X = \bar{A}BC + A\bar{B}$ consists of _____
a. two AND gates, two OR gates, two inverters
b. three AND gates, two OR gates, one inverter
c. **two AND gates, one OR gate, two inverters**
d. two AND gates, one OR gate

207. The binary value of 1010 is converted to the product term $\bar{A}B\bar{C}D$
   a. True
   b. **False**

208. Following is standard POS expression $(A+\bar{B}+C+\bar{D})(A+\bar{B}+C+D)(A+B+\bar{C}+\bar{D})(A+B+C+\bar{D})(A+\bar{B}+\bar{C}+D)$
   a. **True (According to logic)**
   b. False

209. $\bar{A}B+\bar{A}B\bar{C}+AC$ is an example of _____
   a. Product of sum form
   b. **Sum of product form (Page 77)**
   c. Demorgans law
   d. Associative law

210. Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a ____ multiplexer.
   a. 4-input, 8-bit
   b. 4-input, 16-bit
   c. 2-input, 8-bit
   d. **2-input, 4-bit (Page 169)**

211. The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.
   a. **AND (Page 182)**
   b. OR
   c. NOT
   d. XOR

212. In ABEL the variable „A‟ is treated separately from variable ‘a’
   a. **True (Page 201)**
   b. False

213. The ABEL notation equivalent to Boolean expression A+B is:
   a. A & B
   b. A ! B

c. **A # B (Page 201)**
d. A $B

214. **The first Least Significant digit in decimal number system has**
a. **position 0 and weight equal to 1**
b. position 1 and weight equal to0
c. position 1 and weight equal to 10
d. position 0 and weight equal to 10

215. **The decimal equivalent of the binary number "10011" is**
a. **19 (According to rule)**
b. 99
c. 29
d. None of given options

216. **"74ALS" stands for**
a. Advanced Low-frequency Schottky TTL
b. Advanced Low-dissipation Schottky TTL
c. **Advanced Low-Power Schottky TTL (Page 61)**
d. Advanced Low-propagation Schottky TTL

217. **An adder circuit can be used to perform subtraction operation**
a. **True (Page 146)**
b. False

218. **The four outputs of two 4-input multiplexers, connected to form a 16-input multiplexer, are connected together through a 4-input gate**
a. AND
b. **OR (Page 171-172)**
c. NAND
d. XOR

219. **The Programmable Array Logic (PAL) has AND array and a OR array**
a. Fixed, programmable

b. **Programmable, fixed (Page 182)**
c. Fixed, fixed
d. Programmable, programmable

Q1: A product term is 0 when _____.
A) Any one literal is a 0 (page 72) (100% Sure)
B) Any of the literal is 1
C) At least two literals are 1
D) All the literals are 1

Q2: In 8-input multiplexer, the two outputs are connected through a/an _____ gate.
A) AND
B) OR (page 170) (100% Sure)
C) NOT
D) NOR

Q3: _____ devices dissipate varying amount of power depending upon the frequency of operation.
A) TTL
B) CMOS (page 65) (100% Sure)
C) Storage
D) Peripheral

Q4: Boolean Addition operation is performed by a(n) _____ gate.
A) AND
B) OR (page 71) (100% Sure)
C) XOR
D) NAND

Q5: The SOP expression can be implemented by an _____ combination of gates.

A) OR-XOR

B) AND-NAND

C) AND-OR (page 78) (100% Sure)

D) XOR-NOR

Q6: The maximum decimal number that can be represented using the 64-bit unsigned representation is _____.

A) 2^63

B) (2^64)-1 (page 24) (100% Sure)

C) (2^64)+1

D) 2^64

Q7: In 16-bit ALU, the G output is activated if the 4-bit unit generates a Carry _____ irrespective of Carry _____.

A) In, In

B) In, Out

C) Out, In (page 150) (100% Sure)

D) Out, Out

Q8: A standard POS form has _____ terms that have all the variables in the domain of the expression.

A) Sum (page 85) (100% Sure)

B) Product

C) Min

D) Composit

Q9: In Cascading Priority Encoders, the EO output is connected to the EI input of the encoder which handles _____.

A) Lower priority outputs

B) Higher priority outputs

C) Lower priority inputs (page 166) (100% Sure)

D) Higher priority inputs

Q10: Which of the following is the example of comparator?

A) OR

B) AND

C) XOR

D) XNOR (Confirm) (100% Sure)

Q11: In CMOS 5 Volt series, Input voltage of Logic high signal (VH) with a ranges from ____ to ____ volts.

A) 4.5, 5

B) 0, 5

C) 0, 3.5

D) 3.5, 5 (page 63) (100% Sure)

Q12: The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacent 1s are detected in the input, the output is set to high.

A) 2 (page 123) (100% Sure)

B) 4

C) 1

D) 0

Q13: A standard SOP form has _____ terms that have all the variables in the domain of the expression.

A) Sum

B) Product (page 84) (100% Sure)

C) Max

D) Composite

Q14: Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.

A) Negative-OR, Negative-AND (page 74) (100% Sure)

B) Negative-AND, Positive-OR

C) Positive-OR, Negative-AND

D) Positive-OR, Positive-AND

Q15: Adding two octal numbers "36" and "71" result in _____.

A) 213

B) 123

C) 127 (Confirm) (100% Sure)

D) 345

Q16: Any of the _____ forms of the Karnaugh Map can be used to simplify Boolean expressions.

A) Three

B) Four

C) Two (page 89) (100% Sure)

D) Five

Q17: Quine-McCluskey and K-Map methods are used for _____ of Boolean expression.

A) Multiplication

B) Addition

C) Simplification (page 90) (100% Sure)

D) Subtraction

Q18: The number "1259" may belong to _____ number system.
A) Binary number system

B) Octal or Decimal system

C) Decimal or Hexadecimal system (Confirm) (100% Sure)

D) Binary or Hexadecimal system

Q19: The series of TTL chips are characterized by their _____.
A) Switching Speed Only

B) Power Dissipation Only

C) Both (page 61) (100% Sure)

D) None of the above

Q20: All ABEL statements must end with _____.
A) '

B) ; (page 203) (100% Sure)

C) :

D) "

Q21: In sequential circuits memory elements are connected with _____.
A) Logic Circuit

B) Clock (page 311) (100% Sure)

C) Feedback path

D) External Event

Q22: In the 32-bit Single Precision Floating Point format the exponent value _____ is reserved to represent infinity exponents.

A) 98

B) 99

C) 255 (page 26) (100% Sure)

D) 256

Q23: The _____ output has the output of the OR gate connected through an XOR gate to the tri state buffer.

A) Combinational

B) Combinational input

C) PLA

D) Programmed Polarity (Page 186) (100% Sure)

Q24: The limitation in implementation of parallel binary adders is known as _____.

A) Delay

B) Carry Propagation (page 137) (100% Sure)

C) Carry input

D) Carry output

Q25: In 8 input multiplexer, the two outputs are connected through a/an _____ gate.

A) AND

B) OR (page 170) (100% Sure)

C) NOT

D) NOR

Q26: The Gray code is different from the unsigned binary code because _____.

A) Successive values of Gray code offer by only one bit (page 36) (100% Sure)

B) Gray code is positional code

C) Gray code does not support negative values

D) Gray code ranges from "0" to "9"

Q27: In 16-bit ALU, the G output is activated if the 4-bit unit generates a carry _____ irrespective of Carry _____.

A) In, In

B) In, Out

C) Out, In (page 150) (100% Sure)

D) Out, Out

Q28: In Cascading Priority Encoders, the EO output is connected to the El input of the encoder which handles _____.

A) Lower Priority Outputs

B) Higher Priority Outputs

C) Lower Priority Inputs (page 166) (100% Sure)

D) Higher Priority Inputs

Q29: Removing the NOT gate at the output of the NOR gate results in an _____.

A) OR Gate (page 50) (100% Sure)

B) NAND Gate

C) AND Gate

D) NOT Gate

Q30: Portable devices that run on batteries use _____ circuits that have low power dissipation.

A) Series

B) Integrated (page 65) (100% Sure)

C) Parallel

D) Electric