Turn over

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SECTION I

Instructions:

1. No Calculators Allowed.

2. Answer any six questions from the sections.

3. Section No. 1 is compulsory.

Instruction: (1)

Max. Marks: 100

Time: 3 Hours

Digital Electronics

Electronics & Communication Engineering

I Semester Diploma Examination, Nov/Dec, 2012
Sketch and explain the working of Ring-Counter.

Where the logic diagram and truth table of synchronous MOD-8 counter

Explain the working of Serial-in, Serial-out 4 bit shift register with truth table

With suitable sketches, explain the working of 7 segment display

(c) 

List the applications of 7 segment display

(c) 

Compare synchronous and asynchronous counters

(c) 

With logic circuit and truth table explain the operation of JK FF.

SECTION - 1V

(a) 

With gate level circuit, truth table, explain 2-bit magnitude comparator.

(b) 

Y = \overline{A} \overline{B} \overline{C} + \overline{A} \overline{B} \overline{C} + \overline{A} \overline{B} \overline{C}

(c) 

\[ Y = \overline{A} \overline{B} \overline{C} \overline{D} + \overline{A} \overline{B} \overline{C} \overline{D} + \overline{A} \overline{B} \overline{C} \overline{D} \]

(d) 

Simplify:

SECTION - III

(a) 

Distinguish between Serial adder and Parallel adder

(b) 

Explain the operation of Decimal to Binary encoder

(c) 

Sketch and explain the decoder to convert 8 to 4 to 2 to 1 encoder

(d) 

Sketch and explain the functional logic diagram of Decimal to BCD encoder

SECTION - I

(a) 

Where the logic circuit for the expression Y = ABC + BCD + AC

(b) 

\[ Y = ABC \overline{B} + ABCD + \overline{A} \overline{B} \overline{C} + \overline{A} \overline{B} \overline{C} + \overline{A} \overline{B} \overline{C} + ABCD \]

(c) 

The reduced expression

(d) 

Simplify the following expression and draw the logic circuit for

(e) 

Where the function of CMOS family

(f)