Digital Transformation for Analog Chips

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'Software is eating the world' – M. Andreesen, a16z

Today's internet economy is both a marvel of technical accomplishment as well as a harbinger of a fantastic future to come. One could say if hardware (semiconductors and systems) is the 'engine', then software (applications and OS) is the 'rocket fuel' that powers all the technology around us. One of the most exciting evolutions in software is the shift from interactive UI-based systems: computers, smartphones etc.; to autonomous AI-based systems: digital assistants, self-driving cars, enterprise automation etc. This trend enables two massive emerging commercial applications: the Internet of Things and Industrial Automation (aka Digital Transformation). It is projected the next phase of the Internet Era will be driven by massive proliferation of connected autonomous devices and simultaneous automation of high-value enterprise systems and processes. The semiconductor industry will benefit from both of these trends. The end market unit demand is obvious and projected to drive the chip industry to $1T/year and beyond. The less obvious but critical need is for software automation to accelerate the chip industry to meet the enormous emerging demand.

A Brief History of Chips

The Internet Era has been built on fundamental technologies and semiconductors are the most foundational of these. Without semiconductors the features, speed, connectivity, mobility and price of our today's devices would be impossible. Many types of semiconductors are required to make modern technology devices work: Digital (CPU/GPU, DSP, memory) and Analog (Sensors, Power management, RF) among others. To support the global appetite for technology the semiconductor industry has grown over the last 40 years into a nearly $500B/year juggernaut (Fig. 1). And this is just the chip industry, not including the supporting equipment, tools and materials markets.

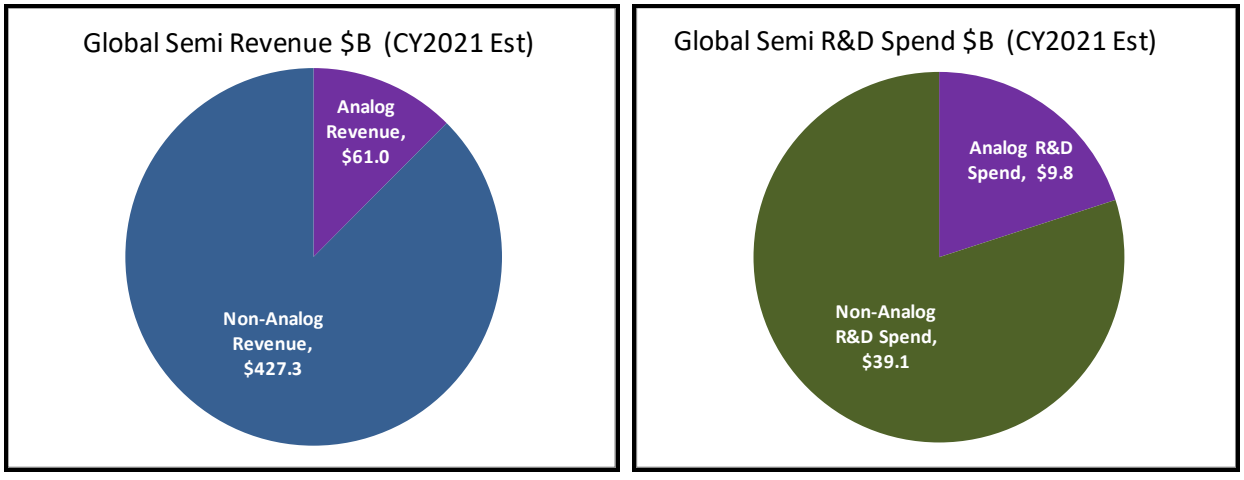


Figure 1 – Global Semiconductor Market and R&D Spend

The first generation of the chip industry was built by IDMs (integrated device manufacturer), in what could be called the 'Silicon 1.0' generation (Fig 2). These were the pioneers of the chip industry and were fully integrated operations with design/development, tools and manufacturing. They were extremely capital intensive and not particularly agile or responsive to market dynamics. The 1990's spawned what is known as the 'fabless' chip company and the 'Silicon 2.0' generation. These firms focused on more design/development and outsourced tools and manufacturing to emerging third party firms (mostly in Asia). This specialization resulted in relative speed, efficiency and growth that birthed many startups that became multi-billion dollar firms.

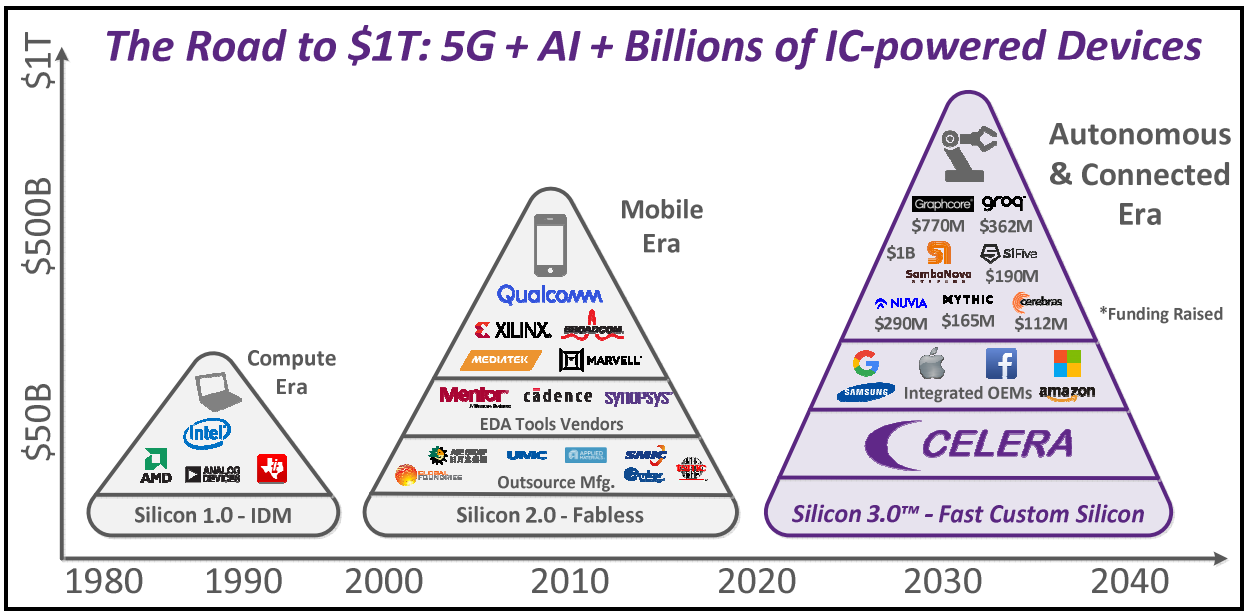


Figure 2 – Semiconductor History

However, despite its massive scale and evolution, one of the most difficult and persistent challenges in the chip industry remains the cost, time, resources and risk required to develop new products; i.e. R&D inefficiency. This limitation has strained innovation and revenue cycles, driven away venture investment for startups and stalled growth for many established firms. As a result, during the last decade, much innovation dried up as startups struggled to secure funding and established firms looked toward mergers and operational consolidation to please public markets. Ultimately, the overwhelming market demand for innovation has recently produced a new wave of chip startups as can be seen in Figure 2. These startups largely support the emerging demand for autonomous systems and massive data processing across billions of new connected devices. Additionally Tier 1 OEM's like Apple have invested aggressively to bring semiconductor R&D and supply chains in-house to improve R&D efficiency and gain control over their key IP and component sourcing. But critically, for OEMs this is a costly brute force effort in the legacy R&D model that only the most cash rich OEM's can afford.

Celera envisions a new paradigm in chip development to support the unprecedented demand for new semiconductor solutions: A third generation - Silicon 3.0™ - focused on dramatically increasing silicon development throughput and efficiency with software automation resulting in faster custom silicon

realization with lower upfront risk and cost. The Silicon 3.0™ generation is inevitable but to fulfill its promise of growth to $1T/year and beyond the industry must develop silicon much faster and more efficiently.

'Analog is Hard'

Analog (as opposed to digital/logic, memory, discrete, MEMS, etc.) is known by industry insiders as the difficult 'black art' of semiconductors that requires highly specialized skills and talent while also costing a disproportionate share of R&D budget and cycle time – up to 60% more spending per revenue dollar than the overall industry (Fig 1). Yet analog IC's comprise a critical and diverse $60B+ segment (Fig. 1) that continues to define much of the performance and capability of the systems and devices we all use. As we move into the new era of connected and autonomous devices and systems the analog functions will become even more critical in the areas of sensors, actuators, motor controls and power/battery management.

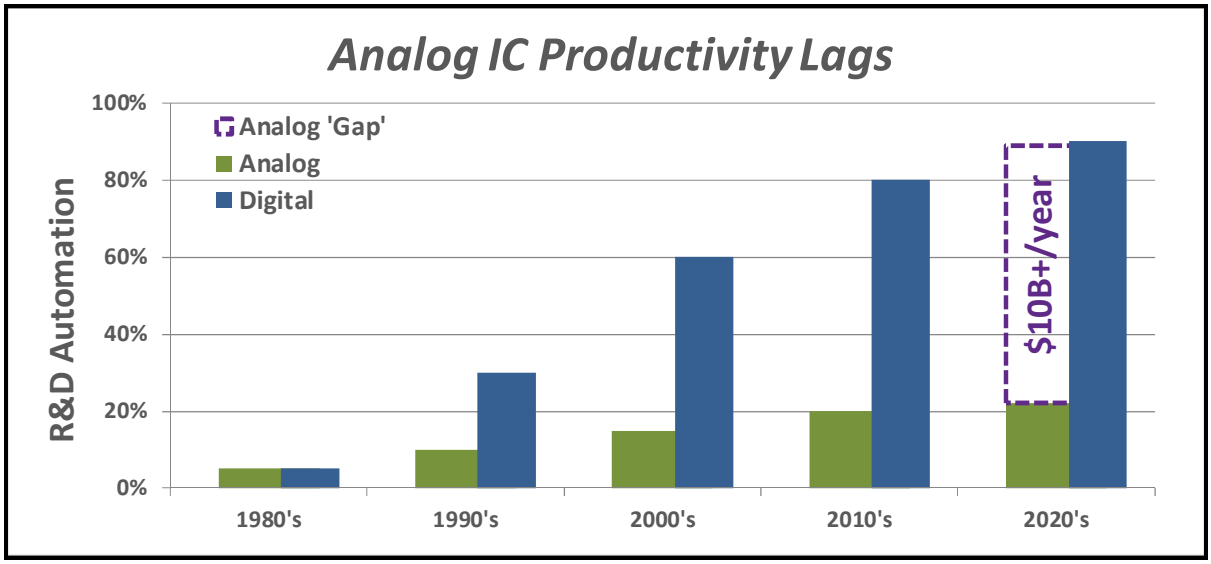


Figure 3 – Analog vs. Digital Development Automation

Indeed, over the last 30 years, advancements in chip developments tools have been delivered by the EDA tool segment (Fig 2) but most have been applied to digital IC's and not to analog. This is due to two major factors: First the digital methodologies for automated synthesis/verification/layout despite adaptations like Verilog-A and VHDL-AMS generally do not apply well to analog chips. Secondly a piecemeal 'tools' approach is not effective for analog because they tend to be much smaller and lower integration , relying more on customization and parametric performance to deliver value. And so analog R&D has lagged in productivity (Fig 3) and resulted in long schedules with manual design or compromised performance for cycle time. This is also the major reason why analog chip development is 60% more expensive than industry average (Fig 1). To deliver on the promise of a $1T/year chip industry a more analog-specific and turnkey approach is needed – a software-powered development service, not just a tool.

'Chips and SaaS' – An R&D Platform for IC's

Taking a holistic approach to the 'analog automation' problem one can aggregate the most challenging parts of the development flow as "modeling + IP + synthesis + layout + verification" (Fig 4). These disciplines require the most skilled and highest cost labor to execute while also being the least automated and driving the longest cycle times. For the simplest of analog chips this is a $1.5M-$3M and 10-18 month proposition – some project can be up to 5x in scale. Considering there is no guarantee of success in a highly competitive chip market it is easy to understand the bulk of ROI risk is tied up in this part of the development flow.

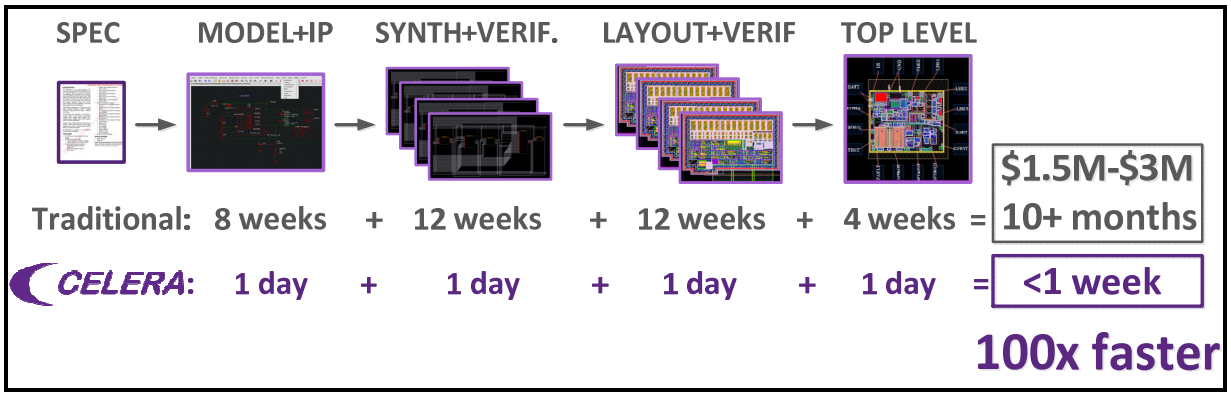


Figure 4 – Analog Chip Development Flow

Celera's solution applies intelligent 'expert system' AI software to each part of this flow. It distills over 250 engineer-years of analog IC design/development experience and decision flow into code that runs in tandem with industry-standard EDA tool suites. In effect Celera's software acts as an extremely fast, tireless and error-free 'robotic engineer' operating and making design decisions under the algorithmic guidance of the platform developers chip design experience built into the software. This methodology is implemented in the entire flow from modeling to verification and delivers a 'fab-ready' chip design from a customer specification input.

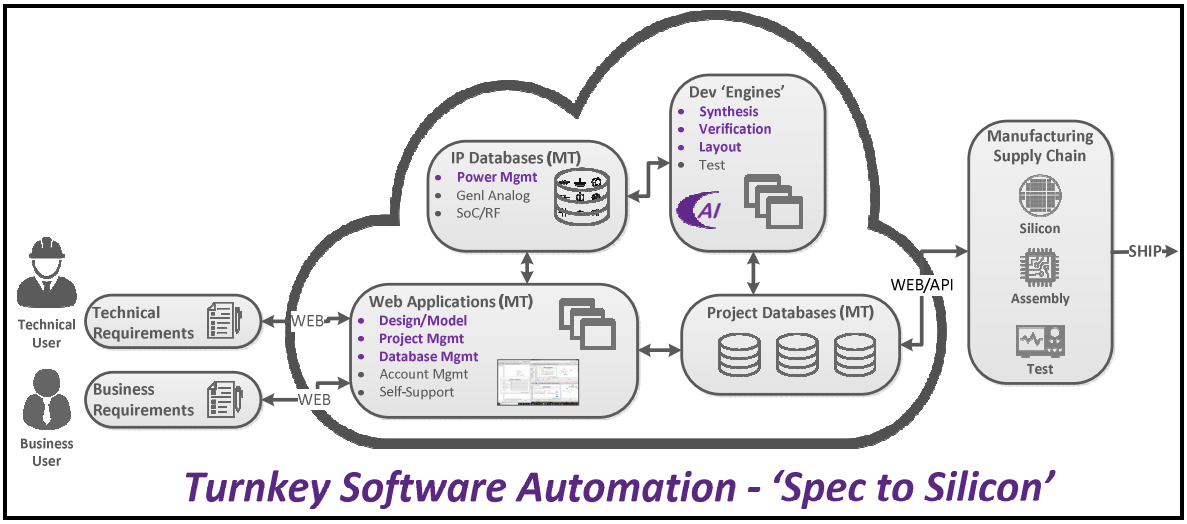


Figure 5 – Analog IC Development as SaaS

Because of this end-to-end 'service-not-a-tool' approach to the IC development flow the software is intrinsically suited to be integrated, deployed and delivered as a Software-as-a-Service platform or 'SaaS' (Fig 5). This automated software architecture enables scaling far beyond any legacy methodology or flow could achieve even with unlimited labor and capital resource. Customers can engage the platform in a 'self-service' mode for development while 'white-labeled' third party supply chain partners can handle manufacturing (silicon fabrication, assembly and test) and fulfillment services. Fortunately the fabless 'Silicon 2.0' era already built this segment into an efficient $200B/year turnkey industry over the last 25 years. It is a perfect and ready complement for Celera's development platform.

Accelerating Growth at 100x

It has been shown that development cycle time and upfront costs have been a persistent challenge throughout the history of the semiconductor industry and especially so in the analog segment. Celera's automated development platform is designed to deliver up to 100x faster chip design, 10x faster time-to-samples and 5x faster time-to-revenue (Fig 7). In the hyper-competitive IC industry, especially in consumer product cycles, this can mean the difference between winning 80%-100% of an opportunity or missing it altogether.

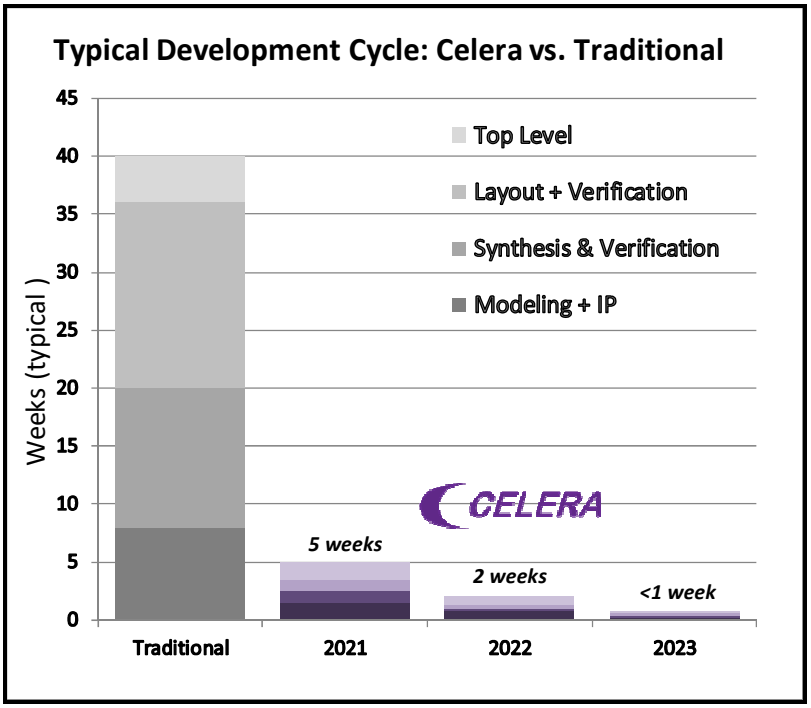
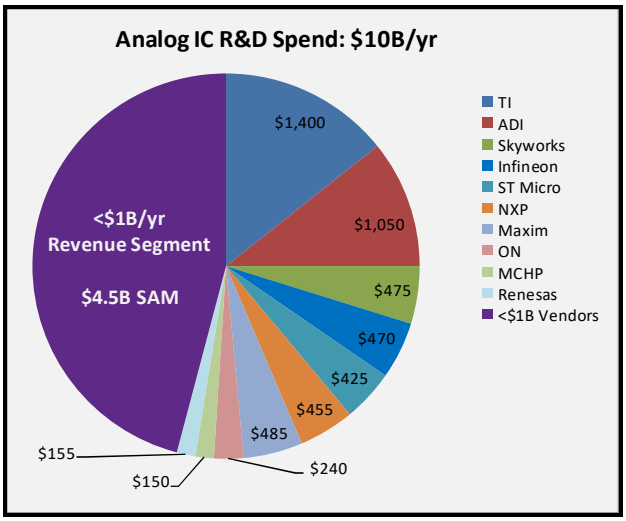


Figure 7 – Accelerated Development

Cycle time alone can drive key quantitative business case metrics for IC vendors with 150%-250% improvements possible in ROI: NPV, IRR and Cash-on-Cash. Additionally, for OEM's adopting the platform directly, it can deliver over 25% TCO improvement during the product lifecycle while securing more control of their supply chain, inherent exclusivity and IP protection.



$M/yr 2020	Analog R&D Spend (SAM)		
Company	Analog Revenue	Analog R&D Spend	% of Revenue
TI	$ 10,000	$ 1,400	14%
ADI	$ 5,200	$ 1,050	20%
Skyworks	$ 4,100	$ 475	12%
Infineon	$ 3,900	$ 470	12%
ST Micro	$ 3,400	$ 425	13%
NXP	$ 2,700	$ 455	17%
Maxim	$ 2,600	$ 485	19%
ON	$ 2,100	$ 240	11%
MCHP	$ 1,100	$ 150	14%
Renesas	$ 1,000	$ 155	16%
<$1B Vendors	$ 22,000	$ 4,500	20%
Total	$ 58,100	$ 9,805	17%

Figure 8 – Analog IC R&D Spend

The opportunity for Celera's platform is twofold: First to capture and accelerate the existing analog IC vendor R&D flow which is valued at ~$10B/year with about half of that in the top 10 vendors (Fig 8.). The second is to enable a new custom analog silicon sourcing model for OEM's that is estimated to be worth another 10B+ in just R&D. Ultimately the paradigm shift in risk reduction will change assumptions and create a new wave of growth. Celera's position is that R&D acceleration must happen in all segments – especially analog semiconductors – to fulfill the promise of a $1T/year chip industry. With the persistent global shortage of skilled talent and ever shrinking product cycles, the only way to successfully implement such a quantum leap in capability is with an automated software platform. Software is indeed 'eating the world'.