POWER ELECTRONICS

Devices, Drivers, Applications, and Passive Components

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Basic Semiconductor Physics and Technology

The majority of power electronic circuits utilise power semiconductor switching devices which *ideally* present infinite resistance when off, zero resistance when on, and switch instantaneously between those two states. It is necessary for the power electronics engineer to have a general appreciation of the semiconductor physics aspects applicable to power switching devices so as to be able to understand the vocabulary and the non-ideal device electrical phenomena. To this end, it is only necessary to attempt a qualitative description of switching devices and the relation between their geometry, material parameters, and physical operating mechanisms.

Typical power switching devices such as diodes, thyristors, and transistors are based on a monocrystalline group IV silicon semiconductor structure or a group IV polytype, silicon carbide. These semiconductor materials are distinguished by having a specific electrical conductivity, σ, somewhere between that of good conductors (>10^{20} free electron density) and that of good insulators (<10^{3} free electron density). Silicon is less expensive, more widely used, and a more versatile processing material than silicon carbide, thus the electrical and processing properties of silicon are considered first, in more detail.

In pure silicon at equilibrium, the number of *electrons* is equal to the number of *holes*. The silicon is called *intrinsic* and the electrons are considered as negative charge-carriers. Holes and electrons both contribute to conduction, although holes have less mobility due to the covalent bonding. Electron-hole pairs are continually being *generated* by thermal ionization and in order to preserve equilibrium previously generated pairs *recombine.* The intrinsic carrier concentrations n_i are equal, small (1.4×10^{10} /cc), and highly dependent on temperature. In order to fabricate a power-switching device, it is necessary to increase greatly the free hole or electron population. This is achieved by deliberately doping the silicon, by adding specific impurities called *dopants.* The doped silicon is subsequently called *extrinsic* and as the concentration of dopant N_c increases, the resistivity ρ decreases.

Silicon doped with group V elements, such as As, Sb or P, will be rich in electrons compared to holes. Four of the five valence electrons of the group V

dopant will take part in the covalent bonding with the neighbouring silicon atom, while the fifth electron is only weakly attached and is relatively 'free'. The semiconductor is called *n-type* because of its free negative charge-carriers. A group V dopant is called a *donor,* having donated an electron for conduction. The resultant electron impurity concentration is denoted by N_D - the donor concentration.

If silicon is doped with atoms from group III, such as B, Al, Ga or In, which have three valence electrons, the covalent bonds in the silicon involving the dopant will have one covalent-bonded electron missing. The impurity atom can accept an electron because of the available thermal energy. The dopant is thus called an *acceptor*, which is ionised with a net positive charge. Silicon doped with acceptors is rich in holes and is therefore called *p-type.* The resultant hole impurity concentration is denoted by N_A - the acceptor concentration.

Electrons in n-type silicon and holes in p-type are called *majority carriers,* while holes in n-type and electrons in p-type are called *minority carriers.* The carrier concentration equilibrium can be significantly changed by irradiation by photons, the application of an electric field or by heat. Such carrier injection mechanisms create *excess carriers.*

If n-type silicon is irradiated by photons with enough energy to ionise the valence electrons, electron-hole pairs are generated. There is already an abundance of majority electrons in the n-type silicon, thus the photon-generated excess minority holes are of more relative and detectable importance. If the light source is removed, the time constant associated with recombination, or decay of excess minority carriers, is called the *minority carrier hole lifetime,* τ_h. For a p-type silicon, exposed to light, excess minority electrons are generated and after the source is removed, decay at a rate called the *minority carrier electron lifetime,* τ_e. The minority carrier lifetime is often called the *recombination lifetime.*

A difficulty faced by manufacturers of high-voltage, large-area semiconductor devices is that of obtaining uniformity of n-type phosphorus doping throughout the usual high-resistivity silicon starting material. Normal crystal-growing and doping techniques give no better than ±10 per cent fluctuation around the wanted resistivity at the required low concentration levels (<10^{14} /cc). Final device electrical properties will therefore vary widely in all lattice directions. Tolerances better than ±1 per cent in resistivity and homogeneous distribution of phosphorus can be attained by neutron radiation, commonly called *neutron transmutation doping,* NTD. The neutron irradiation flux transmutes silicon atoms first into a silicon isotope with a short 2.62-hour half-lifetime, which then decays into phosphorus. Subsequent annealing removes any crystal damage caused by the irradiation. Neutrons can penetrate over 100mm into silicon, thus large silicon crystals can be processed using the NTD technique.

1.1 Processes forming pn junctions

A pn junction is the location in a semiconductor where the impurity changes from p to n while the monocrystalline lattice continues undisturbed. A bipolar diode is thus created, which forms the basis of any bipolar semiconductor device.

The donor-acceptor impurities junction is formed by any one of a number of process techniques, namely alloying, diffusion, epitaxy, ion implantation or the metallization for ohmic contacts.

1.1.1 The alloyed junction

At the desired region on an n-type wafer, a small amount of p-type impurity is deposited. The wafer is then heated in an inert atmosphere and a thin film of melt forms on the interface. On gradual cooling, a continuous crystalline structure results, having a step or abrupt pn junction as shown in figure 1.1. This junction-forming process is rarely employed to form a power pn junction.

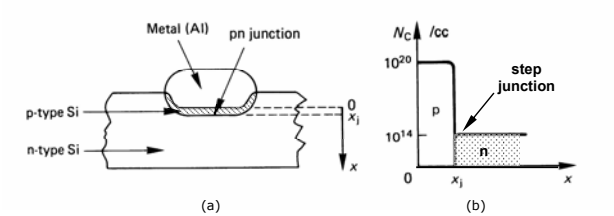

Figure 1.1. *n-Si to Al metal alloy junction: (a) cross-section where x_j is the junction depth below the metal-semiconductor boundary and (b) impurity profile of the formed step junction.*

1.1.2 The diffused junction

An n-type silicon substrate is heated to about 1000°C in a diffusion furnace. A p-type impurity is entered in a mixed vapour compound form. This compound breaks down as a result of the high temperature, and is slowly diffused into the substrate. The maximum impurity concentration occurs at the surface, tailing off towards the inside. The doping profile is mathematically defined and is varied by controlling the vapour mixture concentration, the furnace temperature, and time of diffusion. If the source concentration is continuously replenished, thus maintained constant, the doping profile is given by a complementary error function, erfc. If natural depletion of dopant occurs, then the profile is an exponential function, which gives a Gaussian diffusion distribution. The actual areas of diffusion are selected by a surface-blocking mask of silicon dioxide, as illustrated in figure 1.2.

The diffusion process is the only junction forming technique that is not applicable to silicon carbide wafer processing.

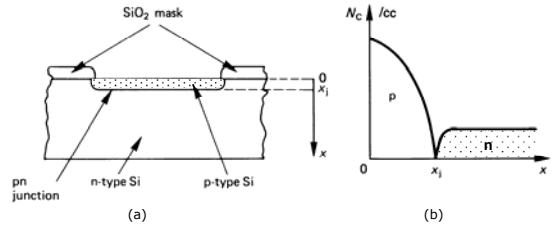

Figure 1.2. *Diffused pn junction: (a) cross-section where x_j is the junction depth below the silicon surface and (b) impurity concentration profile.*

1.1.3 The epitaxy junction

A pre-cleaned, polished, almost perfect silicon crystal surface acts as a substrate for subsequent deposition. The pre-doped silicon is heated to about 1150°C in a quartz reactor. A hydrogen gas flow carrying a compound of silicon such as $SiCl_4$ or SiH_4 is passed over the hot substrate surface, and silicon atoms are deposited, growing a new continuous lattice. If phosphine (PH_3) or diborane (B_2H_6) is included in the silicon compound gas flow, a layer of the required type and resistivity occurs. Up to 100µm of doped silicon can be grown on substrates for power devices at a rate of about 1 µm/min at 1200°C. A very low crystalline fault rate is essential if uniform electrical properties are to be attained.

1.1.4 The ion-implanted junction

Ion impurities (B, P or As) are accelerated in a vacuum at high keV energies at the pre-doped silicon substrate, which is at room temperature. The ions penetrate the lattice to less than a few microns, typically 1µm at about ½MeV. The resultant doping profile is Gaussian, with the smaller ion like boron, penetrating deeper. In so doing, the lattice is disrupted and subsequent annealing at elevated temperatures of about 700°C restores the uniform lattice structure, without activating the implanted atoms. Boron requires higher annealing temperatures which may cause undesired diffusion of the dopant. Ion implantation is the most accurate and controllable doping process, giving excellent doping level uniformity and production repeatability.

1.1.5 The ohmic-contact junction

An ohmic contact is a resistive connection which is voltage independent. Aluminium is commonly evaporated in a vacuum at near room temperature, onto the wafer surface to form a metallised electrical contact. Deposit rates of ½ µm/minute are typical. If the silicon is n-type, a pn Schottky junction is formed, which is undesirable as an ohmic contact. This junction forming aspect is

discussed at the end of section 3.1.4. Ohmic metal contact to p-type semiconductors with a large bandgap, like silicon carbide, is technically difficult.

1.2 The oxidation and masking process

An extremely useful and convenient process employed during device fabrication is the formation of silicon dioxide (silica) $Si0_2$ on the silicon wafer surface.

Wafers of silicon placed in a furnace for three to four hours at 1000-1200°C containing oxygen gas form a surface oxide layer of $Si0_2$ usually less than 1μm thick. The oxide penetration into the silicon is about 40% of its thickness. Wet oxidation, with water added, is about 20 times faster than dry oxidation but the oxide quality is lower. The wafer is effectively encapsulated by silica glass, which will prevent penetration by normal impurity atoms, except gallium atoms. Selective diffusions are made in the silicon by opening windows through the oxide by selective etching with HF following a photo-resist lithography masking process.

The excellent electrical-insulating properties of $Si0_2$ may be utilised for surface junction passivation. Silicon dioxide has an amorphous structure with a very high resistivity and a dielectric constant of 3.85, which make it a useful insulator. Silicon dioxide is used extensively as an insulating barrier between the gate metal and channel of insulated gate semiconductor switching devices.

1.3 Polysilicon deposition

Polycrystaline silicon is used as the gate electrode in metal oxide devices and for metallization. The deposition method involves the pyrolysis of silane $SiH_{4\,(g)} \rightarrow Si_{\,(s)} + 2H_{2\,(g)}$ and at 600°C and normal pressure, deposits about 20nm/minute. The polysilicon is heavily doped to reduce the resistivity using phosphine or diborane *in situ* or by ion implantation. Diffusion is used at higher temperatures in order to attain the lowest resistivities.

1.4 Lifetime control

Two basic processes have been developed to reduce the lifetime of carriers in power devices.

- Thermal diffusion of gold or platinum or
- Bombardment of the silicon with high-energy particles such as electrons and protons.

The diffusion of gold or platinum occurs more rapidly than the diffusion of group III and V dopants, hence the precious metal is diffused at 800 to 900°C, just prior to metallization, which is performed at a lower temperature. The higher the precious metal diffusion temperature the higher the solubility and the lower the carrier lifetime. Disadvantages of precious metal diffusion include:

- devices cannot be tested prior to or immediately after impurity diffusion and
- small temperature changes cause a wide variation in device characteristics.

In high-resistivity silicon used to fabricate power devices, irradiation bombardment causes defects composed of complexes of vacancies with impurity atoms of oxygen and of two adjacent vacancy sites in the lattice. The advantages of the use of irradiation in order to reduce carrier lifetime in power devices are:

- irradiation is performed at room temperature, after fabrication;
- irradiation can be accurately controlled hence a tighter distribution of electrical characteristics results;
- overdose annealing can be performed at only 400°C; and
- it is a clean, non-contaminating process.

Much attention has been focussed on proton irradiation, which has high costs and long processing scan times, but offers the most accurate and precise form of lifetime control. The electrical consequences of lifetime control are an improvement in switching speed at the expense of increased leakage and on-state voltage.

1.5 Silicon Carbide

Wide bandgap semiconductors (GaN, SiC, diamond, etc.) have better high voltage and temperature characteristics than silicon devices. However, because silicon carbide, SiC, sublimes at high temperature, ≈1800ºC, processing is more difficult than for silicon (which melts at a lower temperature of 1415°C). The similar chemistry properties of silicon and silicon carbide (both in group IV) means that many of the existing processes for silicon can be applied to silicon carbide, but with some refinement and higher processing temperatures. The exception is thermal diffusion which is not effective if a good SiC surface morphology is to be retained.

The SiC crystal boules are grown by seeded sublimation using the physical vapour transport (PVT) method. Alternatively, chemical vapour deposition (CVD) can be used, where SiH_4, C_3H_8, and H_2 are typically injected into the chamber. This process is mainly used for producing SiC epitaxial growth. A hot walled CVD reactor can deposit 100μm at a rate of 1 to 5 μm/hour at 1200ºC to 1500ºC. Crystal defects (micropipes, stack faults, etc.) occur at a rate of less than 1 per cm^2. Proprietary defect healing technology can significantly decrease the defect rate. The main single crystal polytypes for power switching device fabrication are 4H-SiC and 6H-SiC (this lattice structure terminology is based on the Ramsdell notation).

Nitrogen for n-type and aluminium or boron for p-type can be used in epitaxial growth and ion implantation. Substrates usually have an n or p epitaxial drift layer. Typical n-type epitaxy (50μm) can be thicker than a p-type layer (10μm), and the n-type epitaxy has a thin 1μm n-type buffer or fieldstop.

Ion implantation is shallow, typically less than 1μm, and requires high temperature and 30 to 300keV. Subsequent annealing is at 1650ºC. The lower the

temperature, the longer the annealing time. Contact metallization can use nickel on highly n-doped SiC, which is annealed at 1150ºC for a few minutes. A nickel and titanium Schottky metal combination is suitable for p^+ region metallization. $Si0_2$ is an electrical-insulator that can be grown on both Si and SiC. Oxide growth for SiC is slower than that on silicon and involves nitridation of nitric oxide, N_20, at 1300ºC. Because of the physical and chemical stability of silicon carbide, acid wet etching is ineffective and dry reactive ion etching tends to be used for etching.

1.6 Si and SiC physical and electrical properties compared

The processing of silicon is a mature, cost efficient technology, with 12-inch wafers and submicron resolution common within the microelectronics industry. So-called wide bandgap semiconductors like silicon carbide offer promising high voltage and temperature power switching device possibilities as material quality and process yields improve. Figure 1.3 shows and allows comparison of the key physical and electrical properties of the main semiconductor materials applicable to power switching device fabrication.

The higher

- the energy bandgap, E_g, the higher the possible operating temperature before intrinsic conduction mechanisms produce adverse effects;
- the avalanche breakdown electric field, ξ_b, the higher the possible rated voltage;
- the thermal conductivity, σ_T, the more readily heat dissipated can be removed; and
- the saturation electron drift velocity, v_{sat}, and the electron mobility, μ_n, the faster possible switching speeds.

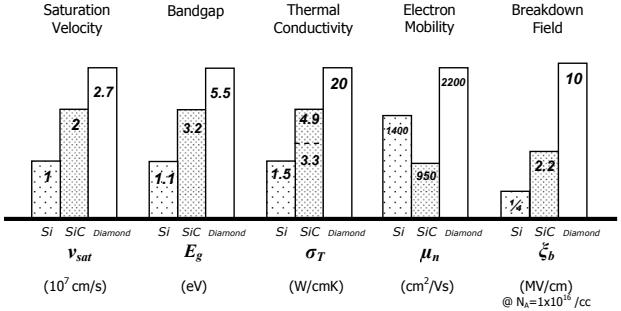

Figure 1.3. *Key electrical and thermal characteristics of group IV monocrystalline silicon and diamond and polytype 4H-silicon carbide, at room temperature.*

Although the attributes of wide bandgap materials are evident, processing is more difficult and some of the parameters vary significantly with a wide operating temperature range. SiC performance figures are slightly better than those for GaN, except, importantly, GaN has better carrier mobility. GaN growth is complicated by the fact that Nitrogen tends to revert to the gaseous state, and therefore only thin layers are usually grown on sapphire or SiC substrates. Lattice-substrate boundary mismatch occurs because of the significant difference in molecule sizes and packing. Such a boundary imperfection may prove problematic with power devices where principle current flow is usual vertically through the structure, hence through the imperfect lattice boundary.

Some of the physical and electrical parameters and their values in figure 1.3 will be explained and used in subsequent chapters. Other useful substrate data is given in table 1.1.

Table 1.1. Other useful substrate material data

			Si	SiC	Diamond
relative dielectric constant	ε_r		11.8	9.7	5.8
maximum operating temperature	T_{max}	°C	300	1240	1100
melting temperature	T_{melt}	°C	1415	sublime >1800	phase change

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2

The pn Junction

The diode is the simplest bipolar semiconductor device. It comprises p-type and n-type semiconductor materials brought together, usually after diffusion, to form a (step or abrupt) junction as shown in figure 2.la.

A *depletion layer*, or alternatively a *space charge layer*, scl, is built up at the junction as a result of diffusion caused by the large carrier concentration gradients. The holes diffuse from the p-side into the n-side while electrons diffuse from the n-side to the p-side, as shown in figure 2.lb. The n-side, losing electrons, is charged positively because of the net donor charge left behind, while the p-side conversely becomes negatively charged. An electric potential barrier, ξ, builds up, creating a drift current which opposes the diffusion flow, both of which balance at thermo-dynamic equilibrium as shown in figure 2.lc. There are no free carriers in the scl.

The zero external bias, built-in, junction potential or scl potential is given by

$$\Phi = \frac{kT_j}{q}\, \ell n \frac{N_A N_D}{n_i^2} \qquad \text{(V)} \qquad (2.1)$$

where q is the electron charge, 1.6 x 10^{-19} C
k is Boltzmann's constant, 1.38 x 10^{-23} J/K
T_j is the junction temperature, K.
Thus $\varphi = kT_j/q = 0.0259$ eV at room temperature, 300 K.

One important feature of the pn junction is that current (holes) flows freely in the p to n direction when forward-biased, that is, the p-region is biased positive with respect to the n-region. Only a small leakage current flows in the reverse voltage bias case. This asymmetry makes the pn junction diode useful as a rectifier, exhibiting static voltage-current characteristics as illustrated in figure 2.2.

2.1 The pn junction under forward bias (steady-state)

If the p-region is externally positively-biased with respect to the n-region as shown in figure 2.3b, the scl narrows and current flows freely. The emf positive potential supplies holes to the p-region, while the negative emf potential provides electrons to the n-region. The carriers both combine, but are continuously replenished from the emf source. A large emf source current flows through the diode, which is termed *forward-biased*.

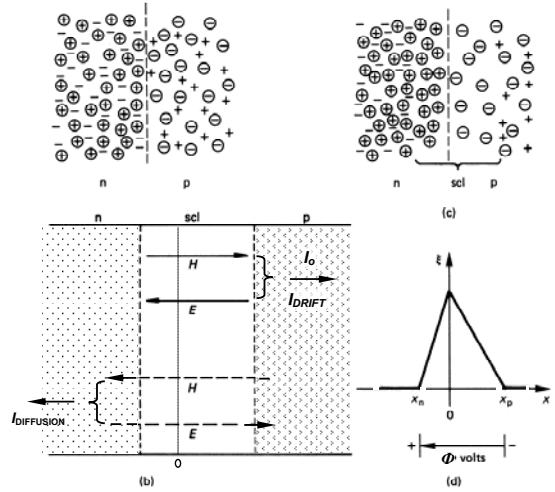


Figure 2.1. *The step junction. (a) The junction if carriers did not diffuse: ⊕ ionised donors, ⊖ ionised acceptors, + holes and - electrons; (b) electron and hole movements: ---- diffusion flows, ——— drift flows; (c) equilibrium distribution of ionised impurities and free carriers; and (d) scl electric field and voltage.*

2.2 The pn junction under reverse bias (steady-state)

If a bias voltage is applied across the p and n regions as shown in figure 2.3c, with the p-terminal negative with respect to the n-terminal, then the scl widens. This is because electrons in the n-region are attracted to the positive external emf source while holes in the p-region are attracted to the negative emf potential. As the scl widens, the peak electric field ξ_m at the junction increases as shown in figure 2.3d.

The only current that flows is the small *leakage current* which is due to carriers generated in the scl or minority carriers which diffuse to the junction and are collected. The junction is termed *reverse-biased.*

Increasing applied reverse bias eventually leads to junction reverse voltage breakdown, V_b, as shown in figure 2.2, and the diode current is controlled by the external circuit. Breakdown is due to one of three phenomena, depending on the doping levels of the regions and, most importantly, on the concentration of the lower doped side of the junction.

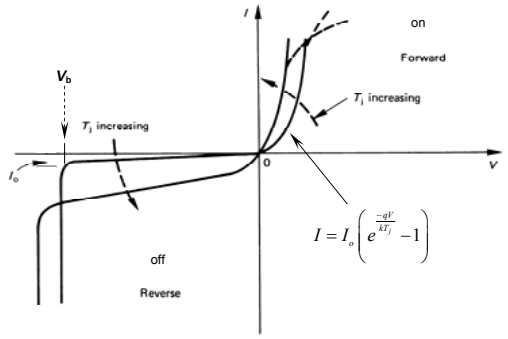


Figure 2.2. *Typical I-V static characteristics of a silicon pn junction diode, and the effects of junction temperature, T_j.*

2.2.1 Punch-through voltage

The reverse voltage extends the scl to at least one of the ohmic contacts and the device presents a short circuit to that voltage in excess of the *punch-through* voltage, V_{PT}. Punch-through tends to occur at low temperatures with devices which employ a low concentration region (usually the n-side), as is usual with high-voltage devices. The punch-through voltage for silicon can be approximated by

$$V_{PT} = 7.67\times10^{-16} N_c W_c^2 \qquad \text{(V)} \qquad (2.2)$$

where N_c is the concentration in /cc of the lighter doped region and
W_c is the width of that region in μm.

2.2.2 Avalanche breakdown

Avalanche breakdown or *multiplication breakdown*, is the most common mode of breakdown and occurs when the peak electric field, ξ_m, in the scl at the junction exceeds a certain level which is dependent on the doping level of the lighter doped

region. Minority carriers associated with the leakage current are accelerated to kinetic energies high enough for them to ionise silicon atoms on collision, thereby creating a new hole-electron pair. These are accelerated in opposite directions, because of the high electric field strength, colliding and ionising repeatedly - hence the term avalanche, impact ionisation or carrier multiplication. If the lighter doped silicon region has a concentration of

$$10^{13} < N_c < 5\times10^{14} \qquad (\text{/cc})$$

then the avalanche voltage may be approximated by

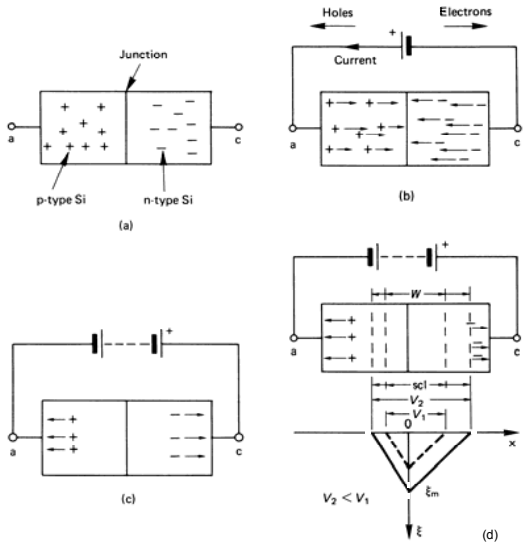
$$V_b = 5.34 \times 10^{13}\, N_c^{-3/4} \qquad \text{(V)} \qquad (2.3)$$

The peak electric field at the junction will be

$$\xi_b = 3.91 \times 10^{5}\, N_c^{1/8} \qquad \text{(V/m)} \qquad (2.4)$$

and the width of the scl, mainly in the lighter doped region, at breakdown is given by

$$W = 2\, V_b / \xi_b \qquad (2.5)$$



Figur ity
c
voltage; (c) with reverse applied voltage; and (d) electric field and scl change with increased reverse applied voltage.

2.2.3 Zener breakdown

Field or Zener breakdown occurs with heavily doped junction regions and at usually less than 5V reverse bias. It occurs when the scl is too narrow for avalanche yet the electric field grows very large and electrons tunnel directly from the valence band on the p-side to the conduction band on the n-side. This reverse current is called the *Zener effect.*

These three modes of reverse voltage breakdown are not necessarily destructive provided the current is uniformly distributed. If the current density in a particular area is too high, a local hot spot may occur, leading to device thermal destruction.

2.3 Thermal effects

The pn junction current, I, shown in figure 2.2, is related to the scl voltage, V, according to

$$I(V) = I_o[e^{-qV/kT_j} - 1] \quad \text{(A)} \qquad (2.6)$$

where I_o, is the reverse leakage current in amps.
The forward conduction voltage decreases with increased junction temperature, T_j. That is, the on-state voltage has a negative temperature coefficient. In practical silicon pn diodes, at low currents, the temperature coefficient is typically -2.4 mV/K, becoming less negative with increased current. At higher currents, the coefficient becomes positive because of the reduced carrier mobility at higher temperatures, which causes non-scl regions to increase in resistance. The effects of the change in temperature coefficient at higher currents, in practical devices, are shown dotted in figure 2.2. Neglecting the exponential silicon bad gap temperature dependence, the temperature effects at high current, on the diffusion constant component of the leakage current I_o in equation (2.6), called the saturation current, is given by

$$I_o(T) = I_o(25°C)\left(\frac{T}{300}\right)^{1.8} \qquad (2.7)$$

Silicon carbide diodes have a higher temperature coefficient, typically +8mV/K.

The avalanche voltage increases with temperature, as does the reverse leakage current. The effects of temperature on the reverse bias characteristics are shown in figure 2.2. In the case of silicon carbide, increased temperature decreases the avalanche voltage and increases the leakage current.

The silicon temperature coefficient for avalanche is positive since the mean distance between collisions is reduced because of the increased thermal energy, which increases the vibrational amplitude. Higher electric fields are necessary for the carriers to gain sufficient kinetic energy for ionisation.

Equation (2.6) also indicates that the reverse bias current increases with increased junction temperature. This positive temperature coefficient does not generally result in thermal instability with silicon devices, provided sufficient heat sinking is employed on smaller devices.

2.4 Models for the junction diode

Semiconductor device models are used extensively for power electronic circuit simulation. A basic piecewise-linear model is applicable to simple manual calculations, where the terminal I-V characteristics are empirically modelled based on ideal circuit elements. A more complex and accurate model is required for computer transient analysis simulation. Such accurate models are based on the semiconductor physics of the device. Many power switching semiconductor device manufacturers provide values for the model parameters suitable for circuit simulation in the packages PSpice and SABER.

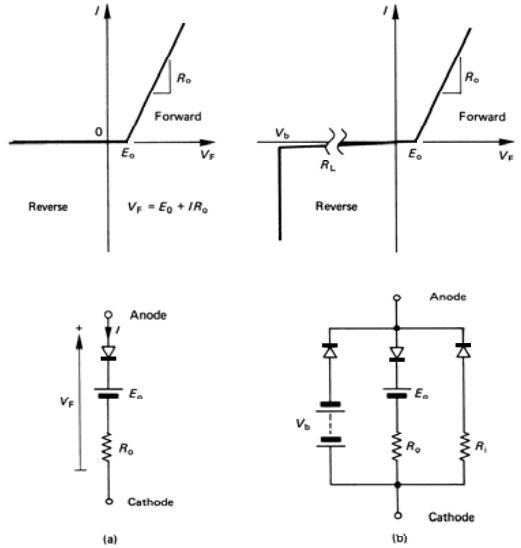


Figure 2.4. *Piecewise-linear approximations of junction diode characteristics: (a) ideal diode with an offset voltage and resistance to account for slope in the forward characteristic and (b) model including reverse bias characteristics.*

2.4.1 Piecewise-linear junction diode model

The pn junction diode is a unilateral device that, to a good approximation, conducts current in only one direction. Figure 2.4a shows a *piecewise-linear* (pwl) model of the diode that is suitable for static modelling in power electronic circuits. It includes a perfect diode, an on-state voltage source E_o, and a series resistor of value R_o to account for the slope in the actual forward characteristic. The forward *I-V* characteristic at a given temperature is given by

$$V_F(I_F) = E_0 + I_F R_0 \quad \text{for } V_F > E_0 \qquad \text{(V)} \qquad (2.8)$$

The model in figure 2.4a does not incorporate the static reverse characteristics of leakage and avalanche. These are shown in figure 2.4b, where V_b from equation (2.3) models the avalanche limit and $R_i(=V_b/I_o)$ gives linear leakage current properties for a given junction temperature. The three diode components are assumed perfect.

The model given by equation (2.8) is adequate for calculation of static balancing requirements of parallel and series connected diodes and thyristors, as considered in section 10.1 and the associated problems, 10.4, 10.5, and 10.9 to 10.12.

Example 2.1: ***Using the pwl junction diode model***

An approximation to the forward characteristic of the diode shown in figure 2.4a, is given by $V_F = 1.0 + 0.01 I_F$. For a constant current of 45A for ⅔ of a cycle, calculate the diode

- ***i.*** on-state voltage;
- ***ii.*** mean power loss; and
- ***iii.*** rms current.

Solution

i. The on-state voltage at 45A is given by

$$V_F(i_F) = 1.0 + i_F\ 0.01 = 1.0 + 45 \times 0.01 = 1.45\text{V}$$

ii. If the on-state duty cycle is δ=⅔, the average power loss is

$$\bar{P} = \delta \times V_F \times I_F = \tfrac{2}{3} \times 1.45\text{V} \times 45\text{A} = 43.2\text{W}$$

iii. The diode rms current is given by

$$I_{rms} = \sqrt{\delta} \times I_{dc} = \sqrt{\tfrac{2}{3}} \times 45\text{A} = 36.7\text{A}$$

♣

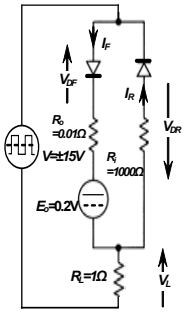
Example 2.2: ***Static diode model***

A Schottky diode is used to half-wave rectify a square wave ±15V source in series with a 1Ω resistor. If the diode model shown in figure 2.4b is modelled by R_o = 0.01 Ω, E_o = 0.2V, R_i = 1000Ω, and V_b = 30V, then determine:

- ***i.*** the diode model forward and reverse bias operating point equations for the series circuit
- ***ii.*** the load current and diode voltage

- ***iii.*** the rectifier losses (neglecting any recovery effects) and the load power dissipation
- ***iv.*** Estimate the power dissipated in the load if the source is ac with the same fundamental component as the square wave.
- ***v.*** What is the non-fundamental power dissipated with the square wave source.

Solution



i. When the diode is *forward biased*

$$i_F = \frac{1}{R_o}\left(v_{DF} - E_o\right) \quad \text{for} \quad v_{DF} \geq 0.2\text{V}$$

Kirchhoff's voltage law for the series circuit gives

$$V_s = i_F R_L + v_{DF}$$

Eliminating the diode voltage v_{DF} gives series circuit current

$$i_F = \frac{V_s - E_o}{R_o + R_L} \quad \text{for} \quad V_s \geq E_o$$

$$i_F = 0 \quad \text{for} \quad 0 < V_s < E_o$$

The diode voltage is therefore given by

$$v_{DF} = \frac{V_s R_o + E_o R_L}{R_o + R_L} = E_o + i_F R_o \quad \text{for } i > 0$$

When the diode is *reversed biased*, below the reverse breakdown voltage V_b

$$i_R = \frac{1}{R_i} v_{DR} \quad \text{for} \quad v_{DR} < V_b$$

$$V_s = i_R R_L + v_{DR}$$

Eliminating the diode voltage v_D gives series circuit current

$$i_R = \frac{V_s}{R_i + R_L}$$

The diode voltage is thus given by

$$v_{DR} = \frac{V_s R_i}{R_i + R_L} = i_R R_i$$

ii. The circuit voltages and current are, when the diode is forward biased,

$$i_F = \frac{15\text{V} - 0.2\text{V}}{0.01\Omega + 1\Omega} = 14.65\text{A}$$

$$V_{D_F} = 0.2\text{V} + 14.65\text{A} \times 0.01\Omega = 0.35\text{V}$$

If $R_L >> R_o$, the diode current equation can be simplified using R_o=0.

When the diode is reverse biased

$$i_R = \frac{15\text{V}}{1000\Omega + 1\Omega} = 15.0\text{mA}$$

$$V_{D_R} = 15\text{mA} \times 1000\Omega = 15.0\text{V}$$

If $R_i >> R_L$ the diode current and voltage equations can be simplified using R_L=0.

iii. The rectifier losses are, when forward biased,

$$P_{D_F} = v_{D_F} \times i_F$$
$$= 0.35\text{V} \times 14.65\text{A} = 5.127\text{W}$$

and when reverse biased

$$P_{D_R} = v_{D_R} \times i_R$$
$$= 15\text{V} \times 15\text{mA} = 0.225\text{W}$$

Total diode losses are therefore ½(5.127 + 0.225) = 2.68W.
The power from the square wave supply is

$$½ \times (15\text{V} \times 14.65\text{A} + 15\text{V} \times 15\text{mA}) = 110\text{W}$$

with 110 – 2.68 = 107.32W dissipated in the 1Ω resistor load.

iv. The magnitude of the fundamental of a square wave is 4/π times the square wave magnitude, that is, 15V×4/π = 19.1V peak.
The forward biased diode does not conduct until the supply voltage exceeds 0.2V. This is a small percentage of the sine wave, hence can be neglected in the loss estimate. The forward current flow is approximately

$$i_F = \frac{19.1\text{V} - 0.2\text{V}}{1\Omega + 0.01\Omega} \times \sin \omega t = 18.7 \times \sin \omega t$$

The rms of a sine is 1/√2 its magnitude and 1/√2 again for a half wave rectified sine. That is

$$i_{Frms} = \frac{18.7\text{A}}{\sqrt{2}\sqrt{2}} = 9.35\text{A rms}$$

The reverse leakage current is given by

$$i_R = \frac{19.1\text{V}}{1000\Omega + 1\Omega} \times \sin \omega t = 0.019 \times \sin \omega t$$

which gives an rms current of

$$i_{Rrms} = \frac{19\text{mA}}{\sqrt{2}\sqrt{2}} = 9.5\text{mA rms}$$

The power dissipated in the 1Ω load resistor is

$$P_L = \left(i_{F_{rms}}^2 + i_{R_{rms}}^2\right) \times R_L$$
$$= \left(9.35^2 + 0.0095^2\right) \times 1\Omega = 87.42\text{W} + 90\mu\text{W} = 87.42\text{W}$$

Clearly, the reverse leakage current related component is negligible.

v. With the square wave, from part iii., 107.32W are dissipated in the load but from part ii., only 87.42W are dissipated for a sine wave with the same fundamental magnitude. The 19.9W difference is power produced by the harmonics of the fundamental (3rd, 5th, …). For a resistive heating load this power produces useful heating, but in a motor the harmonic power would produce unwanted torque pulsations and motor heating.

♣

2.4.2 Semiconductor physics based junction diode model

The charge-carrier diode model shown in figure 2.5 is necessary for transient circuit analysis involving diodes. The pn junction diode is assumed to have an abrupt or step junction. The model components are voltage dependant current sources, I_n and I_b, voltage dependant capacitance C_t and C_j, and series access resistance R_s.

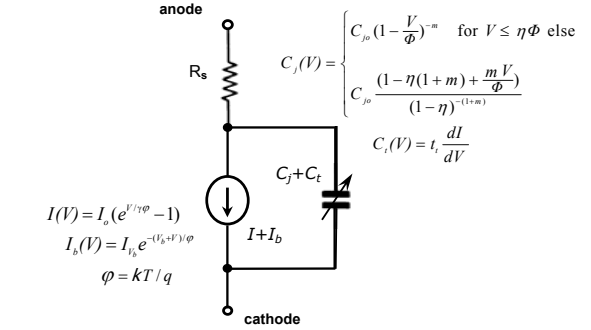


Figure 2.5. *PSpice transient analysis circuit model of the pn junction diode.*

The ideal diode current I is given by equation (2.6). The diode current I_b models reverse voltage breakdown, where the breakdown voltage V_b is assumed due to avalanche and is given by equation (2.3). The voltage dependant transit capacitance, C_t, which is dominant under forward bias, is related to the minority carrier lifetime t_t. The voltage dependant scl (depletion layer) capacitance C_j, which is dominant under reverse bias, involves the zero bias junction potential voltage Φ, given by equation (2.1) and the zero bias junction capacitance C_{jo}. In the case of the silicon carbide Schottky diode, $C_j >> C_t$. The scl capacitance, $C_j(V)$ can be evaluated from the pn diode structure and doping profile, as follows.

2.4.2i - Determination of C_{jo}

Poisson's equation, in conjunction with Gauss's law, for the one dimensional step junction shown in figure 2.6, give

$$\frac{d^2V}{dx^2} = -\frac{d\xi}{dx} = \frac{qN_D}{\varepsilon_s} = -\frac{qN_A}{\varepsilon_s} \qquad (2.9)$$

The dielectric permittivity $\varepsilon_s = \varepsilon_r \varepsilon_o$ comprises the free space permittivity $\varepsilon_o = 8.854\text{x}10^{-12}$ F/m and the relative permittivity $\varepsilon_r = 11.8$ for silicon and 9.7 for SiC.

$$\frac{d\xi(x)}{dx} = \begin{cases} \frac{q}{\varepsilon_s} N_D & \text{for} \quad -x_n < x < 0 \\ -\frac{q}{\varepsilon_s} N_A & \text{for} \quad 0 < x < x_p \end{cases} \tag{2.10}$$

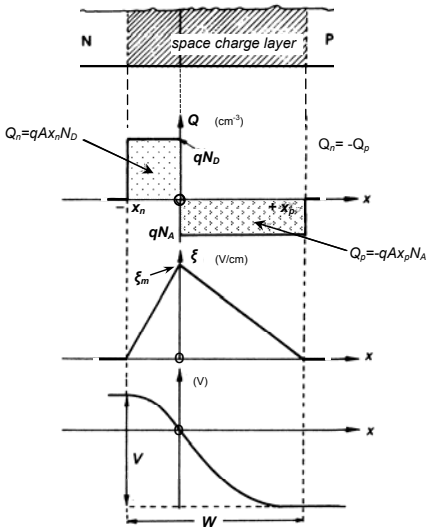


Figure 2.6. *The charge Q, electric field ξ, and voltage potential V, in the space charge layer of a step pn junction.*

Integrating both parts of equation (2.10) over the shown bounds, gives $\xi(x)$:

$$\frac{dV(x)}{dx} = \xi(x) = \begin{cases} \frac{q}{\varepsilon_s} N_D x + \xi_m & \text{for} \quad -x_n < x < 0 \\ -\frac{q}{\varepsilon_s} N_A x + \xi_m & \text{for} \quad 0 < x < x_p \end{cases} \tag{2.11}$$

where the maximium field intensity (at $x = 0$) is $\xi_m = \frac{q}{\varepsilon_s} N_D x_n = \frac{q}{\varepsilon_s} N_A x_p$

The piece-wise parabolic voltage potential across the scl shown in figure 2.6, is given by integration of the electric field, that is

$$\begin{aligned} V &= \int_{-x_n}^{0} \left(\frac{q}{\varepsilon_s} N_D x + \xi_m\right) dx \; + \; \int_{0}^{x_p} \left(-\frac{q}{\varepsilon_s} N_A x + \xi_m\right) dx \\ &= \tfrac{1}{2} \xi_m W \end{aligned} \tag{2.12}$$

Since the charges each side of the metallurgical junction must balance, equation (2.12) can be rearranged to give the scl width.

$$W = \sqrt{\left[\frac{2\varepsilon_s V}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]} \tag{2.13}$$

From equation (2.1), a zero bias voltage Φ exists without the presence of any external voltage. Therefore, to incorporate non-equilibrium conditions, the electrostatic barrier potential becomes Φ-V, where V is the externally applied reverse bias voltage. Consequently the expression for the scl width becomes:

$$W = \sqrt{\left[\frac{2\varepsilon_s (\boldsymbol{\Phi} - \boldsymbol{V})}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]} \tag{2.14}$$

The scl width voltage dependence can be expressed in terms of the zero bias scl width, W_0

$$\begin{aligned} W(\boldsymbol{V}) &= \sqrt{\left[\frac{2\varepsilon_s \boldsymbol{\Phi}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]} \sqrt{1 - \frac{\boldsymbol{V}}{\boldsymbol{\Phi}}} \\ &= W_0 \sqrt{1 - \frac{\boldsymbol{V}}{\boldsymbol{\Phi}}} \end{aligned} \tag{2.15}$$

$$\begin{aligned} x_{n0} &= \frac{W_0}{1 + N_D / N_A} \qquad & x_{p0} &= \frac{W_0}{1 + N_A / N_D} \\ x_n(V) &= x_{n0} \sqrt{1 - \frac{\boldsymbol{V}}{\boldsymbol{\Phi}}} \qquad & x_p(V) &= x_{p0} \sqrt{1 - \frac{\boldsymbol{V}}{\boldsymbol{\Phi}}} \end{aligned} \tag{2.16}$$

The magnitude of the voltage dependant charge on each side of the junction is

$$\begin{aligned} |Q(V)| &= q A \frac{N_D N_A}{N_D + N_A} W = A\left[2q\varepsilon_s \boldsymbol{\Phi} \frac{N_D N_A}{N_D + N_A}\right]^{\frac{1}{2}} \sqrt{1 - \frac{\boldsymbol{V}}{\boldsymbol{\Phi}}} \\ &= Q_0 \sqrt{1 - \frac{\boldsymbol{V}}{\boldsymbol{\Phi}}} \end{aligned} \tag{2.17}$$

The junction capacitance is given by differentiation of equation (2.17) with respect to Φ-V

$$C_j = \left|\frac{dQ}{d(\boldsymbol{\Phi} - V)}\right| = \varepsilon_s A \left[\frac{q}{2\varepsilon_s (\boldsymbol{\Phi} - \boldsymbol{V})} \frac{N_D N_A}{N_D + N_A}\right]^{\frac{1}{2}} = \frac{\varepsilon_s A}{W} \tag{2.18}$$

Equation (2.18) can be rearranged to give the PSpice capacitance form, in terms of the zero bias junction capacitance C_{jo}.

$$C_j(V) = \frac{C_{jo}}{\left(1 - \frac{V}{\Phi}\right)^{\frac{1}{2}}} \qquad \text{where } C_{jo} = \varepsilon_s A \left[\frac{q}{2\varepsilon_s \Phi} \frac{N_D N_A}{N_D + N_A}\right]^{\frac{1}{2}} \qquad (2.19)$$

The electric field at the metallurgical junction, from equation (2.12) is given by

$$\xi_j(V) = \xi_0 \sqrt{1 - \frac{V}{\Phi}} \quad \text{where} \quad \xi_0 = 2\Phi / W_0 \qquad (2.20)$$

2.4.2ii - One-sided pn diode equations

When $N_A >> N_D$, which is the usual case in high voltage pn diodes, equations (2.12) to (2.20) are approximated by the following one-sided diode equations.

$$W_0 = \sqrt{\left[\frac{2\varepsilon_s \Phi}{q N_D}\right]} \approx x_{no} \quad \text{and} \quad x_{po} \approx 0$$

$$Q_0 = A\sqrt{2q\varepsilon_s \Phi N_D} \qquad (2.21)$$

$$C_{jo} = \varepsilon_s A \sqrt{\frac{q N_D}{2\varepsilon_s \Phi}}$$

These equations show that the scl penetrates mostly into the n-side, (hence the name one-sided), which supports most of the voltage.

Example 2.3: ***Space charge layer parameter values***

A 10μm thick p-type $2\text{x}10^{16}$ /cc silicon epitaxial layer is grown on an n^--type $1\text{x}10^{14}$ /cc silicon substrate, of area 1 cm^2, to form an abrupt pn junction.

Calculate the following PSpice parameter values, at room temperature:

- ***i.*** zero bias junction potential, Φ;
- ***ii.*** zero bias scl width, maximum electric field, charge, and junction capacitance, W_0, ξ_0, Q_0, C_{jo}; and
- ***iii.*** avalanche breakdown voltage, V_b.

If the substrate is 150μm thick, for a 1000V reverse bias, calculate:

- ***iv.*** scl width and penetration depth each side of the junction, W, x_n, x_p;
- ***v.*** charge each side of the junction, maximum electric field, and the capacitance, Q, ξ_0, C_j.

Solution

i. From equation (2.1), the zero bias built-in voltage is

$$\Phi = \frac{kT_j}{q} \ln \frac{N_A N_D}{n_i^2} = 0.0259 \ln \frac{2\times10^{16} \times 1\times10^{14}}{2.25\times10^{20}}$$
$$= 0.0259 \ln(8.89\times10^{0}) = 0.534\text{V}$$

ii. From equations (2.15), (2.20), (2.17), and (2.19)

$$W_0 = \sqrt{\left[\frac{2\Phi\,\varepsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]}$$

$$W_0 = \sqrt{\left[\frac{2\times0.53\times11.8\times8.85\times10^{-12}}{1.6\times10^{-19}}\left\{\frac{1}{2\times10^{22}} + \frac{1}{1\times10^{20}}\right\}\right]} = 2.65\,\mu\text{m}$$

$$\xi_0 = 2\ \Phi / W = 2\times0.534/2.65\mu\text{m}$$
$$\xi_0 = 0.40\ \text{MV/m}$$

$$Q_0 = A\left[2q\varepsilon_s \Phi \frac{N_D N_A}{N_D + N_A}\right]^{\frac{1}{2}}$$

$$Q_0 = 1\times10^{-4}\sqrt{2\times0.53\times1.6\times10^{-19}\times11.8\times8.85\times10^{-12}\ \frac{2\times10^{42}}{2.01\times10^{22}}} = 4.21\ \text{nC}$$

$$C_{jo} = A\left[\frac{q\varepsilon_s}{2\Phi} \frac{N_D N_A}{N_D + N_A}\right]^{\frac{1}{2}}$$

$$C_{jo} = 1\times10^{-4}\left[\frac{1.6\times10^{-19}\times11.8\times8.85\times10^{-12}}{2\times0.53} \frac{2\times10^{42}}{2.01\times10^{22}}\right]^{\frac{1}{2}} = 3.95\times10^{-9}\,\text{F} = 3.95\ \text{nF}$$

iii. From equation (2.2), the estimated punch-through voltage is

$$V_{PT} = 7.67\times10^{-16} N_c W_c^2 = 7.67\times10^{-16}\times10^{14}\times(150)^2 = 1727\text{V}$$

That is, punch through occurs when the reverse bias is greater than the operating voltage, 1000V. If the diode is to breakdown due to avalanche then the avalanche breakdown voltage given by V_b (equation (2.3)) must be less than V_{PT}, 1727V.

$$V_b = 5.34\times10^{13}\ N_c^{-2/7} = 5.34\times10^{13}\times(1\times10^{14})^{-2/7} = 1689\text{V}$$

iv. From equation (2.15) the scl width at -1000V reverse bias is

$$W = W_0\sqrt{1 - \frac{V}{\Phi}} = 2.65\mu\sqrt{1 + \frac{1000}{0.533}}$$
$$= 114.6\mu\text{m}$$

From equation (2.16) the scl penetration into each side of the junction at -1000V is

$$x_n = \frac{W}{1+N_D/N_A} = \frac{114.6}{1+0.005} \qquad x_p = \frac{W}{1+N_A/N_D} = \frac{114.6}{1+200}$$

$$x_n = 114.0\mu\text{m} \qquad x_p = 0.57\mu\text{m}$$

Note that when $N_A >> N_D$, $x_n \approx W$, thus the lower the relative concentration, the deeper the scl penetration and the higher the portion of V supported in N_D. The junction scl can under these circumstances be analysed based on simplified equations – called one-sided junction equations.

v. The charge magnitude each side of the junction, shown in figure 2.6, is given by equation (2.17). The electric field at the junction is given by equation (2.20), while the junction capacitance at -1000V is given by equation (2.19):

$$Q_j = Q_0\sqrt{1-\frac{V}{\Phi}} = 4.21\text{n}\sqrt{1+\frac{1000}{0.533}}$$

$$= 182{\cdot}4\,\text{nC}$$

$$\xi_j = \xi_0\sqrt{1-\frac{V}{\Phi}} = 0.40\text{M}\sqrt{1+\frac{1000}{0.533}}$$

$$\xi_j = 17.5\,\text{MV/m} \qquad \left(< \xi_b = 25\text{MV/m}\right)$$

$$C_j = C_{jo}\left(1-\frac{V}{\Phi}\right)^{-\frac{1}{2}} = 3.95\text{n}\left(1+\frac{1000}{0.533}\right)^{-\frac{1}{2}}$$

$$= 91\text{pF}$$

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Reading list

See chapter 1 reading list.

Fraser, D. A., *The Physics of Semiconductor Devices*, OUP, 1977.

Wolf, H. F., *Semiconductors*, John Wiley-Interscience, New York, 1977.

Yang, E. S., *Fundamentals of Semiconductor Devices*, McGraw-Hill, 1978.

Problems

2.1. A silicon diode is to have a breakdown voltage of 1000 V. If breakdown is due to the avalanche mechanism calculate
   i. the concentration of the n^- region
   ii. the width of the n^- region
   iii. the maximum electric field
   iv. the expected punch-through voltage based on parts i. and ii.
   [2×10^{14}/cc, 83µm, $2.4\text{x}10^5$ V/cm, 1057 V]

2.2. What is the punch-through voltage for a silicon step junction with an n^- doping level of $5\text{x}10^{13}$ /cc and a width of 20µm? Calculate the doping level and scl width for a similarly voltage rated silicon avalanche diode assuming equations (2.3) and (2.5) are valid.
   [15.3 V, $5.27\text{x}10^{16}$/cc, 0.63µm]

2.3. An abrupt silicon pn junction consists of a p-type region containing 10^{16} cm^{-3} acceptors and an n-type region containing $5\text{x}10^{14}$ cm^{-3} donors. Calculate
   i. the built-in potential of this p-n junction.
   ii. the total width of the scl region if the applied voltage V_a equals 0, 0.5 and -100 V.
   iii. maximum electric field in the scl region at 0, 0.5 and -100 V.
   iv. the potential across the scl region in the n-type semiconductor at 0, 0.5 and -100 V.

2.4. Consider an abrupt pn diode with $N_A = 10^{18}$ cm^{-3} and $N_D = 10^{16}$ cm^{-3}. Calculate the junction capacitance at zero bias if the diode area is 10^{-4} cm^2. Repeat the problem while treating the diode as a one-sided diode and calculate the relative error.

2.5. Repeat example 2.1 using the single-sided diode equations in equation (2.21), where $N_A >> N_D$. Calculate the percentage error in using the assumptions.

2.6. A silicon pn diode with $N_A = 10^{18}$ cm^3 has a capacitance of 10^{-7} F/cm^2 at an applied reverse voltage of 1V. Calculate the donor density N_D.

2.7. A silicon pn diode has a maximum electric field magnitude of 10^7 V/cm and a scl width of 200µm. The acceptor concentration is 100 times the donor density. Calculate each doping density.

2.8. Repeat example 2.1 for the equivalent 4H silicon carbide junction diode having the same electrical operating conditions. Use the silicon carbide data given below.

See problems 10.4, 10.5, and 10.9 to 10.12.
Useful *SI* data for silicon and silicon carbide:
$q = -1.6\text{x}10^{-19}$ C $\xi_0 = 8.85\text{x}10^{-12}$ F/m $\xi_{r\text{Si}} = 11.8$ $\xi_{r\text{SiC}} = 9.7$ $kT/q = 0.0259$ eV at 300ºC
$n_{i\text{Si}} = 1.5\text{x}10^{16}$ m^{-3} $n_{i\text{SiC}} = 2.5\text{x}10^{-3}$ m^{-3}

3

Power Switching Devices and their Static Electrical Characteristics

There is a vast proliferation of power switching semiconductor devices, each offering various features, attributes, and limitations. The principal device families of concern in the power switching semiconductor range are the diode, transistor, and thyristor. Each family category has numerous different members. The basic characteristics of the three families and a range of their members will be analysed.

3.1 Power diodes

The diode is the simplest semiconductor device, comprising one pn junction. In attempts to improve both static and dynamic diode electrical properties for different application conditions, numerous diode types have evolved.

3.1.1 The pn fast-recovery diode

The doping concentration on each side of the junction influences the avalanche breakdown voltage, the contact potential, and the series resistance of the diode. The junction diode normally has the p-side highly doped compared with the n-side, and the lightly doped n-region determines many of the properties of the device. The n-region gives the device its high-voltage breakdown and under reverse bias, the scl penetrates deeply into the n-side. The lower the n-type concentration and the wider the n-side, the higher will be the reverse voltage rating and also, the higher the forward resistance. These n-region requirements can lead to thermal I^2R problems in silicon. Larger junction areas help reduce the thermal instability problem.

It is usual to terminate the lightly doped n-region with a heavily doped n^+ layer to simplify ohmic contact and to reduce the access resistance to the scl. For better n-region width control, n-type silicon is epitaxially grown on an n^+ substrate. The p^+ anode is diffused or implanted into the epitaxial region, forming an epitaxial diode.

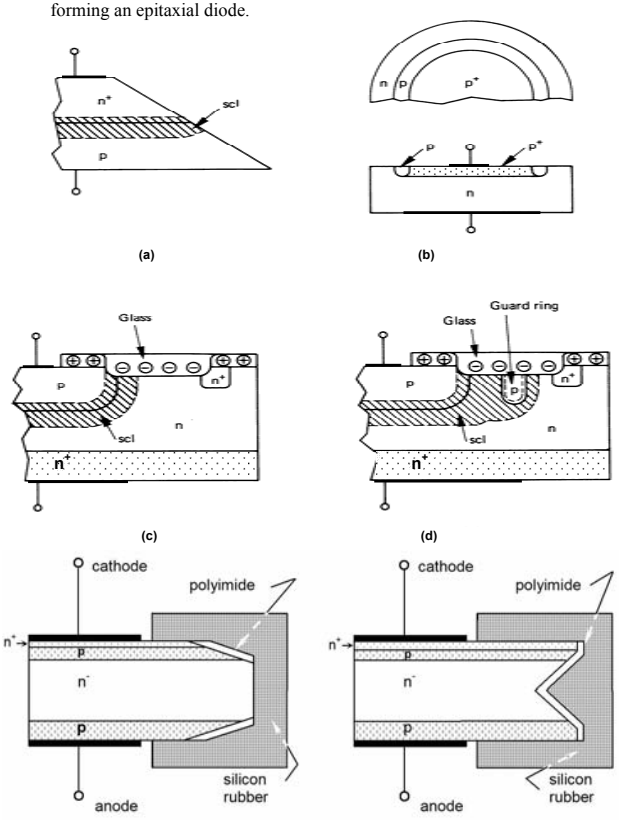

Figure 3.1. *To prevent edge breakdown under junction reverse bias: (a) reduction of the space charge region near the bevel; (b) p-type guard ring; (c) glass guard ring; (d) glass plus p-type guard ring; (e) double negative bevel; and (f) double positive bevel angle.*

In devices specifically designed for high reverse bias applications, care must be taken to avoid premature breakdown across the edge of the die or where the junction surfaces. Premature edge breakdown is reduced by *bevelling* the edge as shown in figure 3.la, or by diffusing a *guard ring* as shown in figure 3.lb, which isolates the junction from the edge of the wafer. The scl electric field is lower at the bevelled edge than it is in the main body of the device. In the case of a lightly doped p-type guard ring, the scl is wider in the p-ring, because of its lower concentration, than in the p^+ region. The maximum electric field is therefore lower at the pn-ring junction for a given reverse bias voltage. Negatively charged glass film techniques are also employed to widen the scl near the surface, as shown in figures 3.1c and 3.1d. Multiple guard rings are sometimes employed for very high breakdown voltage devices. Similar techniques are extendable to devices other than diodes, such as thyristors. Field control bevelling on more complex junction structures is achieved with double-negative or double-positive bevelling as shown in parts e and f of figure 3.1. The bevelling is accomplished by grinding, followed by etching of the bevel surface to restore the silicon crystalline mechanical and structure quality. The processed area is passivated with a thin layer of polyimide, which is covered in silicon rubber. Negative bevels tend to be more stable electrically with ageing.

The foregoing discussion is directly applicable to the rectifier diode, but other considerations are also important if fast switching properties are required. The turn-on and reverse recovery time of a junction are minimised by reducing the amount of stored charge in the neutral regions and by minimising carrier lifetimes. *Lifetime killing* is achieved by adding gold or platinum, which is an efficient recombination centre. Electron and proton irradiation are preferred non-invasive lifetime control methods. Irradiation gives the lowest forward recovery voltage and the lowest reverse leakage current. The improved switching times must be traded off against increased leakage current and on-stage voltage. Switching times are also improved by minimising the length (thickness) of the n-region.

3.1.2 The p-i-n diode

The transient performance of diodes tends to deteriorate as the thickness of the silicon wafer is increased in attaining higher reverse voltage ratings. Gold lifetime killing only aggravates the adverse effects incurred with increased thickness. The p-i-n diode allows a much thinner wafer than its conventional pn counterpart, thus facilitating improved switching properties.

The p-i-n diode is a pn junction with a doping profile tailored so that an intrinsic layer, the i-region, is sandwiched between the p-layer and the n-layer, as shown in figure 3.2. In practice, the idealised *i-region* is approximated by a high resistivity n-layer referred to as a *v-layer*. Because of the low doping in the v-layer, the scl will penetrate deeply and most of the reverse bias potential will be supported across this region.

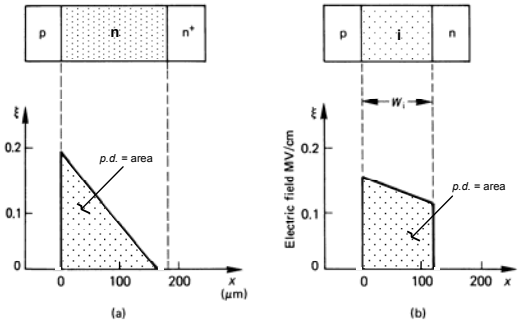

Figure 3.2. *Cross-section and electric field distribution of: (a) a pn diode and (b) a p-i-n diode.*

The power p-i-n diode can be fabricated by using either the epitaxial process or the diffusion of p and n-regions into a high-resistivity semiconductor substrate. The i-region width W_i, specifies the reverse voltage breakdown of the p-i-n diode, which is the area under the electric field in figure 3.2b, viz.,

$$V_b \approx \xi_b W \approx 25 W_i \text{ (in μm)} \quad \text{(V)} \qquad (3.1)$$

The thickness W_i, along with the distribution of any gold within it, determines the nature of the reverse and forward-conducting characteristics. These characteristics are more efficient in fast p-i-n diodes than in the traditional pn structures.

3.1.3 The power Zener diode

Zener diodes are pn diodes used extensively as voltage reference sources and voltage clamps. The diode reverse breakdown voltage is used as the reference or clamping voltage level.

The leakage current in a good pn diode remains small up to the reverse breakdown point where the characteristic has a sharp bend. Such a characteristic is called *hard*. Premature breakdown at weak spots in the junction area or periphery cause high leakage currents before final breakdown, and such diodes are said to have *soft* breakdown characteristics.

Zener diodes are especially made to operate in the breakdown range. Above a few volts, the breakdown mechanism is avalanche multiplication rather than Zener and the breakdown reference voltage V_Z is obtained by proper selection of the pn junction doping levels. Once in breakdown V_Z remains almost constant provided the manufacturer's power rating, $P = V_Z I$, is not exceeded. Where the breakdown

mechanism is due to the Zener effect, the temperature coefficient is negative, about -0.1 per cent/K, changing to positive, +0.1 per cent/K, after about 4.5V when the avalanche multiplication mechanism predominates.

Zener diodes require a hard breakdown characteristic not involving any local hot spots. They are available in a voltage range from a few volts to about 280V and with power dissipations ranging from 250mW to 75W, with heat sinking. Transient suppressing Zener diodes can absorb up to 50kW, provided energy limits and number of cycles are not exceeded, as shown in figure 10.19.

Practically, Zener diodes are difficult to make, less than ideal in application, and should be avoided if possible. The basic *I-V* characteristics, and electrical circuit symbol for the different types of diodes, are shown in figure 3.3.

3.1.4 The Schottky barrier diode

The *Schottky diode* is a metal-semiconductor device which offers low on-state voltages, but in silicon is presently restricted to applications imposing a reverse bias of less than 400V. At lower voltages, less than 40V, devices of up to 300A are available and the maximum junction operating temperature is 175°C, which is higher than for conventional silicon pn junction devices.

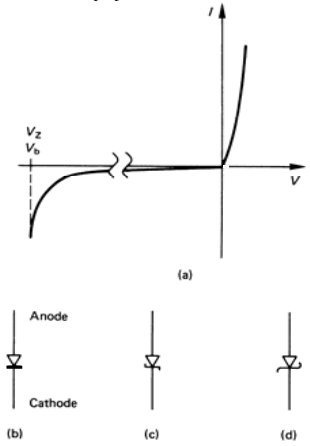

Figure 3.3. *Diodes: (a) static I-V characteristic; (b) symbol for a rectifier diode; (c) voltage reference or Zener diode; and (d) Schottky barrier diode.*

The Schottky diode is formed by a metal (such as chromium, platinum, tungsten or molybdenum) in homogeneous contact with a substrate piece of n-type silicon, as shown in figure 3.4a. The contact is characterised by a potential barrier Φ_b

which determines the forward and reverse properties of the Schottky diode.

In forward conduction, electrons are emitted from the negative potential n-type silicon to the positive potential metal, passing over the barrier potential. Unlike the bipolar pn diode, only electrons are carriers, hence the Schottky barrier diode is a unipolar device. The forward on-state voltage drop is dominated by and proportional to the barrier potential Φ_b, while unfortunately the reverse leakage current is approximately inversely related. Thus a Schottky diode with a very low forward voltage drop will have very high reverse leakage current relative to the pn diode counterpart, as shown in figure 3.5.

Chromium provides the lowest forward voltage drop but is limited to an operating temperature of 125°C and has a high leakage current. Platinum allows operating temperatures to 175°C with a leakage current several orders of magnitude lower than chromium. The trade-off is a higher forward voltage.

A guard ring is used to improve device robustness, but its function is to act like a Zener diode and thus protect the Schottky barrier under excessive reverse bias. An optimally designed epitaxial layer, as shown in figure 3.4b, is also employed which reduces the field at the less than perfect metal-semiconductor interface and allows the whole interface to go safely into reverse bias breakdown.

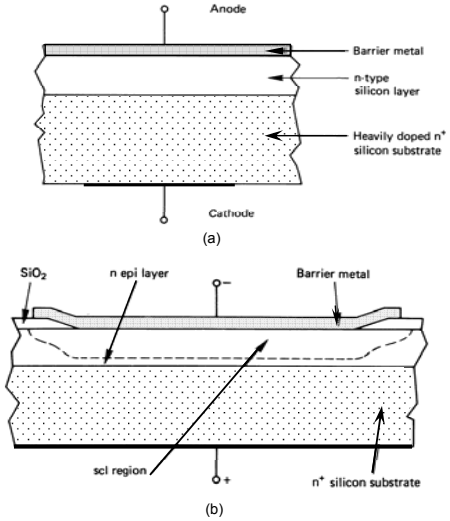

Figure 3.4. *The Schottky barrier diode: (a) the basic structure and (b) the space charge layer region extending into the epi-substrate region under reverse bias.*

There are a number of important differences between Schottky barrier and pn junction diodes.

- In a pn diode, the reverse bias leakage current is the result of minority carriers diffusing into the scl and being swept across it. This current level is highly temperature-sensitive. In the Schottky-barrier case, reverse current is the result of majority carriers that overcome the barrier. A much higher value results at room temperature, but is not temperature-dependent.
- The forward current is mostly injected from the n-type semiconductor into the metal and very little excess minority charge is able to accumulate in the semiconductor. Since minimal minority carrier recombination occurs, the Schottky barrier diode is able to switch rapidly from forward conduction to reverse blocking.
- Since under forward bias, barrier injection comes only from the semiconductor, and there is little recombination in the scl; thus the device can be well represented by the ideal diode equation (2.6).
- The majority electrons injected over the barrier into the metal have much higher energy than the other metal electrons which are in thermal equilibrium. Those injected electrons are therefore called *hot,* and the diode in some applications is referred to as a *hot electron diode.*

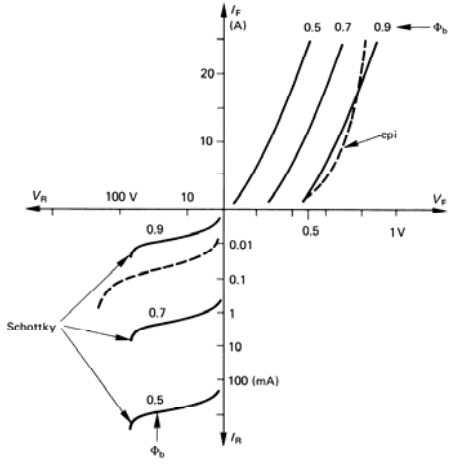

Figure 3.5. *Schottky and epi diode I-V characteristics with different Schottky barrier potentials.*

An important point arising from this brief consideration of the Schottky barrier diode is the importance of the connection of an n-type region to aluminium metallization that occurs in unipolar and bipolar semiconductor devices. A practical method of forming aluminium ohmic contacts on n-type materials is by doping the semiconductor very heavily, above the degeneracy level. Thus, in the contact region, if a barrier exists, the scl width is small enough to allow carriers to tunnel through the barrier in both directions. On the other hand, aluminium makes a good ohmic contact on p-type silicon since the required p^+ surface layer is formed during the heat treatment of the contact after the aluminium is deposited. An ohmic contact acts as a virtual sink for minority carriers, because it has an enormous supply of majority carriers.

3.1.5 The silicon carbide Schottky barrier diode

Silicon carbide Schottky diodes are attractive for high voltages because the field breakdown of silicon carbide is eight times that of silicon. Additionally the wide band gap allows higher operating temperatures. Both nickel and titanium can be used as Schottky metals. Boron atoms (a dose of $1x10^{15}$ /cm^2 at 30keV) are implanted to form the edge termination that spreads any field crowding at the edge of the metal contact, as shown in figure 3.6. The lower barrier height of titanium produces a lower forward voltage device, but with a higher reverse leakage current, than when nickel is used as the barrier metal.

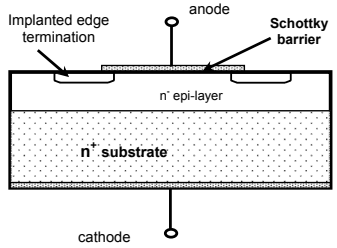

Figure 3.6. *The silicon carbide Schottky barrier diode structure.*

3.2 Power switching transistors

Two types of transistor are extensively used in power switching circuits, namely the power metal oxide semiconductor field effect transistor (MOSFET) and the insulated gate bipolar transistor (IGBT). The IGBT has a bipolar junction transistor (BJT) output stage and a MOSFET input stage, in a *Darlington* pair configuration. Many of the IGBT power handling properties are associated with the limitations of the BJT. Thus some attention to the BJT's electrical characteristics is necessary, even though it is virtually obsolete as a discrete power-switching device.

- The **BJT** consists of a pnp or npn single-crystal silicon structure. It operates by the injection and collection of minority carriers, both electrons and holes, and is therefore termed a *bipolar transistor.*
- The **MOSFET** depends on the voltage control of a depletion width and is a majority carrier device. It is therefore a *unipolar transistor*.
- The **IGBT** has the desirable voltage input drive characteristics of the MOSFET but the power switching disadvantages of the minority carrier mechanisms of the BJT.

3.2.1 The bipolar npn power switching transistor (BJT)

As a discrete electrical device, the high-voltage, power-switching bipolar junction transistor, BJT, is virtually obsolete. The BJT has one unique redeeming electrical characteristic, viz.; it can conduct hundreds of amperes with an extremely low on-state voltage of less than 100mV, when saturated. Although superseded, its basic electrical operating characteristics are fundamental to the operation of most other power switching devices. Specifically, the MOSFET has a parasitic npn BJT, as shown in figure 3.14, that can cause false turn-on other than for the fact that understanding of BJT characteristics allows circumvention of the problem. The fundamental operation of thyristors (SCR, GTO, and GCT) relies totally on BJT characteristics and electrical mechanisms. The IGBT has two parasitic BJTs, as shown in figure 3.16, that form an undesirable pnp-npn SCR structure. Understanding of BJT gain mechanisms allows virtual deactivation of the SCR.

The first bipolar transistors were mainly pnp, and were fabricated by alloying techniques and employed germanium semiconductor materials. Most transistors are now npn, made of silicon, and utilise selective diffusion and oxide masking.

A typical high-voltage *triple-diffused* transistor doping profile is shown in figure 3.7a. The n-collector region is the initial high-resistivity silicon material and the collector n^+ diffusion is performed first, usually into both sides. One n^+ diffusion is lapped off and the p-base and n^+ emitter diffusions are sequentially performed.

A *planar epitaxial* structure is often used for transistors with voltage ratings of less than 1000V. The basic structure and processing steps are shown in figure 3.7b. The n-type collector region is an epitaxial layer grown on an n substrate. The base and emitter are sequentially diffused into the epitaxy. Ion implantation is also used. This approach allows greater control on the depth of the n-type collector region, which is particularly important in specifying device switching and high-voltage properties. Also, the parasitic series collector resistance of the substrate is minimised without compromising the pellet's mechanical strength as a result of a possible reduction in thickness.

3.2.1i - BJT gain

Figure 3.8 shows an npn bipolar transistor connected in the *common emitter* configuration. In this configuration, injection of electrons from the lower n^+p junction into the centre p-region supplies minority carrier electrons to participate in the reverse current through the upper np junction.

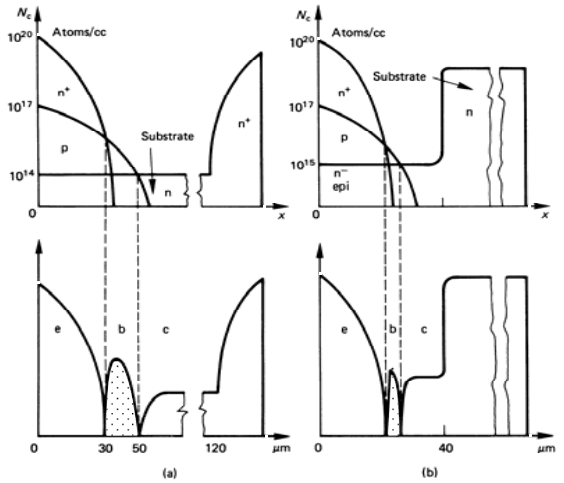

Figure 3.7. *Impurity profile in two types of npn transistors: (a) a planar triple-diffused npn transistor obtained by three consecutive diffusions into a uniformly doped n-type substrate and (b) planar epitaxial npn transistor, obtained after two diffusions into n-type epitaxial layer which is first grown on a low-resistivity n-type silicon substrate.*

The n^+ region which serves as the source of injected electrons is called the *emitter* and forms the emitter junction with the *p-base,* while the n-region into which electrons are swept by the reverse bias np junction is called the *collector* and, with the p-base, forms the collector junction.

To have a 'good' npn transistor almost all the electrons injected by the emitter into the base should be collected. Thus the p-base region should be narrow and the electron minority carrier lifetime should be long to ensure that the average electron injected at the emitter will diffuse to the collector scl without recombining in the base. The average lifetime of electrons in the p-base increases as the p-base concentration decreases, that is as the hole concentration decreases. The fraction of electrons which reach the collector is called the *base transport factor,* b_t. Electrons lost to recombination in the p-base must be re-supplied through the base contact. It is also required that the emitter junction carrier flow should be composed almost entirely of electrons injected into the base, rather than holes crossing from the base region to the emitter. Any such holes must be provided by the base current, which is minimised by doping the base region lightly compared with the emitter such that an n^+p emitter results. Such a junction is said to have a high *injection efficiency,* γ. A low lattice defect density also increases the injection efficiency.

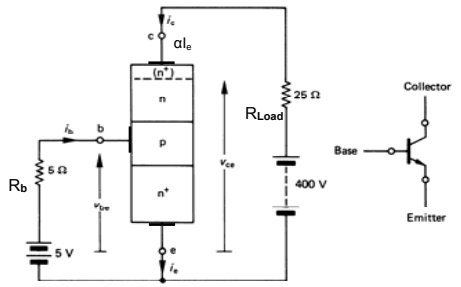

Figure 3.8. *Common emitter junction bias conditions for an npn transistor and the npn bipolar junction transistor circuit symbol.*

The relationship between collector and emitter current is

$$\frac{i_c}{i_e} = b_t \gamma = \alpha \tag{3.2}$$

The factor α is called the *current transfer ratio.* Since base current is necessary, α is less than 1, but close to 1, if the BJT

- has a good base transport factor, $b_t \approx 1$
  (narrow base width and with long minority carrier lifetimes) and
- a high emitter injection efficiency, $\gamma \approx 1$
  (high emitter doping relative to the base concentration).

In the common emitter configuration shown in figure 3.8 the ratio between the base current i_b and the collector current i_c, is of practical importance. Since the base current is the difference between the emitter and the collector current

$$\frac{i_c}{i_b} = \frac{i_c}{i_e - i_c} = \frac{i_c / i_b}{1 - i_c / i_b} \tag{3.3}$$

$$= \frac{\alpha}{1-\alpha} = \beta \tag{3.4}$$

The factor β, relating the collector current to the base current, is defined as the base-to-collector *current amplification factor.* If α is near unity, β is large, implying the base current is small compared with the collector current.

3.2.1ii - BJT operating states

In power switching applications, a transistor is controlled in two states which can be referred to as the *off-state* or *cut-off state* and the conduction *on-state.* Ideally the transistor should appear as a short circuit when on and an open circuit when in

the off-state. Furthermore, the transition time between these two states is ideally zero. In reality, transistors only approximate these requirements.

The typical BJT collector output characteristics are shown in figure 3.9 which illustrates the various BJT operating regions. The *saturated on-state* shown in figure 3.9 occurs when both the collector and emitter junctions are forward biased. Consequently, the collector emitter voltage $V_{ce(sat)}$ is less than the base to emitter voltage $V_{be(sat)}$. The voltage breakdown phenomenon is of particular importance to the high-voltage, power-switching BJT, and is due to the characteristics of the device structure and geometry.

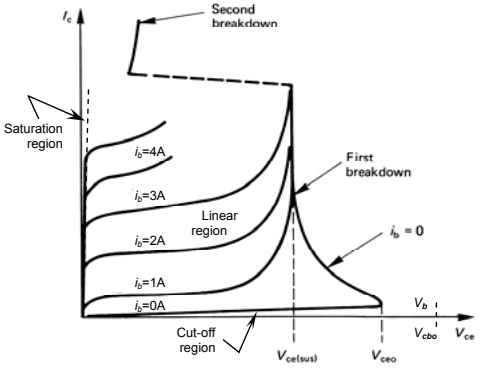

Figure 3.9. *Output characteristics of a common emitter connected transistor showing its operating regions and the voltage breakdown range.*

3.2.1iii - BJT maximum voltage - first and second breakdown

The collector junction supports the off-state voltage and in so doing develops a wide scl. This scl increases in width with increased reverse bias, penetrating into the base. It is unusual that a correctly designed high-voltage power switching BJT would break down as a result of punch-through of the collector scl through the base to the emitter scl. Because of the profile of the diffused base, collector junction voltage breakdown is usually due to the avalanche multiplication mechanism, created by the high electric field at the collector junction. In the common emitter configuration shown in figure 3.9, the transistor usually breaks down gradually, but before the collector junction avalanches at V_b. This occurs because the avalanche-generated holes in the collector scl are swept by the high field into the base. The emitter injects electrons in order to maintain base neutrality. This emitter junction current in turn causes more collector current, creating more avalanche pairs and causing a regenerative action. This voltage dependant avalanche effect is modelled by

$$M = \frac{1}{1-(v_{ce}/V_b)^m} \qquad (3.5)$$

Thus the gain mechanisms of the transistor cause collector to emitter breakdown - *first breakdown,* at voltage V_{ceo}, to occur before collector to base avalanche breakdown, at voltage V_{cbo}, which from $\alpha M = 1$ are related according to

$$V_{ceo} = V_{cbo}(1-\alpha)^{1/m} \approx V_{cbo}/\beta^{1/m}$$
$$= V_b/\beta^{1/m} \quad \text{(V)} \qquad (3.6)$$

where the avalanche breakdown voltage V_b is given by equation (2.3);
$m \approx 6$ for a silicon p^+n collector junction; and
$m \approx 4$ for a silicon n^+p collector junction.

Contradictory device properties are that the higher the forward gain, the lower the breakdown voltage. A much higher collector emitter breakdown voltage level can be attained if the base emitter junction is reverse biased in the off-state.

First breakdown need not be catastrophic provided junction temperature limits are not exceeded. If local hot spots occur because of non-uniform current density distribution as a result of crystal faults, doping fluctuation, etc., *second breakdown* occurs. Silicon crystal melting and irreparable damage results, the collector voltage falls and the current increases rapidly as shown in figure 3.9.

3.2.2 *The metal oxide semiconductor field effect transistor (MOSFET)*

The basic low-power lateral structure of the metal oxide semiconductor field effect transistor (MOSFET) is illustrated in figure 3.10a. The n^+ *source* and *drain* regions are diffused or implanted into the relatively lightly doped p-type substrate, and a thin silicon dioxide layer insulates the aluminium *gate* from the silicon surface. No lateral current flows from the drain to source without a conducting n-channel between them, since the drain-to-source path comprises two series, oppositely-directed pn junctions.

When a positive gate voltage is applied with respect to the source as shown in figure 3.10b, positive charges are created on the metal gate. In response, negative charges are induced in the underlying silicon, by the formation of a depletion region and a thin surface region containing mobile electrons. Effectively the positive gate potential *inverts* the p-channel, forming an electron-enhanced low-resistance *n-channel,* allowing current to flow freely in either direction between the drain and source. The inversion channel is essentially devoid of the thermal properties associated with the typical BJT.

An important parameter in mos transistors is the *threshold voltage* V_{TH}, which is the minimum positive gate voltage to induce the n-conducting channel. With zero gate voltage the structure is normally off. The device is considered to operate in the *enhancement mode* since the application of a positive gate voltage in excess of V_{TH} induces an n-conducting channel. The typical output characteristics of the MOSFET are shown in figure 3.10c.

3.2.2i - *MOSFET structure and characteristics*

The conventional horizontal structure in figure 3.10a has severe limitations associated with increasing die area that make it uneconomical for consideration as a viable high-current structure. A planar vertical n-channel dmos structure like those shown in figure 3.11 is used to overcome the inherent poor area utilisation of the basic mos structure. The peripheral p floating field guard is not shown.

The dmos structure is a vertical current flow device. An n^- epitaxial layer is grown on an n^+ substrate. A series of p body regions are next diffused into the epitaxial layer. Then n^+ source regions are diffused within the p body regions and a polycrystalline silicon gate is embedded in the silicon dioxide insulating layer. Source and gate metallization are deposited on the top surface of the die and the drain contact made to the bottom surface. Cell density is inversely related to voltage rating and varies from 200,000 to 1,000,000 cells per cm^2.

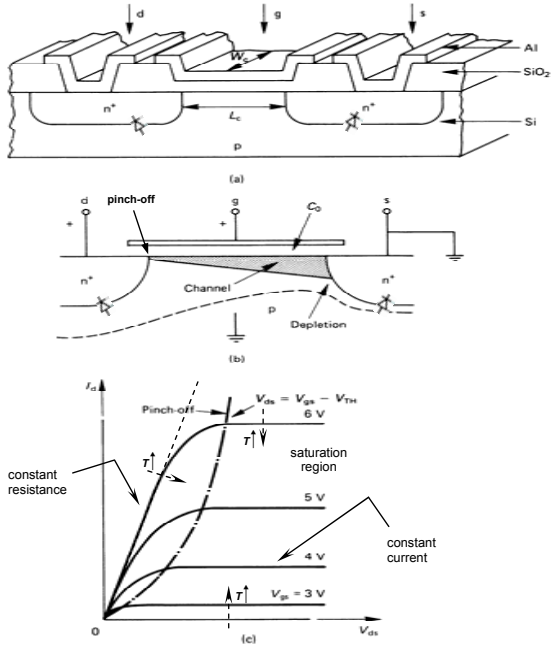

Figure 3.10. *Enhancement-type n-channel mos transistor: (a) device cross-section; (b) induced n-channel near pinch-off; and (c) drain I-V characteristics as a function of gate voltage, showing the pinch-off locus and effects of increased temperature.*

With a positive gate voltage, the device turns on and majority carriers flow laterally from the source to the drain region below the gate and vertically to the drain contact. Current can also flow freely in the reverse direction in the channel since the channel is bipolar conducting once enhanced.

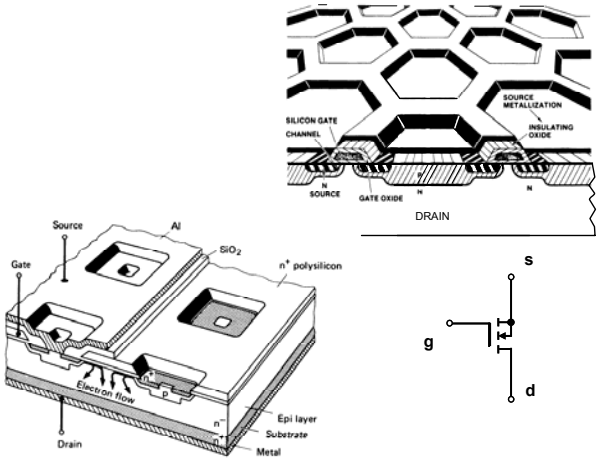

Figure 3.11. *Two designs for the n-channel MOSFET and its circuit symbol (courtesy of Infineon and International Rectifier).*

The obtainable drain-to-source breakdown voltage is not limited by the gate geometry. The scl associated with voltage blocking penetrates mostly in the n-type epitaxial layer. Thickness and doping concentration of this layer are thus decisive in specifying the blocking capability of the power MOSFET.

The basic drain current versus drain to source voltage static operating characteristics of the power MOSFET are illustrated in figure 3.10c. For a given gate voltage, there are two main operating regions on the drain current-voltage characteristic.

- The first is a *constant resistance* region, where an increase in drain to source voltage results in a proportional increase in drain current. (In practice, the effective resistance increases at higher drain currents.)
- At a certain drain current level, for a given gate voltage, a channel pinch-off effect occurs and the operating characteristic moves into a *constant current* region.

3.2.2ii - MOSFET drain current

When the power MOSFET is used as a switch, it is controlled in the on-condition, such that it is forced to operate in the resistive region. This ensures that the voltage

drop across the device is low so that the drain current is essentially defined by the load and the device power dissipation is minimal. Thus for switching applications, the on-resistance $R_{ds(on)}$ is an important characteristic because it will specify the on-state power loss for a given drain current. The lower $R_{ds(on)}$ is, the higher the current-handling capabilities of the device; thus $R_{ds(on)}$ is one important figure of merit of a power MOSFET.

A quadratic MOSFET model allows the inversion layer charge between the source and the drain to vary. For power MOSFETs that have short channels, the drain current I_d is related to the channel dimensions and the gate voltage V_{gs} according to

at low current, above pinch-off

$$I_d = \tfrac{1}{2}\mu\frac{W_c}{L_c}C_a(V_{gs}-V_{TH})^2 \qquad \text{(A)} \qquad (3.7)$$

if $V_{ds} \geq V_{gs}-V_{TH}$ for n-channel MOSFETs, as shown to the left of the pinch-off locus in figure 3.10c.

at high current after electron velocity saturation, the quadratic model is invalid and

$$I_d = \tfrac{1}{2}v_{sat}W_cC_a(V_{gs}-V_{TH}) \qquad \text{(A)} \qquad (3.8)$$

where C_a is the capacitance per unit area of the gate oxide (ε/t_{ox})
W_c is the width of the channel
v_{sat} is the saturation velocity of electrons in silicon, ($5.0\text{x}10^6$ cm/s)
L_c is the effective channel length
μ is the conducting channel carrier mobility, (300 cm^2/V-s).

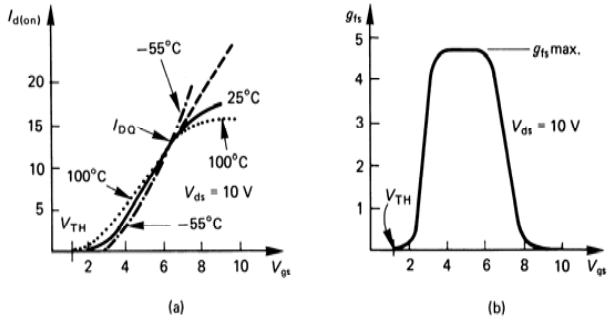

Figure 3.12. *MOSFET gate voltage characteristics: (a) transfer characteristics of gate voltage versus drain current and (b) transconductance characteristics of gate voltage versus transconductance, g_{fs}.*

Figure 3.12a shows that drain current exhibits both a positive and negative temperature coefficient with the drain current I_{DQ} being the boundary condition. If the drain current is greater than I_{DQ} there is a possibility of destruction by over-

current at low temperatures, while if the drain current is less than I_{DQ}, over-current can produce thermal runaway and destruction. Operation with a gate voltage corresponding to I_{DQ} avoids the need for any gate drive temperature compensation.
At high gate voltages, the on-resistance of the resistive region and the drain current in the constant current region, become somewhat independent of the gate voltage. This phenomenon is best illustrated in the I_d versus V_{ds} characteristic by the curve cramping at high gate voltages in figure 3.10c.

3.2.2iii - MOSFET transconductance

Inspection of the static drain source characteristics of figure 3.10c reveals that as the gate voltage increases from zero, initially the drain current does not increase significantly. Only when a certain threshold gate voltage, V_{TH}, has been reached, does the drain current start to increase noticeably. This is more clearly illustrated in figure 3.12b which shows the characteristics of drain current I_d and small signal transconductance g_{fs} versus gate voltage, at a fixed drain voltage. It will be seen from these characteristics that no conduction occurs until V_{gs} reaches the threshold level, V_{TH}, after which the I_d versus V_{gs} characteristic becomes linear, the slope being the transconductance g_{fs}.
The amplification factor, forward *transconductance, g_{fs},* is defined as

$$g_{fs} \triangleq \left| \frac{\partial I_d}{\partial V_{gs}} \right|_{V_{ds}=\text{constant}}$$

Differentiating equations (3.7) and (3.8) gives

at low current

$$g_{fs} = \mu \frac{W_c}{L_c} C_a (V_{gs} - V_{TH}) \qquad \text{(mho)} \qquad (3.9)$$

at high current

$$g_{fs} = \tfrac{1}{2} v_{sat} W_c C_a \qquad \text{(mho)} \qquad (3.10)$$

At high electric fields, that is high currents, the carrier velocity v_{sat} saturates. Inherent in the MOSFET structure are voltage-dependent capacitances and on-state resistance.

A typical minimum threshold voltage is about 2V and exhibits temperature dependence of approximately -10mV per K (α = 0.5 per cent/K), as shown in figure 3.13. At high gate voltages, the drain current becomes constant as the transconductance falls to zero, implying the upper limit of forward drain current. The temperature variation of transconductance is small, typically -0.2 per cent/K, which results in extremely stable switching characteristics. The typical temperature coefficient for the gain of a bipolar transistor, the MOSFET equivalent to g_{fs} is +0.8 per cent/K. The temperature dependence of the MOSFET forward conductance is approximated by

$$g_{fs}(T) \approx g_{fs}(25°\text{C}) \times \left(\frac{T}{300} \right)^{-2.3} \qquad \text{(mho)} \qquad (3.11)$$

since temperature effects are dominated by mobility variation with temperature.

3.2.2iv - MOSFET on-state resistance

In the fully on-state the drain-source conduction characteristics of the MOSFET can be considered as purely resistive. The *on-resistance* $R_{ds(on)}$ is the sum of the epitaxial region resistance, the channel resistance, which is modulated by the gate source voltage, and the lead and connection resistance. One reason for the wide proliferation of special gate geometries is to produce extremely short, reproducible channels, in order to reduce $R_{ds(on)}$. In high-voltage devices, the on-resistance is dominated by the resistance of the epitaxial drain region when the device is fully enhanced. For high-voltage n-channel devices the on-state resistance is approximated by

$$R_{ds(on)} = 8.3 \times 10^{-7} \times V_b^{2.5} / A \qquad (\Omega) \qquad (3.12)$$

where V_b is the breakdown voltage in volts
A is the die area in mm^2.

A p-channel device with the same V_b as an n-channel device has an $R_{ds(on)}$ two to three times larger.
For low-voltage devices

$$R_{ds(on)} = L_c D / 34 A \qquad (\Omega) \qquad (3.13)$$

where D is the distance between cells in µm.

The factor $1/g_{fs}$ of $R_{ds(on)}$ is added to give the total $R_{ds(on)}$. On-state drain-source loss can therefore be based on $I_d^2 R_{ds(on)}$. On-resistance $R_{ds(on)}$ increases with temperature and approximately doubles over the range 25°C to 200°C, having a positive temperature coefficient of approximately +0.7 per cent/K above 25ºC, as shown in figure 3.13. The temperature dependence of the on-state resistance is approximated by

$$R_{ds(on)}(T) = R_{ds(on)}(25°\text{C}) \times \left(\frac{T}{300} \right)^{2.3} \qquad (\Omega) \qquad (3.14)$$

where the temperature T is in degrees Kelvin. This relationship closely follows the mobility charge dependence with temperature.
Since $R_{ds(on)}$ increases with temperature, current is automatically diverted away from a hot spot. Thus unlike the bipolar transistor, second breakdown cannot occur within the MOSFET. The breakdown voltage V_b has a positive temperature coefficient of typically 0.1 per cent/K as shown by $V_{(BR)DSS}$ in figure 3.13.

3.2.2v - MOSFET p-channel device

P-channel MOSFETs are very similar to n-channel devices except that the n and p regions are interchanged. In p-channel devices the on-resistance, for a given die area, will be approximately twice that of a comparable n-channel device. The reason for this is that in the n-channel device the majority carriers are electrons but in the p-channel device, the majority carriers are holes which have lower mobility. If the area of a p-channel device is increased to produce an equal $R_{ds(on)}$, then the various capacitances of the p-channel device will be larger, and the device costs will be greater.

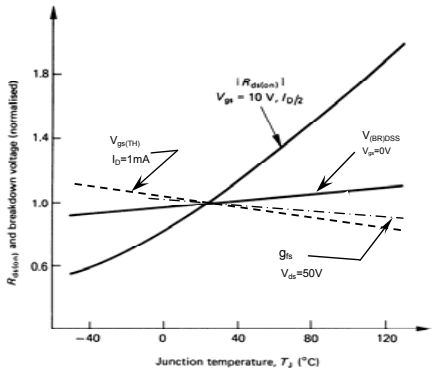

Figure 3.13. *Normalised drain-source on-resistance, transconductance, gate threshold voltage, and breakdown voltage versus junction temperature.*

Example 3.1: ***Properties of an n-channel MOSFET cell***

A silicon n-channel MOSFET cell has a threshold voltage of V_{TH} = 2V, W_c = 10μm, L_c = 1μm, and an oxide thickness of t_{ox} = 50nm. The device is biased with V_{GS} = 10V and V_{DS} = 100V.

i. Assuming a quadratic model and a surface carrier mobility of 300 cm^2/V-s, calculate the drain current and transconductance.

ii. Assuming carrier velocity saturation ($5x10^6$ cm/s), calculate the drain current and transconductance.

Solution

i. The MOSFET is biased in saturation since $V_{ds} > V_{gs}$ - V_{TH} . Therefore, from equation (3.7) the drain current equals:

$$I_d = ½\mu C_a \frac{W_c}{L_c}(V_{gs} - V_{TH})^2$$

$$= \frac{300\times10^{-4}}{2} \times \frac{3.85\times8.85\times10^{-12}}{50\times10^{-9}} \times \frac{10}{1} \times (10-2)^2 = 6.5 \text{ mA}$$

From equation (3.9), the transconductance equals:

$$g_{fs} = \mu C_a \frac{W_c}{L_c}(V_{gs} - V_{TH})$$

$$= 300\times10^{-4} \times \frac{3.85\times8.85\times10^{-14}}{50\times10^{-9}} \times \frac{10}{1} \times (10\text{-}2) = 1.64 \text{ mho}$$

ii. When the electron velocity saturates, the drain current is given by equation 3.8

$$I_d = ½ v_{sat} W_c C_a (V_{gs} - V_{TH})$$

$$= ½ \times 5\times10^4 \times 10^{-5} \times \frac{3.85\times8.85\times10^{-12}}{50\times10^{-9}} \times (10\text{-}2) = 136 \text{ mA}$$

The transconductance is given by equation 3.10

$$g_{fs} = ½ v_{sat} W_c C_a$$

$$= ½ \times 5\times10^4 \times 10^{-5} \times \frac{3.85\times8.85\times10^{-12}}{50\times10^{-9}} = 16.1 \text{ mho}$$

♣

3.2.2vi - MOSFET parasitic BJT

Figure 3.14 shows the MOSFET equivalent circuit based on its structure and features. The parasitic npn transistor shown in figure 3.14b is key to device operation and limitations.

Capacitance exists within the structure from the gate to the source, C_{gs}, the gate to the drain, C_{gd}, and from the drain to the source, C_{ds}. The capacitance C_{gs}. varies little with voltage; however C_{ds} and C_{gd} vary significantly with voltage. Obviously these capacitances influence the switching intervals, an aspect considered in chapter 4.4.2.

The emitter of the parasitic npn transistor is the source of the MOSFET, the base is the p-type body and the collector is the drain region. In the construction of the MOSFET, the emitter and base of the npn transistor are purposely shorted out by the source metallization to disable the parasitic device by reducing its injection efficiency. However, this short circuit cannot be perfect and R_{be} models the lateral p-body resistance, while C_{ob} is essentially C_{ds}. The npn transistor has a collector-emitter breakdown voltage, between V_{cbo} and V_{ceo}. If an external *dv/dt* is applied between the drain and source as shown in figure 3.14b, enough displacement current could flow through C_{ob} to generate a voltage drop across R_{be} sufficient to turn on the parasitic bipolar device, causing MOSFET failure in second breakdown.

When the drain to source voltage is negative, current can flow from the source to drain through R_{be} and the base to collector junction of the parasitic npn transistor within the structure, the dashed line shown in figure 3.14b. This is termed the *body diode*, inherent in the MOSFET structure.

3.2.2vii - MOSFET on-state resistance reduction

Most power switching devices have a *vertical structure*, where the gate and source of the MOSFET (or emitter in the case of the IGBT) are on one surface of the substrate, while the drain (or collector) is on the other substrate surface. The principal current flows vertically through the substrate but the conductive channel is lateral due to the *planar gate structure*, as shown in figure 3.11. The structure resistance components between the drain and source are:

- the drift region;
- the JFET region;
- the accumulation region; and
- the channel region.

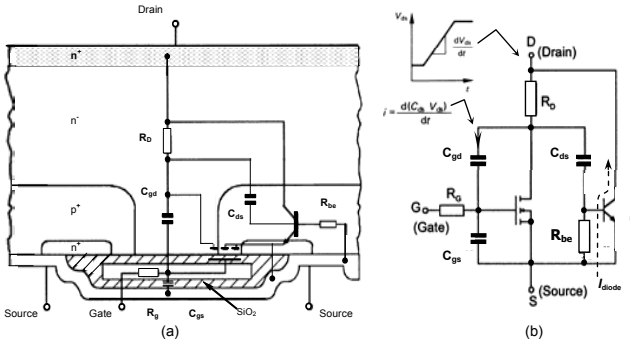

Figure 3.14. *MOSFET: (a) structure and (b) equivalent circuit diagram with parasitic npn bipolar transistor forming an inverse diode.*

The drift region contribution dominates whilst the contribution from the ohmic contacts and n^+ substrate are not significant, in high voltage devices. The channel voltage drop is proportional to channel length and inversely related to width. The channel should therefore be short, but its length is related to voltage rating since it must support the off-state scl.

Whilst retaining the necessary voltage breakdown length properties, two basic approaches have been pursued to achieve a more vertical gate (channel) structure, viz., the trench gate and vertical super-junction, as shown in parts b and c of figure 3.15. Both techniques involve increased fabrication complexity and extra costs.

1 - Trench gate

A channel is formed on the vertical sidewalls of a trench etched into the die surface as shown in figure 3.14b. The JFET resistive region is eliminated, which not only reduces the total resistance but allows smaller cell size thereby increasing channel density and decreases the short-circuit capacity. The trench corners must be rounded to avoid high electric field stress points. By extending the gate into the drift region, the gate to drain capacitance increases, hence increases gate charge requirements.

2 - Vertical super-junction

The structure has vertical p-conducting regions in the voltage sustaining n^- drift area, that are extend to the p-wells below the gate, as shown in figure 3.14c. In the off-state, the electric field is not only in the vertical direction but also in the horizontal plane. This means the n-drift region width can be decreased, the on-state resistance is decreased, and the gate charge is reduced for a given surface area. Up to sixteen mask steps are needed which involves repeated cycles of n-type epi-layer growth, masked boron implantation, and finally diffusion. The resultant specific resistance is near linearly related to breakdown voltage, as opposed to $R_{ds(on)} \times Area \propto V_{br}^{2.5}$, equation (3.12). Typically $R_{ds(on)}$ is five times lower than for the conventional MOSFET, which only uses up to six mask steps.

Whilst the trench gate concept can be readily applied to other field effect devices without voltage rating limits, the vertical super-junction is confined to the MOSFET, and then at voltage ratings below about 1000V.

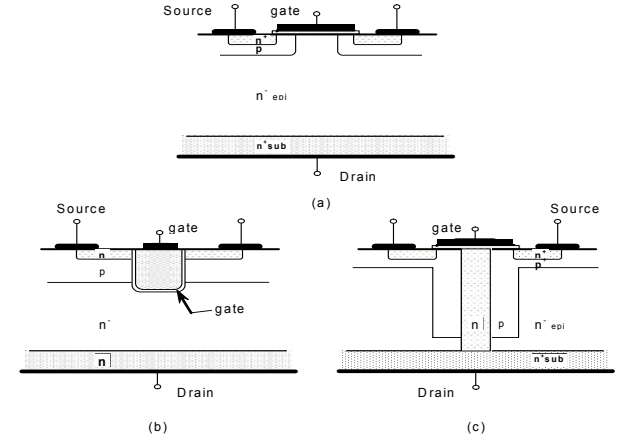

Figure 3.15. *Three MOSFET channel structures: (a) conventional planar gate; (b) trench gate; and (c) vertical superjunction.*

3.2.3 The insulated gate bipolar transistor (IGBT)

The high off-state and low on-state voltage characteristics of the bipolar junction transistor are combined with the high input impedance properties of the MOSFET to form the insulated gate bipolar transistor, IGBT, as shown in figure 3.16. The basic structure is that of a MOSFET but with a p^+ substrate. This p^+ collector provides reverse blocking capabilities of typically 40V.

3.2.3i -IGBT at turn-on

Electrons from the n^- drift region flowing into the p^+ collector region, cause holes to be emitted from the high efficiency p^+ region into the drift region. Some of the holes flow to the emitter p^+ region as well as through the lateral mos-channel into the n^+ well. This charge enhancement causes the scl, hence collector voltage, to collapse as the device turns on.

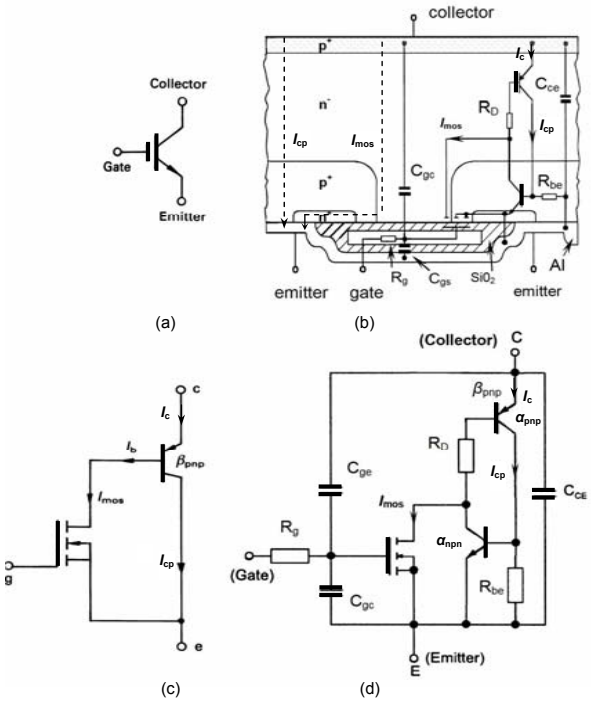

Figure 3.16. *Insulated gate bipolar transistor (IGBT): (a) circuit symbol; (b) physical structure showing current paths: (c) normal operation equivalent circuit; and (d) high current latching equivalent circuit.*

3.2.3ii - IGBT in the on-state

The p^+ substrate conductively modulates the n^- region with minority carriers, which whilst conducting the main collector current, produces a low on-state voltage at the expense of a 0.6 to 0.8V offset in the output voltage characteristics due to the collector pn junction. From figure 3.16c, the IGBT collector current is approximated by

$$I_c = I_{mos}(1+\beta_{pnp}) \qquad (3.15)$$

3.2.3iii - IGBT at turn-off

Excess p-stored charge that remains after the high voltage scl has been established must recombine in the externally inaccessible n^- drift region. This storage charge produces a tail current.

The operational mechanisms are those of any minority carrier device and result in slower switching times than the majority carrier MOSFET. On-state voltage and switching characteristics can be significantly improved by using the trench gate technique used on the MOSFET, as considered in section 3.2.1 and shown in figure 3.15b. A less stable structure improvement involves using wider trenches, judiciously spaced, so that accumulate holes under the trench enhance emitter injection of electrons. This injection enhancement reduces the on-state voltage without degrading the switching performance.

Further performance enhancement is gained by using the punch through, PT-IGBT, structure shown in figure 3.17a, which incorporates an n^+ buffer region. The conventional non-punch through NPT-IGBT structure is shown in figure 3.17b. Both collector structures can have the same emitter structure, whether a lateral gate as shown, or the MOSFET trench gate in figure 3.15b.

Figure 3.17 shows the electric field in the off-state, where the PT-IGBT develops a field as in the pin diode in figure 3.2b, which allows a thinner wafer. The NPT-IGBT requires a thicker wafer (about 200µm for a 1200V device) which results in a larger substrate resistance and a slower switching device.

- **The PT-IGBT** has n^+ and n^- layers formed by epitaxial growth on a p^+ substrate. The electric field plot in figure 3.17b shows that the off-state voltage scl consumes the n^- substrate and is rapidly reduced to zero in the n^+ buffer.
- **The NPT-IGBT** has a lightly doped n^- substrate with the p-regions (p wells and p collector) formed by ion implantation. The electric field distribution in figure 3.17b shows that the n^- drift region has to be wide enough to support all the off-state voltage, without punch through to the p collector implant.

3.2.3iv - IGBT latch-up

The equivalent circuit in figure 3.16d shows non-ideal components associated with the ideal MOSFET. The parasitic npn bipolar junction transistor (the n^+ emitter/ p^+ well/ n^- drift region are the BJT e-b-c) and the pnp transistor (p^+ collector/ n^- drift/ p^+ well are the BJT e-b-c) couple together to form an SCR thyristor structure, as considered in section 3.3. Latching of this parasitic SCR can occur:

- in the on-state if the current density exceeds a critical level, which adversely decreases with increased temperature or
- during the turn-off voltage rise when the hole current increases in sensitive regions of the structure due to the charge movement associated with the scl widening.

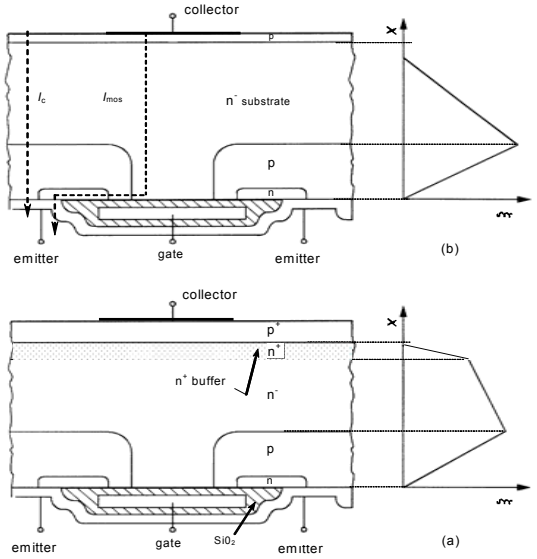

Figure 3.17. *Insulated gate bipolar transistor structures and electric field profile: (a) fieldstop PT-IGBT and (b) conventional NPT-IGBT.*

1 - IGBT on-state SCR static latch-up is related to the temperature dependant transistor gains which are related to the BJT base transport factor b_t and emitter injection efficiency γ, defined for the BJT in equation (3.2)

$$\alpha_{pnp} + \alpha_{npn} = b_{t_{pnp}}\gamma_{pnp} + b_{t_{pnp}}\gamma_{pnp} = 1 \qquad (3.16)$$

To avoid loss of control and possible IGBT failure, the factors in equation (3.16), which is valid for on-state latch-up, are judiciously adjusted in the device design.

Common to both device types is the gate structure, hence the base-emitter junction of the npn parasitic BJT have the same properties. In each structure, the shorting resistor R_{be} decreases the injection efficiency of the npn BJT emitter. This resistance is minimized by highly doping the p^+ wells directly below the n-emitters and by shortening the length of the n-emitter. The gain α_{npn} in equation (3.16) is decreased since the injection efficiency γ_{npn} is lowered.

Reduction of the pnp BJT gain of the PT-IGBT and NPT-IGBT is achieved with different techniques.

- ***For the NPT-IGBT***, the emitter injection efficiency of holes from the p^+ zone into the n^- drift region is high because of the large difference in doping concentrations at the junction. This yields a high injection efficiency γ_{pnp}. The base transport factor $b_{t\ pnp}$ is already low because of the large width of the n^- drift region, and is further reduced by lifetime killing of minority carriers in the n^- drift region by using gold doping or electron beam radiation.
- ***For the PT-IGBT***, the p^+ emitting junction at the collector is a well-controlled shallow implant thus reducing the injection efficiency γ_{pnp}. Charge carrier lifetime killing in the n^- drift region to reduce the base transport factor b_{tpnp}, is therefore not necessary.

2 - IGBT turn-off SCR dynamic latch-up can occur while the collector voltage is rising, before the collector current decreases. Equation (3.16) is modified by equation (3.5) to account for voltage avalanche multiplication effects.

$$M_{npn}\alpha_{npn} + M_{pnp}\alpha_{pnp} = 1 \qquad (3.17)$$

where $M = \dfrac{1}{1-(v_{ce}/V_b)^m}$

This dynamic latch-up mode is adversely affected by increased temperature and current magnitude during the voltage rise time at turn-off.
Since $v_{ce} \ll V_b$, $M \to 1$, and the multiplication effect is not significant in the on-state static latch-up analysis. IGBTs are designed and rated so that the latch-up current is 10 to 15 times the rated current.

PT IGBT and NPT IGBT comparison

Generally, faster switching speed is traded for lower on-state losses.

Table 3.1 PT versus NPT IGBTs

IGBT TYPE	PT IGBT	NPT IGBT
conduction loss (same switching speed)	Lower $v_{ce(sat)}$ Decreases slightly with temperature A slight positive temperature co-efficient at high current densities allows parallel connection.	Higher $v_{ce(sat)}$ Increases with temperature Suitable for parallel connection
switching speed (same on-state loss)	Faster switching due to high gain and reduced minority carrier lifetime	
short circuit rating		more rugged due to wider base and low pnp gain
turn-on switching loss	Largely unaffected by temperature	Largely unaffected by temperature
turn-off switching loss	Loss increases with temperature but lower than NPT devices to start with	Virtually constant with temperature

3.2.4 The junction field effect transistor (JFET)

The field effect for a FET may be created in two ways:

- A voltage signal controls charge indirectly using a capacitive effect as in the MOSFET, section 3.2.2.
- In a junction FET (JFET), the voltage dependant scl width of a junction is used to control the effective cross-sectional area of a conducting channel. If the zero bias voltage cuts off the channel then the JFET is *normally off*, otherwise if a reverse bias is needed to cut-off the channel, the JFET is termed *normally on*.

The electrical properties of SiC make the JFET a viable possibility as a power switch. Two normally on JFET structures are shown in figure 3.18, where it is seen how the scl layer decreases the channel width as the source to gate voltage reverse bias increases. In SiC, the channel has a positive temperature coefficient, $R_{on} \propto T^{2.6}$, hence parallel connection is viable. Natural current saturation with a positive temperature coefficient means lengthy short-circuit currents of over a millisecond can be sustained. Although the channel is bidirectional, in the biased off-state an integral fast, robust pn body diode is inherent as seen in figure 3.18b.

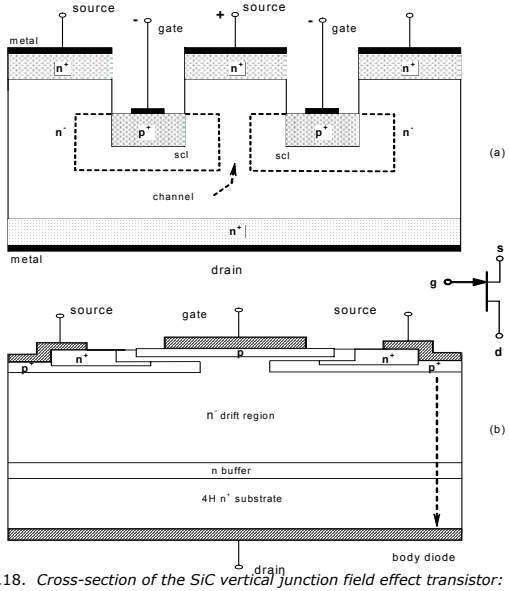

Figure 3.18. *Cross-section of the SiC vertical junction field effect transistor: (a) trench gate with channel shown and (b) variation incorporating a pn body diode.*

3.3 Thyristors

The name thyristor is a generic term for a bipolar semiconductor device which comprises four semiconductor layers and operates as a switch having a latched on-state and a stable off-state. Numerous members of the thyristor family exist. The simplest structurally is the silicon-controlled rectifier (SCR) while the most complicated is the triac.

3.3.1 The silicon-controlled rectifier (SCR)

The basic SCR structure and doping profile in figure 3.19 depicts the SCR as three pn junctions J1, J2, and J3 in series. The contact electrode to the outer p-layer is called the ***anode*** and that to the outer n-layer is termed the ***cathode.*** With a ***gate*** contact to the inner p-region, the resultant three-terminal thyristor device is technically called the silicon-controlled rectifier (SCR).

A low concentration n-type silicon wafer is chosen as the starting material. A single diffusion process is then used to form simultaneously the p1 and p2 layers. Finally, an n-type layer, n1, is diffused selectively into one side of the wafer to form the cathode. The masked-out areas are used for the gate contact to the p1 region. To prevent premature breakdown at the surface edge, bevelling is used as in figure 3.1, to ensure that breakdown will occur uniformly in the bulk.

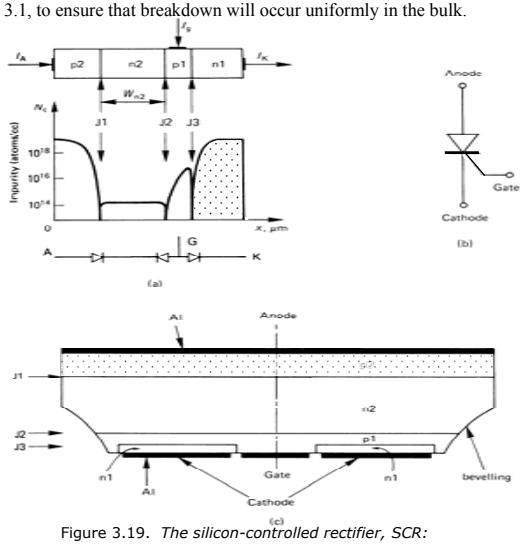

Figure 3.19. *The silicon-controlled rectifier, SCR:*
(a) net impurity density profile;(b) circuit symbol; and (c) cross-sectional view.

A number of observations can be made about the doping profile of the SCR which relate to its electrical characteristics.

The anode and cathode would both be expected to be good emitters of minority carriers into the n2 and p1 regions respectively because of their relative high concentrations with respect to their injected regions.

The n2 region is very wide, typically hundreds of micrometres, and low concentration, typically less than 10^{14} /cc. Even though the hole lifetime may be very long, 100µs, the base transport factor for hole minority carriers, $b_{t\text{-}n2}$ is low. The low-concentration provides high forward and reverse blocking capability and the associated reverse-biased scl's penetrate deeply into the n2 region. Gold lifetime killing or electron irradiation, most effective in the n2 region, is employed to improve the switching speed by increasing the number of carrier recombination centres.

The two-transistor model of the SCR shown in figure 3.20 can be used to represent the p2-n2-pl-nl structure and explain its characteristics. Transistor T_1 is an npn BJT formed from regions n2-pl-nl while T_2 is a pnp BJT formed from SCR regions p2-n2-pl.

The application of a positive voltage between anode and cathode does not result in conduction because the SCR central junction J2 is reverse-biased and *blocking*. Both equivalent circuit transistors have forward-biased emitter junctions and with reverse-biased collector junctions, both BJT's can be considered to be cut off.

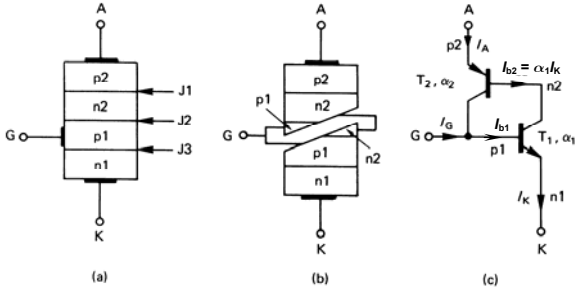

Figure 3.20. *Cross-section of the SCR showing its model derivation: (a) schematic of the SCR cross-section; (b) the division of the SCR into two transistors; and (c) the npn-pnp two-transistor model of the basic SCR.*

3.3.1i - SCR turn-on

It is evident from figure 3.20c that the collector current of the npn transistor provides the base current for the pnp transistor. Also, the collector current of the pnp transistor along with any gate current I_G supplies the base drive for the npn transistor. Thus a *regenerative* situation occurs when the loop gain exceeds unity.

The base current of the pnp transistor T_2 with dc current gain α_2 is

$$I_{b2} = (1 - \alpha_2) I_A - I_{co2}$$

which is supplied by the collector of the npn transistor. The current I_{co} is the collector junction reverse bias leakage current. The collector current of the npn transistor T_1 with a dc current gain of α_1 is given by

$$I_{c1} = \alpha_1 I_K + I_{co1}$$

By equating I_{b2} and I_{c1}

$$(1 - \alpha_2) I_A - I_{co2} = \alpha_1 I_K + I_{co1}$$

Since $I_K = I_A + I_G$

$$I_A = \frac{\alpha_1 I_G + I_{co1} + I_{co2}}{1 - (\alpha_1 + \alpha_2)} = \frac{\alpha_1 I_G + I_{co1} + I_{co2}}{1 - G_1} \qquad \text{(A)} \qquad (3.18)$$

where $\alpha_1+\alpha_2$ is called the *loop again, G_1*. At high voltages, to account for avalanche multiplication effects, the gains are replaced by *Mα,* where *M* is the avalanche multiplication coefficient in equation 3.15. Hence, G_1 becomes $M_1a_1 + M_2a_2$. By inspection of equation (3.18) it can be seen that a large anode current results when $G_1 \rightarrow 1$, whence the circuit regenerates and each transistor drives its counterpart into saturation. All junctions are forward-biased and the total device voltage is approximately that of a single pn junction, with the anode current limited by the external circuit. The n2-p1-n1 device acts like a saturated transistor and provides a remote contact to the n2 region. Therefore the device behaves essentially like a p-i-n diode (p2-i-n1), where the voltage drop across the i-region is inversely proportional to the recombination rate. Typical SCR static *I-V* characteristics are shown in figure 3.21.

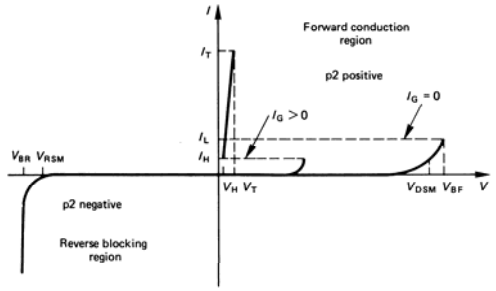

Figure 3.21. *The silicon-controlled rectifier static I-V characteristics.*

At low current levels, α_1 and α_2 are small because of carrier recombination effects, but increase rapidly as current increases. The conventional gate turn-on mechanism is based on these current gain properties. External gate current starts the regeneration action and the subsequent increase in anode current causes the

gains to increase, thus ensuring a high loop gain, whence the gate current can be removed. The *I-V* characteristics in figure 3.21 show this property, where a minimum anode current I_L is necessary for the loop gain to increase sufficiently to enable the SCR to latch on by the regeneration mechanism.
The SCR can be brought into conduction by a number of mechanisms other than via the gate (other than the light activated SCR used in high-voltage dc converters).

- If the anode-cathode voltage causes avalanche multiplication of the central junction, the increased current is sufficient to start the regenerative action. The forward anode-cathode breakover voltage V_{BF} is dependent on the central junction J2 avalanche voltage and the loop gain according to

$$V_{BF} = V_b (1 - \alpha_1 - \alpha_2)^{1/m} \quad \text{(V)} \qquad (3.19)$$

  where the avalanche breakdown voltage, at room temperature, for a typical SCR p^+n central junction is given by (equation (2.3)

$$V_b = 5.34 \times 10^{13} \times N_D^{-3/4} \quad \text{(V)} \qquad (3.20)$$

  where N_D is the concentration of the high resistivity n2 region when $10^{13} < N_D < 5\text{x}10^{14}$ /cc.
- Turn-on can also be induced by means of an anode-to-cathode *applied dv/dt* where the peak ramp voltage is less than V_{BF}. The increasing voltage is supported by the central blocking junction J2. The associated scl width increases and a charging or displacement current flows according to $i = d(Cv)/dt$. The charging current flows across both the anode and cathode junctions, causing hole and electron injection respectively. The same mechanism occurs at the cathode if gate current is applied; hence if the terminal *dv/dt* is large enough, SCR turn-on occurs.
- The forward SCR leakage current, which is the reverse-biased pn junction J2 leakage current, doubles approximately with every 8K temperature rise. At elevated temperatures, the thermally generated leakage current can be sufficient to increase the SCR loop gain such that turn-on occurs.

3.3.1ii - SCR cathode shorts

All SCR turn-on mechanisms are highly temperature-dependent. A structural modification commonly used to reduce device temperature sensitivity and to increase *dv/dt* rating is the introduction of *cathode shorts*. A cross-sectional structure schematic and two-transistor equivalent of the cathode shorting technique are shown in figure 3.22. It will be seen that the cathode metallization overlaps the p1 region, which is the gate contact region. The technique is based on some of the anode forward-blocking current being shunted from the cathode junction via the cathode short. The cathode electron injection efficiency is effectively reduced, thereby decreasing α_1 which results in an increase in the forward voltage-blocking rating V_{BF} and *dv/dt* capability. The holding and latching currents are also increased.

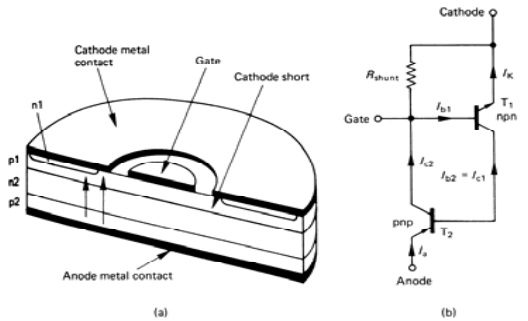

Figure 3.22. *Shorted cathode SCR:*
(a) SCR cross-section showing some anode current flowing through cathode shorts and (b) the SCR two-transistor equivalent circuit SCR with cathode shorts.

The cathode-anode, reverse breakdown voltage V_{BR} is shown in figure 3.21. The anode $p2^+n2$ junction J1 characterises SCR reverse blocking properties and V_{BR} is given by (equation (3.6))

$$V_{BR} = V_b (1 - \alpha_2)^{1/m}$$

If a very high resistivity n2 region, N_{Dn2}, is used and breakdown is due to punch-through to J2, then the terminal breakdown voltage will be approximated by (equation (2.2))

$$V_{PT} = 7.67 \times 10^{-16} N_{Dn2} W_{n2}^2$$

where W_{n2} is the width of the n2 region. This relationship is valid for both forward and reverse SCR voltage breakdown arising from punch-through.

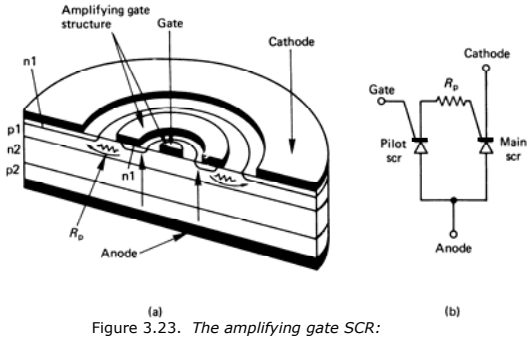

Figure 3.23. *The amplifying gate SCR:*
(a) cross-section of the structure and (b) two-SCR equivalent circuit.

3.3.1iii - SCR amplifying gate

At SCR turn-on, only a small peripheral region of the cathode along the gate region conducts initially. The conducting area spreads at about 50m/s, eventually encompassing the whole cathode area. If at turn-on a very large anode current is required, that is a high *initial di/dt,* a long gate-cathode perimeter is necessary in order to avoid excessively high initial cathode current densities. The usual method employed to effectively enlarge the SCR initial turn-on area is to fabricate an integrated *amplifying gate,* as shown in figure 3.23. A small gate current is used to initiate the *pilot SCR,* which turns on very rapidly because of its small area. The cathode current of this pilot SCR provides a much larger gate current to the main SCR section than the original triggering current. Once the main device is fully on, the pilot device turns off if the gate current is removed.

An important property of the SCR is that once latched on, the gate condition is of little importance. The regenerative action holds the device on and SCR turn-off can only be achieved by reducing the anode current externally to a level below which the loop gain is significantly less than unity.

3.3.2 The asymmetrical silicon-controlled rectifier (ASCR)

The doping profiles and cross-sectional views comparing the asymmetrical SCR and SCR are shown in figure 3.24. In each case the electric field ξ within the p1n2 junction reverse-bias scl is shown and because the n2 region is lightly doped, the scl extends deeply into it. The scl applied reverse-bias voltage is mathematically equal to the integral of the electric field, ξ (area under the curve).

If, in the conventional SCR, the scl edge reaches the $p2^+$ layer, then punch-through has occurred and the SCR turns on. To prevent such a condition and to allow for manufacturing tolerances, the $n2^-$ region is kept thick with the unfortunate consequence that on-state losses, which are proportional to n2 layer thickness, are high.

In the case of the ASCR, a much thinner $n2^-$ region is possible since a highly doped n layer adjacent to the $p2^+$ anode is utilised as an *electric field stopper.* The penalty paid for this layer construction is that in the reverse voltage blocking mode, the $n2p2^+$ junction avalanches at a low voltage of a few tens of volts. Thus the ASCR does not have any usable repetitive reverse-blocking ability, hence the name asymmetrical SCR. By sacrificing reverse-blocking ability, significant improvements in lower on-state voltage, higher forward-blocking voltage, and faster turn-off characteristics are attained.

3.3.3 The reverse-conducting thyristor (RCT)

The RCT is electrically equivalent to an SCR in anti-parallel with a diode, but both are integrated into the same wafer. The reason for integrating the SCR and diode is to minimise the interconnecting lead inductance. The circuit symbol, cross-sectional wafer view, and typical doping profile are shown in figure 3.25.

Since no reverse voltage will be applied to the RCT there is only the cathode-side deep p-diffused layer. This and the ASCR n-region type field stopper result in low forward voltage characteristics. As in the ASCR case, the highly n-type doped anode end of the wide n-region also allows higher forward voltages to be blocked. Both anode and cathode shorts can be employed to improve thermal and *dv/dt* properties. As shown in figure 3.25a, an amplifying gate can be used to improve initial *di/dt* capability.

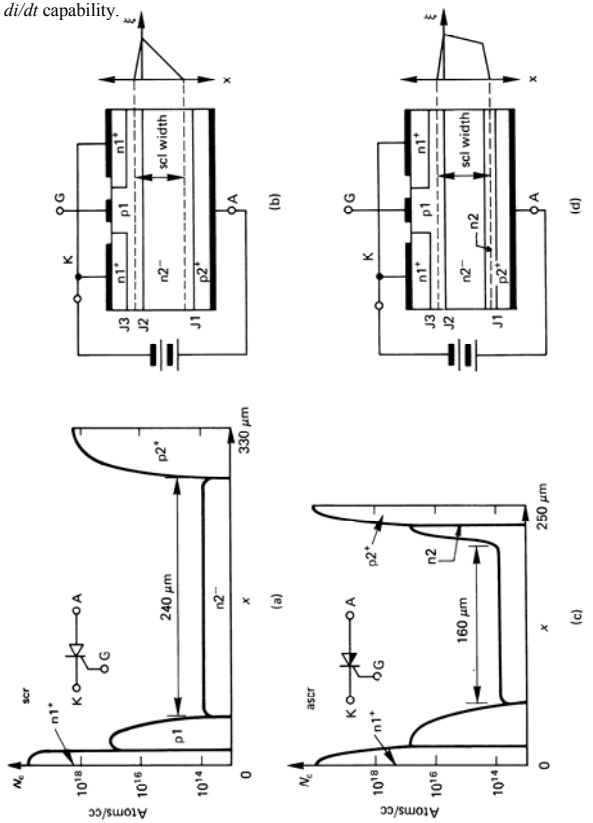

Figure 3.24. *Doping profile and cross-section, including the electric field of J2 in the forward biased off-state for:*
(a) and (b) the conventional SCR; (c) and (d) the asymmetrical SCR.

The integral anti-parallel diode comprises an outer ring and is isolated from the central SCR section by a diffused guard ring, or a groove, or by irradiation lifetime control techniques. The guard ring is particularly important in that it must confine the carriers associated with the reverse-blocking diode to that region so that these carriers do not represent a forward displacement current in the SCR section. If the carriers were to spill over, the device *dv/dt* rating would be reduced - possibly resulting in false turn-on.

Gold or irradiation lifetime killing can be employed to reduce the turn-off time without significantly increasing the on-state voltage.

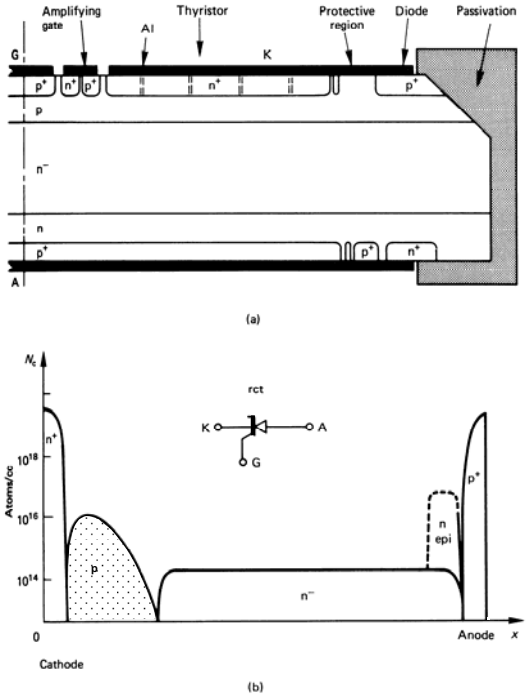

Figure 3.25. *Reverse conducting thyristor with an amplifying gate structure: (a) cross-section of the structure and (b) typical doping profile of the SCR section.*

3.3.4 The bi-directional-conducting thyristor (BCT)

Two anti-parallel connected SCRs can be integrated into one silicon wafer, as shown in figure 3.26. As a result of integrated symmetry, both devices have near identical electrical properties. The mechanical feature different to the triac, is that there are two gates – one on each side of the wafer. Also, unlike the triac, the two SCR sections are physically separated in the wafer to minimise carrier diffusion interaction. The equivalent circuit comprises two SCRs connected in anti-parallel. As such, one device turning off and supporting a negative voltage, represents a positive *dv/dt* impressed across the complementary device, tending to turn it on. Also, any charge carries which diffusion from the SCR previously on, exasperate the *dv/dt* stress on the off SCR.

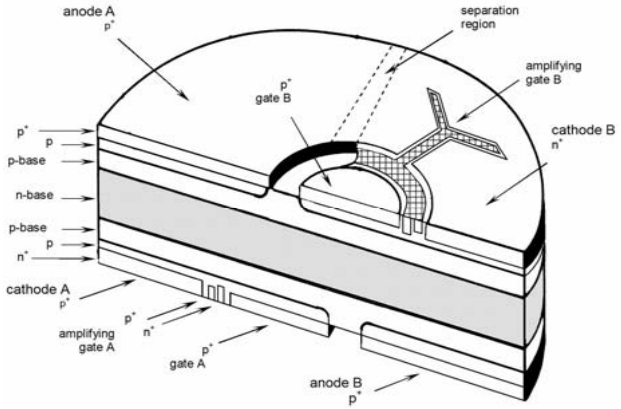

Figure 3.26. *Cross-section structure of the bidirectional conducting phase-control SCR with an amplifying gate structure.*

The two central amplifying gate structures are as for the RCT, in figure 3.25a. A separation of a few minority carrier lateral diffusion lengths, along with an increased density of cathode shorts along the separating edge of each cathode and in the amplifying gate region close to the anode of the complementary SCR, enhance the physical separation. The amplifying gate fingers are angled away from the separation regions to minimise the shorting effect of the complementary SCR anode emitter shorting.

The on-state voltage of each SCR is fine tuned, match for on-state loss, using electron irradiation.

3.3.5 The gate turn-off thyristor (GTO)

The gate turn-off thyristor is an SCR that is turned on by forward-biasing the cathode junction and turned off by reverse-biasing the same junction, thereby preventing the cathode from injecting electrons into the p1 region. Other than its controlled turn-off properties, the GTO's characteristics are similar to the conventional SCR. The basic structure and circuit symbol are shown in figure 3.27.

***3.3.5i* - GTO turn-off mechanism**

In the on-state, due to the high injection efficiency of junctions J1 and J3, the central p-base is flooded with electrons emitted from the n-cathode and the central n-base is flooded with holes emitted from the p-anode,. If a reverse gate current flows from the cathode to the gate, with a driving voltage tending to reverse bias the gate-cathode junction – then p-base holes are extracted from the gate, suppressing the cathode junction from injecting electrons. Eventually the cathode junction is cut-off and the pnp transistor section, now without base current turns off, thereby turning off the GTO.

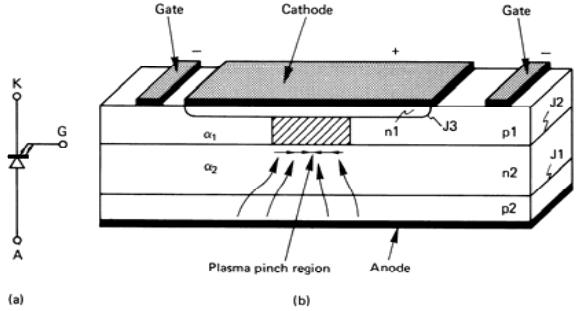

Figure 3.27. *The gate turn-off thyristor: (a) circuit symbol and (b) the basic structure along an interdigitated finger showing plasma focussing in the p1 region at the cathode junction at turn-off.*

The turn-off mechanism can be analyzed by considering the two-transistor equivalent circuit model for the SCR shown in figure 3.20c. The reverse gate current I_{GQ} flows from the gate and is the reverse base current of the npn transistor T_1. The base current for transistor T_1 is $I_B = \alpha_2 I_A - I_{GQ}$, where $I_{GQ} = -I_G$. The reverse base current in terms of the gain of T_1 is $I_{RB} = (1-\alpha_1) I_K$. The GTO as a three terminal device must satisfy $I_A = I_K + I_{GQ}$ and to turn-off the GTO, $I_B < I_{RB}$. These conditions yield

$$(\alpha_1 + \alpha_2 - 1) I_A < \alpha_2 I_{GQ}$$

The turn-off gain of the GTO, β_Q, is defined as the ratio of anode current I_A to reverse gate current I_{GQ}, that is

$$\begin{aligned} \beta_Q &\equiv I_T / I_{GQ} \\ &< \alpha_1 / (\alpha_1 + \alpha_2 - 1) \end{aligned} \qquad (3.21)$$

Thus for high turn-off gain it is important to make α_1 for the npn section as close to unity as possible, while α_2 of the pnp section should be small. A turn-off current gain of 5 is typical.

During the turn-off process, the conducting plasma is squeezed to the centre of the cathode finger, since the lateral p1 region resistance causes this region to be last in changing from forward to reverse bias. This region has the least reverse bias and for reliable GTO operation, the final area of the squeezed plasma must be large enough to prevent an excessive current density. Device failure would be imminent because of overheating.

The doping profile is characterised by a low p1 region sheet resistance and an inter-digitated cathode region to ensure even distribution of the reverse bias across the cathode junction at turn-off. Both turn-off and temperature properties are enhanced by using an anode shorting and defocusing technique as shown in figure 3.28a, but at the expense of any reverse-blocking capability and increased on-state voltage.

The shown two-level cathode and gate metallization used on large-area devices allow a flat metal plate for the cathode connection. As with the conventional SCR, a reverse conducting diode structure can be integrated, as shown in figure 3.28b.

3.3.6 The gate commutated thyristor (GCT)

GTO frequency limitations and the need for an external parallel connected capacitive turn-off snubber (to limit re-applied *dv/dt*), have motivated its enhancement, resulting in the gate commutated thyristor, GCT. As shown in figure 3.28c, a number of processing and structural variations to the basic GTO result in a more robust and versatile high power switch.

- *n-type buffer*
  An n-type buffer layer allows a thinner n-drift region. A 40% thinner silicon wafer, for the same blocking voltage, reduces switching losses and the on-state voltage. An integral reverse conducting diode is also possible, as with the conventional SCR and GTO.
- *transparent emitter*
  A thin lightly doped anode p-emitter is used instead of the normal GTO anode shorts. Some electrons pass through the layer as if the anode were shorted and recombine at the anode contact metal interface, without causing hole emission into the n-base. Effectively, a reduced emitter injection efficiency is achieved without anode shorts. Consequently, gate current triggering requirements are an order of magnitude lower than for the conventional GTO.
- *low inductance*
  A low inductance gate structure, contact, and wafer assembly allow the full anode current to be shunted from the gate in less than 1µs, before the anode voltage rises at turn-off.

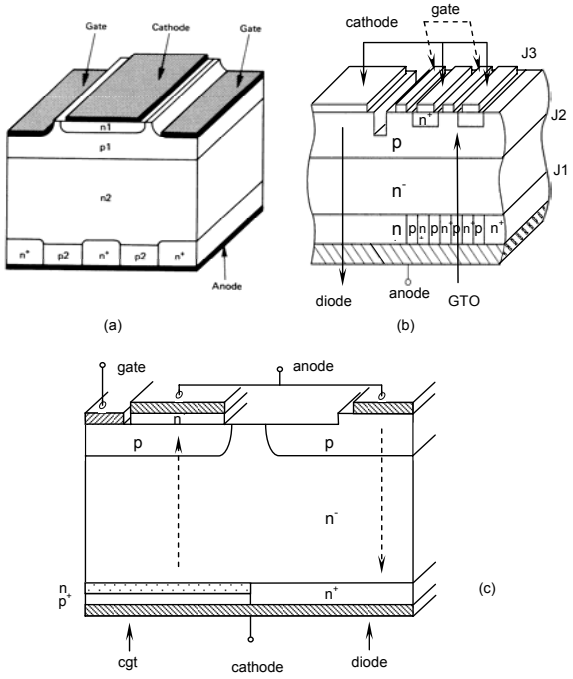

Figure 3.28: *GTO structure variations:*
(a) schematic structure of GTO finger showing the anode defocusing shorts, n^+;
(b) an integrated diode to form a reverse conducting GTO; and
(c) the reverse conducting gate controlled thyristor.

3.3.6i - GCT turn-off

Unity turn-off gain, β_Q=1, means the modified GTO turns off as a pnp transistor without base current, since the cathode junction is cut-off. Without npn BJT regenerative action, the pnp transistor rapidly traverses the linear region, thus eliminating the need for a capacitive turn-off snubber in the anode circuit. The high reverse gate current results in a very short saturation delay time, enabling accurate turn-off synchronisation necessary for devices to be series connected.

3.3.6ii - GCT turn-on

With high gate current, turn-on is initially by npn BJT action, not SCR regeneration. The pnp transistor section is inoperative since the carriers in the n-base are initially ineffective since they require a finite time to transit the wide n-base.

The SCR on-state regenerative mechanism is avoided at both turn-off and turn-on switching transitions thereby yielding a device more robust than the GTO.

As with the GTO, an inductive series turn-on snubber is still required to cope with the initial high *di/dt* current. The GCT switch is thermally limited, rather than frequency limited as with the conventional GTO. Electron irradiation trades on-state voltage against switching performance.

3.3.7 The light triggered thyristor (LTT)

The light triggered thyristor is series connected in HVDC applications. Five inch wafers offer 8kV ratings with onstate voltages of 2.3V at 3000A, with surge ratings of up to 63kA. Turn-off time is 350µs, and turn-on requires about 40mW of light power for 10 µs, with a half microsecond rise time. Because of this low turn-on energy, multiple cascaded amplifying gates are integrated to achieve modest initial current rises limited to 300A/µs. Reapplied voltages are limited to 3500V/µs.

3.3.8 The triac

Pictorial representations of the triac are shown in figure 3.29. The triac is a thyristor device that can switch current in either direction by applying a low-power trigger pulse of either polarity between the gate and main terminal Ml. The main terminal *I-V* characteristics, device symbol, and four trigger modes for the triac are shown in figure 3.30.

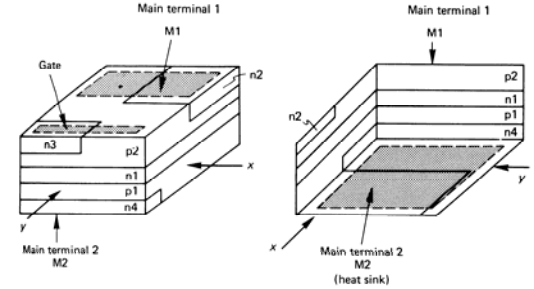

Figure 3.29. *Two views of the typical triac structure, showing main terminal M1 and M2, and a single gate.*

The triac comprises two SCR structures, pl-nl-p2-n2 and p2-nl-pl-n4 which utilise the n3 and p2 regions for turn-on. It should be noted that n2-p2, pl-n4, and p2-n3 are judiciously connected by terminal metallizations, but are laterally separated from their associated active parts.

The four different trigger modes of the triac are illustrated in figure 3.31 and the turn-on mechanism for each mode is as follows.

(a) M2 positive, I_g positive (Mode I)
The main terminal M2 is positive with respect to Ml and gate current forward-biases the p2-n2 junction, J3. The active main SCR section is pl-nl-p2-n2. Turn-on is that for a conventional SCR, as shown in figure 3.31a.

(b) M2 positive, I_g negative (Mode II)
In figure 3.31b, M2 is positive with respect to Ml but negative gate voltage is applied. Junction J4 is now forward-biased and electrons are injected from n3 into p2. A lateral current flows in p2 towards the n3 gate and the auxiliary SCR section pl-nl-p2-n3 turns on as the gain of the n3-p2-nl transistor section increases. Current flow in this auxiliary SCR results in a current flow across J3 into n2, hence piloting the SCR pl-nl-p2-n2 into conduction.

(c) Ml positive, I_g negative (Mode III)
Figure 3.31c shows the bias condition with M2 negative with respect to Ml and the gate negative with respect to Ml such that J4 is forward-biased and electrons are injected from n3 into the p2 region. The potential in n1 is lowered, causing holes to be injected from p2 into the n1 layer which provide base current for the p2-nl-pl transistor section. This brings the p2-nl-pl-n4 SCR into conduction.

(d) Ml positive, I_g positive (Mode IV)
When M2 is negatively biased with respect to Ml and the gate is positively biased such that J3 is forward-biased, as in figure 3.31d, electrons are injected from n2 to p2 and diffused to nl. This increases the forward bias of J2 and eventually the SCR section p2-nl-pl-n4 comes into full conduction.

The various turn-on mechanisms are highly reliant on the judicious lateral separation of the various contacts and regions. The main advantage of the triac lies in the fact that two anti-parallel SCR's in the one silicon structure can be triggered into conduction from the one gate. Because of the need for extra structure layers, hence processing steps, some conventional SCR characteristics are sacrificed and poor device area utilisation results. Two anti-parallel SCR's therefore tend to be more robust than a triac but unlike the BCT device in section 3.3.4, only one gate drive circuit is needed.

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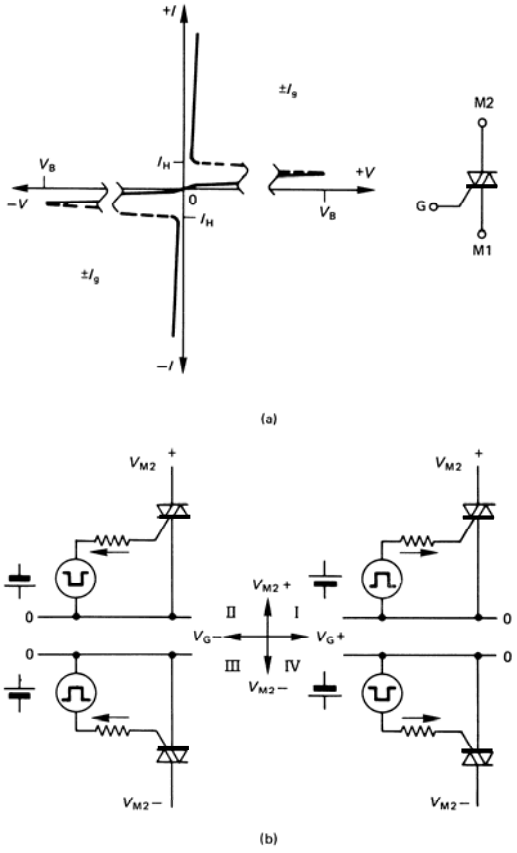
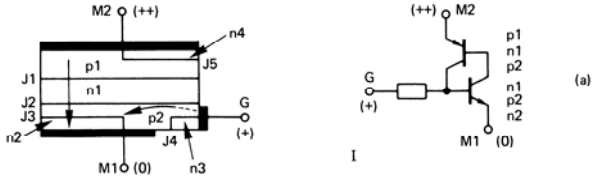
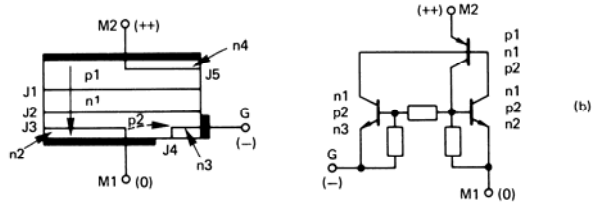


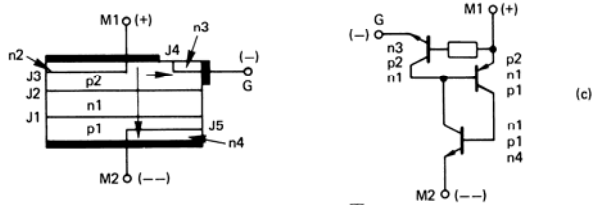
Figure 3.30. *The triac:*
(a) I-V characteristics and circuit symbol and (b) its four firing modes.



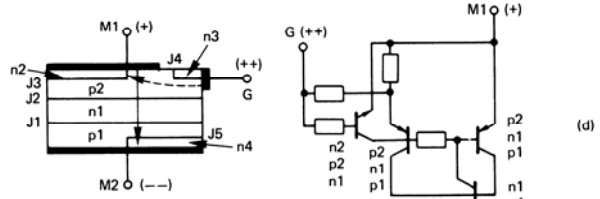
I (a)



II (b)



III (c)



IV (d)

Figure 3.31. *Current flow for the four different triggering modes of the triac.*

4

Electrical Ratings and Characteristics of Power Semiconductor Switching Devices

Device characteristics and ratings are primarily concerned with electrical and thermal properties. The thermal properties and cooling design aspects are similar for all power switching semiconductor devices. A common, unified thermal design approach is applicable since manufacturers use the concept of a semiconductor device being thermally represented by one *virtual junction*. This virtual junction is considered as the point source of all losses, which comprise on-state and off-state losses as well as switch-on and switch-off losses and any control input loss.

Not only are the power dissipation characteristics similar for all semiconductor devices, but many similarities exist in the area of maximum device ratings.

4.1 General maximum ratings of power semiconductor devices

The maximum allowable limits of current, applied voltage, and power dissipation are defined as the *maximum ratings* for that device. These absolute maximum ratings are important and the device must not experience a condition under which any one limit is exceeded if long life and reliability are to be attained. Generally, at worst, the device should experience only one near maximum rating at any instant.

Ratings are dependent on the materials used, the structure, the design, the mount, and the type of processes employed. The one property inherent in these physical features is temperature dependence and its interaction on electrical properties. Maximum ratings are therefore generally based on the variation of

electrical characteristics that arises from the created variations. Because of this close correlation between properties, different ratings cannot be considered independently. Also, ratings are highly dependent on the device external circuit conditions.

This interdependence of device properties and the effects of external circuit condition are no more evident than during *thermal runaway* - a condition to be avoided. Such a condition can occur in all devices that have bipolar junctions. For example, with the diode, thyristor, and the MOSFET's parasitic diode, reverse recovery current increases junction temperature. The reverse recovery charge increases with temperature, thus increasing junction power dissipation and further raising the junction temperature. This endless increasing of temperature and recovery charge results in thermal runaway and eventual device destruction. A similar thermal runaway condition occurs in the bipolar transistor and devices employing BJT mechanisms, like the thyristor and the IGBT. Here, collector current causes an increase in temperature which increases the conductivity of the bipolar transistor. More current then flows, further increasing the device temperature. If external circuit conditions allow, thermal runaway occurs, thus resulting in irreversible device damage.

Figure 4.1 shows the electrical operating bounds of common semiconductor power switches, where the general trend is the higher the *I-V* ratings the slower the possible switching frequency, (because of increased losses associated with attaining higher sustaining voltages), hence increased junction temperature. High-frequency low-power switching applications are dominated by the MOSFET or possibly trench-gate IGBTs while high-power low-frequency switching applications are dominated by thyristor type devices or possibly IGBT modules. Rectifying or fast recovery diodes, as appropriate, are available with matched *I-V* ratings for all the switch device types in figure 4.1.

4.1.1 Voltage ratings

The absolute voltage limit is characterised by a sharp increase in leakage current when the device has at least one junction reverse-biased. The most commonly experienced voltage-limiting mechanism is that of avalanche multiplication, as considered in chapters 2.2.2 and 3.1.2. Since leakage current increases significantly with increased temperature, as shown in figure 2.2 and given by equation (2.7), the absolute repetitive voltage rating must be assigned such that thermal runaway does not occur. Most voltage ratings, because of historic reasons, are characterised at an impractical case temperature of 25°C. The leakage current at rated voltage and 25°C varies from hundreds of microamperes for low voltage devices (less than 600V) to milliamperes for high voltage devices (> 3.3kV).

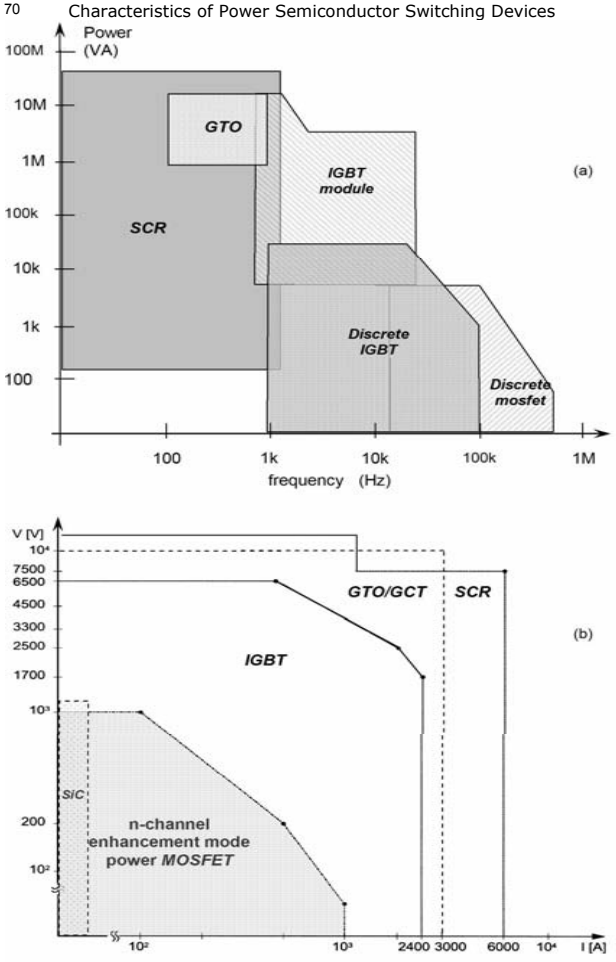


Figure 4.1. *Electrical rating bounds for power switching silicon devices, where (a) frequency related losses limit upper power through-put and (b) voltage is restricted by silicon limitations while current is bounded by packaging and die size constraints.*

4.1.2 Forward current ratings

The forward current ratings are usually specified after consideration of the following factors.

- Current at which the junction temperature does not exceed a rated value.
- Current at which internal leads and contacts are not evaporated.
- External connector current-handling capabilities.

4.1.3 Temperature ratings

The maximum allowable junction temperature $T_{j\,\max}$, is dependent on the quality of the materials used and the type of junction, and is traded off against the reduced reliability that arises from deterioration and accelerated service life. The higher the junction temperature, the higher the rate of deterioration. The relationship between service life L_t in hours, and the junction temperature T_j (K) is approximated by

$$\log_{10} L_t \approx A + B / T_j \tag{4.1}$$

where A and B are constants which are related to the device type.

4.1.4 Power ratings

Power dissipated in a semiconductor device is converted into thermal energy which produces a temperature rise. The major parameters limiting the maximum allowable power dissipation $P_{d\,\max}$ are the maximum allowable junction temperature and the device case temperature T_c. These parameters are related to one another by the *thermal resistance* R_{θ}, according to

$$P_{d\,\max} = \frac{T_{j\,\max} - T_c}{R_{\theta\,\mathrm{j\text{-}c}}} \quad \text{(W)} \tag{4.2}$$

The virtual junction to case thermal resistance $R_{\theta\mathrm{j\text{-}c}}$ is a physical value representing the ratio, junction temperature rise per unit power dissipation. Thermal resistance is a measure of the difficulty in removing heat from the junction to the case. Most maximum power values are specified at a case temperature of 25°C, and are derated linearly to zero as the case-operating temperature increases to $T_{j\max}$, which is typically 175°C for silicon power switching devices.

4.2 The fast-recovery diode

Static *I-V* diode characteristics were considered in chapter 2 and chapter 3.1. In low-frequency applications the only problem posed by a rectifier is heat dissipation, which can be readily calculated if the current waveform is known. On the other hand, calculation of losses in rectifiers for high-frequency application requires knowledge of device switching phenomena. The forward and reverse recovery characteristics are the most important fast-recovery bipolar pn diode electrical switching properties.

4.2.1 *Turn-on characteristics*

During the forward turn-on period of a rectifier, an overshoot voltage is impressed in a forward bias direction across the diode as the forward current increases. The forward recovery characteristics of time t_{fr} and peak forward voltage V_{fp} are measured as shown in figure 4.2, with a specified increase in forward current di_F/dt, rising to a maximum forward current level I_F.

Two mechanisms predominate and contribute to the voltage overshoot phenomenon. The first mechanism is resistive, while the second is inductive.

Initially at turn-on, the device resistance is dominated by the ohmic resistance of the low-concentration n-region. As the concentration of the injected minority carriers increases, the n-region becomes conductively modulated and the associated ohmic drop decreases significantly. These charging effects contribute to a minor initial capacitive component which serves to clamp V_{fp} initially to zero.

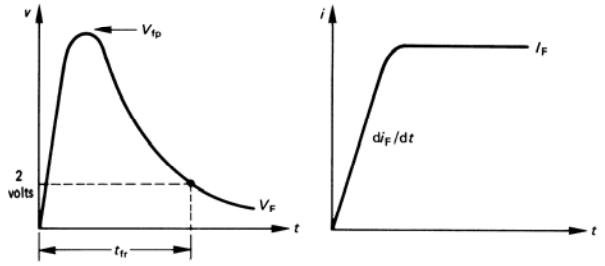


Figure 4.2. *Diode forward recovery measurement:*
(a) specification of forward recovery time, t_{fr} and peak forward voltage, V_{fp} and
(b) diode anode current test waveform.

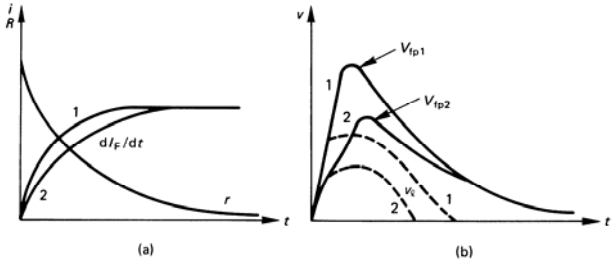


Figure 4.3. *Diode forward turn-on characteristics for two initial anode di/dt cases:*
(a) forward current and effective change in resistive component, r and
(b) anode voltage and voltage contribution v_L as a result of die inductance.

The forward di_F/dt causes a voltage drop across the internal device inductance. This inductance comprises both the diode wafer inductance and the bonding and connection inductance. In bipolar power devices, the inductance of the wafer predominates. Any inductance contribution to the forward transient voltage ceases when the steady-state current level I_F is reached, as shown in figure 4.3. It will be seen that the peak forward transient voltage increases as di_F/dt increases. The resistive component predominates at low di_F/dt.

As with most minority carrier based power semiconductor characteristics, the turn-on phenomenon is significantly worsened by an increase in junction temperature. That is, both t_{fr} and V_{fp} are increased with temperature. Although a pre-reversed biased junction condition does not significantly prejudice the turn-on characteristics, if the junction is pre-forward biased slightly, the turn-on transitional phase can be significantly reduced. The Schottky diode, a majority carrier device, does not suffer from forward turn-on transient effects.

4.2.2 *Turn-off characteristics*

When a forward-conducting bipolar junction diode is abruptly reverse-biased, a short time elapses before the device actually regains its reverse blocking capabilities. Most importantly, before the diode does regain blocking ability, it may be considered as a short circuit in its normally blocking direction.

During forward conduction there is an excess of minority carriers in each diode region and the holes in the n-region and electrons in the p-region must be removed at turn-off. The attempted reverse bias results in a reverse current flow as shown in figure 4.4.

The total *recovery charge* Q_0 is given by

$$Q_0 = \tau I_F \tag{4.3}$$

where I_F is the forward current before switching. In the usual p^+n diode, the excess minority holes in the n-region are most dominant. The lifetime τ is therefore the hole lifetime τ_h. Since carrier lifetime increases with temperature, recovery charge increases with temperature.

The recovery charge Q_0 has two components, one due to internal excess charge natural recombination and the other, the *reverse recovery charge* Q_R, due to the reverse diode current shown in figure 4.4.

The excess charges reside in the neutral scl regions of the diode that border the junction. The excess charge concentration is largest at the scl edge on the n-side, reducing to zero well before the cathode contact.

Turn-off is initiated at t_f and the reverse recovery current i_{rr} commences. The rate of rise of this current is determined solely by the external inductance L of the switching circuit and the circuit applied reverse voltage E, according to

$$\frac{dI_F}{dt} = -E/L \qquad \text{(A/s)} \tag{4.4}$$

Until the time t_0, the diode carries forward current and is forward-biased. When the current reverses, the forward voltage drop decreases slightly but the device still

remains positively biased. The external circuit inductance L supports the voltage E. The excess carrier concentrations now begin to reduce as holes leave via the junction, in providing the reverse current, i_{rr}. Holes are therefore extracted first and quickest at the edge of the scl.

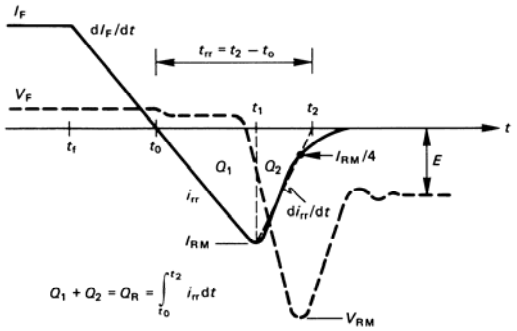


Figure 4.4. *Diode voltage and current during reverse recovery at turn-off.*

At time t_1, the hole concentration at the scl edge reaches zero, the charge Q_1 has been removed and charge Q_2 remains. The reverse current now reduces rapidly since insufficient holes exist at the scl edge. The scl widens quickly, as it is charged. That is, the diode regains its ability to support reverse voltage and at the maximum reverse current I_{RM}, dI_F/dt reduces to zero.

Since $dI_F/dt = 0$, the voltage across the circuit inductance L drops rapidly to zero and E is applied in reverse bias across the diode. Between t_1 and t_2 the rate of change of reverse current di_{rr}/dt is high and, in conjunction with L, produces a reverse voltage overshoot to V_{RM}. After time t_2, di_{rr}/dt reduces to zero, the circuit inductance supports zero volts, and the diode blocks E.

In specifying the *reverse recovery time,* $t_{rr} = t_2 - t_0$, the time t_2 is defined by projecting i_{rr} through $\frac{1}{4}I_{RM}$ as shown in figure 4.4. The reverse recovery time t_{rr} and peak reverse recovery current I_{RM}, at high magnitude dI_F/dt such that $Q_R \approx Q_0$, are approximated by

$$t_{rr} \approx 2.8 \times 10^{-6}\ V_b\sqrt{I_F / |dI_F/dt|} \quad \text{(s)}$$
$$\text{and} \qquad I_{RM} \approx 2.8 \times 10^{-6}\ V_b\sqrt{I_F\,|dI_F/dt|} \quad \text{(A)} \qquad (4.5)$$

where the avalanche breakdown voltage for a step junction, V_b, is given by equation (2.3). The reverse recovery charge Q_R is therefore given by

$$Q_R = \tfrac{1}{2} I_{RM}\, t_{rr} = 3.92\times10^{-12}\ V_b^2\ I_F \quad \text{(C)} \qquad (4.6)$$

that is, the reverse recovery charge is proportional to the forward current, as shown in figure 5.9a for $dI_F/dt > 100$ A/µs.

Figure 4.5 illustrates *snap-off* and *soft recovery* diode properties (S_r) which are characterised by the recovery di_{rr}/dt magnitude. The higher the value of di_{rr}/dt, the higher is the induced diode overshoot V_{RM} and it is usual to produce soft recovery diodes so as to minimise voltage overshoot V_{RM}, resulting from inductive ringing.

Reverse recovery properties are characterised for a given temperature, forward current I_F, and dI_F/dt as shown in figure 5.9.

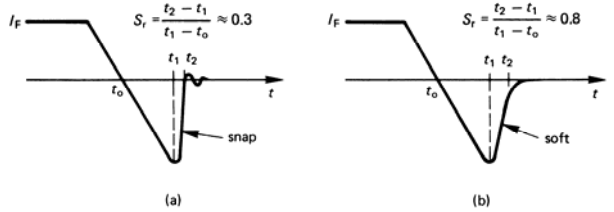


Figure 4.5. *Comparison of fast recovery diode di_{rr}/dt characteristics of: (a) short current tail, producing snap-off (low S_r) and (b) gradual current tail, producing soft recovery (high S_r).*

4.2.3 Schottky diode dynamic characteristics

Being a minority carrier device, the Schottky barrier diode, both in silicon and silicon carbide, is characterised by the absence of forward and reverse recovery, plus the absence of any temperature influence on switching.
Forward recovery traits tend to be due to package and external circuit inductance.
Reverse recovery is dominated by the barrier charging – a capacitive effect, which increases slightly with increased temperature, reverse di/dt, and I_F. The barrier charge requirements are significantly less than the highly temperature dependant minority carrier charge Q_o, associated with the bipolar pn junction diode. Unlike the pn diode, as Schottky junction charging occurs, the junction reverse bias voltage begins to increase immediately. Turn-off voltages are well controlled, less snappy, as the capacitor barrier junction acts like a capacitive turn-off snubber, as considered in chapter 8.3.

Whereas the transient performance is virtually independent of temperature, the static of forward and reverse *I-V* characteristics are highly temperature dependant. In the case of silicon carbide, the reverse leakage current increases by 4% /K, the reverse breakdown voltage decreases by -4% /K while a 0.45% /K increase in on-state voltage means die can be readily parallel connected. In contrast, it will be noticed in figure 2.2 that reverse breakdown voltage and leakage current of a bipolar junction diode, both have a positive temperature co-efficient.

4.3 The bipolar, high-voltage, power switching npn transistor

The electrical properties of the high-voltage power switching npn transistor are related to and dominated by the wide low-concentration n^- collector region

employed to obtain high-voltage characteristics in all semiconductor devices. Many of the limitations and constraints on the MOSFET, IGBT, and the different thyristors are due to their parasitic bjt structures, which introduce undesirable BJT characteristics and mechanisms. It is therefore essential to understand the electrical characteristics and properties of the BJT if the limitations of other devices are to be appreciated.

4.3.1 Transistor ratings

4.3.1i – BJT collector voltage ratings

The breakdown voltage ratings of a transistor can be divided into those inherent to the actual transistor (V_{ceo}, V_{cbo}) and those that are highly dependent on the external base circuit conditions (V_{cer}, V_{ces}, V_{cev}).

Figure 4.6 shows the various voltage breakdown modes of the BJT, which are defined as follows.

V_{cbo} Collector to base voltage-current characteristics with the emitter open; that is, $I_e = 0$, where $V_{(BR)cbo}$ is the collector to base breakdown voltage with $I_e = 0$ and the collector current I_c specified as I_{cbo}.

V_{ceo} Collector to emitter characteristics with the base open circuit such that the base current $I_b = 0$, where $V_{(BR)ceo}$ is the collector to emitter breakdown voltage with $I_b = 0$ and I_c specified as I_{ceo}.

V_{ces} Collector to emitter characteristics with the base shorted to the emitter such that $V_{be} = 0$, where $V_{(BR)ces}$ is the collector to emitter breakdown voltage with I_c specified as I_{ces}.

V_{cer} Collector to emitter characteristics with resistance R between the base and the emitter such that R_{be} = R, where $V_{(BR)cer}$ is the collector to emitter breakdown voltage with I_c specified as I_{cer}.

V_{cev} Collector to emitter characteristics with reverse base to emitter bias V_{eb} = X, where $V_{(BR)cex}$ is the collector to emitter breakdown voltage with I_c specified as I_{cex}.

Each breakdown voltage level and its relative magnitude can be evaluated.

1 – BJT $V_{(BR)cbo}$ - maximum collector-base voltage with the emitter open circuit

The $V_{(BR)cbo}$ rating is just less than the voltage V_b, where the base to collector junction breaks down because of avalanche multiplication, as illustrated in figure 4.6. The common base avalanche breakdown voltage V_b is determined by the concentration of the collector n-region, N_c /cc, and as its resistivity increases, V_b increases according to (equation (2.3))

$$V_b = 5.34\times10^{13} \times N_c^{-3/4} \quad \text{(V)} \tag{4.7}$$

It can be assumed that $V_{(BR)cbo} \approx V_b$.

2 – BJT $V_{(BR)ceo}$ - maximum collector-emitter voltage with the base open circuit

Avalanche multiplication breakdown of a common emitter connected transistor occurs at a collector voltage V_a when the common emitter amplification factor β becomes infinite. The gain β, from equation 3.4 and accounting for avalanche multiplication, is defined by

$$\beta = \frac{\alpha_0 M}{1-\alpha_0 M} \tag{4.8}$$

where M is the avalanche multiplication factor, which is collector junction voltage V_{cb} dependent, according to (equation 3.17)

$$M = 1/\left(1-\frac{V_{cb}}{V_b}\right)^m \tag{4.9}$$

The factor m is empirically determined and is between 2 and 4 for the collector-base doping profile of the high-voltage silicon npn transistor. The common base current amplification factor α_0 is for a voltage level well below any avalanche.

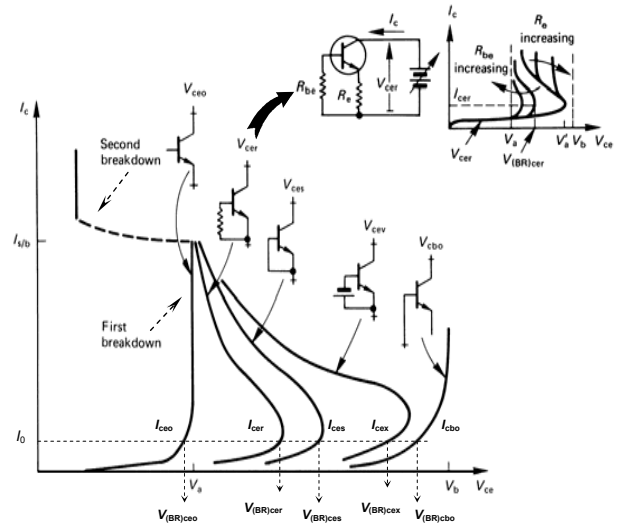


Figure 4.6. *Relative magnitudes of npn transistor collector voltage breakdown characteristics, showing first and second breakdown.*

At high V_{cb} voltages, near V_a, avalanche multiplication causes a high injection of hole carriers. Thus no base current is required and a $\beta \rightarrow \infty$ condition effectively occurs. With such conditions, equation (4.8) indicates that $\alpha_0 M \rightarrow 1$ which, upon substitution into equation (4.9), yields

$$V_a = V_b \sqrt[m]{1-\alpha_0} \approx V_{(BR)ceo} \quad \text{(V)} \tag{4.10}$$

V_a becomes the common emitter avalanche breakdown voltage and $V_{(BR)ceo}$ is

commonly called the collector emitter sustaining voltage, $V_{ceo(sus)}$.

It can be shown that

$$V_{(BR)cbo} > V_{(BR)cex} > V_{(BR)ces} > V_{(BR)cer} > V_{(BR)ceo} \quad (4.11)$$

With low-gain BJTs, V_a is almost V_b in value, but with high-gain devices V_b may be 2 to 3 times that of V_a. Notice in figure 4.6 that negative resistance characteristics occur after breakdown, as is the case with all the base circuit-dependent breakdown characteristics.

The inserted diagram in figure 4.6 shows how base-emitter resistance affects collector-emitter voltage breakdown. Importantly, the breakdown voltage increases as the base-emitter resistance decreases. This is because the injection efficiency of the emitter is reduced. This shorting feature is exploited extensively in alleviating problems in the MOSFET, IGBT, and thyristor devices, and is discussed in the respective device sections.

***4.3.1ii – BJT safe operating area** (SOA)*

The safe operating area represents that electrical region where a transistor performs predictably and retains a high reliability, without causing device destruction or accelerated deterioration.

Deterioration or device destruction can occur when operating within the absolute maximum device ratings, as a result of second breakdown (s/b) or excessive thermal dissipation. Typical SOA characteristics are shown in figure 4.7. These collector characteristics are for a single pulse, of a given duration, such that the transistor operates in the linear region and at a case temperature of 25°C. The dc or continuous operation case has the most restrictive SOA curve, while a short single pulse of 1µs duration enables the full device *I-V* ratings to be exploited.

The SOA is basically bounded by the maximum collector I_{cmax} and the collector emitter breakdown voltage $V_{(BR)ceo}$. In figure 4.7 it will be seen that four distinct operating region limits exist, viz., A to D.

Ⓐ Maximum collector current which is related to allowed current density in the leads and contacts and the minimum gain of the transistor. The maximum lead current is given by $I = Kd^{2/3}$ where the diameter d is in mm and K depends on the type and length of wire. For lengths greater than 1mm, K = 160 for both copper and silver.

Ⓑ Maximum thermal dissipation, which is related to the absolute maximum junction temperature T_{jmax}, and the thermal resistance or impedance from the virtual junction to the case. In this thermally limited region, the collector power loss is constant and $I_c = P\,V_c^{-1}$. Thus the thermal limit gradient is -1, when plotted on logarithmic axes as in figure 4.7.

Ⓒ Limit of forward second breakdown. This breakdown occurs when the local current density is too high and a hot spot is created which causes thermal runaway. The physical causes of the high current concentration phenomenon are a fall in electrical potential or instability of lateral temperature distribution in the base area. These occur as a consequence of base-width concentration non-uniformity, a faulty junction or improper chip mounting. A typical s/b characteristic is shown in figure 4.6, and is characterised by a rapid drop in collector voltage to the low-impedance area after s/b. The s/b SOA limit can be modelled by $I_{s/b} = PV^{-n}$, where *n,* the gradient in figure 4.7, ranges from 1.5 to 4 depending on the fabrication processes and structures that have been employed. S/b, with a forward-biased base emitter is usually characterised by a short circuit at the emitter periphery, since this area is more forward-biased than central regions because of lateral base resistance effects. S/b, with a reverse-biased base-emitter junction, occurs in the central emitter region because of current focussing to that area as a result of the same lateral base resistance effects.

Ⓓ Maximum collector voltage under worst case conditions. In switching applications the $V_{(BR)ceo}$ limit can be exceeded provided suitable base conditions exist. At turn-off, when the collector current has fallen below I_{cex}, the collector supporting voltage can be increased from $V_{(BR)ceo}$ to $V_{(BR)cex}$ if the proper reverse bias base emitter junction conditions exist. The SOA together with this small extension area form the *reverse bias SOA*. Turn-on in switching applications can take place from a $V_{(BR)cex}$ condition, provided the collector current rise time is very short, usually much less than 1µs. As the rise time value decreases, the current that can be switched at turn-on increases. Under such conditions a significant portion of I_{cmax} can be switched from $V_{(BR)cex}$. The SOA together with this quite large switch-on extension area form the *forward bias SOA,* as shown in figure 4.7.

The SOA is usually characterised for a case temperature of 25°C. In practice much higher case temperatures are utilised and then the power and s/b SOA limits are modified with the aid of the derating curves of figure 4.8. At a given case temperature, above 25°C, power derating is greater than s/b derating. No derating is necessary for case temperatures below 25°C.

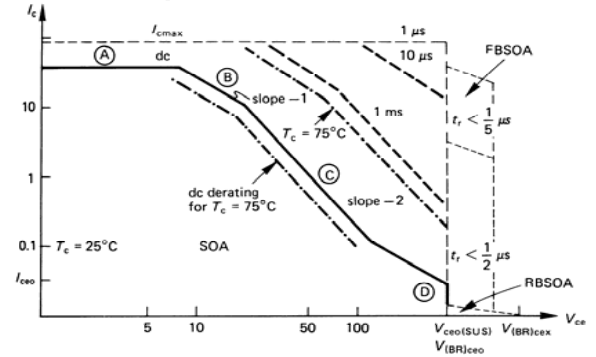


Figure 4.7. *Safe operating area (SOA) bounds of an npn high-voltage power switching transistor including forward and reverse bias SOA. Temperature derating for a case temperature of 75°C is shown.*

Figure 4.7 shows the derating, according to figure 4.8, of the dc and 1ms operating loci when the case temperature is increased from 25°C to 75°C. Figure 4.8 indicates that the power limit line (B) is derated to 71.5 per cent, while the s/b limit line (C) is reduced to 80 per cent. The slope of the 10μs single pulse limit line indicates that no s/b component exists, thus only power derating need be employed. This is because the pulse period of a few microseconds is short compared to the die thermal constant, whence the rate of local heating is too brief to disperse and cause second breakdown.

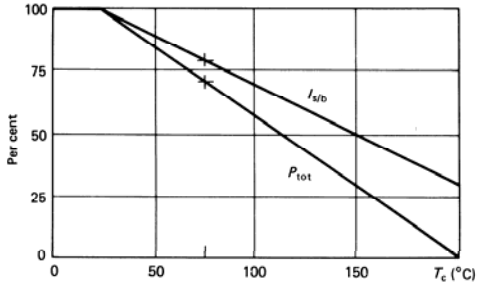


Figure 4.8. *Power and second breakdown derating versus case temperature.*

It is important to note that when a transistor is employed in a switching application, where the device is either cut-off or hard-on, the full SOA bounded by I_{cmax} and $V_{(BR)ceo}$ can usually be exploited. As indicated in figure 4.7, provided the collector switching times are of the order of a microsecond or less, no power or s/b derating need be factored. Design is based on total power losses, such that the maximum allowable junction temperature, T_{jmax} is not exceeded. For high reliability and long device lifetime only one limit, either I_{cmax} or $V_{(BR)ceo}$, should be exploited in a given application.

4.3.2 Transistor switching characteristics

If a current pulse is supplied into the base of a common emitter connected transistor, as shown in figure 3.8, the resultant collector current waveform is as shown in figure 4.9. The collector voltage waveform is essentially collector load circuit dependent and therefore is not used to characterise transistor switching.

4.3.2i – BJT turn-on time: $t_{on} = t_d + t_{ri}$
Turn-on consists of a delay time t_d followed by a current rise time t_{ri}.
The delay time corresponds mainly to the charging of the base-emitter junction diffusion capacitance. The turn-on delay time can be significantly reduced by increasing the applied rate and magnitude of the forward base current I_{bf}.
The current rise time is related to the effective base zone width and, as the base charge increases because of the base current, the collector current increases.

4.3.2ii – BJT turn-off time: $t_{off} = t_s + t_{fi}$
In order to cut-off a transistor from the saturated state, all the accumulated charges must be neutralised or removed from the base and from the lightly doped n^- region of the collector. The turn-off process is started by removing the forward base current I_{bf}, and applying the reverse base current I_{br}. The excess minority carriers, namely holes, in the collector n^- region are progressively reduced in the process of providing the collector current. The excess minority carriers in the base are removed by the reverse base current. The reverse base current does not influence the collector n^- region recombination process. The period after the cessation of positive base current until the transistor enters the linear region is termed storage or *saturation time*, t_s. Generally, and undesirably, the larger the forward gain β_f, the greater the saturation time, t_s.

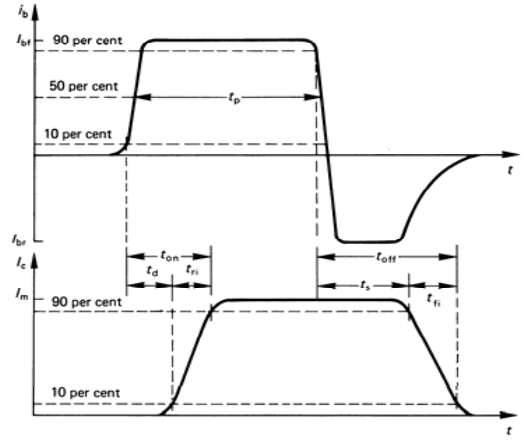


Figure 4.9. *Defining transistor base and collector current switching times for turn-on and turn-off.*

Optimal turn-off occurs when the emitter junction cuts off, as a result of I_{br}, just as the collector junction cuts off and enters the linear region. Thus the collector current fall time can be decreased by increasing the reverse base current immediately after the collector junction has cut off.

In switching applications, operation in the linear region is to be avoided, or at least traversed rapidly, because of the associated high device power losses. Although in the saturated state, with $I_{bf} >> I_c / \beta_f$, minimum forward gain and losses, this state is not conducive to a rapid turn-off transition to the cut-off region. In switching applications, in order to increase turn-off speed (decrease t_s and t_{fi}), the transistor may be held in the quasi-saturation region by reducing and

controlling the forward base current magnitude such that the device is on the verge of saturation, $I_{bf} \approx I_c / \beta_f$, but is not in the linear region. The quasi-saturation on-state losses are slightly higher. In the quasi-saturated on-state the collection n^- region can be considered as extra series collector circuit resistance, which decreases as the neutral base region penetrates and reduces to zero when saturation occurs.

4.3.3 BJT phenomena

Although the BJT is virtually obsolete as a discrete power switching device for new circuit designs, it has been considered in some detail both in this chapter and chapter 3.2.1. This is because its operating electrical mechanisms explain the major limiting electrical operating factors of all controlled power switching devices.

- ***mosfet***: In chapter 3.2.2 the reverse conducting inherent body diode in the MOSFET is part of a parasitic npn transistor. This BJT structure can produce unwanted MOSFET *dv/dt* turn-on. Notice in figure 3.14a that the source metallization overlaps the p^+ well, there-in producing a base to emitter shunting resistor, as shown by R_{be} in figure 3.14b. The emitter shunts perform two essential functions, but inadvertently creates a non-optimal diode.
  - First, the shunt decreases the injection efficiency hence gain of the BJT, decreasing the likelihood of a drain *dv/dt* resulting in sufficient Miller capacitance current to turn-on the parasitic BJT, as considered in chapter 3.2.1.
  - Second, by decreasing the BJT gain, the npn section voltage rating is increased from V_{ceo} to V_{cer} as considered in section 4.3.1.
- ***igbt***: In figure 3.16d the equivalent circuit of the IGBT has a parasitic pnp-npn thyristor structure. Once again, the emitter metallization (R_{be}) shunts the base to emitter of the npn BJT, helping to avoid latch-up of the SCR section, as modelled by the derivation of equation (3.18). Also the voltage rating of the npn section is increased from V_{ceo} to V_{cer}. Improved thermal stability also results. Judicious profiling of the transistor sections is essential.
- ***gto thyristor***: All the electrical operating mechanisms of the SCR are explainable in terms of BJT mechanisms, including turn-on, turn-off, and thermal stability. Emitter shorts are used extensively to decrease gain, increase thermal stability, and increase voltage ratings and are essential in providing separation in the bi-directional conducting thyristor, as considered in chapter 3.3.4. The GTO thyristor also uses emitter shorts in order to achieve a stable device at turn-off, as shown in figure 3.28.

An understanding of BJT electrical operating mechanisms is fundamental to the design and operation of semiconductor power switching devices, whether principally bipolar operating devices or unipolar devices which have bipolar parasitic structures.

4.4 The power MOSFET

The main electrical attributes offered by power MOSFETs are high switching speeds, no second breakdown (s/b), and high impedance on and off voltage control. MOSFETs, along with IGBTs, have replaced the bipolar junction transistor due to their superior switching performance and simpler gate control requirements.

4.4.1 MOSFET absolute maximum ratings

The basic enhancement mode power MOSFET structure and electrical circuit symbol are shown in figure 3.11. The SOA bounds shown in figure 4.10 is confined by four outer bounds.

Ⓐ The n^- epitaxial layer concentration and thickness is the key parameter in specifying the drain high-voltage ratings, such as V_{ds} and V_{dg}, which increase with temperature at approximately +0.1 per cent/K, as shown in figure 3.13.

Ⓑ One important rating feature of the power MOSFET is that it does not display the s/b that occurs with the bipolar transistor. Figure 4.10 shows the safe operating area for transistors, with the bipolar transistor s/b limitation area shaded. The physical explanation as to why MOSFETs do not suffer from s/b is based on the fact that carrier mobility in the channel decreases with increased temperature at -0.6 per cent/K. If localised heating occurs, the carrier mobility decreases in the region affected and, as a consequence, the localised current reduces. This negative feedback, self-protection mechanism forces currents to be uniformly distributed along the channel width and through the silicon die. This property is exploited when paralleling MOSFET devices. As a result of the enlarged SOA, the power MOSFET is generally a much more robust device than its bipolar counterpart. This region is thermally limited, as defined by $I = P/V^{-1}$ giving the -1 slope in figure 4.10.

Ⓒ The drain current rating is also related to the epitaxial properties. Its resistance specifies the $I_d^2 R_{ds(on)}$ power loss, which is limited by the junction to case thermal resistance, $R_{\theta j\text{-}c}$. The continuous, usable drain current above 25°C is thus given by

$$I_d = \sqrt{\frac{T_{j\max} - T_c}{R_{ds(on)}\, R_{\theta j\text{-}c}}} \quad \text{(A)} \qquad (4.12)$$

Ⓓ When the MOSFET is on, with minimum drain voltage at maximum drain current, it operates in the resistive mode where the drain current is given by

$$I_d = \frac{1}{R_{ds(on)}}\, V_{ds} \quad \text{(A)} \qquad (4.13)$$

The SOA region at high currents and low voltages is thus characterised by a line of slope 1, on logarithmic axes, as shown in figure 4.10.

The gate to source voltage V_{gs} controls the channel and the higher the value of V_{gs}, the higher the possible drain current. The gate to source is a silicon dioxide dielectric capacitor which has an absolute forward and reverse voltage that can be impressed before dielectric breakdown. Typical absolute maximum voltage levels vary from ±10V to ±40V, as the oxide layer increases and capacitance

advantageously decreases.

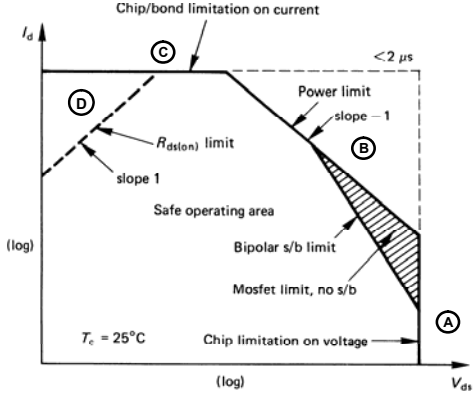


Figure 4.10. *The safe operating area of the power MOSFET, which does not suffer second breakdown.*

4.4.2 Dynamic characteristics

The important power MOSFET dynamic characteristics are inter-terminal voltage-dependent capacitance and drain current-switching times. The various MOSFET capacitances are dominant in specifying switching times.

4.4.2i – MOSFET device capacitances

Figure 4.11 shows an equivalent circuit for the power MOSFET, extracted from figure 3.14, which includes three inter-terminal, non-linear voltage-dependent capacitances C_{gd}, C_{gs}, and C_{ds}. The magnitudes are largely determined by the size of the chip and the cell topology used. Therefore higher current devices inherently have larger capacitances. Electrically, these capacitances are strongly dependent on the terminal drain-source voltage.

Manufacturers do not generally specify C_{gd}, C_{gs}, and C_{ds} directly but present input capacitance C_{iss}, common source output capacitance C_{oss}, and reverse transfer capacitance C_{rss}. These capacitances, as a function of drain to source voltage, are shown in figure 4.12a. The manufacturers' quoted capacitances and the device capacitances shown in figure 4.12b are related according to

$$C_{iss} = C_{gs} + C_{gd}; \qquad C_{ds} \text{ shorted (F)} \tag{4.14}$$

$$C_{rss} = C_{gd} \qquad \text{(F)} \tag{4.15}$$

$$C_{oss} = C_{ds} + \frac{C_{gs} \cdot C_{gd}}{C_{gs} + C_{gd}}; \qquad C_{gs} \text{ shorted} \approx C_{ds} + C_{gd} \qquad \text{(F)} \tag{4.16}$$

The measurement frequency is usually 1 MHz and any terminals to be shorted are connected with large, high-frequency capacitance, so as to present a short circuit at the measurement frequency.

Device capacitances are predominant in specifying the drain current switching characteristics, particularly C_{gd} with its large capacitance variation at low drain voltage levels.

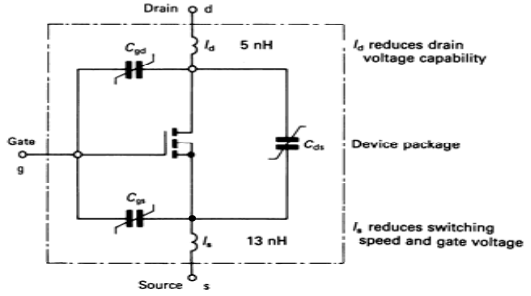


Figure 4.11. *MOSFET equivalent circuit including terminal voltage dependent capacitance and inductance for the TO247 package.*

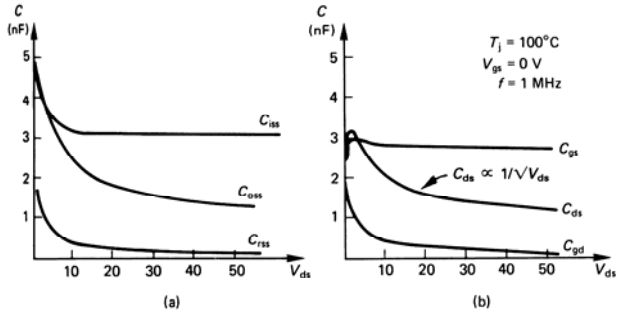


Figure 4.12. *MOSFET capacitance variation with drain-to-source voltage: (a) manufacturers' measurements and (b) inter-terminal capacitance values.*

4.4.2ii – MOSFET switching characteristics

The simple MOSFET circuit with an inductive load L_L in figure 4.13, can illustrate how device capacitances influence switching. The MOSFET gate is driven from a voltage source whose output impedance is represented by R_g, which also includes any MOSFET gate series internal resistance. The dc input resistance of a power MOSFET is in excess of 10^{12} Ohms and when used as a switch, the power required to keep it on or off is negligible. However energy is required to change it from one state to another, as shown in figure 4.14. This figure shows the relationship between gate charge, gate voltage, and drain current for a typical MOSFET. The initial charge Q_{gs} is that required to charge the gate-source capacitance and Q_{gd} is that required to supply the drain-gate Miller capacitance. For a given gate charging current, switching speed is proportional to gate voltage. The gate charge required for switching, and hence switching speed, is not influenced significantly by the drain current magnitude, and not at all by the operating temperature. The switching speed is directly related to time delays in the structure because of the channel transit time of electrons. External to the device the switching time is determined by the energy available from the drive circuit. A gate drive design example based on gate charge requirement is presented in chapter 7.1.2.

The switching transients can be predicted for an inductive load, when the load is the parallel inductor and diode, with no stray unclamped inductance, as shown in figure 4.13. It is assumed that a steady load current I_L flows. The various turn-on and turn-off periods shown in figure 4.15 are related to the sequential charging periods shown in figure 4.14. Any gate circuit inductance is neglected.

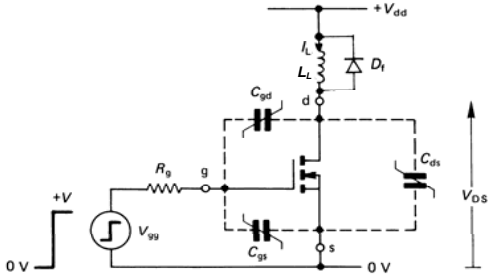


Figure 4.13. *MOSFET basic switching circuit used to demonstrate current switching characteristics.*

1 – MOSFET turn-on

Period I - turn-on delay, $t_{d\,on}$

The gate voltage rises exponentially to the gate threshold voltage V_{TH} according to equation (4.17), that is

$$V_{gs}(t) = V_{gg}\,[1 - e^{-t/C_{in}R_g}] \qquad \text{(V)} \qquad (4.17)$$

where C_{in}, the gate input capacitance is approximated by $C_{gd} + C_{gs}$, or C_{iss}. The

drain voltage remains unchanged, that is, it supports the supply voltage V_{dd} and no MOSFET drain current flows. The turn-on delay time is given by

$$t_{d\,on} = C_{in}R_g\;\ell n\left(1 - \frac{V_{TH}}{V_{gg}}\right)^{-1} \qquad \text{(s)} \qquad (4.18)$$

Equations (4.17) and (4.18) can be modified to account for a negative initial gate voltage (as presented in Appendix 4.1), a condition which increases the turn-on delay time, but increases input noise immunity.

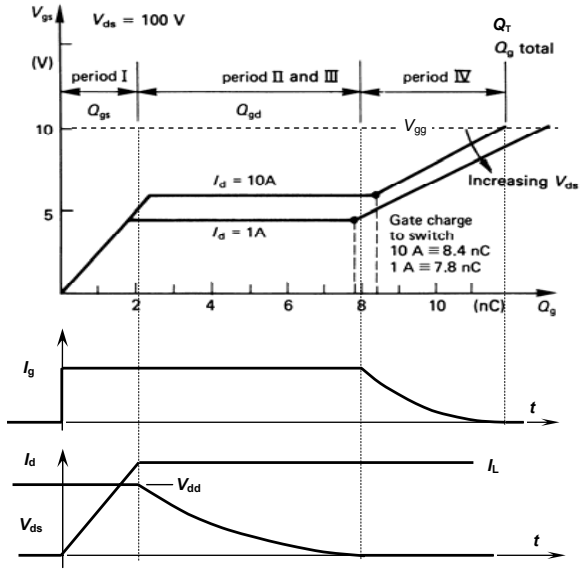


Figure 4.14. *Typical relationships between gate charge, voltage, and current and magnitude of drain current and voltage being switched.*

Period II - current rise, t_{ri}

Drain current commences to flow in proportion to the gate voltage as indicated by the transconductance characteristics in figure 3.12a. The gate voltage continues to rise according to equation (4.17). The drain voltage is clamped to the rail voltage V_{dd} and the drain current rises exponentially to the load current level I_L, according to

$$I_d(t) = g_{fs}\left(V_{gg} - V_{TH}\right)[1 - e^{-t/R_gC_{in}}] \qquad \text{(A)} \qquad (4.19)$$

The current rise time t_{ri} can be found by equating $I_d = I_L$ in equation (4.19).

Period III - voltage fall, t_{fv}

When the drain current reaches the load current level, the drain voltage will fall from V_{dd} to the low on-state voltage. This decreasing drain voltage produces a feedback current via C_{gd} to the gate, which must be provided by the gate drive. This feedback mechanism is called the *Miller effect* and the effective gate input capacitance increases to $C_{in} = C_{iss} + (1 - A_v)C_{gd}$ where $A_v = \Delta V_{ds}/\Delta V_{gs}$. For a constant load current, from figure 3.12a, the gate voltage remains constant at

$$V_{gs} = V_{TH} + I_L / g_{fs} \quad \text{(V)} \qquad (4.20)$$

as shown in figure 4.15b.

Since the gate voltage is constant, the Miller capacitance C_{gd} is charged by the constant gate current

$$I_g = \frac{V_{gg} - V_{gs}}{R_g} = \frac{V_{gg} - (V_{TH} + I_L / g_{fs})}{R_g} \quad \text{(A)} \qquad (4.21)$$

and the rate of change of drain voltage will be given by

$$\frac{dV_{gd}}{dt} = \frac{dV_{ds}}{dt} = \frac{I_g}{C_{gd}} \quad \text{(V/s)} \qquad (4.22)$$

that is

$$V_{ds}(t) = V_{dd} - \frac{I_g}{C_{gd}} t \quad \text{(V)} \qquad (4.23)$$

The drain voltage decreases linearly in time and the voltage fall time is decreased by increasing the gate current. Assuming a low on-state voltage, the voltage fall time t_{fv} is given by

$$t_{fv} = V_{dd} C_{gd} / I_g \quad \text{(s)} \qquad (4.24)$$

Period IV

Once the drain voltage reaches the low on-state voltage, the MOSFET is fully on and the gate voltage increases exponentially towards V_{gg}.

***2 – MOSFET** turn-off*

Period V - turn-off delay, $t_{d\,off}$

The MOSFET is fully on, conducting the load current I_L, and the gate is charged to V_{gg}. The gate voltage falls exponentially from V_{gg} to $V_{TH} + I_L / g_{fs}$ according to

$$V_{gs}(t) = V_{gg} e^{-t/R_g C_{in}} \quad \text{(V)} \qquad (4.25)$$

in a time given by

$$t_{d\,off} = R_g C_{in} \ell n \frac{V_{gg}}{V_{TH} + I_L / g_{fs}} \quad \text{(s)} \qquad (4.26)$$

This delay time can be decreased if a negative off-state gate bias is used. The drain conditions are unchanged.

Period VI - voltage rise, t_{rv}

The drain voltage rises while the drain current is fixed to the load current level, I_L. Accordingly the gate voltage remains constant and the gate current is given by

$$I_g = \frac{V_{TH} + I_L / g_{fs}}{R_g} \quad \text{(A)} \qquad (4.27)$$

This current discharges the Miller capacitance according to

$$\frac{dV_{ds}}{dt} = \frac{dV_{dg}}{dt} = \frac{I_g}{C_{gd}} \quad \text{(V/s)} \qquad (4.28)$$

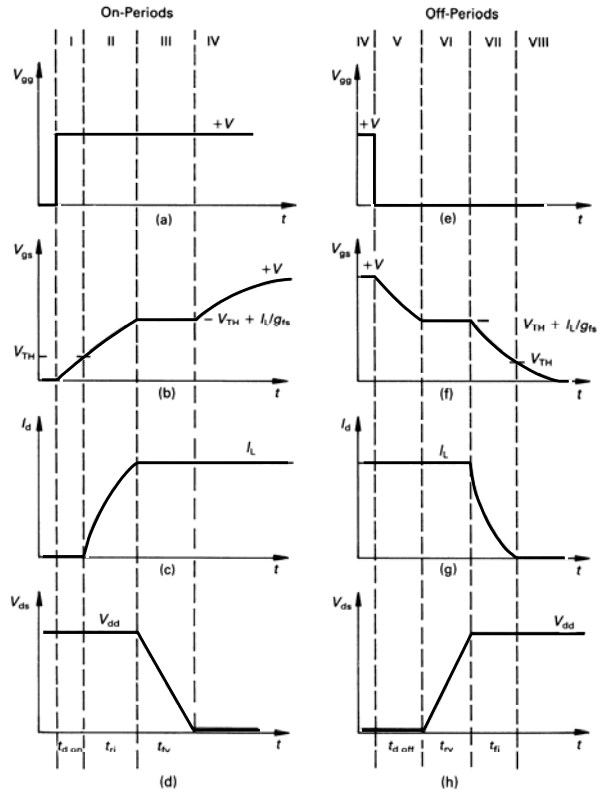


Figure 4.15. *Distinct switching periods of the MOSFET with an inductive load at: (a) (b) (c) (d) comprising turn-on; (e)* (f) *(g) (h) forming turn-off.*

Thus $$V_{ds}(t) = \frac{I_g}{C_{gd}}\ t \qquad \text{(V)} \qquad (4.29)$$

where the low on-state voltage has been neglected.
The drain voltage rises linearly to the supply V_{dd}. The voltage rise time t_{rv} is given by

$$t_{rv} = \frac{C_{gd}\ V_{dd}}{I_g} \qquad \text{(s)} \qquad (4.30)$$

and is decreased by increasing the gate reverse current magnitude.

Period VII - current fall, t_{fi}
When the drain voltage reaches the supply rail, the load current in the MOSFET begins to decrease, with load current being diverted to the diode D_f.
The gate voltage decreases exponentially according to

$$V_{gs}(t) = (V_{TH} + I_L / g_{fs})\ e^{-t/R_g C_{in}} \qquad \text{(V)} \qquad (4.31)$$

and is mirrored by the drain current

$$I_d(t) = (I_L + g_{fs} V_{TH})\ e^{-t/R_g C_{in}} - g_{fs} V_{TH} \qquad \text{(A)} \qquad (4.32)$$

The current fall time t_{fi} is given by $I_d = 0$ in equation (4.32) or when the gate-source voltage reaches the threshold voltage, that is, from equation (4.31)

$$t_{fi} = R_g\ C_{in}\ \ell n\left(1 + \frac{I_L}{g_{fs}\ V_{TH}}\right) \qquad \text{(s)} \qquad (4.33)$$

Period VIII – off-state
The MOSFET drain is cut-off and the gate voltage decays exponentially to zero volts according to

$$V_{gs}(t) = V_{TH}\ e^{-t/R_g C_{in}} \qquad \text{(V)} \qquad (4.34)$$

Based on the total gate charge Q_T delivered by the gates source V_{gg}, shown in figure 4.14, the power dissipated in the MOSFET internal gate resistance, hence contributing to device losses, is given by

$$P_G(R_{\text{int}}) = V_{gg} Q_T f_s \frac{R_{G\text{int}}}{R_{G\text{int}} + R_{G\text{ext}}} \qquad \text{(W)} \qquad (4.35)$$

4.5 The insulated gate bipolar transistor

4.5.1 IGBT switching

The IGBT gate charge characteristics for switching and the switching waveforms are similar to those of the MOSFET, shown in figures 4.14 and 4.15 respectively, whilst the *I-V* on and off state characteristics are similar to the BJT. The collector switching characteristics depend on the injection efficiency of the collector p^+ emitting junction. The higher the injection efficiency, the higher the pnp transistor section gain and the lower the on-state voltage. The poorer the injection efficiency, the more the characteristics resemble a MOSFET.

The turn-on waveforms and mechanisms are essentially those for the MOSFET shown in figure 4.15. Figure 4.16 shows IGBT turn-off which has components due to MOSFET and BJT action. As with the MOSFET, distinct turn-off stages exist when switching an inductive load.
Period V - turn-off delay, $t_{d\,\text{off}}$
The gate voltage falls to a level determined by the gate threshold, V_{TH}, the forward transconductance, g_{fs} and the MOSFET section current level.
Period VI - voltage rise, t_{rv}
As the collector voltage rises the collector current remains constant, hence the gate voltage remains constant while charging the Miller capacitance. For a high gain pnp section the voltage rise time is virtually independent of gate resistance, while for an IGBT closely resembling a MOSFET the voltage rise is gate current magnitude dependent.
Period VII - current fall, t_{fi}
The current falls in two sections, the first, phase VII, due to MOSFET action, as are the previous two phases (periods V and VI). As with the conventional MOSFET the current falls rapidly as the MOSFET section current, shown in figure 4.16b reduces to zero.

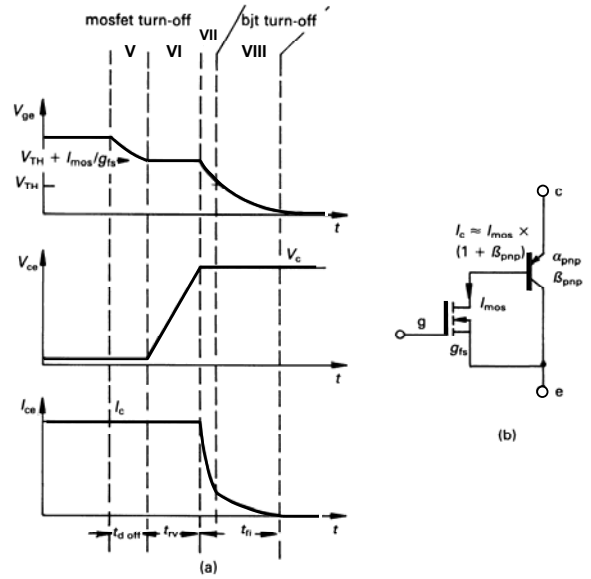


Figure 4.16. *IGBT (a) turn-off waveforms and (b) equivalent circuit during turnoff.*

Period VIII – current tail time
With the gate voltage at the threshold level, the pnp transistor section turns off in a V_{ceo} mode, phase VIII. A relatively low-magnitude, lengthy current tail results which is dependent on the pnp transistor section minority carrier lifetime in the n base and the injection efficiency of the p^+ collector region.

The switching frequency and current rating of an IGBT are both limited by the minimum of the package dissipation limit (as with any other semiconductor device) and a factor solely dependant on the switching times at turn-on and turn-off. As the switching frequency increases, the current rating decreases. The MOSFET upper frequency is restricted solely by losses, that is, temperature.

4.5.2 IGBT short circuit operation

Under certain electrical conditions the IGBT may be subjected to short circuits, and safely turned off with out damage. Two different short circuit conditions are characterised:

I IGBT turn-on into a pre-existing load short circuit
II subsequent to IGBT turn-on, a short circuit load condition occur during the on-state period

I Pre-existing short circuit at turn-on
The collector electrical characteristics are determined by the gate drive parameters and conditions. As the collector voltage falls, the collector current *di/dt* is determined by the stray inductance, characterised at less than 25uH. In this fault mode the IGBT is characterised for up to ten times the rated current, provided the IGBT is turned off within 10us, but at a slower rate than normal.

II Short circuit arising during the normal on-period
When a load short circuit occurs during the IGBT on period, the collector current rises rapidly and is determined by to the supply voltage V_s and stray inductance L_s according to $di_{rise}/dt=V_s/L_s$. The collector voltage de-saturates and as the collector voltage rise towards the supply V_s the resultant *dv/dt* produced a Miller capacitance charging current, which flows into the gate circuit. Depending on the gate drive impedance, the gate voltage rises which allows higher collector current.
When turn-off is initiated, by reducing the gate voltage to below the threshold level, the resultant collector current fall produces a high voltage across the stray inductance, $V= L_s\ di_{fall}/dt$, which adds to the collector voltage which is already near the supply rail V_s. Because of this over voltage, this mode of short circuit turn-off is more than turning off into a pre-existing short circuit.
The maximum allowable short circuit current at turn-off is dependant on the gate voltage and reduces from ten times rated current at a gate voltage of 18V down to five time rated current at 12V. The short circuit must be commutated within 10us at a slower than normal rate so as to ensure the over voltage due to stray inductance remains within rated voltage limits. Repetitive short circuits are restricted to a frequency of less than one Hertz and can only accumulate to 1000 before device deterioration; both mechanical and electrical.

Stress during the fault period can be reduced if the gate voltage is clamped so that it cannot rise during the Miller capacitance charge period. A Zener diode (and reverse series diode if reverse gate bias is used) across the gate to emitter provides low inductance gate voltage clamping, but the Zener standby to clamping voltage ratio of 1:1.4 limits clamping effectiveness. The preferred method is to clamp the gate to the gate supply voltage by a Schottky diode between gate (diode anode) and gate positive supply (diode cathode). Judicious gate supply ceramic capacitance decoupling will minimise loop inductance which otherwise would deteriorate clamping effectiveness.
A difficulty arises when attempting to utilise the 10us short circuit capabilities of the IGBT. To improve device robustness, short circuit turn-off is staged, or slowed down. It is prudent to utilise the over current capability of the IGBT in order to improve nuisance tripping or brief capacitor charging which are not true faults. A difficulty arises when a demand pulse is significantly less than 10us. The gate drive must be able to cater for sub 10us pulses with normal turn-off yet differentiate 10us delayed slow turn-off when a short circuit fault is serviced.

4.6 The thyristor

Most of the thyristor ratings and characteristics to be considered are not specific to only the silicon-controlled rectifier, although the dynamic characteristics of the gate turn-off thyristor are considered separately.

4.6.1 SCR ratings

The fundamental four layer, three junction thyristor structures and their basic electrical properties were considered in chapter 3.3.

4.6.1i - SCR anode ratings
Thyristors for low-frequency application, such as in 50-60 Hz ac supply systems, are termed *converter-grade* thyristors. When a higher switching frequency is required, so-called *gate commutated* devices like the GTO and GCT are applicable. Such devices sacrifice voltage and current ratings for improved self-commutating capability.

The repetitive peak thyristor voltage rating is that voltage which the device will safely withstand in both the forward off-state V_{DRM}, and reverse direction V_{RRM}, without breakdown. The voltage rating is primarily related to leakage or blocking current I_{RRM} and I_{DRM} respectively, at a given junction temperature, usually 125°C. Since blocking current doubles with every 10K rise in junction temperature T_j, power dissipation increases rapidly with T_j, which may lead to regenerative thermal runaway, turning the device on in the forward direction.

Current related maximum ratings reflecting application requirements include

- peak one cycle surge on-state current I_{TSM}
- repetitive and non-repetitive *di/dt*
- I^2t for fusing.

The maximum junction temperature can be exceeded during non-recurrent over-

current cycles. The maximum non-repetitive on-state surge current is generally quoted for one 10 millisecond sinusoidal period at T_{jmax}. Any non-recurrent rating can be tolerated only a limited number of times before failure results. Such non-recurrent ratings are usually specified to allow fuse and circuit breaker short-circuit protection. The I^2t rating for a 10ms period is another parameter used for fuse protection, where I is non-repetitive rms current.

If the device is turned on into a fault the initial current-time relationship, *di/dt*, during turn-on must be within the device's switching capability. In cases where the initial *di/dt* is rapid compared with the active area-spreading velocity of 50 μm/μs, local hot spot heating will occur because of the high current densities in those areas that have started to conduct.

A repetitive *di/dt* rating is also given for normal operating conditions, which will not lead to device deterioration. This repetitive *di/dt* rating will be specified for a given initial blocking voltage and peak forward current. Certain gate drive conditions are specified and the device must survive for 1000 hours.

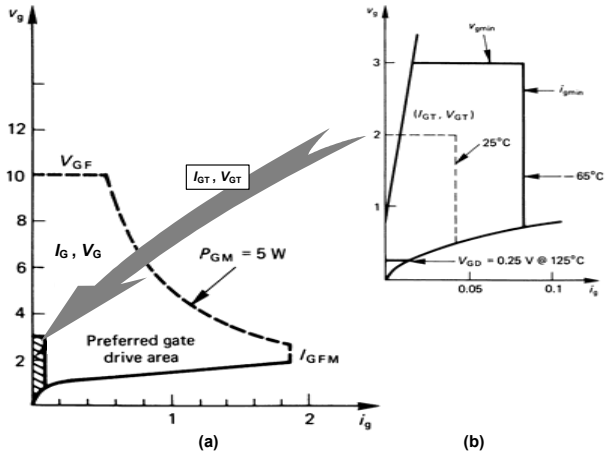


Figure 4.17. *Thyristor gate ratings illustrating: (a) the preferred operating region and (b) minimum gate requirements and their temperature dependence.*

4.6.1ii - SCR gate ratings

The gate ratings usually specified are

- peak and mean gate power, P_{GM} and P_G
- peak forward and reverse gate to cathode voltage, V_{GFM} and V_{GRM}
- peak forward gate current, I_{FMG}.

These gate ratings are illustrated in figure 4.17. The peak gate power rating is obtained by using a low duty cycle pulse, with a mean power that does not exceed

P_G. The reverse gate voltage limit, V_{GRM}, is specified by the avalanche voltage breakdown limit of the reverse-biased gate-to-cathode junction. Figure 4.17 not only shows limit ratings, it also indicates the preferred gate voltage and current, and the minimum requirements which will ensure turn-on at different junction temperatures.

4.6.2 Static characteristics

The static anode voltage-current characteristics of a thyristor are very similar to those of a diode. Gate commutated thyristors tend to have higher on-state voltages for a given current than comparable converter-grade devices. This higher on-state voltage is one of the trade-offs in improving the switching performance.

4.6.2i - SCR gate trigger requirements

Below a certain gate voltage, called the *gate non-trigger voltage* V_{GD}, the manufacturer guarantees that no device will trigger. This voltage level is shown in figure 4.17b. The shaded insert area in figure 4.17a (figure 4.17b) contains all the possible minimum trigger values (I_{GT}, V_{GT}) for different temperatures, that will result in turn-on. The gate requirements (I_{GT}, V_{GT}) have a negative temperature coefficient as indicated in figure 4.17b. To ensure reliable turn-on of all devices, independent of temperature, the trigger circuit must provide a dc signal (I_G, V_G) outside the shaded area. This area outside the uncertainty area, but within the rating bounds, is termed the *preferred gate drive* area.

An increase in anode supporting voltage tends to decrease the gate drive requirements. But if the gate signal is a pulse of less than about 100μs, the turn-on (I_G, V_G) requirement is increased as the pulse duration is decreased. The gate current increase is more significant than the voltage requirement increase. Typically, for a pulse reduced from 100μs to 1μs, the voltage to current increase above the original requirement is 2:10 respectively. This increased drive requirement with reduced pulse time is accounted for by the fact that some of the initial gate p-region charge recombines. When the free charge reaches a certain level the device triggers. Thus, to get the required charge into the gate in a relatively short time compared with the recombination time requires higher current, and hence higher voltage, than for dc triggering.

4.6.2ii – SCR holding and latching current

If the on-state anode current drops below a minimum level, designated as the *holding current* I_H, the thyristor reverts to the forward blocking state. This occurs because the loop gain of the equivalent circuit pnp-npn transistors falls below unity and the regenerative hold-on action ceases. The holding current has a negative temperature coefficient; that is, as the junction temperature falls, the device holding current requirement increases. The holding current is typically about 2% of the rated anode current.

A somewhat higher value of anode on-state current than the holding current is required for the thyristor to latch on initially. If this higher value of anode *latching current* I_L is not reached, the thyristor will revert to the blocking state as soon as the gate trigger signal is removed. After latch-on, however, the anode current may

be reduced to the holding current level, without turn-off occurring. These two static current properties are shown in the *I-V* characteristics in figure 3.21. With inductive anode circuits, it is important to ensure that the anode current has risen to the latching current level before the gate turn-on signal is removed. Continuous gate drive avoids this inductive load problem but at the expense of increased thyristor gate power losses.

4.6.3 Dynamic characteristics

The main thyristor dynamic characteristics are the turn-on and turn-off switching intervals, which are associated with the anode and gate circuit interaction.

4.6.3i– SCR anode at turn-on

Turn-on comprises a delay time t_d and a voltage fall time t_{fv}, such that the turn-on time is $t_{on} = t_d + t_{fv}$.

The turn-on delay time for a given thyristor decreases as the supporting anode voltage at turn-on is increased. The delay time is also decreased by increased gate current magnitude. The gate p-region width dominates the high gate current delay time characteristics while carrier recombination is the dominant factor at low gate current levels.

The anode voltage fall time is the time interval between the 90 per cent and 10 per cent anode voltage levels. The associated anode current rise characteristics are load dependent and the recurrent *di/dt* limit must not be exceeded.

As introduced in chapter 3.3.1, a thyristor can be brought into conduction by means of an anode impressed *dv/dt*, called *static dv/dt* capability, even though no gate current is injected. The anode voltage ramp produces a displacement current according to $i = dQ/dt$ as the central junction scl charges and its width increases. The resultant displacement current flows across the cathode and anode junctions causing emission and, if sufficient in magnitude, turn-on occurs. Static *dv/dt* capability is an inverse function of device junction temperature and is usually measured at $T_{j\max}$.

4.6.3ii – SCR anode at turn-off

As analysed in chapter 3.3.1, once a thyristor is turned on, it remains latched-on provided that

- the holding current remains exceeded
- it is forward biased.

If the supply voltage is ac, a thyristor will turn off after the supply voltage has reversed and the anode current attempts to reverse. The thyristor is thus reverse-biased and this turn-off process is called *line commutation* or *natural commutation.* If the supply voltage is dc and the load is a series *L-C* resonant circuit, the anode current falls to zero when the capacitor is charged. The load current falls below the holding current level and the SCR turns off. This is termed *load commutation.*

In thyristor applications involving dc supplies and resistive/inductive loads, a thyristor once on will remain on. Neither the supply nor the load is capable of reducing the anode current to below the holding current level, or producing a reverse bias across the thyristor. Such a thyristor can be turned off only if the anode current is interrupted or forced below the holding current level. External

circuitry, called a *commutation circuit,* is employed to accomplish turn-off, by reverse-biasing the thyristor and reducing the anode current to near zero. This external turn-off approach, now obsolete, is called *forced commutation*. The gate turn-off thyristor eliminates the need for this external commutation circuitry since the GTO can be commutated from its gate. A topological variation of the forced commutated circuitry method is called *resonant link commutation*.

4.7 The gate turn-off thyristor

In essence, the gate turn-off (GTO) thyristor has similar ratings and characteristics to those of the conventional converter grade SCR, except those pertaining to turn-off. Both GTO turn-on and turn-off are initiated from the gate, hence the power-handling capabilities of the GTO gate are much higher than those of SCR devices.

4.7.1 Turn-on characteristics

Because of the higher p1 gate region concentration, the GTO holding current level and gate trigger requirements are somewhat larger than those of the conventional SCR. Higher anode on-state voltages also result.

At low anode current levels, a steep trailing edge at the end of the gate on-pulse may cause the GTO to unlatch even though the anode current is above the dc holding current level. For this reason, together with the fact that the cathode comprises many interdigitated islands, a continuous, dc gate on-drive is preferred. Continuous gate current prevents any cathode islands from falling out of conduction should the anode current be reduced to near the holding current level. If cathode islands should turn off prematurely and the anode current subsequently rise, the GTO no longer has its full current handling capability and it could overheat, leading to device destruction.

With very high voltage GTO's, turn-on is like that of a high voltage npn transistor which has low gain, limiting the initial rate of rise of anode current, until the regenerative latching action has occurred. Hence an initial, high current of up to six times the steady-state gate requirement is effective for a few microseconds.

4.7.2 Turn-off characteristics

Before commencing turn-off, a minimum on-time of tens of microseconds must be observed so that the principal current may distribute uniformly between the cathode islands. This is to ensure that all cells conduct, such that turn-off occurs uniformly in all cells, rather than being confined to a few cells, where the current to be commutated may be higher than individual cells can survive.

The anode current of a GTO in the on-state is normally turned off via a low voltage, negative gate current, I_{RG}. The negative gate current I_{GQ}, which is just sufficient to turn-off the on-state current I_T is defined as the minimum turn-off current. Turn-off amplification (equation 3.21) is defined as

$$\beta_Q = I_{TGQ} / I_{GQ} \tag{4.36}$$

where β_Q is related to the internal construction of the GTO.

Figure 4.18 illustrates typical gate and anode turn-off waveforms for the GTO.

Application of reverse gate current causes the anode current to reduce after a delay period t_s. This delay time is decreased as the reverse gate current di_{GQ}/dt increases; that is, as I_{RGM} increases and t_s decreases. Increased anode on-state current or junction temperature increases the delay time.

The reverse gate current prevents cathode injection and the anode current rapidly falls to the storage current level, I_{tail}. The subsequently slow current fall time, t_{tail}, is due to charges stored in regions other than the gate and cathode that are not influenced by the reverse gate current and must decrease as a result of natural recombination. Anode n^+ shorts are used to accelerate the recombination process, reducing both storage current and storage time, but at the expense of reverse blocking ability and on-state voltage. Avalanche of the cathode junction (typically -20V) is acceptable on turn-off for a specified time. Reverse gate bias should be maintained in the off-state in order to prevent any cathode injection.

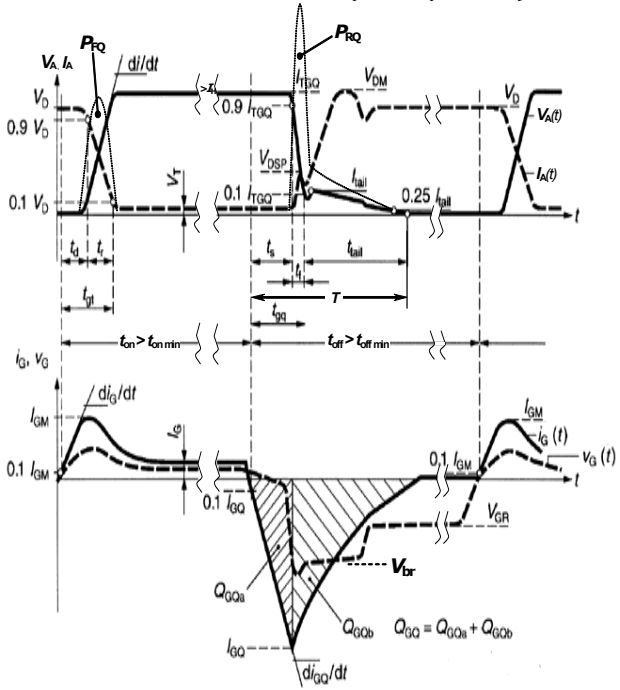


Figure 4.18. *Schematic representation of GTO thyristor turn-off waveforms.*

After turn-off some dispersed charges still exist. A minimum off-time of the order of tens of microseconds is needed for these charges to recombine naturally. This time increases with increased blocking voltage rating. If a turn-on were to be initiated before this recombination is complete, the area of un-combined charge will turn-on first, resulting in a high *di/dt* in a confined area, which may cause a hot spot and possibly destruction.

During the storage and fall time, power loss P_{RQ} occurs as illustrated in figure 4.18 and is given by

$$P_{RQ} = \frac{1}{T}\int_0^T V_A(t)\, I_A(t)dt \qquad \text{(W)} \qquad (4.37)$$

where $T = t_{gq} + t_{tail}$.

The actual anode voltage turn-off waveform is dependent on the load circuit. Care is needed in preventing excessive loss at turn-off, which can lead to device destruction. One technique of minimising turn-off loss is to increase the rate at which the reverse gate current is applied. Unfortunately, in reducing the turn-off time, the turn-off current gain β_Q is decreased, from typically 25 to 3. The anode turn-off voltage $V_A(t)$ in figure 4.18 assumes a capacitive turn-off snubber is used. Such a switching aid circuit is not essential with the GCT, which uses unity reverse gain at turn-off, as considered in chapter 3.3.5.

4.8 Appendix: Effects on MOSFET switching of negative gate drive

The effects of negative gate voltage on MOSFET turn-on and turn-off delays which was analysed in section 4.4.2 are given by

$$V_{gs}(t) = (V_{gg} - V_{gg-})\,[1 - e^{-t/C_{in}R_g}] + V_{gg-} \qquad \text{(V)} \qquad (4.38)$$

$$t_{d\,on} = R_g C_{in}\, \ell n\, \frac{V_{gg} - V_{gg-}}{V_{gg} - V_{TH}} \qquad \text{(s)} \qquad (4.39)$$

$$V_{gs}(t) = (V_{gg} - V_{gg-})\, e^{-t/R_g C_{in}} + V_{gg-} \qquad \text{(V)} \qquad (4.40)$$

$$t_{d\,off} = R_g C_{in}\, \ell n \frac{V_{gg} - V_{gg-}}{V_{TH} + I_L / g_{fs} - V_{gg-}} \qquad \text{(s)} \qquad (4.41)$$

Reading list

See chapter 3 reading list

5

Cooling of Power Switching Semiconductor Devices

Semiconductor power losses are dissipated in the form of heat, which must be transferred away from the switching junction. The reliability and life expectancy of any power semiconductor are directly related to the maximum device junction temperature experienced. It is therefore essential that the thermal design determines accurately the maximum junction temperature from the device power dissipation.

Heat can be transferred by any of, or a combination of, three mechanisms, viz., convection, conduction, and radiation.

Electromagnetic thermal *radiation* is given by

$$P_d = \sigma \varepsilon A (T_1^4 - T_2^4) \qquad (5.1)$$

where σ is the Stefen-Boltzmann constant (5.67×10^{-8} W/m^{2}K^4)
ε is a surface property, termed emissivity, see table 5.4
A is the area involved in the heat transfer
T is absolute temperature

The one dimensional model for general molecular heat transfer is given by

$$P_d = -\lambda A \frac{\delta T}{\delta \ell} + \gamma A \ell \frac{\delta T}{\delta t} \qquad \text{(W)} \qquad (5.2)$$

where P_d is the rate of heat transfer (that is, the power dissipated)
$\delta T = T_2 - T_1$ or ΔT, is the temperature difference between regions of heat transfer
λ is thermal conductivity, see Table 5.2
γ is density of the heatsink material
c is specific heat capacity, $\Delta T = W/mc$
ℓ is distance (thickness).

Assuming steady-state heat dissipation conditions, then $\delta T / \delta t = 0$ in equation (5.2).

Conduction through a solid is given by

$$P_d = \frac{\lambda A}{\ell} \Delta T \qquad \text{(W)} \qquad (5.3)$$

Convection heat transfer through fluid or air, under steady-state conditions, is given by

$$P_d = h A \Delta T \qquad \text{(W)} \qquad (5.4)$$

The heat transfer coefficient h ($=\lambda / \ell$) depends on the heat transfer mechanism used and various factors involved in that particular mechanism.

For natural vertical convection in free air the losses for a plane surface may be approximated by the following empirical formula

$$P_d = 1.35 A \sqrt[4]{\frac{\Delta T^5}{\ell}} \qquad \text{(W)} \qquad (5.5)$$

where ℓ is the vertical height in the direction of the air flow.

Two case occur for forced air flow, and the empirical losses are

for laminar flow

$$P_d = 3.9 A \Delta T \sqrt{\frac{v}{\ell}} \qquad \text{(W)} \qquad (5.6)$$

for turbulent flow

$$P_d = 6.0 A \Delta T \sqrt[3]{\frac{v^4}{\ell}} \qquad \text{(W)} \qquad (5.7)$$

where v is the velocity of the vertical air flow.

It is generally more convenient to work in terms of thermal resistance which is defined as the ratio of temperature to power. From equation (5.4), thermal resistance R_θ is

$$R_\theta = \frac{\Delta T}{P_d} = \frac{1}{hA} = \frac{\ell}{\lambda A} \qquad \text{(K/W)} \qquad (5.8)$$

The average power dissipation P_d and maximum junction temperature $T_{j\max}$, plus the ambient temperature T_a, determine the necessary heat sink, according to equation (5.8)

$$P_d = \frac{T_{j\max} - T_a}{R_{\theta j\text{-a}}} \qquad \text{(W)} \qquad (5.9)$$

where $R_{\theta j\text{-a}}$ is the total thermal resistance from the junction to the ambient air. The device user is restricted by the thermal properties from the junction to the case for a particular package, material, and header mount according to

$$P_d = \frac{T_{j\max} - T_c}{R_{\theta j\text{-c}}} \qquad \text{(W)} \qquad (5.10)$$

where T_c is the case temperature, K and
$R_{\theta j\text{-c}}$ is the package junction-to-case thermal resistance, K/W.

An analogy between the thermal equations and Ohm's law is often made to form models of heat flow. The temperature difference ΔT could be thought of as a voltage

drop ΔV, thermal resistance R_θ corresponds to electrical resistance R, and power dissipation P_d is analogous to electrical current I. *[viz., $\Delta T = P_d R_\theta \equiv \Delta V = IR$]*

5.1 Thermal resistances

A general thermal radiation model, or thermal equivalent circuit for a mounted semiconductor is shown in figure 5.1. The total thermal resistance from the virtual junction to the open air, $R_{\theta j\text{-}a}$, is

$$R_{\theta j\text{-}a} = R_{\theta j\text{-}c} + \frac{R_{\theta c\text{-}a}(R_{\theta c\text{-}s} + R_{\theta c\text{-}a})}{R_{\theta c\text{-}a} + R_{\theta c\text{-}s} + R_{\theta s\text{-}a}} \quad \text{(K/W)} \qquad (5.11)$$

In applications where the average power dissipation is of the order of a watt or so, power semiconductors can be mounted with little or no heat sinking, whence

$$R_{\theta j\text{-}a} = R_{\theta j\text{-}c} + R_{\theta c\text{-}a} \quad \text{(K/W)} \qquad (5.12)$$

Generally, when employing heat sinking $R_{\theta c\text{-}a}$ is large compared with the other model components and equation (5.11) can be simplified to

$$R_{\theta j\text{-}a} = R_{\theta j\text{-}c} + R_{\theta c\text{-}s} + R_{\theta s\text{-}a} \quad \text{(K/W)} \qquad (5.13)$$

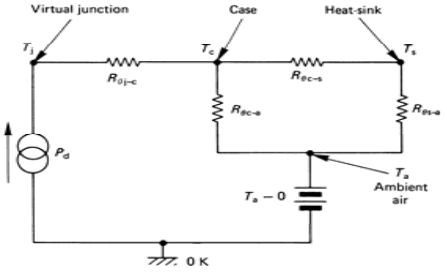


Figure 5.1. *Semiconductor thermal radiation equivalent circuit.*

5.1.1 Contact thermal resistance, $R_{\theta c\text{-}s}$

The case-to-heat-sink thermal resistance $R_{\theta c\text{-}s}$ depends on the package type, interface flatness, mounting pressure, and whether thermal-conducting grease and/or an insulating material is used. In general, increased mounting pressure decreases the interface thermal resistance, and no insulation with thermal grease results in minimum

$R_{\theta c\text{-}s}$. Common electrical insulators are mica, aluminium oxide, and beryllium oxide in descending order of thermal resistance, for a given thickness and area. Table 5.1 shows typical contact thermal resistance values for smaller power device packages, with various insulating and silicone grease conditions.

5.1.2 Heat-sink thermal resistance, $R_{\theta s\text{-}a}$

The thermal resistance for a flat square plate heat sink may be approximated by

$$R_{\theta s\text{-}a} = \frac{3.3}{\sqrt{\lambda \ell}} C_f^{1/4} + \frac{650}{A} C_f \quad \text{(K/W)} \qquad (5.14)$$

Typical values of heatsink thermal conductance λ in W/K cm at 350 K, are shown in Table 5.2 and

ℓ is the thickness of the heat sink in mm
A is the area of the heat sink in cm^2
C_f is a correction factor for the position and surface emissivity of the heat-sink orientation according to Table 5.3.

Table 5.1. Typical case-to-heat-sink thermal resistance value for various packages

Package	*Insulating washer*	$R_{\theta c\text{-}s}$ *(K/W)*	
		Silicone grease	
		with	*without*
TO-3	No insulating washer	0.10	0.3
	Teflon	0.7-0.8	1.25-1.45
	Mica (50 -100 µm)	0.5-0.7	1.2-1.5
TO-66	No insulating washer	0.15-0.2	0.4-0.5
	Mica (50 -100 µm)	0.6-0.8	1.5-2.0
	Mylar (50 -100 µm)	0.6-0.8	1.2-1.4
TO-220	No insulating washer	0.3-0.5	1.5-2.0
	Mica (50 -100 µm)	2.0-2.5	4.0-6.0
TO-247	No insulating washer	0.1-0.2	0.4-1.0
	Mica (50 -100 µm)	0.5-0.7	1.2-1.5

Table 5.2. Thermal conductivity

Material	*λ (W/K cm)*
diamond	2
aluminium	2.08
copper	3.85
brass	1.1
steel	0.46
mica	0.006
beryllium	2.10
oxide ceramic	1.4
$A1_20_3$	0.27
solder (non-lead)	0.44
silicon grease	0.01
still air	0.0004

Table 5.3. Heatsink correction factor

Surface position		
C_f	*Shiny*	*Blackened*
vertical	0.85	0.43
horizontal	1.0	0.50

Table 5.4. Emissivity values

Material	*ε*
Matt surface	0.95
Polished aluminium	0.04
$A1_20_3$	0.15

The correction factor C_f illustrates the fact that black surfaces are better heat radiators and that warm air rises, creating a 'chimney' effect. Equation (5.14) is valid for one power-dissipating device, in the centre of the sink, at a static ambient temperature up to about 45°C, without other radiators in the near vicinity.

In order to decrease thermal resistance, inferred by equation (5.8), finned-type heat sinks are employed which increase sink surface area. Figure 5.2 illustrates graphs of thermal performance against length for a typical aluminium finned heat sink. This figure shows that $R_{\theta s\text{-}a}$ decreases with increased sink length. Minimal reduction results from excessively increasing length as shown in figure 5.2b.

Unless otherwise stated, the heat sink is assumed black and vertically mounted with negligible thermal resistance from case to sink. In accordance with the data in table 5.3, a general derating of 10 to 15 per cent for a bright surface and 15 to 20 per cent in the case of a horizontal mounting position, is usually adopted.

The effective sink thermal resistance can be significantly reduced by *forced air cooling*, as indicated in figure 5.3 and equations (5.6) and (5.7). If the air flow is

- laminar, heat loss is proportional to the square root of air velocity;
- turbulent, velocity to the power of 0.8.

Liquid cooling can further reduce effective thermal resistance to as low as 0.1K/W and may provide a much more compact heat-sink arrangement. Both oil and water are used as the coolant and the heat-sink arrangement can either be immersed in the fluid, or the fluid is pumped through the heat sink. The heat can then be dissipated remotely. Water has the advantage of low viscosity, so can be pumped faster than oil. While oil may be inflammable, water corrodes thus requiring the use of de-ionised water with an oxide inhibitor, like antifreeze. Oil emersion has the added advantage of offering possibilities of increasing the breakdown and corona voltage levels, particularly with devices rated above a few kilovolts.

Heat pipes are efficient, passive, thermal devices for extracting and remotely dissipating heat. A heat pipe is a hollow metal or ceramic tube (for high voltage isolation), typically less than 1mm diameter and a few hundred cm long, closed at each end and containing a dielectric, non-electrical conducting transfer fluid (refrigerant such as methanol, Freon or even water) under reduced pressure so as to reduce the fluid boiling point. The component to be cooled is mounted on the evaporator end (the hot end), where the heat boils and expands the liquid to the vapour phase. This vapour rises through the adiabatic tube section to the remote condenser end of the tube (the cold end), taking the heat within it. The vapour condenses back to the liquid phase, releasing its latent heat of vaporisation, and creating a pressure gradient which helps draw more vapour towards the condenser. The temperature difference between the ends may only be a couple of degrees. The remotely situated condenser end is connected to an external heatsink or a radiator type grill, for cooling. The condensed working fluid runs back to the evaporator end due to gravity, or along a wick due to capillary pressure action, depending on the physical application orientation design for the heat pump. The typical temperature operating range is -55°C to over 200°C.

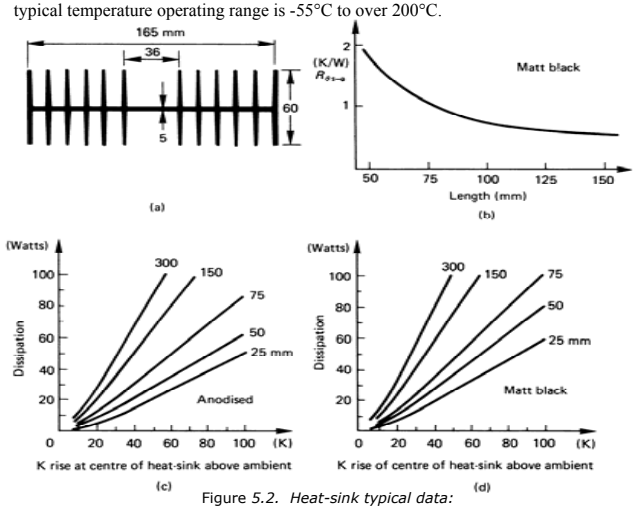


Figure *5.2. Heat-sink typical data:*
(a) cross-section view; (b) heat-sink length versus thermal resistance for a matt black surface finish; (c) temperature rise versus dissipation for an anodised finish and different lengths; and (d) as for (c) but with a matt black surface finish.

The heat power transfer capabilities of a heat pipe are related to its cross-sectional area A and length ℓ according to

$$P = k\frac{A}{\ell} \quad \text{(W)} \tag{5.15}$$

while the temperature difference ΔT between the hot and cold ends is

$$\Delta T = k'P\left(\frac{1}{A_e}+\frac{1}{A_c}\right) \quad \text{(K)} \tag{5.16}$$

where A_e and A_c are the effective evaporator and condenser areas.

5.2 Modes of power dissipation

For long, >1ms, high duty cycle pulses the peak junction temperature is nearly equal to the average junction temperature. Fortunately, in many applications a calculation of the average junction temperature is sufficient and the concept of *thermal resistance* is valid.

Other applications, notably switches driving highly reactive loads, may create severe current-crowding conditions which render the traditional concepts of thermal design invalid. In these cases, transistor safe operating area or thyristor *di/dt* limits must be observed, as applicable.

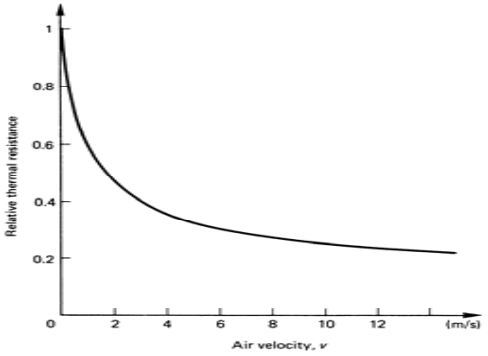


Figure 5.3. *Variation of forced air cooled heat-sink relative thermal resistance with surface air flow.*

In yet other applications, intermittent operation in extreme temperature conditions may cause thermal shock and can introduce deep thermal cycling problems with wafer mountings in multi-chip large area packages. Large rapid temperature changes in excess of 80°C, stress the hard solder bonding, causing fatigue and eventual failure after a finite number of cycles N, approximated by

$$N = \frac{k}{A \times \Delta T^2} \tag{5.17}$$

where A is the die area and ΔT is the thermal shock temperature change. The constant k depends on the package, type of hard soldering, etc. Large, multiple die IGBT packages suffer from thermal shock limitations, relatively low reliability, because of the sheer large number of die interconnected over a large area in the module.

Floating silicon wafers in disc type packages suffer from differential thermal expansion.

In a related thermal application, where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. Figure 5.4 shows by comparison such a condition, where the operating frequency, not the maximum power dissipated, is dominant in determining junction temperature. In this case *thermal impedance* $Z_{\theta j\text{-}c}$ is used instead of thermal resistance $R_{\theta j\text{-}c}$ such that $Z_{\theta j\text{-}c} = r(t_p)\ R_{\theta j\text{-}c}$, where $r(t_p)$ is the normalising factor yielded from the normalised transient thermal impedance curves for the particular device. Appropriate values for the pulse width t_p and duty cycle factor δ must be used.

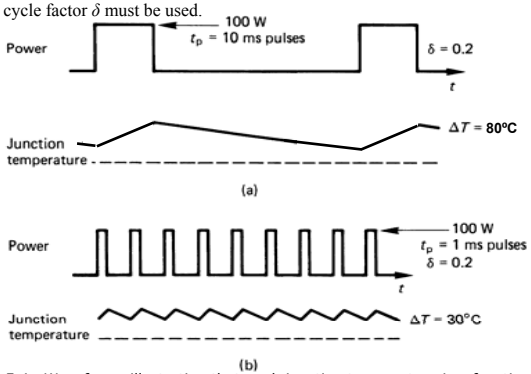


Figure 5.4. Waveforms illustrating that peak junction temperature is a function of switching frequency:
(a) lower switching frequency with 10 ms pulse and a 20 per cent duty cycle and (b) high frequency and 1 ms pulse with a duty cycle the same as in (a).

5.2.1 Pulse response

The concept of thermal impedance is based on rectangular power pulses. Non-rectangular pulses are converted to equivalent energy, rectangular pulses having the same peak power, P_p, of period t_p, as shown in figure 5.5. The resultant rectangular power pulse will raise the junction temperature higher than any other wave shape with the same peak and average values, since it concentrates its heating effects into a shorter period of time, thus minimising cooling during the pulse. Worse case semiconductor thermal conditions result.

Figure 5.6 shows the thermal impedance curves for a power switching device, normalised with respect to the steady-state thermal resistance $R_{\theta j\text{-}c}$. The curve labelled 'single pulse' shows the rise of junction temperature per watt of power dissipated as a function of pulse duration. The thermal impedance for repetitive pulses Z, of duty cycle δ, can be determined from the single pulse value z according to

$$Z(t_p,\delta) = \delta + (1-\delta)z(t_p) \qquad \text{(K/W)} \qquad (5.18)$$

The equation (5.10) becomes

$$P_p = \frac{T_{j\max} - T_c}{Z(t_p,\delta)} \quad = \frac{T_{j\max} - T_c}{r(t_p)R_{\theta j-c}} \qquad \text{(W)} \qquad (5.19)$$

Note that the peak power value P_p is employed, and then only for thermal analysis from the junction to the case. That is, $Z_{\theta j\text{-}c}$ is the only thermal impedance that exists.

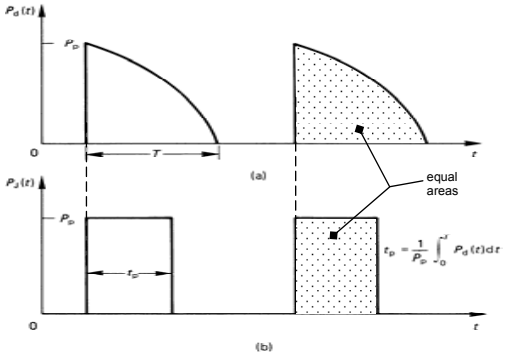


Figure 5.5. *Conversion of non-rectangular power pulse (a) into equivalent rectangular pulse (b).*

5.2.2 Steady-state response

Large cycle-by-cycle temperature fluctuations occur at low frequencies. As frequency increases, thermal inertia of the junction smoothes out instantaneous temperature fluctuations, as shown in figure 5.4b, and the junction responds more to average, rather than peak power dissipation. At frequencies above a kilohertz and duty cycles above 20 per cent, cycle-by-cycle temperature fluctuations usually become small, and the peak junction temperature rise approaches the average power dissipation multiplied by the steady-state junction-to-case thermal resistance, within a few per cent.

Because of thermal inertia, the heat sink responds only to average power dissipation, except at low frequencies. The steady-state thermal conditions for the heat sink are given by

$$P_d = \frac{T_c - T_a}{R_{\theta c\text{-}s} + R_{\theta s\text{-}a}} \qquad \text{(W)} \qquad (5.20)$$

where P_d is the average power dissipation, which is the peak power multiplied by the on-time duty cycle δ for rectangular power pulses. The difficulty in applying equation (5.20) often lies in determining the average power dissipation.

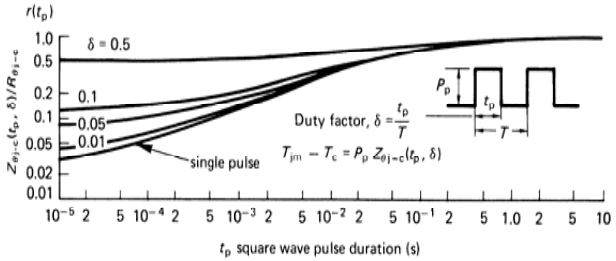


Figure 5.6. *Transient thermal impedance curves; normalised with respect to the steady state thermal resistance, $R_{\theta j\text{-}c}$.*

5.3 Average power dissipation

Two commonly used empirical methods for determining power dissipation P_d are

- graphical integration and
- power superposition.

5.3.1 Graphical integration

Graphical integration may be formulated by digitally storing a complete cycle of test device voltage and current under limiting steady-state temperature conditions. Each voltage and current time-corresponding pair are multiplied together to give instantaneous values of power loss. Numerical integration techniques are then employed to give the average power dissipation.

5.3.2 Practical superposition

This technique is based on substituting a smooth dc voltage source for a complex waveform. A two-pole, two-position switching arrangement is used, which firstly allows operation of the load with the device under test, until the monitored case temperature stabilises. Then, by throwing the switch to the test mode position, the device under test (DUT) is connected to a dc power supply, while the other pole of the switch supplies the normal power to the load to keep it operating at full power level conditions. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc source voltage and current values are multiplied together to obtain the average power dissipated.

5.4 Power losses from manufacturers' data sheets

The total power dissipation P_d is the sum of the switching transition loss P_s, the on-conduction loss P_d, drive input device loss P_G, and the off-state leakage loss P_ℓ.
The average total power loss is given by

$$P_d = f_s \int_0^{1/f_s} v(t)i(t)dt \qquad \text{(W)} \qquad (5.21)$$

where f_s is the switching frequency and *v(t)* and *i(t)* are the device instantaneous voltage and current over one complete cycle of period $1/f_s$. The usual technique for determining total power loss is to evaluate and sum together each of the individual average power loss components.

5.4.1 Switching transition power loss, P_s

Figure 5.7 shows typical power device voltage-current switching waveforms. Normally an exact solution is not required and an approximation based on straight line switching intervals is usually adequate.
For a resistive load, as derived in chapter 6

$$P_s = \tfrac{1}{6} V_s I_m \tau f_s \qquad \text{(W)} \qquad (5.22)$$

and for an inductive load, as derived in chapter 6

$$P_s = \tfrac{1}{2} V_s I_m \tau f_s \qquad \text{(W)} \qquad (5.23)$$

where τ is the period of the switching interval (both on and off), and V_s and I_m are the maximum voltage and current levels as shown in figure 5.7. Switching losses occur at both turn-on and turn-off.

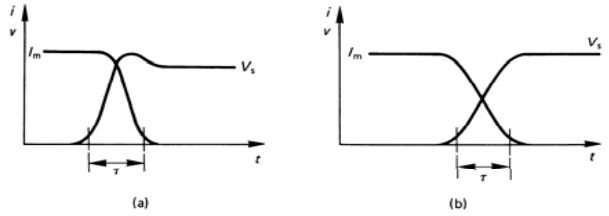


Figure 5.7. *Typical voltage and current at turn-off switching transition for: (a) an inductive load and (b) a resistive load. Current and voltage are interchanged at turn-on.*

5.4.2 Off-state leakage power loss, P_ℓ

During the switched-off period, a small, exponentially temperature dependent current I_ℓ, will flow through the switch. The loss due to this leakage current is

$$P_\ell = I_\ell V_s (1 - \delta) \qquad \text{(W)} \qquad (5.24)$$

where δ is the on-time duty cycle of the switch. Normally P_ℓ is only a small part of the total loss so that the error in neglecting P_ℓ is not usually significant.

5.4.3 Conduction power loss, P_c

The average conduction power loss under a steady-state current condition is given by

$$P_c = \delta I_{on} V_{on} \qquad \text{(W)} \qquad (5.25)$$

although equation (5.21) is valid in the general case when the integration is performed over the interval corresponding to δ.
The conduction loss for the MOSFET is usually expressed in terms of its on-state resistance (equations (3.14) and (4.12))

$$P_c = \delta\, I^2_{d(rms)} R_{ds(on)}$$
$$\simeq \delta\, I^2_{d(rms)} R_{ds(on)}(25°C)\left\{1+\frac{\alpha}{100}\right\}^{T_J-25°C} \quad \text{(W)} \tag{5.26}$$

where α is the temperature coefficient of the on-state resistance, which is positive. A linear resistance approximation of equation (5.26) is quite accurate above 25°C if α is small, such that P_c can be approximated by

$$P_c \approx \delta\, I^2_{d(rms)} R_{ds(on)}(25°C)\left\{1+\alpha\,(T_j - 25°C)\right\} \quad \text{(W)} \tag{5.27}$$

5.4.4 Drive input device power loss, P_G

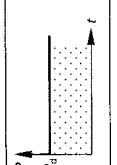
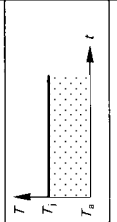
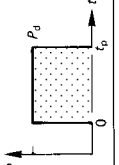
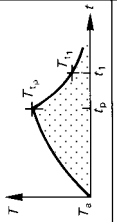
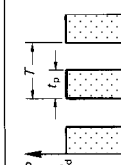
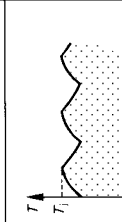
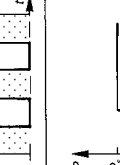
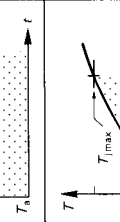
A portion of the drive power is dissipated in the controlling junction or, in the case of the MOSFET, in the internal gate resistance. Usually more power is dissipated in the actual external drive circuit resistance. Drive input loss is normally small and insignificant compared with other losses, and can usually be ignored.
Two possible exceptions are:

- One notable exception is in the case of the power thyristor, where continuous gate drive is used to avoid loss of latching or when the holding current is high. The holding current can be 3% of the anode current thus the gate to cathode junction loss can be included in the total loss calculation for better accuracy. Thus, for a gate junction voltage V_{GC} the gate losses are given by
$$P_g = \delta\, I_G V_{GC} \tag{5.28}$$
The recovery loss of the gate commutated thyristor (GCT) cathode junction can be included since it is significant because the full anode current is extracted from the gate, thus is involved in recovery of the cathode junction.
- A second exception is the MOSFET and IGBT at high switching frequencies, >50kHz, when the loss in the device, associated with providing the gate charge Q_T is given by equation (4.35):
$$P_G(R_{\text{int}}) = V_{gg} Q_T f_s \frac{R_{G\text{int}}}{R_{G\text{int}} + R_{G\text{ext}}} \quad \text{(W)} \tag{5.29}$$

5.5 Heat-sinking design cases

Heat-sink design is essentially the same for all power devices, but the method of determining power loss varies significantly from device type to device type. The information given in data sheets, in conjunction with the appropriate equation in table 5.2, allows the designer to calculate power semiconductor thermal rating for a variety of conditions.

Table 5.4. Power rating equations based on thermal considerations

Load condition	Junction power loss waveform	Junction temperature rise waveforms	Junction temperature solution
(a) Continuous			$T_j - T_a = P_d R_\theta$
(b) Single pulse			$T_{t_p} - T_a = P_d z_\theta(t_p),\ \delta = 0$ $T_{t_1} - T_a = P_d\{z_\theta(t_1) - z_\theta(t_1 - t_p)\}$
(c) Constant frequency and duty cycle			$\delta = t_p/T$ approximate steady state solution $T_j - T_a = P_d\{\delta R_\theta + (1-\delta) z_\theta(T + t_p) - z_\theta(T) + z_\theta(t_p)\}$
(d) Continuous duty followed by a step in power			$T_{j\max} - T_j = P_d R_\theta + (P_s - P_d) z_\theta(t_s)$

5.5.1 Heat-sinking for diodes and thyristors

At low switching frequencies (<100 Hz), switching loss can be ignored. In the case of rectifying diodes or converter-grade thyristors, 50 to 60 Hz, switching loss can usually be ignored. Fast-recovery power diodes switching at less than 500Hz can also have switching losses neglected at low *VA* levels.

5.5.1i - *Low-frequency switching*
At a given current level I_F and on-time duty cycle δ, on-state power loss can be read directly from the manufacturers' data. Figure 5.8a illustrates loss for square-wave power pulses, while figure 5.8b illustrates loss in the case of half-wave sinusoidal current. Figure 5.8b gives energy loss per cycle, which may be converted to power when multiplied by the sinusoidal pulse frequency.
Thyristor loss due to the current waveform initial rate of rise of current, *di*/*dt*, can be incorporated and its contribution is added into the manufacturers' conduction loss data for a given device type.

5.5.1ii - *High-frequency switching*
At frequencies greater than about 100 Hz, fast-recovery diodes are normally employed and at about 500Hz, switching losses must be added to the on-state conduction loss. Diode turn-off loss is usually more significant than turn-on loss. Manufacturers provide maximum reverse recovery charge, Q_R, characteristics as shown in figure 5.9. The reverse recovery charge is a linear function of temperature and between the given junction temperatures of 25°C in figure 5.9a and 150°C in figure 5.9b, interpolation of Q_R is used.
The reverse recovery W.s/pulse, J_R, can be approximated by

$$J_R = V_R Q_R \qquad \text{(J)} \qquad (5.30)$$

where V_R is the reverse voltage applied to the diode just after turn-off. The reverse recovery average power loss is given by

$$P_s = V_R Q_R f_s \qquad \text{(W)} \qquad (5.31)$$

The total average power loss is the algebraic sum of the steady-state conduction loss and the recovery loss.

Example 5.1: ***Heat-sink design for a diode***
A fast-recovery diode switches 60 A rectangular current pulses at 10 kHz. The off-state bias is 400 V and the external circuit inductance limits the reverse dI_F/dt to 100 A/μs. If the device junction-to-case thermal resistance is 0.7 K/W, calculate the minimum heat-sink requirement with a 50 per cent duty cycle, if the maximum ambient temperature is 40°C.

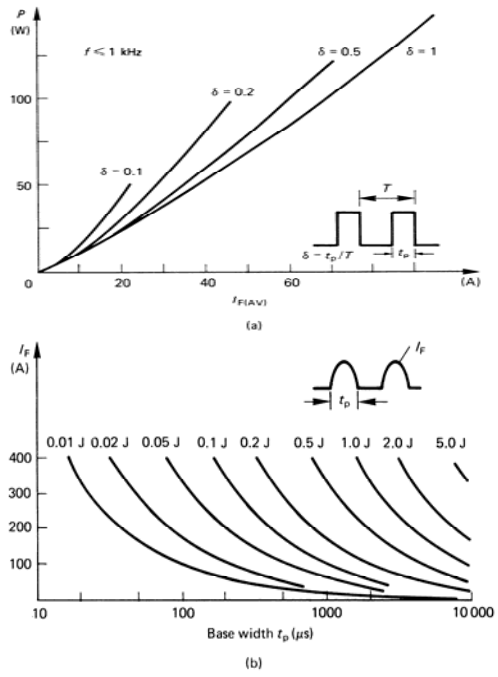


Figure 5.8. *Diode on-state energy loss at low frequency as a function of forward current for: (a) squarewave power pulses and (b) sinusoidal power pulses.*

Solution
The steady-state loss given from figure 5.8a is about 40 W when using $I_{F(AV)} = 30$ A for $\delta = 0.5$.
Minimum heat-sinking requirements occur when T_j is a maximum, that is 150°C from figure 5.9b. From figure 5.9b, for dI_F/dt = 100 A/μs and I_F = 60 A, the maximum reverse recovery charge is 1.3 μC. The switching power loss (over estimate) is given by

$$P_s = Q_R V_R f_s$$
$$= 1.3\mu C \times 400V \times 10kHz = 5.2W$$

The total power loss is therefore

$$P_d = 40 + 5.2 = 45.2W$$

Since the frequency and duty cycle are both high, the concept of thermal resistance is appropriate; that is

$$T_j = T_a + P_d (R_{\theta j\text{-}c} + R_{\theta c\text{-}a})$$

Therefore $$150°C = 40V + 45.2A \times (0.7 + R_{\theta c\text{-}a})$$

whence $$R_{\theta c\text{-}a} = 1.73 \text{ K/W}$$

Figure 5.2b shows that a minimum of 50 mm length of matt black heat sink is required. This assumes that the case-to-sink thermal resistance is negligible. In order to improve device reliability and lifetime, operation at $T_{j\max}$ is avoided. A derating of 40 to 50°C significantly reduces junction thermal fatigue and can result in a tenfold improvement in reliability. To restrict $T_{j\max}$ to 100°C, $R_{\theta c\text{-}a}$=0.7 K/W, necessitating 120 mm of the heat sink as characterised in figure 5.2b. The flatness of the $R_{\theta s\text{-}a}$ curve means that the effectiveness of the heat sink is diminished and a shorter length of a profile offering lower thermal resistance would be more effective in reducing device thermal fatigue.

♣

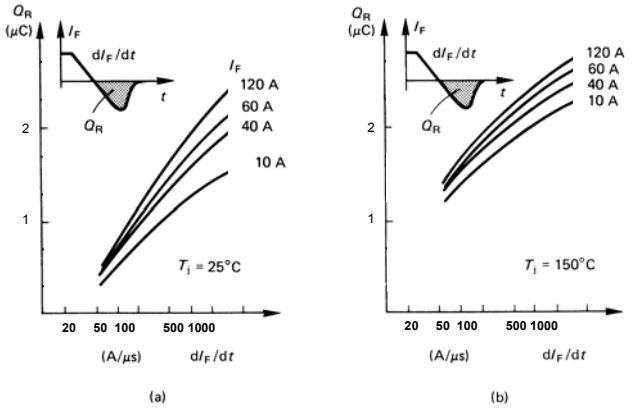


Figure 5.9. Reverse recovery charge as a function of forward current and dI_F/dt at:

(a) 25°C and (b) 150°C junction temperature.

5.5.2 Heat-sinking for IGBTs

The IGBT conduction loss is related to the gate voltage and the collector current magnitude, which specify the on-state voltage. No simple power loss characteristic is possible, as in figure 5.8 for the diode and thyristor. Fortunately, the power switching IGBT is used in such a way that its on-state collector-emitter voltage is fairly constant, whence conduction loss is given by

$$P_c = \delta \, v_{ce} \bar{I}_c \qquad \text{(W)} \qquad (5.32)$$

Example 5.2: ***Heat-sink design for an IGBT- repetitive operation at a high duty cycle***
A power IGBT is used to switch a 20 A, 100 V highly inductive load at 10 kHz. The transistor maximum on-state duty cycle is 90 per cent and the device has a junction-to-case thermal resistance of 0.7 K/W. The transistor on-state voltage is maintained at 2 V and the switch-on and switch-off times are 1 and 2 μs respectively. If the junction temperature is not to exceed 125°C with a maximum ambient temperature of 35°C, what is the minimum heat-sink requirement? Assume that the transistor is in a T0247 package, which is mounted directly on the heat sink but with silicone grease used.

Solution
Since both the duty cycle and switching frequency are high, the peak junction temperature is closely approximated by the average junction temperature. That is, the concept of thermal resistance is valid.
The on-state power loss is given by

$$P_c = \delta v_{ce} \bar{I}_c$$
$$= 0.9 \times \ 2V \times 20A \ = 36 \text{ W}$$

From equation (5.23), the switching losses for an inductive load are

$$P_s = P_{s(\text{on})} + P_{s(\text{off})}$$
$$½ \times 100 \times 20 \times (1\mu s + 2\mu s) \times 10 \text{ kHz} = 30 \text{ W}$$

Total power losses P_d are 36W+30W = 64 W.
From

$$T_{j\max} = T_a + P_d (R_{\theta j\text{-}c} + R_{\theta c\text{-}s} + R_{\theta s\text{-}a})$$
$$125°C = 35°C + 64W \times (0.7 + 0.1 + R_{\theta s\text{-}a})$$

Therefore $$R_{\theta c\text{-}a} = 0.53 \text{ K/W}$$

The case-to-heat-sink thermal resistance value of 0.1 K/W for a T0247 non-insulated case using silicone thermal grease was obtained from table 5.1. To obtain the minimum heat-sink thermal resistance of 0.53 K/W, 150 mm of the heat sink with cross-section shown in figure 5.2a is required. Clearly a sink profile that has a lower thermal resistance per unit length would be more suitable.

♣

5.5.3 Heat-sinking for power MOSFETs

Switching losses in MOSFETs tend to be low at frequencies below 20 kHz and therefore may be neglected, along with gate and off-state losses. Conduction loss is generally expressed in terms of the on-state resistance as I^2R loss. The first step in the thermal design is to determine the total power dissipation in the device, which is generally dominated by the conduction loss. Determination of this loss is not trivial since, while the power dissipation determines junction temperature, the power dissipation itself is a function of junction temperature, because the on-state resistance increases with temperature, as shown in figure 3.13.

Example 5.3: ***Heat-sink for a MOSFET - repetitive operation at high peak current, low duty cycle***

Find the thermal resistance of the heat sink needed for a MOSFET conducting a repetitive 20 A rectangular current waveform. On-time is 10 μs, duty cycle is 0.1 per cent and the maximum ambient temperature is 40°C. Assume $R_{ds(on)}$ at 150°C and 20 A is 5 Ohms, and $R_{\theta j\text{-}c}$ = 1.5 K/W.

Solution

Since the on-state duty cycle and switching frequency are both low, the peak junction temperature at the end of the on-period will be significantly different from the average junction temperature. The concept of thermal resistance from junction to case is therefore invalid; the concept of thermal impedance is used instead.

The power per pulse = $P_p = I^2R = 20^2 \times 5\Omega = 2 \times 10^3$ W

The case temperature is given by

$$\begin{aligned} T_j &= T_c + P_p \times Z_{\theta j\text{-}c} \\ &= T_c + P_p\, r(t_p)\, R_{\theta j\text{-}c} \end{aligned}$$

where $r(t_p)$ is the transient thermal impedance factor for the junction-to-case. For a 10 μs pulse from figure 5.6, $r(t_p)$ = 0.03, assuming δ=0.001≈ a single pulse condition, thus

$$150°C = T_c + 2\times10^3 \times 0.03 \times 1.5$$

that is $T_c = 60°C$

Because of the heat-sink thermal inertia, the concept of thermal resistance is used for calculations involving the heatsink. That is

$$T_c = T_a + \overline{P}_d R_{\theta c\text{-}a} = T_a + \delta P_d R_{\theta c\text{-}a}$$

$$60°C = 40°C + 0.001 \times 2\times10^3 \times R_{\theta c\text{-}a}$$

thus $R_{\theta c\text{-}a} = 10$ K/W

The heat sink of cross-section shown in figure 5.2a is not suitable in this application,

and one of a much smaller surface area is applicable. A heatsink may not be necessary since the package thermal resistance $R_{\theta c\text{-}a}$, shown in figure 5.1, may be less than 10K/W, there in satisfying equation (5.12). See problem 5.4.

♣

If the junction operating temperature is unknown but can be assumed greater than 25°C, from equation (5.27), the total power loss can be expressed as

$$P_d = P_o + I^2_{d(\text{rms})} R_{ds(\text{on})}(25°C)\left\{1+\alpha\,(T_j - 25°C)\right\} \quad \text{(W)} \qquad (5.33)$$

where P_o represents all losses other than the conduction loss, and is assumed temperature independent The temperature coefficient α for $R_{ds(on)}(25°C)$ is positive, typically 1 per cent/K as indicated in figure 3.13. The usual thermal equality holds, that is

$$T_j = T_a + R_{\theta j\text{-}a}\, P_d \quad \text{(K)} \qquad (5.34)$$

Combining equations (5.33) and (5.34) by eliminating T_j yields

$$P_d = \frac{P_o + I^2_{d(\text{rms})} R_{ds(\text{on})}(25°C)\left\{1+\alpha\,(T_a - 25°C)\right\}}{1 - I^2_{d(\text{rms})} R_{ds(\text{on})}(25°C)\alpha\, R_{\theta j\text{-}a}} \quad \text{(W)} \qquad (5.35)$$

The denominator yields an asymptotic maximum drain current of

$$I_{d(\text{rms})} = \frac{1}{\sqrt{R_{ds(\text{on})}(25°C)\ \alpha\ R_{\theta j\text{-}c}}} \quad \text{(A)} \qquad (5.36)$$

at which current thermal runaway would result. In practice, insufficient gate voltage is available and the device would leave the constant-resistance region and enter the constant-current region, where the above analysis is invalid.

Example 5.4: ***Heat-sink design for a MOSFET -repetitive operation at high duty cycle***

A power MOSFET switches 5 A rms at 10 kHz with a maximum on-state duty cycle of 90 per cent. The junction-to-case thermal resistance is 0.7 K/W, the maximum ambient temperature 35°C, and on-state resistance at 25°C is 1 Ohm. If the heat-sink arrangement yields an effective case-to-ambient thermal resistance of 1.3 K/W and α=0.01 /K, what is the junction operating temperature?

Solution

Since the switching frequency and duty cycle are both relatively high, the thermal resistance concept based on average junction power dissipation is valid.

Assuming zero losses other than conduction losses, then P_o = 0. Equations (5.33) and (5.34) rearranged to eliminate P_d yielding

$$T_j = \frac{T_a + R_{\theta j\text{-a}} I^2_{d(\text{rms})} R_{ds(\text{on})}(25°\text{C})\{1-25\alpha\}}{1-\alpha R_{\theta j\text{-a}} I^2_{d(\text{rms})} R_{ds(\text{on})}(25°\text{C})} \quad \text{(W)} \qquad (5.37)$$

Assuming typical $\alpha = 0.01$/K and $R_{\theta j\text{-a}} = R_{\theta j\text{-c}} + R_{\theta c\text{-a}}$

$$T_j = \frac{35°\text{C} + 2\times 5^2 \times 1\Omega \times (1\text{-}25\times 0.01)}{1 - 0.01\times 2\times 5^2 \times 1\Omega} = 145°\text{C}$$

♣

Example 5.5: ***Two thermal elements a common heatsink***

A dc chopper has a MOSFET switch that dissipates 40W and a load freewheel diode that dissipates 24W. Each power device is mounted on a common heatsink. The MOSFET has a junction-to-case thermal resistance of 0.7K/W and a case-to-heatsink thermal resistance of 0.5K/W. The diode has a junction-to-case thermal resistance of 0.8K/W and a case-to-heatsink thermal resistance of 0.6K/W.

i. Determine the maximum heatsink thermal resistance that maintains both junction temperatures below 90°C in a 30°C ambient.

ii. Semiconductor lifetime approximately doubles for every 10°C decrease in junction temperature. If the heatsink in the previous case is fan cooled, estimate the lifetime improvement if the heatsink thermal impedance is halved with fan cooling.

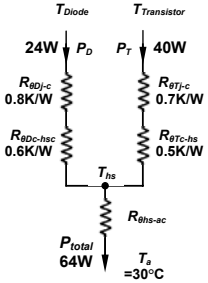
iii. If the load current is constant (25A) and the switch and diode on-state voltages are the same, determine the chopper on-time duty cycle and device instantaneous losses assuming no switching losses (only on-state losses).

Solution

i. Applying Kirchhoff's voltage law to each loop of the equivalent thermal circuit shown gives:

$$T_{Dj} - T_{hs} = 20\text{W}\times(0.8\text{K/W} + 0.6\text{K/W}) = 28°\text{C}$$

$$T_{Tj} - T_{hs} = 40\text{W}\times(0.7\text{K/W} + 0.5\text{K/W}) = 48°\text{C}$$



Since both semiconductor devices are mounted on the same heatsink, T_{hs} is the same in each case, the MOSFET virtual junction will operate 20°C hotter than the diode junction. Therefore the MOSFET junction temperature should not exceed 90°C, that is

$$90°\text{C} - T_{hs} = 40\text{W}\times(0.7\text{K/W} + 0.5\text{K/W}) = 48°\text{C}$$

giving a heat sink surface temperature of 90°C - 48°C = 42°C and a diode junction temperature of 42°C + 28°C = 70°C. The heatsink thermal resistance requirement is

$$T_{hs} - T_a = 42°\text{C} - 30°\text{C} = R_{\theta hs-a}\times(40\text{W} + 24\text{W})$$

$$R_{\theta hs-a} = 42°\text{C} - 30°\text{C} \,/\, 40\text{W} + 24\text{W} = 12°\text{C} \,/\, 64\text{W} = 0.19\text{K/W}$$

ii. Assume device losses are not affected by temperature and the heatsink thermal resistance is decrease to ½×0.19=0.095K/W, then

$$T_{hs} - T_a = T_{hs} - 30°\text{C} = 0.095\text{K/W}\times(40\text{W} + 24\text{W})$$

$$T_{hs} = 0.095\text{K/W}\times(40\text{W} + 24\text{W}) + 30°\text{C} = 36.1°\text{C}$$

The device junction temperatures are given by

$$T_{Dj} - 36.1°\text{C} = 20\text{W}\times(0.8\text{K/W} + 0.6\text{K/W}) \text{ that is } T_{Dj} = 64.1°\text{C}$$

$$T_{Tj} - 36.1°\text{C} = 40\text{W}\times(0.7\text{K/W} + 0.5\text{K/W}) \text{ that is } T_{Tj} = 84.1°\text{C}$$

The junction temperature of each device has decreased by about 6°C, so although the lifetime will have increased, lifetime improvement is not doubled. Device package thermal properties are more dominant than the heatsink in determining junction temperatures.

iii. If the on-state duty cycle is δ and the instantaneous device losses are P (and the same since on-state voltage is the same for both devices and the current is constant hence the same when each device is conducting) then

$$\text{mosfet} \quad \delta P = 40\text{W}$$

$$\text{diode} \quad (1-\delta)P = 24\text{W}$$

Summing these two equations gives an instantaneous loss of P = 64W, whence a switch on-state duty cycle of δ = ⅝, that is the switch conducts for 62½% of the cycle period. The diode on-state voltage is therefore 64W/30A= 2.13V and the MOSFET on-state resistance is 64W/30A^2 = 71mΩ.

♣

Example 5.6: ***Six thermal elements in a common package***

A three phase full-wave diode rectifier package consists of six diode die within a single module. The junction-to-case thermal resistance of each die is 0.24K/W. The module is mounted on a heatsink with a module-to-heatsink contact thermal resistance of 0.2K/W and a heatsink-to-ambient thermal resistance of 0.1K/W. The maximum ambient temperature is 30°C and high inductive load current is constant at 100A. If the diode on-state voltage is 1V, determine

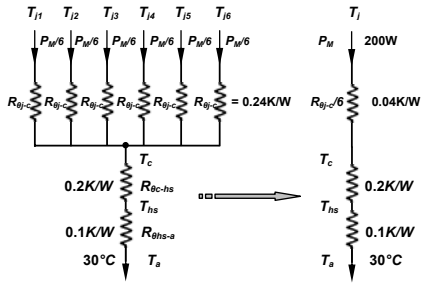
i. the diode junction temperature
ii. current to double the rectifier lifetime (decrease junction temperature by 10°C
iii. the heatsink to double the rectifier lifetime (at 100A).

Solution

i. During rectification two diodes always conduct therefore total module conduction losses are

$$P_M = 2 \times I_o \times V_{Don} = 2 \times 100\text{A} \times 1\text{V} = 200\text{W}$$

The figure shows how the six thermal paths can be reduced to the simplified equivalent thermal model on the right.



Applying Kirchhoff's voltage law

$$T_j - T_a = P_M \times \left(\tfrac{1}{6} R_{\theta j-c} + R_{\theta c-hs} + R_{\theta hs-a}\right)$$

$$T_j - 30°\text{C} = 200\text{W} \times \left(\tfrac{1}{6} \times 0.24\text{K/W} + 0.2\text{K/W} + 0.1\text{K/W}\right) \quad \Rightarrow \quad T_j = 98°\text{C}$$

ii. If the current is to reduce so as to decrease the diode junction temperature by 10°C then

$$T_j - T_a = P_M \times \left(\tfrac{1}{6} R_{\theta j-c} + R_{\theta c-hs} + R_{\theta hs-a}\right)$$

$$88°\text{C} - 30°\text{C} = P_M \times \left(\tfrac{1}{6} \times 0.24\text{K/W} + 0.2\text{K/W} + 0.1\text{K/W}\right) \quad \Rightarrow \quad P_M = 170.6\text{W}$$

Assuming the diode on-state voltage drop is independent of current, that is remains 1V then

$$P_M = 2 \times I_o \times V_{Don}$$

$$170.6\text{W} = 2 \times I_o \times 1\text{V} \quad \Rightarrow \quad I_o = 85.3\text{A}$$

iii. When the junction temperature is reduced by 10°C to 88°C by decreasing the heatsink thermal resistance, and the constant load current is maintained at 100A

$$T_j - T_a = P_M \times \left(\tfrac{1}{6} R_{\theta j-c} + R_{\theta c-hs} + R_{\theta hs-a}\right)$$

$$88°\text{C} - 30°\text{C} = 200\text{W} \times \left(0.04\text{K/W} + 0.2\text{K/W} + R_{\theta hs-a}\right) \quad \Rightarrow \quad R_{\theta hs-a} = 0.5\text{K/W}$$

♣

Reading list

Fishenden, M. and Saunders, 0. A., *An Introduction to Heat Transfer,* Oxford University Press, 1982.

International Rectifier, *HEXFET Data Book,* HDB-5, 1987.

Toshiba, *Power Transistor Semiconductor Data Book,* 1983.

Problems

5.1. A thyristor bridge switches at 1 kHz and the total energy losses per thyristor are 0.01 Joule per cycle. The thyristors have isolated studs and a thermal resistance of 2 K/W. The heat sink has a thermal resistance of 1.8 K/W. Calculate the maximum number of thyristors that can be mounted on one heat sink if the thyristor junction temperature is not to exceed 125°C in an ambient of 40°C. What is the heat sink temperature?

[3 devices, T_s= 94°C]

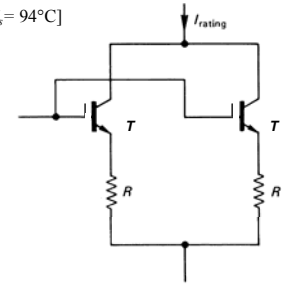


Figure 5.10

5.2. A transistorised switch consists of two IGBTs and two 1 Ohm current-sharing resistors, as shown in figure 5.10, mounted on a common heat-sink. Each transistor has a thermal resistance $R_{\theta j\text{-hs}}$ of 2 K/W, while each resistor has a thermal resistance $R_{\theta r\text{-hs}}$ of 1 K/W. The maximum switching frequency is 1 kHz and the maximum duty cycle is 99.99 per cent. The heat-sink thermal resistance $R_{\theta hs\text{-a}}$ is 1 K/W. The energy losses per transistor are 5 mJ/A per cycle. If the ambient temperature is 30°C, maximum allowable junction temperature is 150°C, and the maximum allowable resistor internal

temperature is 100°C, calculate the switch maximum current rating based on thermal considerations. What are the operating temperatures of the various components, assuming ideal current sharing?
[6.88 A, T_r = 100°C, T_{hs} = 88°C, T_j = 122.5°C]

5.3. Figure 5.11a shows the circuit diagram for a power current sink which utilises a 40V source. Both the IGBTs *T* and wire wound resistors *R* are mounted on a common heat-sink, of thermal resistance $R_{\theta hs\text{-}a}$ = 1 K/W. The transistor has a thermal resistance of 2 K/W from the junction to the heat-sink, and 10 K/W from the junction to air via the transistor casing exposed to the air. The resistor has a mounting thermal resistance from the insulated wire to the heat-sink of 1 K/W and 10 K/W from the wire to the air via its casing exposed to the air. The maximum transistor junction temperature is 423 K, the maximum resistor wire temperature is 358 K and the ambient air temperature is 303 K.

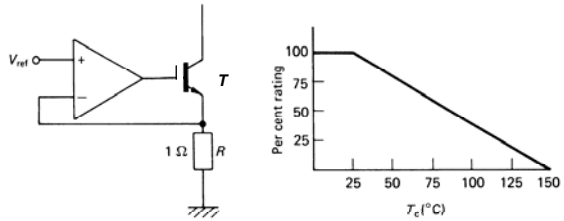


Figure 5.11

Based on thermal considerations, what is the maximum current rating of the current sink and under such conditions, what is the heat-sink temperature?
What power rating would you suggest for the 1 Ohm current measurement resistor?
Are there any difficulties in operating the transistor in the linear region in this application if it is in a 120 W dissipation package which is derated according to figure 5.11b?
[1.36 A, 69°C, > 2 W]

5.4. A power IGBT switches a 600 V, 25 A inductive load at 100 kHz with a 50 per cent on-time duty cycle. Turn-on and turn-off both occur in 100 ns and the collector on-state voltage is to be 2 V.
Calculate the total power losses, P_d, of the switch.
The switch has a thermal resistance $R_{\theta j\text{-}hs}$ = 0.05 K/W, and the water-cooled heatsink provides a thermal resistance $R_{\theta hs\text{-}w}$ = 0.05 K/W. Calculate the operating junction temperature if the water for cooling is maintained at 35°C.

The 25 A steady state load current is stepped to 200 A. Calculate the surge power dissipation P_s, at 200 A, assuming transistor switching and on-state characteristics remain unchanged.
The junction temperature for a power surge during steady-state operation is given by case (d) in table 5.2.
With the aid of figure 5.6, determine the junction temperature at the end of a 0.1s, 200 A pulse. How long is it before the junction temperature reaches $T_{j\max}$ = 125°C, with a collector current of 200 A? (Assume $R_{\theta c\text{-}hs}$ =0).
[175 W, 52.5°C, 1400 W, 112.6°C, 0.5 s]

5.5 Rework example 5.4, finding the case temperature when the switching losses equal the on-state loss.

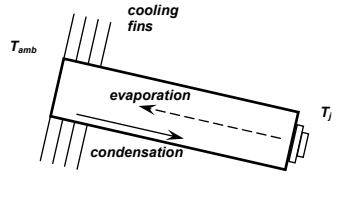


Figure 5.12. *Heat pipe.*

6

Load, Switch, and Commutation Considerations

Power switching devices are employed for controlling inductive, resistive or capacitive loads. Inductive loads include transformers, solenoids, and relays. High-current in-rush occurs with loads such as incandescent lamps, pulse-forming networks, snubbers, and motors. Incandescent lamps are essentially resistive, but the cold resistive in-rush current during turn-on is 12 to 18 times the steady-state current. This turn-on surge presents special switch-on problems. Capacitive loads, such as fluorescent lighting, also present high-current in-rush at turn-on.

The interaction of the load circuit on the switch arrangement and its commutation depends on three inter-related factors.

- The type of load, usually inductive.
- Switching mechanism classification, how the load effects switching commutation, namely hard switching, resonant, etc.
- The switch characteristics required to fulfil the supply and load *I-V* requirements, such as a bidirectional current switch, an asymmetrical sustaining voltage switch, etc.

Each of the three factors and their interdependence with the switching mechanisms are considered separately.

6.1 Load types

The two principal load types of general interest in power electronics are

- the resistive load and
- the inductive load.

Turn-on and turn-off voltage and current switching waveforms, hence losses in a switch, depend on the type of load.

6.1.1 The resistive load

A purely resistive load is rarely encountered in power switching applications. Figure 6.1 shows a simple resistive load being switched by a common emitter-connected IGBT transistor, which could equally be another appropriate semiconductor switch, for example, a MOSFET. When the gate is driven by the voltage waveform shown in figure 6.2a, the resultant collector voltage and current waveforms are as shown in figures 6.2b and 6.2c. These figures show that at turn-on, as the collector current increases, the voltage across the load increases proportionally, as the collector voltage v_{ce} decreases at the same rate. That is, at turn-on, $v_{ce}(t) = V_s - i_c(t)R_L$, while at turn-off the inverse process occurs. Figure 6.2d shows transistor instantaneous power loss during turn-on and turn-off, which in each case has a peak value of $\frac{1}{4}V_sI_m$ when the collector voltage and current reach half their respective maximum values. The energy loss W during switching is given by

$$W = \int v_{ce}(t)\, i_c(t)\, dt \quad \text{(J)} \tag{6.1}$$

where the integration is performed over the switching transition period.

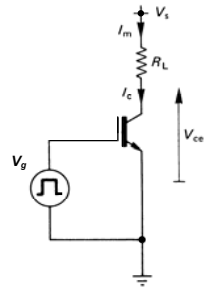


Figure 6.1. *A typical IGBT transistor switching circuit incorporating a resistive load.*

Figure 6.3 shows the safe operating area (SOA) characteristics for an IGBT, on logarithmic axes. Illustrated are the collector switch-on and switch-off trajectories, which are virtually coincident. In the off-state, point A on figure 6.2b, the transistor supports the supply rail voltage V_s while in the fully on-state, point C on figure 6.2b, the collector current I_m is V_s/R_L, neglecting the low on-state voltage of the transistor. During switching the collector voltage and current traverse the *I-V* switching trajectory between the steady-state operating conditions V_s/R_L and V_s, as shown in figure 6.3.

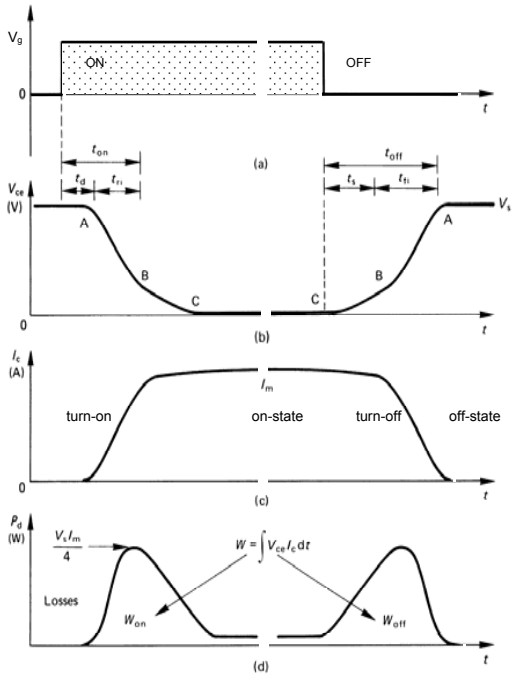


Figure 6.2. *Transistor switching waveforms for a resistive load: (a) on-off gate drive voltage; (b) collector-to-emitter voltage; (c) collector and load current waveform; and (d) instantaneous collector-emitter losses.*

It is important that this trajectory does not exceed the shown SOA bounds set by the device voltage and current limits, and that the SOA region be traversed rapidly. For slow transitions, greater than a few microseconds, power dissipation considerations become the limiting design factor, which is a thermal limitation.

In order to perform the required thermal design calculations it is necessary to be able to specify device-switching losses. To simplify analysis, the switching waveforms shown in figure 6.2 are linearised as shown in figure 6.4. As indicated on these waveforms, the collector voltage at turn-on is given by $v_{ce}(t) = V_s(1 - t/t_{on})$ while the collector current is $i_c(t) = I_m t/t_{on}$, where $I_m = V_s/R_L$. Combining $v_{ce}(t)$ and $i_c(t)$ by eliminating time *t*, gives

$$i_c = V_s(1 - v_{ce}/V_s)/R_L \tag{6.2}$$

As shown in figure 6.3, this describes the linear turn-on transition of slope $-1/R_L$ from the on-state voltage with V_s/R_L collector current, shown as C, to the off-state at A where no current flows and the collector supports the supply V_s. Note figure 6.3 uses logarithmic axes, so the transition trajectory does not appear as a straight line.

Using equation (6.1), the switch-on loss for a resistive load is given by

$$W_{on}^{r} = \int_0^{t_{on}} V_s\left(1 - \frac{t}{t_{on}}\right) I_m \frac{t}{t_{on}}\, dt$$
$$= \tfrac{1}{6} I_m V_s t_{on} \quad \text{or} \quad \tfrac{1}{6}\frac{V_s^2}{R_L} t_{on} \qquad \text{(J)} \tag{6.3}$$

where $I_m = V_s/R_L$ and t_{on} is the period of the switch-on interval, as shown in figure 6.4.

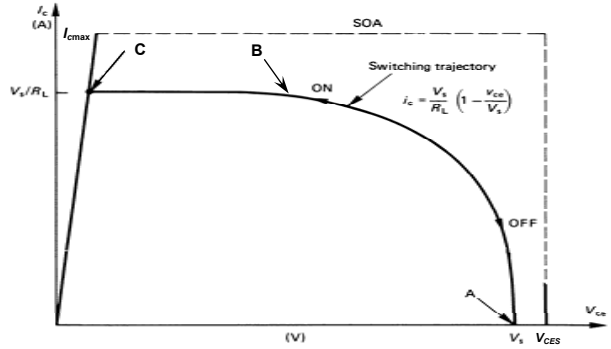


Figure 6.3. *Transistor I-V characteristics showing safe operating area and the switching trajectory with a resistive load, on logarithmic axes.*

Similarly, using the time dependant collector voltage and current equations shown on figure 6.4a, the turn-off switching loss is given by

$$W_{off} = \int_0^{t_{off}} V_s \frac{t}{t_{off}} I_m (1 - \frac{t}{t_{off}}) dt$$
$$= \tfrac{1}{6} I_m V_s t_{off} \quad \text{or} \quad \tfrac{1}{6} \frac{V_s^2}{R_L} t_{off} \quad \text{(J)} \tag{6.4}$$

where t_{off} is the turn-off period as shown in figure 6.4.

The average power loss due to switching, which is required for the thermal design outlined in chapter 5, is obtained by multiplying energy loss W by the switching frequency f_s. That is, the turn-on switching loss is given by

$$P_{on} = \tfrac{1}{6} I_m V_s t_{on} f_s \quad \text{(W)} \tag{6.5}$$

while the turn-off loss is given by

$$P_{off} = \tfrac{1}{6} I_m V_s t_{off} f_s \quad (W) \tag{6.6}$$

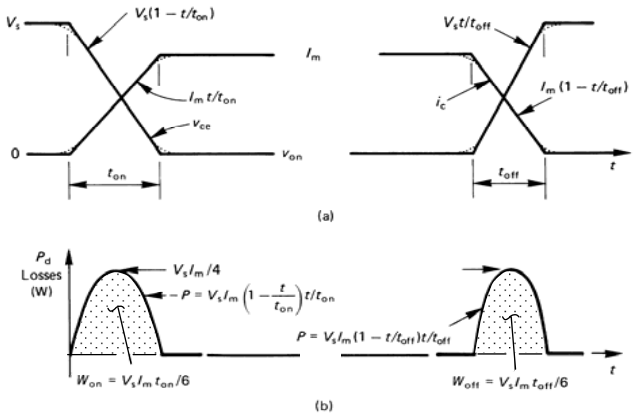


Figure 6.4. *Linear approximations of switching intervals for a purely resistive load: (a) collector voltage and current linear waveforms and (b) corresponding energy and power losses.*

Because of IGBT current tailing and voltage overshoot at turn-off, the practical switching losses will be larger than those given by the linear approximating methods outlined.

Example 6.1: ***Resistive load switching losses***
An IGBT switches a 10 ohms resistive load across a 100V dc supply. If the switch on-state duty cycle is 25%, (δ=¼), calculate the average load voltage and current. Calculate the switch losses if the switch on time is t_{on}=1μs, switch off time is t_{off}=2μs, and the on-state voltage is 2V.

Solution
When the switch is on, the current in the resistor is $I_L = V_s/R$ = 100V/10Ω = 10A.
The average load voltage is

$$V_o = \delta V_s$$
$$= 0.25 \times 100\text{V} = 25\text{V}$$

The average load current is

$$\bar{I}_o = V_o / R = 25\text{V}/10\Omega = 2.5\text{A}$$

The total switch losses P_T are made up of three components.

P_T = on-state loss + loss at switch-on + loss at switch-off

$$P_T = \delta \times v_{ce} \times I_L + \tfrac{1}{6} V_s I_L t_{on} f_s + \tfrac{1}{6} V_s I_L t_{off} f_s$$
$$= 0.25 \times 2\text{V} \times 10\text{A} + \tfrac{1}{6} \times 100\text{V} \times 10\text{A} \times 1\mu\text{s} \times 10\text{kHz} + \tfrac{1}{6} \times 100\text{V} \times 10\text{A} \times 2\mu\text{s} \times 10\text{kHz}$$
$$= 5\text{W} + \tfrac{5}{3}\text{W} + \tfrac{10}{3}\text{W}$$
$$= 10\text{W}$$

Since the off-state leakage current and gate power losses are not specified, it is assumed these are insignificant. Technically the load current should be calculated based on 98V across the load since the switch supports 2V. Also the switching loss calculations should use a voltage of 98V, rather than 100V and a load current of 9.8A rather that 10A. The percentage error is small, and becomes insignificant at higher voltages.

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Example 6.2: ***Transistor switching loss for non-linear electrical transitions***
Assume the transistor collector current at turn-off falls according to

$$i_c = \tfrac{1}{2} I_m (1 + \cos \pi t / T_0) \quad \text{for } 0 \le t \le T_0 \tag{6.7}$$

i. For a resistive load, R_L, calculate transistor loss at turn-off.
ii. Show that the switching trajectory across the SOA is as for the linear current fall case, as given by equation (6.2) and shown in figure 6.3.
iii. Calculate the peak power dissipation and the time when it occurs.

Solution

i. The collector voltage for a resistive load, on a dc supply V_s, is given by

$$v_{ce}(t) = V_s - i_c(t)R_L$$
$$= V_s - \tfrac{1}{2}I_m(1+\cos\pi t/T_0)R_L$$

and since $V_s = I_m R_L$

$$v_{ce}(t) = \tfrac{1}{2}V_s(1-\cos\pi t/T_0)$$

The turn-off energy loss is given by

$$W_{off} = \int_0^{T_0} p(t)\,dt = \int_0^{T_0} i_c(t)v_{ce}(t)\,dt$$
$$= \int_0^{T_0} \tfrac{1}{2}I_m(1+\cos\pi t/T_0)\times\tfrac{1}{2}V_s(1-\cos\pi t/T_0)\,dt$$
$$= \tfrac{1}{8}V_s I_m T_0$$

ii. Combining $v_{ce}(t)$ and $i_c(t)$ so as to eliminate the time variable, yields

$$i_c = \frac{V_s}{R_L}(1-\frac{v_{ce}}{V_s})$$

which is the same straight line expression as in equation (6.2) and shown in figure 6.3, for the linear transition case.

iii. Instantaneous power dissipation is given by

$$P = v_{ce}i_c = v_{ce}\frac{V_s}{R_L}(1-\frac{v_{ce}}{V_s})$$

Peak power $\hat{P}$ occurs when $dP/dv_{ce} = 0$, that is, when $v_{ce} = \tfrac{1}{2}V_s$, whence on substitution into the power expression P, yields

$$\hat{P} = \tfrac{1}{4}V_s^2/R_L = \tfrac{1}{4}V_s I_m \quad \text{at} \quad t = \tfrac{1}{2}T_0$$

♣

Turn-on loss can be similarly analysed to yield virtually identical expressions, as is required in problem 6.4.

6.1.2 The inductive load

The voltage spikes generated by inductive loads at turn-off may have high energy content, and the power generated may cause excessive device temperature, voltage stressing, and device failure.

At turn-off, the switch decreases the inductive load current from I_m to zero at a high *di/dt* and the resultant voltage spike is given by

$$v(t) = L\frac{di}{dt} \qquad \text{(V)}$$

where L is the load inductance. The spike energy to be absorbed by the switch is given by

$$W = \tfrac{1}{2}LI_m^2 \qquad \text{(J)}$$

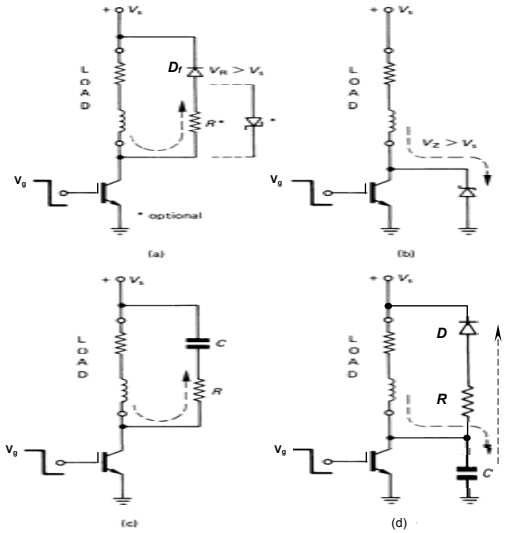


Figure 6.5. *Four methods of limiting inductive load turn-off voltage spike and of absorbing the associated energy: (a) freewheel clamping diode; (b) Zener diode clamp; (c) R-C snubber circuit; and (d) capacitor soft clamp.*

Both the voltage spike and its associated energy may be well outside the capabilities of the switching device. The peak voltage induced must be limited to a value below the breakdown rating of the device. Four commonly employed voltage limiting techniques are shown in figure 6.5.

The freewheel diode D_f in figure 6.5a is used to clamp the maximum device voltage to the supply rail voltage. The stored load energy is dissipated after turn-off as a result of the current that flows in the diode and load. The low impedance of the diode causes the current to decay slowly, since the inductor stored energy can only dissipate slowly in the freewheeling loop resistive components. A shorter current decay time can be achieved if series loop resistance R is added, as shown in figure 6.5a. Now the peak off-state voltage experienced by the switch is increased from V_s in the case of the diode, to $V_s + I_m R$ because of the initial voltage drop across the optionally added resistor. This extra voltage drop, $I_m R$, decreases exponentially to zero. The resistor in figure 6.5a can be replaced by a Zener diode, thereby clamping the switch voltage to $V_s + V_Z$. The load now freewheels at a fixed voltage V_Z thereby improving the rate of current decay, which is now constant. The inductive load current will fall linearly to zero in a time given by

$$t = LI_m / V_z \qquad \text{(s)}$$

An alternative Zener diode clamping circuit, as shown in figure 6.5b, can be employed in low power applications. The Zener breakdown voltage V_z is selected between the rail voltage V_s, and the switch breakdown voltage $(V_s < V_z < V_{BR})$. At turn-off, the Zener diode clamps the switch voltage to a safe level V_Z and absorbs the stored inductive load energy. The higher the clamping voltage level, the faster the energy is dissipated. The inductive load current decays linearly to zero in a time given by

$$t = LI_m / (V_z - V_s) \qquad \text{(s)} \qquad (6.8)$$

The two different Zener diode approaches perform the same switch clamping function in the same current decay time, if the voltage experienced by the switch is the same, but with different Zener diode losses. The desirable feature in the case of the Zener diode in parallel to the switch as in figure 6.5b, is that the protection component is directly across the element to be voltage protected. When placed in parallel with the load as in figure 6.5a, the switch is indirectly voltage protected, relying on the supply decoupling being a low inductance path. A reverse blocking diode D_f is needed.

The parallel switch approach in figure 6.5b has a number of disadvantages

- The Zener diode voltage rating must be in excess of the supply rail, V_s, while any Zener value can be used when the Zener diode is in parallel with the load.
- At higher voltages, >280V, Zener diodes will have to be series connected, thus the advantage of clamping with just one component is diminished.
- Assuming no resistance in the load, the energy dissipated with the two Zener diode approaches differs. When in parallel with the load, the load energy $½LI_m^2$ is dissipated while in the second case, load and supply energy are dissipated in the clamping Zener diode. The extra supply energy, in addition to $½LI_m^2$, dissipated in the Zener diode, is $½LI_m^2 V_s/(V_z - V_s)$. This is derived by recognising that, assuming a purely inductive load, the supply V_s delivers a current I_m which linearly falls to zero over the period given by equation (6.8).

The *R-C* snubbing circuit shown in figure 6.5c is commonly used in power conversion circuits to limit spikes caused by transformer leakage inductance, diode recovery, and interconnection wire inductance. The stored load energy is resonated to the snubber capacitor at switch turn-off. The reset resistor R (non-inductive) must overdamp the *L-C-R* oscillation by absorbing the transferred energy. The resistor also limits the snubber capacitor charging current to V_s/R at switch turn-on. For a purely inductive load, the snubber resistor power losses are given by the sum of the turn-off and turn-on losses, that is

$$P = \left(½LI_m^2 + ½CV_s^2\right) f_s \qquad \text{(W)}$$

Figure 6.5d shows a capacitive voltage clamp used to soft clamp the switch voltage overshoot caused by the inductive energy stored in the load. The capacitor retains a charge of at least V_s. At switch turn-off, when the switch voltage reaches the capacitor (supply V_s) voltage level, the inductive stored load energy is transferred to the capacitor and concurrently, the capacitor discharges the energy in excess of V_s into the supply. When the capacitor is over charging, energy is taken from both the load inductance and the supply. When the capacitor discharges through the resistor back into the supply, the earlier energy taken from the supply is returned. The net effect is that only the energy $½LI_m^2$ is dissipated in the resistor. A low inductance reset resistor is not necessary. This capacitive soft voltage clamp is analysed further in chapter 8.2.

Example 6.3: ***Zener diode, switch voltage clamping***

A reed relay coil of 1 mH inductance is switched at 20 kHz with a 20 per cent on-time duty cycle, across a 100 V dc rail. The energy stored in the coil at turn-off is dissipated in a 25 V Zener diode connected as shown in figure 6.5a.

i. Sketch the coil current and voltage, and the switch voltage waveforms.
ii. What is the average coil voltage?
iii. What Zener diode voltage is required for the circuit in figure 6.5b so as to produce the same coil current waveform as in figure 6.5a using a 25 V Zener diode?
iv. For each circuit calculate the power requirement of the Zener diode and the average power delivered from the 100 V supply.
v. Calculate the minimum resistance that replaces the Zener diode in figure 6.5a if the coil is to be switched on with almost zero current. Draw the coil current and switch voltage waveform, showing the switch peak voltage at turn-off.
vi. Discuss the relative features of each voltage clamping approach.

Solution

The three voltage clamping circuits being considered are shown in figure 6.6a.

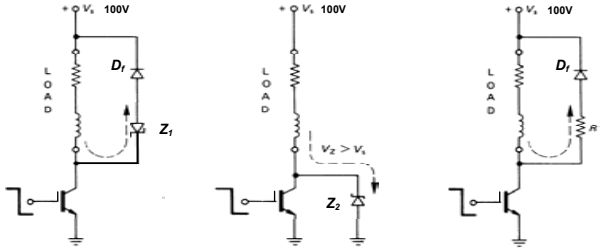


Figure 6.6a. *Three inductive load clamping circuits.*

i. With a 20kHz switching frequency, the coil current rises and falls every 50µs, with an on-state duty cycle representing 10µs for the current to increase in the coil and 40µs for the current reset decay to reach zero.
From $V=Ldi/dt$, in steady-state, with zero coil resistance and initial current, the peak coil current is $I = V_s\ t/L$ = 100Vx10µs/1mH = 1A. Thus the coil current rises linearly from zero to 1A in 10 µs. During reset, the coil current waveform depends on the reset circuit. For Zener diode (constant voltage) reset, the current falls linearly, with a resistor it decays with an L/R exponential time constant, as shown in figure 6.6b for each case.
The various circuit voltage and current waveforms are shown in figure 6.6b, where data derived from the rest of this example has been incorporated.

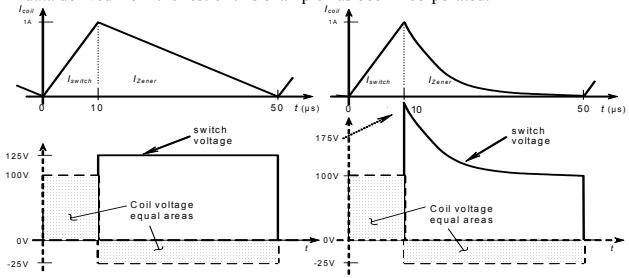


Figure 6.6b. *Coil voltage and current waveforms.*

ii. From $V=Ldi/dt$, for a steady-state continuous waveform, $\int V_L(t)dt = 0$, thus $1/T\int v(t)dt = V_{ave} = 0$, as shown on the coil voltage waveform.

iii. The parallel Zener diode requirement is V_{Z2} = 125V = V_s+V_{Z1} = 100V+25V.

iv. **Zener diode V_{Z1}** in the reset circuit:
The energy $½LI^2$ is transferred from the coil to the Zener diode when the switch is turned off. The power dissipated in the Zener diode at 20kHz is therefore $½LI^2 f_s = ½\times 1\text{mH}\times 1\text{A}^2\times 20\text{kHz} = 10$ W. The total power drawn from the supply is the power stored by the coil during the 10µs on-time, 10W.
Zener diode V_{Z2} in the reset circuit:
When the coil releases its stored energy (10W) into the Zener, current is also drawn from the supply. The total average power delivered by the supply over the 50µs period is given by $V_s I_{ave} = ½\times 100\text{V}\times 1\text{A} = 50$W. This comprises $½LI^2$ (10W) from the supply into the coil when the switch is on for 10 µs, and the remainder (40W) into the Zener diode (plus the coil energy, 10W), when the switch is off for 40 µs.

v. When a resistor is used in the reset circuit, the current decays exponentially from 1A to 0A. The resistance determines the peak switch voltage. The resistance does not affect the amount of energy dissipated, only the period over which the coil energy is released, dissipated as heat. Assume the coil current to be near zero after three L/R time constants, that is $3L/R$=40µs. For L = 1mH, this gives R = 75Ω, with a power dissipation rating of 10W from part iv. Use an 82Ω (preferred value), 15W metal oxide resistor for low inductance.

vi. A Zener diode approach gives a fixed over-voltage on the switch, independent of current or stored energy. When clamping is in parallel with the switch, only one clamping element is needed, but its power requirement is significantly higher than when the clamp is in parallel to the load. Any resistive element must have low inductance. This is restrictive given the power levels involved, and may result in only wire wound elements being viable.

♣

By far the most common technique used to limit inductive switch-off voltage spikes in power circuits involves the use of a freewheel diode without R_{opt}, as shown in figure 6.5a and 6.7a. Typical switching waveforms for an inductive load clamped by a freewheel diode are shown in figure 6.7.

- **At turn-off**, the switching device conducts the full load current as the collector voltage rises to the supply rail. When the collector voltage reaches the supply rail level the freewheel diode becomes forward-biased and begins to conduct. The switch current then falls to zero. The freewheel diode conducts the load current.
- **At switch turn-on**, assuming the diode is still freewheeling load current, the switch current increases, displacing freewheeling diode current, while the load is clamped to the rail voltage by the conducting freewheel diode. When the switch conducts the full load current and the freewheel diode has recovered, the switch voltage falls to the low on-state level.

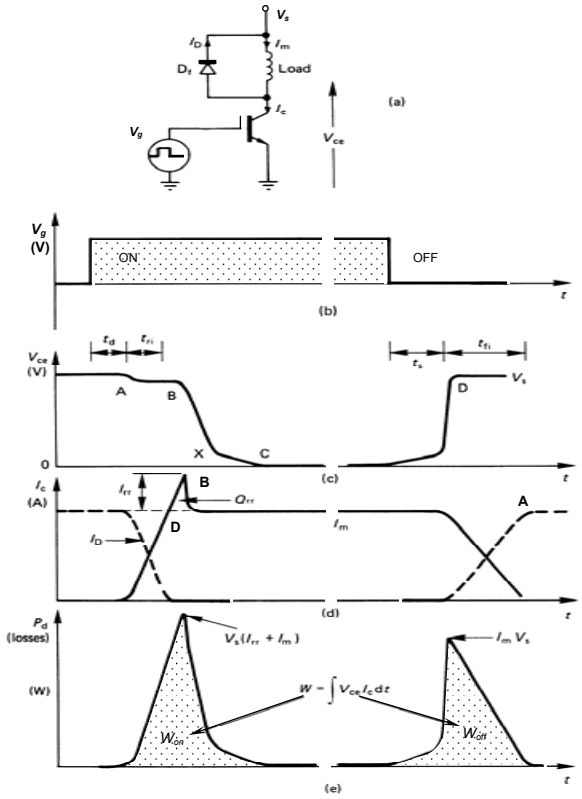


Figure 6.7. *Inductive load switching waveforms: (a) the circuit including the freewheel diode D_f;(b) on-off gate drive voltage; (c) collector-to-emitter voltage; (d) collector and freewheel diode current; and (e) switch instantaneous power losses.*

It will be seen in figure 6.7 that during both turn-on and turn-off the switch must support instantaneously a maximum voltage, V_s, and full load current, I_m, condition. These severe electrical conditions are shown on the SOA characteristics in figure 6.8. In switching on from the operating point A to C, a maximum voltage and current condition occurs at point D. Because of freewheel diode current reverse recovery effects at turn-on, an SOA trajectory point B is reached. At turn-off, due to stray inductance, voltage over shoot occurs and the point E is reached. By comparison with figure 6.2, it is seen that power losses during the switching intervals are higher for an inductive load than a resistive load.

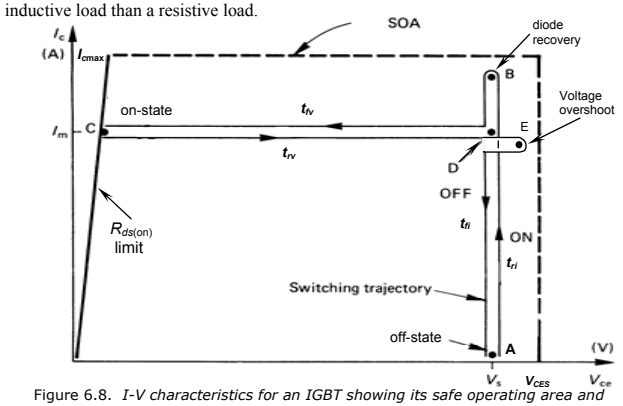


Figure 6.8. *I-V characteristics for an IGBT showing its safe operating area and switching trajectory for an inductive load.*

Switching losses can be calculated by using linear approximations to the switching transitions. It can be assumed that a silicon carbide Schottky freewheel diode is employed so as to allow reverse recovery effects to be neglected. Figure 6.9 shows the linearised switching waveforms for an inductive load, where maximum voltage V_s and current I_m occur simultaneously during both turn-on and turn-off. The equations for the collector voltage and current at turn-on and turn-off are shown in figure 6.9.

The turn-on switching interval loss is given by the time integral over the current rise period plus the voltage fall period,

$$W_{on} = \int_0^{t_{ri}} V_s I_m \frac{t}{t_{ri}}\, dt + \int_0^{t_{fv}} V_s \left(1 - \frac{t}{t_{fv}}\right) I_m\, dt \qquad (6.9)$$

$$= \tfrac{1}{2} V_s I_m t_{on} \quad \text{(J)}$$

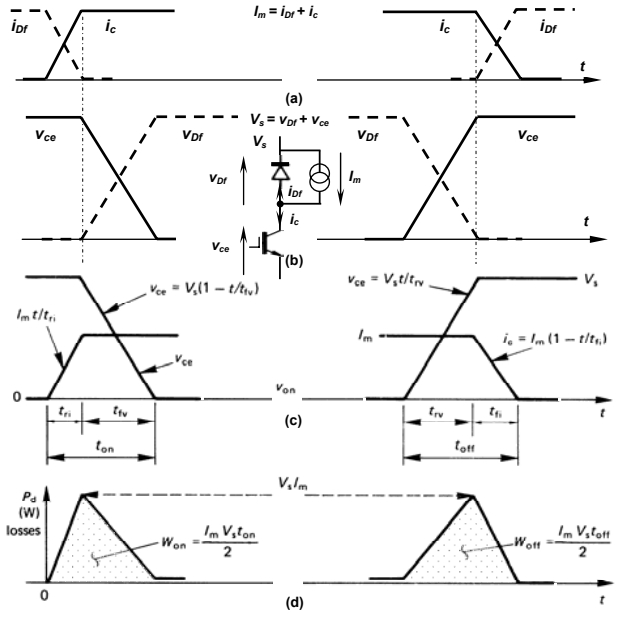


Figure 6.9. *Linear approximations of transistor switching intervals for an inductive load: (a) Kirchhoff's current law $I_m = i_{Df} + i_c$; (b) Kirchhoff's voltage law $V_s = v_{Df} + v_{ce}$; (c) collector voltage and current waveforms with switching parameters defined; and (d) corresponding switching losses.*

where $t_{on} = t_{ri} + t_{fv}$, as shown in figure 6.9. The current rise time at turn-on is termed t_{ri}, while the switch voltage fall time at turn-on is termed t_{fv}.

Similarly, the turn-off loss is given by

$$W_{off} = \int_0^{t_{rv}} V_s \frac{t}{t_{ri}} I_m \, dt + \int_0^{t_{fi}} V_s I_m \left(1 - \frac{t}{t_{fv}}\right) dt \qquad (6.10)$$
$$= \tfrac{1}{2} V_s I_m t_{off} \quad \text{(J)}$$

where $t_{off} = t_{rv} + t_{fi}$, as shown in figure 6.9. The switch voltage rise time at turn-off is termed t_{rv}, while its current fall time is termed t_{fi}.

Comparison of switching losses for a resistive load, equations (6.3) and (6.4), and an inductive load, equations (6.9) and (6.10), shows that inductive switching losses are three times those for the resistive load case. The peak power experienced by the switch during switching of an inductive load, $V_s I_m$, is four times greater than that experienced with a resistive load, $\frac{1}{4} V_s I_m$. As for the resistive load switching circuit, actual switch losses with an inductive load are higher than those predicted by equations (6.9) and (6.10). The effects of current tailing, voltage over-shoot, and freewheel diode reverse recovery can produce losses of the same order as those predicted for theoretical switching by equations (6.3), (6.4), (6.9), and (6.10).

Example 6.4: ***Inductive load switching losses***

A MOSFET switches a 10A 100V highly inductive load.
Calculate the worse case switch losses if the switch on time is $t_{on} = 1\mu s$, switch off time is $t_{off} = 2\mu s$, and the MOSFET channel on-state resistance is 0.2Ω.
Calculate the maximum instantaneous power dissipation in the switch, and when it occurs.

Solution

Maximum switch losses occur when the duty cycle approaches one ($\delta \rightarrow 1$) such the both turn-on and turn-off still occur.
The total switch losses P_T are made up of three components

P_T = on-state loss + loss at switch-on + loss at switch-off

$$P_T = \delta \times I_L^2 \times R_{ds(on)} + \tfrac{1}{2} V_s I_L t_{on} f_s + \tfrac{1}{2} V_s I_L t_{off} f_s$$
$$= 1 \times 10^2 \times 0.2\Omega + \tfrac{1}{2} \times 100V \times 10A \times 1\mu s \times 10kHz + \tfrac{1}{2} \times 100V \times 10A \times 2\mu s \times 10kHz$$
$$= 20W + 5W + 10W$$
$$= 25W$$

Since the off-state leakage current and gate power losses are not specified, it is assumed these are insignificant. The switching loss calculations should use a voltage of 98V, rather than 100V, since (10A×0.2Ω) 2V is dropped across the channel resistance of the MOSFET. The percentage error is small, and becomes insignificant at higher voltages.
Maximum switch loss occurs half-way through the switching period, when the current is 10A and the drain voltage is 50V. That is, the maximum instantaneous loss is 10A×50V=500W, ($\frac{1}{4} \times I_L \times V_s$).

♣

6.1.3 Diode reverse recovery with an inductive load

When a diode conducts the pn region accumulates charge. When the diode turns off and the current falls to zero, the junction retains charge that must recovery before diode reverse voltage can be supported. Negative diode current flows. This phenomenon was considered in chapter 4.2.2 and is shown in figure 6.10. The maximum collector current at turn-on is increased above the load current level I_m by the reverse recovery current I_{rr}. The diode begins to support reverse voltage once the peak reverse recovery current is reached. As a consequence the turn-on losses are increased as shown in figure 6.10c.

The circuit current at peak recovery has a discontinuous derivative, and as a consequence, high circuit voltages are induced across circuit stray inductance due to $v = Ldi/dt$. High-frequency voltage ringing occurs as the stored energy in the stray inductance is dissipated and reverse voltages far in excess of V_s are experienced by the recovering diode.

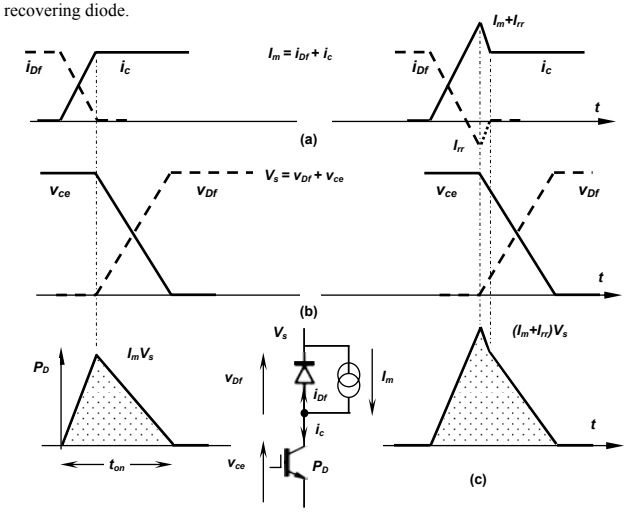


Figure 6.10. *Linear approximations of transistor switching turn-on interval for an inductive load showing freewheel diode reverse recovery effects on the right: (a) Kirchhoff's current law $I_m = i_{Df} + i_c$; (b) Kirchhoff's voltage law $V_s = v_{Df} + v_{ce}$; and (d) corresponding switching losses.*

6.2 Switch characteristics

Having considered the switching of inductive and resistive loads, the following are the electrical and thermal characteristics desirable of commutable switching devices:

off-state:

- Low, temperature independent leakage current in the off-state, to minimise off-state power loss.
- High forward and reverse voltage blocking ratings to reduce the need for series connection, which would otherwise complication control and protection circuitry requirements. Series connection increase the on-state voltage, hence on-state loss. When a diode is used in antiparallel across the switch to allow reverse principal current flow, the switch does not require a significant reverse voltage blocking rating.
- High static off-state avalanche capability to absorb transient overvoltage stresses
- High static and re-applied *dv/dt* capability to withstand high applied off-state voltages without avalanche or false turn-on

on-state:

- Low on-state conducting voltage or low on-state resistance, in order to minimise on-state conduction power loss: with a slight positive temperature co-efficient to allow reliable parallel device connection.
- High on-state current density so as to avoid need for and problems associated with parallel device current sharing and differential thermal coefficients.

switching:

- Low control power to switch between states.
- Short, temperature independent, turn-on and turn-off times to result in low switching losses which will allow high frequency switching.
- High initial *di/dt* at turn-on to allow rapid low loss build-up of turn-on principal current.
- High surge current capability to withstand transient over current fault condition, resulting in better fault tolerance and nuisance tripping ride through.
- Large switching safe operating area, being able to simultaneously support rated voltage and rated current, without the need for snubber circuits across the switch.

thermal:

- Low thermal resistance and impedance for efficient heat removal.

6.3 Switching classification

There are four principal *I-V* switching conditions during the commutation of a switch current, viz.

- Hard switching
- Soft switching
- Resonant switching and
- Naturally-commutated switching.

These four possibilities are classified in terms of the *switching time* t_s and the *commutation time* t_q, where $t_q \le t_s$. Figure 6.11 shows the four cases and specifies the switching and commutation times for each.

- *Switching time* t_s is the time for a switch to change from fully on (v=0, i=I_L) to fully off (v=V_s, i=0), such that no further change occurs in the switch voltage or current due to the change of state.
- *Commutation time* t_q is associated with the external circuitry and is defined as the time the switch takes to reach zero current at turn-off or to reach zero volts at turn-on. Alternatively, commutation time is the period of power loss at turn-on or turn-off, due to the switch changing states.

Generally, the switch loss magnitude for a given set of electrical and thermal operating conditions, decrease when progressing from severe hard switching through to virtually lossless naturally-commutated switching.

6.3.1 Hard switching

The turn-on and turn-off switching waveforms in figure 6.11a show that hard switching is characterised by $t_q = t_s$. The resistive and inductive switching considered in sections 6.1.1 and 6.1.2 are examples of hard switching. In figure 6.4 for a resistive load, the switching periods t_{on} and t_{off} correspond to the period of switch losses during each state transition. In figure 6.9 for the inductive load, the t_q periods correspond to the power loss periods at switching (t_{rv}+t_{fi} and t_{fv}+t_{ri}).

6.3.2 Soft switching

Figure 6.11b shows typical soft-switching waveforms for turn-on and turn-off. The switching losses are complete before the switch has reached its final steady-state condition. That is, t_s>t_q such that the periods t_s and t_q both start at the same time.

At turn-on, the switch voltage reaches zero before the switch current reaches the steady-state full-load value I_L. Once the switch voltage reaches zero, the rising current no longer results in a power loss. This *I-V* characteristic at turn-on is a form of *zero current switching*, ZCS.

The inverse occurs at turn-off. The switch current reaches zero before the switch voltage has settled at the supply voltage level V_s. This is a form of *zero voltage switching*, ZVS.

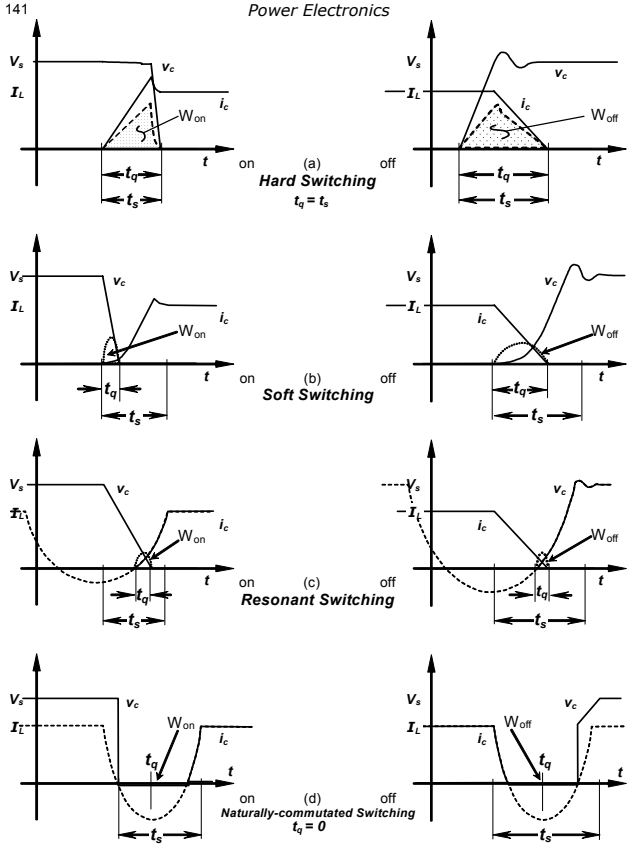


Figure 6.11. *Switch voltage (v_c), current (i_c), and power loss (W_{on} and W_{off}) of four switching classifications: (a) hard switching; (b) soft switching; (c) resonant switching; and (d) naturally-commutated switching.*

Soft-switching results when auxiliary circuits, called snubber circuits, are used, as will be considered in chapters eight and nine.

6.3.3 Resonant switching

Resonant-switching waveforms at turn-on and turn-off are shown in figure 6.11c, with switching periods t_s shown. Resonant switching occurs if the switching period is associated with either the switch voltage or current being zero, due to external load circuit conditions. That is $t_s > t_q$.

Switching of the voltage when the switch current is zero, usually at turn-on, is called *zero current resonant switching*, ZCRS, while commutating the current while the switch voltage is zero, usually at turn-off, is called *zero voltage resonant switching,* ZVRS. Because the exact instant of zero may vary, being load circuit dependant, some control restriction is inevitable. Zero voltage or current switching can be readily attained with ac mains converter circuits since switching can be synchronised with supply zero voltage crossing, or zero current when the load current reverses due to the supply voltage reversal.

6.3.4 Naturally-commutated switching

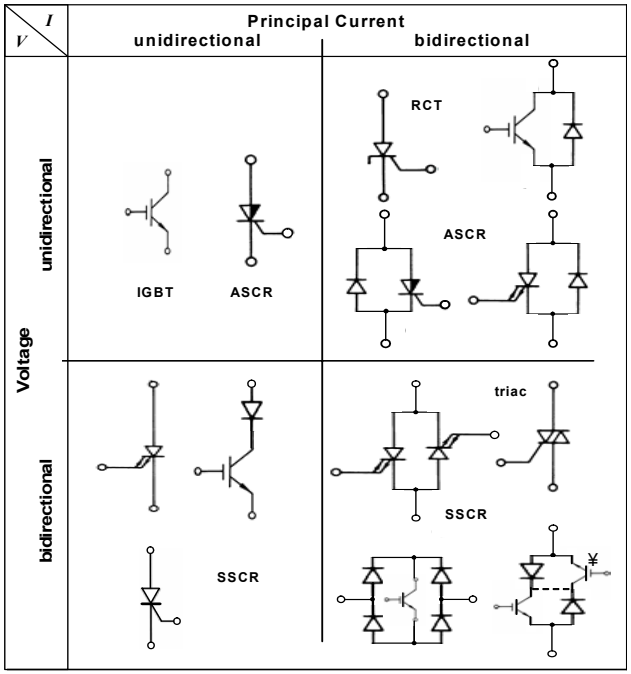
Figure 6.11d shows switching when the voltage and current are both zero, called *naturally-commutated switching*. This was a commonly used technique for force turn-off of thyristors before the advent of the GTO thyristor. Current from an auxiliary commutation circuit displaces the device principal current and reverse biases the device, at turn-off. The method was not used at turn-on. Commutated turn-on and turn-off occurs in inverter circuits where the switch has an anti-parallel connected diode. When the diode conducts and the switch is on but not conducting, if the load power factor causes the current to reverse, then the main switch automatically starts conducting with the switch voltage at zero because the diode was previously conducting, clamping the switch voltage slightly negative.

Naturally-commutated switching occurs for ac mains zero crossing switching, with a purely resistive load such that the load V and I are in phase. Switching losses are virtually zero.

6.4 Switch configurations

Most semiconductor switches are unipolar, that is, allow current and/or voltage to be supported in one direction. The MOSFET allows uncontrolled reverse current flow, hence can not support reverse voltage because of its parasitic body diode. Some structures, like the RCT considered in chapter 3.3.3, integrate an anti-parallel diode with a thyristor. Generally, such integrated approaches sacrifice some electrical characteristics. Many applications require a bi-directional current and/or bi-directional supporting voltage switches, so the basic switches can be configured as shown in figure 6.12, to give the necessary *I-V* characteristics. The net effect of the bi-directional

voltage arrangements is good dynamic electrical characteristics but poor static characteristics. Specifically, the switching performance is as for the principal switch but the on-state loss is that of two series connected devices. In the case of the bidirectional blocking thyristor, the on-state voltage is increased slightly because an n-buffer can not used in its fabrication. The bi-direction conducting thyristor discussed in chapter 3.3.4 attempts to minimise the sacrificed on-state voltage limitation.



¥ can be arranged so that emitters are at the same potential

Figure 6.12. *Switch configurations for uni-directional and bi-directional I-V characteristics.*

Reading list

Peter, J. M., *The Power Transistor in its Environment,*
Thomson-CSF, Sescosem, 1978.

Problems

6.1. During turn-on and turn-off of a power transistor the current-voltage relationships are as shown in figure 6.13. Calculate the energy loss during both turn-on and turn-off periods and the mean power loss if the transistor is being switched at a frequency of 10 kHz. What is the maximum instantaneous power dissipated?
[1.66 mJ, 16.6 mJ, 183 W, 5kW]

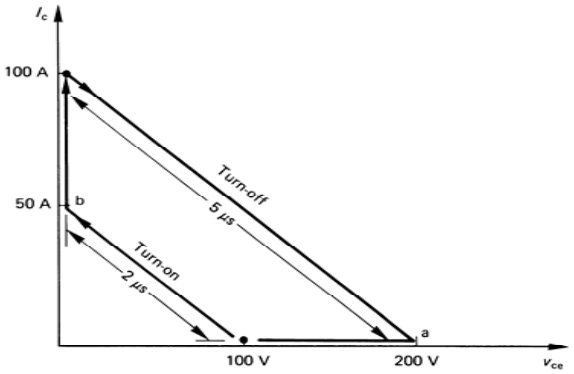


Figure 6.13.

6.2. The equivalent circuit in figure 2.4a involving parameters E_o and R_o can be extended to model a thyristor by replacing the ideal diode by an ideal thyristor. Derive general expressions for the thyristor mean power loss P_d and rms current i_o with a constant load current I_o and switch on-time duty cycle δ.
If E_o = 1 V and R_o = 0.01 Ohms, for I_o = 50 A and a 25 per cent on-time duty cycle, calculate the thyristor:

i. On-state voltage, V_F
ii. Mean power, P_d
iii. rms current, i_o.

[See example 2.1: 1.5 V, 18.75 W, 25 A]

6.3. If the collector voltage at turn-on falls according to
$v_c = ½V_s(1 + \cos \pi t / T_o)$ for $0 \le t \le T_o$

i. For a resistive load, R_L, calculate transistor loss at turn-off.
ii. Show that the switching trajectory across the SOA is as for the linear current fall case.
iii. Calculate the peak power dissipation and when it occurs.

6.4. A transistor is used to switch an inductive load with a current of I_m.
At transistor turn-off, the collector voltage rises to the supply rail V_s according to
$v_{ce} = ½V_s\ (1 - \cos \pi t/T_{ov})$ for $t \le T_{ov}$,
then the collector current falls according to
$i_c = ½I_m(1 + \cos \pi t/T_{oi})$ for $t \le T_{oi}$.
Using the same integration form as in equation (6.10), show that the turn-off loss is
$P = ½V_sI_m\ T_o$ where $T_o = T_{ov} + T_{oi}$.

7

Driving Transistors and Thyristors

The thyristor, being a multiple bipolar junction device, is essentially a current-controlled device. As illustrated in figure 7.la, a current must be supplied between the gate and cathode terminals to produce anode current flow, provided the anode is forward biased. The magnitude of gate drive current determines the delay time and the anode current rise time. In gate commutated thyristors, a negative gate current must be produced, the magnitude determining the turn-off delay time and anode current fall time.

The power MOSFET and IGBT are voltage controlled devices and are fundamentally different to bipolar devices. With the n-channel enhancement-mode power MOSFET and IGBT, a positive voltage must be applied between the gate and source terminals to produce a drain current, if the drain is positively biased with respect to the source, as shown in figure 7.lb. Generally the MOSFET and IGBT are easier to drive than the bipolar thyristor, and only a few basic considerations are required for MOSFET and IGBT gate circuit implementation.

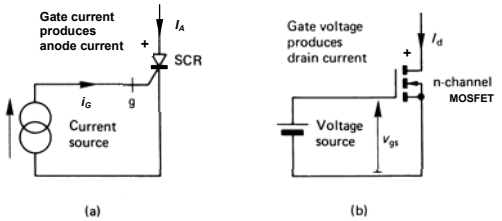


Figure 7.1. *Transistor and thyristor drive requirements: (a) current drive for the bipolar junction thyristor and (b) voltage drive for the MOSFET and IGBT.*

7.1 Application of the power MOSFET and IGBT

The MOSFET gate is isolated electrically from the source by a layer of silicon dioxide. Theoretically no current flows into the gate when a dc voltage is applied to it. In practice, gate current is required to charge device capacitances and a small leakage current of the order of nano-amps does flow in order to maintain the gate voltage.

When no voltage is applied between the gate and source terminals, the drain-to-source impedance is very high and only a small leakage current of less than a milli-amp flows in the drain, until the applied voltage exceeds the drain-to-source avalanche voltage, V_{DSS}.

When a positive gate voltage is applied, an electric field is produced which modulates the drain-to-source resistance. When a gate voltage exceeds the threshold voltage level the channel resistance reduces to a low resistance and drain current flows. The maximum drain current depends on the gate voltage magnitude, assuming that the impedance of the external drain circuit is not current-limiting.

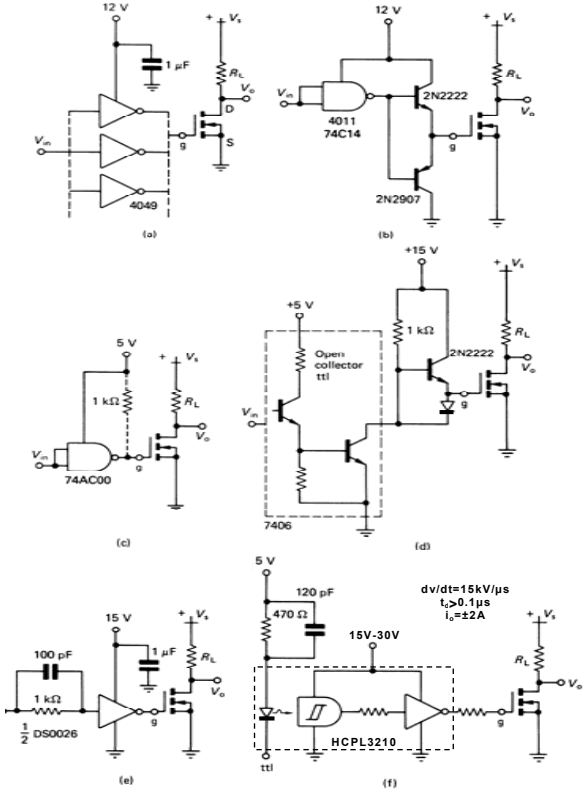
Turnoff - reducing the drain current to the leakage level - is achieved by reducing the gate voltage to below the gate threshold voltage level. The drain switching speeds are essentially determined by that speed at which the gate voltage can reach a level above the threshold voltage (for turn-on) or below the threshold voltage (for turn-off). Although the gate-to-source capacitance is an important parameter, the gate-to-drain capacitance is more significant because of the Miller effect, as considered in section 4.4.2. During switching the dynamic gate-to-drain capacitance can be effectively much larger than the gate-to-source capacitance. The Miller capacitance typically requires more charge for switching than the gate-to-source capacitance.

7.1.1 Gate drive circuits

The n-channel enhancement-mode power MOSFET (or IGBT) with a low threshold voltage interfaces easily with logic level integrated circuits. This allows low-power digital logic circuits to control directly high-power levels. Figure 7.2 shows a series of ttl and cmos circuits driving power MOSFETs, each circuit offering different levels of switching speed and performance.

When driving a MOSFET directly from a cmos gate output, as shown in figure 7.2a, only modest rise and fall times can be expected because of the limited source and sink current available from a cmos gate. Figure 7.3a illustrates the output configuration of a typical cmos output stage, which consists of a series-connected p and n-channel MOSFET with the gates connected together. The cmos totem pole output stage is driven by a common signal, hence the name complementary mos - cmos - and when the input is high the n-channel device is on and the p-channel off, while when the input is low, the p-channel turns on and the n-channel turns off. However, cmos has a limited current output capability as shown in the source-to-sink output characteristics in figure 7.3b and c. The cmos gate output has to drive as a load the power MOSFET capacitive

gate. In this configuration, the turn-on current is supplied from the p-channel fet, which has the poorer characteristics of the cmos pair. The turn-off current is sunk by the n-channel fet. Table 7.1 shows cmos typical current source and sink capabilities, switching speeds, and output impedance. It will be seen that the best performance, by far, is achieved from the 4049 and 4050 buffers.



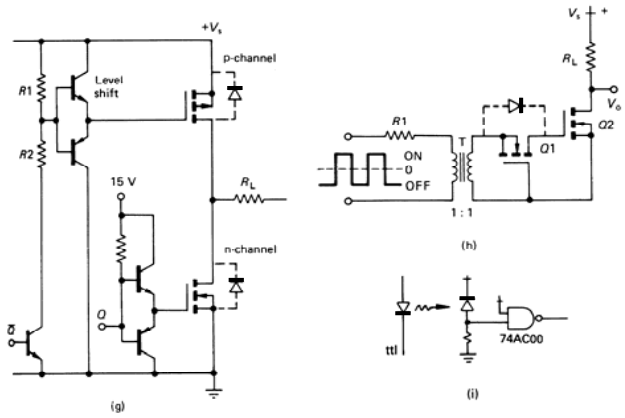


Figure 7.2. *Gate drive circuits for the MOSFET and IGBT: (a) driven from cmos; (b) driven from cmos and an emitter follower; (c) driven from ttl with pull-up resistor which increases sourcing capability; (d) driven from open collector ttl with an external current source; (e) driven from a high-current cmos clock driver; (f) opto-isolated driver circuit; (g) drive circuits for a totem pole connected p and n-channel MOSFET leg; (h) driven from a pulse transformer; and (i) fibre optic translation stage.*

If shorter delays and faster drain rise and fall times are required there are several ways to obtain them. The simplest is to parallel a number of identical cmos inputs and outputs as shown dotted in figure 7.2a. The additional current capability, with the six parallel connected gates of the 4049, will significantly improve MOSFET switching performance.

In figure 7.2b the gate drive current is the output current of the cmos gate multiplied by the gain β of the bipolar transistors. No bipolar saturation times are incurred since the transistors are operating as emitter followers, which cannot saturate. The operating frequency is no longer restricted by the cmos output current limitations.

MOSFETs can also be driven directly from ttl gates. Table 7.2 shows ttl typical current source and sink capabilities and switching speeds. Low supply voltage, typically 5V, and high internal sourcing impedance characteristics, restrict MOSFET switch-on speed and gate voltage level. The ttl sink capability is significantly higher than source capability, hence a pull-up resistor as shown in figure 7.2c enables the sinking

capability to be exploited at turn-on, as well as at turn off. A limitation of using ttl for driving MOSFETs is that the gate voltage is restricted to less than 5V, hence if the drain current is not to be restricted, low gate threshold voltage trench gate MOSFETs and IGBTs are used. An open collector ttl drive technique as shown in figure 7.2d overcomes the gate voltage limitation as well as improving the current source limit.

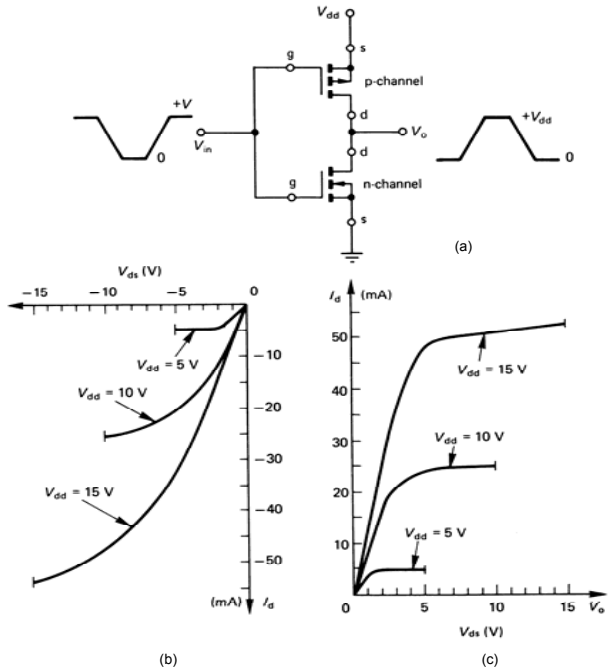


Figure 7.3. *CMOS inverter output: (a) output cmos totem pole; (b) p-channel drain sourcing; and (b) n-channel drain sinking, both at 25°C.*

Table 7.1 Driving mosfets from cmos (buffered)

	Logic conditions		Standard buffered outputs at logic supply voltage (V_{dd}) of			4049/4050 drivers at logic supply voltage (V_{dd}) of			
			5 V	10 V	15 V	5 V	10 V	15 V	
Logic zero									
Approximate sink current I_{OL} (mA) for $V_{OL} \leqslant 1.5$ V		1.5	3.5	4.0	20	40	40		
Logic one									
Minimum source current I_{OH} (mA)			−0.51	−1.3	−3.4	−1.25	−1.25	−3.75	
for V_{OH}			≥4.6 V	≥9.5 V	≥13.5 V	≥2.5 V	≥9.5 V	≥13.5 V	
Typical switching times (ns)									
of logic drive signals:									
Rise			100	50	40	100	50	40	
Fall			100	50	40	40	20	15	
		Typ.	1.7k	500	430				
$R_{ds(on)}$ (ohms)	Source	Max.	12.5k	2.5k	–				
(calculated)		Typ.	500	420	190				
	Sink	Max.	2k	1k	–				

Table 7.2 Driving mosfets from TTL

Logic conditions	Logic type									
	74	*74AC*	*74L*	*74LS*	*74S*	*74ALS*	*74HC*	*DS0026*	*Open collector 74, 30 V*
Logic zero									
Min. sink current I_{OL} for V_{OL} = 0.4 V (mA)	16	24	3.6	8	20	18	4	1.5A	40
Logic one									
Max. source current I_{OH} for V_{OH} = 2.4 V (mA)	−0.4	−24	−0.2	−0.4	−1.0	−0.4	−4	−1.5A	22
Typical gate propagation delay (ns)	10	7	50	12	4	4	10	15	12
V_{IL} max. (V)	0.8	1.35	0.7	0.8	0.8	0.8	0.9	—	0.8
V_{IH} min. (V)	2.0	3.15	2.0	2.0	2.0	2.0	3.15	—	2.0

Very fast switching speeds are attained with the capacitive driver shown in figure 7.2e. Such drivers can both source and sink typically 1.5 A in tens of nanoseconds. An isolated gate-to-source drive version is shown in figure 7.2f, where a floating 15 V rail is used and the gate control signal is optically transmitted with high *dv/dt* capability. The driver incorporates high current output, with modest propagation delays.

Drive circuits for p-channel MOSFETs may be complicated by the reference signal voltage level, as shown in the series n and p-channel totem pole in figure 7.2g. This figure illustrates how the p-channel drive may be derived by means of a level shifter. The emitter follower, pnp transistor used for turn-on must have a breakdown voltage rating in excess of the totem pole rail voltage. Above 300 V the pnp transistor can be replaced by a diode as shown in figure 7.2d, or a low current high voltage MOSFET. Restricted charging of the translation MOSFET output capacitance can lead to increased delay times. The resistor divider, *R1-R2,* ensures that the p-channel gate voltage limit is not exceeded. In order to increase gate drive capability *R2* can be decreased provided a 15 V Zener is used across the p-channel MOSFET gate to source. The low-voltage npn transistor in the p-channel driver stage is used for fast turn-off, shorting the p-channel source to its gate.

A simple method of driving an n-channel MOSFET, with its source not referenced to ground, is shown in figure 7.2h. Electrical (galvanic) isolation is achieved by means of a pulse transformer. The internal parasitic diode in Q1 provides the path for the n-channel MOSFET gate to charge. When the pulse transformer saturates, Q1 blocks any discharge of the gate until turn-off, when a negative transformer pulse turns on Q1, thereby discharging the n-channel gate charge.

An alternative translation method using a fibre optic stage is shown in figure 7.2i. The temperature-independent, high threshold characteristics of 74AC technology is used for a simple detector comparator. A Schmitt input (hysteresis) gate improves noise immunity. Translation from ttl levels can be achieved with Zener diode bias circuits.

From the circuits in figure 7.2 it is seen that there are two basic types of gate drives.

- Low-side
- High-side

Essentially a low-side driver is one where the control signal and the power device gate are at almost the same potential. The lower switches in bridge legs usually use a low-side driver, while the upper switches require high-side drivers which translate the control signal to a different potential. The gate drive circuits 7.2a to 7.2e are basic low-side gate drive circuits. The high-side drivers in figures 7.2f to 7.2i translate the control signal to the gate level.

Although the gate drive circuits in figures 7.2a to 7.2i translate the control signal to the device gate, these circuits do not address two important gate drive issues.

- The derivation of the gate drive supply, particularly for floating gate drives as encountered in inverters.
- The derivation of negative gate bias at turn-off for better immunity to false turn-on due to noise and induced Miller charging effects.

7.1.1i - *Negative gate drive*

The gate drive circuits shown in figure 7.2 only clamp the gate to near zero volts during the off period.

The lower bridge leg switch in figure 7.4 uses ±15V gate voltage. The complementary buffers drive the gate-source of the shown device in an H-bridge configuration. The buffers require an isolated 15V dc supply. Practically a negative gate bias of -5V is sufficient for noise immunity while any voltage in excess of this unnecessarily increases turn-on delay and increases gate power requirements. Manufacturers are continually improving power device properties and characteristics. Gate threshold voltage levels are constantly being decreased, and coupled with the fact that the threshold voltage decreases with temperature, negative voltage gate drive is necessary for high noise immunity to prevent false turn-on with high power devices.

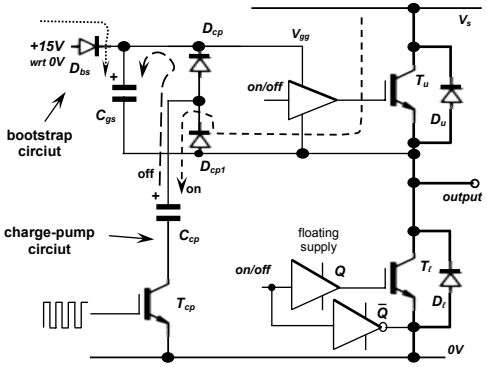


Figure 7.4. *Typical IGBT bridge leg showing ±15V gate drive on the leg lower switch and charge pump plus boot strap gate supply circuits for the leg upper switch.*

7.1.1ii - *Floating power supplies*

There are three basic methods for deriving floating power supplies for gate drives.

- A low inter-winding capacitance, high-frequency transformer
- A capacitive coupled charge pump
- A diode bootstrap

The upper bridge leg switch T_u in figure 7.4 uses both a diode bootstrap via D_{bs} and capacitor charge pumping via C_{cp}, in order to derive gate power.

1 - *capacitive coupled charge pump*

By switching T_{cp} at high frequency the low capacitance capacitor C_{cp} is successively charged through D_{cp1} and discharged through D_{cp}. Discharge through D_{cp} involves charging C_{gs}, the gate voltage supply capacitor. The shown charge and discharge paths both rely on either the upper switch T_u or diode D_u being in a conducting state.

2 - *diode bootstrap*

When the lower switch T_l or diode D_l conduct, diode D_{bs} allows the upper gate supply capacitor C_{gs} to charge from a 15V supply which is referenced to the 0V rail. When the upper switch or diode conduct, the bootstrap diode is reverse bias and supports V_s. Start-up is a problem since the gate of the upper switch T_u is in a high impedance state while its supply is being charged after the lower switch is turned on. For this reason, the boot strap is usually used in conjunction with a capacitor charge pump.

The only foolproof method to ensure gate power at all times, particularly at start-up and during prolong on-state periods, is to use a high-frequency transformer approach.

7.1.2 Gate drive design

The effective gate to source capacitance, C_{in}, can be calculated from

$$C_{in} \triangleq \delta Q_g / \delta V_{gs} \tag{7.1}$$

The initial slope of the charge in figure 7.5a, 740 pF, is due to the gate source capacitance charging below the gate threshold level. The next section between Q_{g1} and Q_{g2} in figure 7.5c is due to the Miller effect. The horizontal charge portion is due to the very high drain-source depletion field capacitance as the drain falls below the gate voltage level.

The drain switching times, similar to those derived in 4.4.2, can be calculated from the charge transfer characteristics in figure 7.5, using the following equations.

(i) From figure 7.5c

$$t_{d\,on} = \frac{Q_{g1}}{V_{g1}} R_g \ \ell n \left(\frac{V_{gg}}{V_{gg} - V_{g1}}\right) \quad \text{(s)} \tag{7.2}$$

$$t_r = \frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}} R_g \ \ell n \left(\frac{V_{gg} - V_{g1}}{V_{gg} - V_{g2}}\right) \quad \text{(s)} \tag{7.3}$$

(ii) From figure 7.5d

$$t_{d\,off} = \frac{Q_{g2} - Q_{g2}}{V_{g2} - V_{g2}} R_g \ \ell n \frac{V_{gg}}{V_{g2}} \quad \text{(s)} \tag{7.4}$$

$$t_f = \frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}} R_g \ \ell n \frac{V_{g2}}{V_{g1}} \quad \text{(s)} \tag{7.5}$$

where R_g is the gate equivalent resistance and $V_{g1} = V_{TH}$.

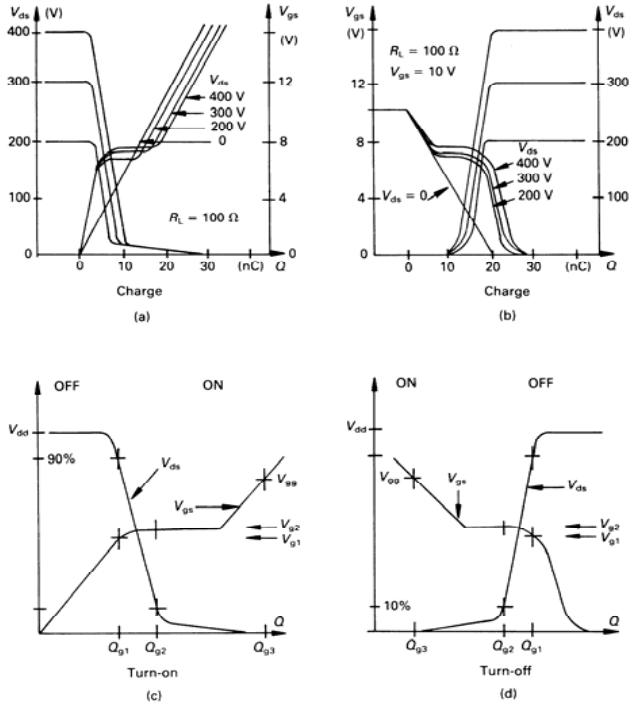


Figure 7.5. *Typical MOSFET charge transfer characteristics at: (a) turn-on; (b) turn-off; (c) turn-on showing switching parameters; and (d) turn-off showing switching parameters.*

The energy required for switching is given by

$$W = \tfrac{1}{2} Q_{g3} V_{gg} \quad \text{(J)} \qquad (7.6)$$

which will be dependent on the drain current and voltage. The gate drive power requirements are given by

$$P = Q_{gs}\ V_{g3}\ f_s \quad \text{(W)} \qquad (7.7)$$

Obviously the faster the switching speed requirement, the higher and faster the gate drive current delivery necessary.

If only 15 mA is available for gate drive then, based on figure 7.5, switching occurs in about 1 µs. This level of performance could be expected with circuit 7.2a, and longer switching for the circuit in figure 7.2c. By employing the gate drive in figure 7.2c, the gate voltage is limited to 5 V, hence the MOSFET represented by figure 7.5 could not be switched.

The circuits in figures 7.2b and 7.2d are capable of delivering about 100 mA, which yields switching speeds of the order of 150 ns, with only 50 mW of drive power dissipation at 100 kHz. The drive circuit in figure 7.2e is capable of delivering ± 1.5 A. Hence the device characterised by figure 7.5 can be switched in only 10 ns.

Switching times deteriorate slightly if reverse gate-to-source biasing is used for higher noise immunity in the off-state. Analysis of the increase in turn-on delay as a result of the use of negative gate drive is presented in Appendix 4.1.

Example 7.1: ***MOSFET input capacitance and switching times***

A MOSFET switching a resistive load has the following circuit parameters:

$$R_g = 47\Omega, \qquad R_L = 100\Omega$$

$$V_{gg} = 10\ \text{V}, \qquad V_{ds} = 400\ \text{V}$$

Based on the charge transfer characteristics in figure 7.5, calculate the gate input capacitance and switching times for MOSFET turn-on and turn-off.

Solution

The charge transfer characteristics shown in figure 7.5 are valid for 100 Ω resistive load and a 0-10 V gate voltage. A 400 V drain switching characteristic is shown.

At turn-on, from figure 7.5a and using equations (7.2) and (7.3)

(i) $C_{in} = C_{gs} = Q_{g1}/V_{g1} = 4.4\ \text{nC}/6\text{V} = 740\ \text{pF}$

$t_{d\,on} = 740\ \text{pF} \times 47\Omega\ \ell n\ (10\text{V}/10\text{V}\text{-}6\text{V}) = 31.9\ \text{ns}$

(ii) $C_{in} = (Q_{g2} - Q_{g1})/(V_{g2} - V_{g1}) = 5.6\ \text{nC}/1.5\text{V} = 3.7\ \text{nF}$

$t_r = 3.7\ \text{nF} \times 47\Omega\ \ell n\ 5.6/2.5 = 141.3\ \text{ns}$

At turn-off, from figure 7.5b and using equations (7.4) and (7.5)

(i) $C_{in} = (Q_{g3} - Q_{g2})/(V_{gg} - V_{g2}) = 7.5\ \text{nC}/2.5\text{V} = 3\ \text{nF}$

$t_{d\,off} = 3\ \text{nF} \times 47\Omega\ \ell n\ 10\text{V}/7.5\text{V} = 40\ \text{ns}$

(ii) $C_{in} = (Q_{g2} - Q_{g1})/(V_{g2} - V_{g1}) = 7.5\ \text{nC}/0.9\text{V} = 8.3\ \text{nF}$

$t_f = 8.33\ \text{nF} \times 47\Omega\ \ell n\ 7.5/6.6 = 50\ \text{ns}$

An underestimate of the fall time results if figure 7.5a is used for all calculations (C_{in} = 3.7 nF and t_f = 39.1 ns).

♣

7.2 Application of the Thyristor

The basic gate requirements to trigger a thyristor into the conduction state are that the current supplied to the gate is

- of adequate amplitude and sufficiently short rise time
- of sufficient duration.

The gate conditions are subject to the anode being forward-biased with respect to the cathode. Figure 7.6 illustrates a typical thyristor gate current waveform for turn-on.

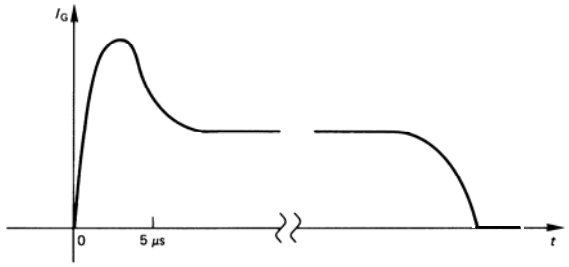


Figure 7.6. *Ideal thyristor gate current waveform for turn-on.*

The initial high and rapid current quickly turns on the device so as to increase the anode initial *di/dt* capability. After a few microseconds the gate current can be decreased to a value in excess of the minimum gate requirement. After the thyristor has latched on, the gate drive may be removed in order to reduce gate power consumption, namely the losses. In some inductive load applications, where the load current lags, a continuous train of gate pulses is usually applied to ensure turn-on.
Gate drives can be divided broadly into two types, either electrically isolated or non-isolated. To obtain electrical isolation usually involves the use of a pulse-transformer or an opto-coupler but above a few kilovolts fibre-optic techniques are applicable.

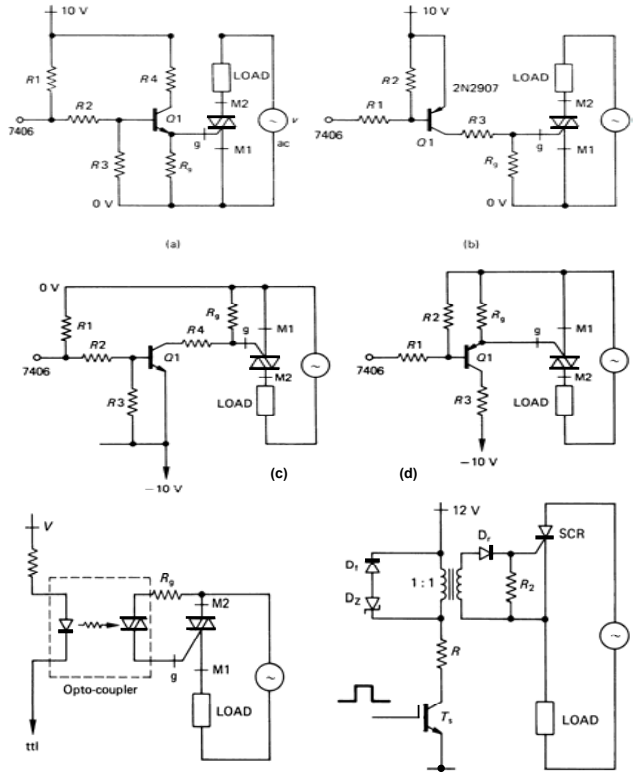


Figure 7.7. *Integrated circuit compatible triac gate drive circuits: (a) high level ttl activation;(b) low level ttl activation using an interfacing pnp transistor; (c) negative gate drive interface with high ttl output for triac activation;(d) negative gate drive interface with low ttl level for triac turn-on; (e) a triac opto-coupler isolated gate drive used to gate-drive a higher power triac and (f) a pulse transformer drive isolated gate drive for a thyristor.*

7.2.1 Thyristor gate drive circuits

Only low-power thyristors with amplifying gates can be triggered directly from ttl or cmos. Usually a power interface stage is employed to convert ttl current sink and source levels of a few milliamps up to the required gate power levels.

Figure 7.7a and b shows two power interface circuits for triggering a triac. The triac could equally be another thyristor device. An important safety default feature of both these circuits is that no active device exists between the gate and Ml. During the off-state the gate is clamped by the resistor R_g to a voltage well below the minimum voltage level for turn-on.

Bidirectional gate current can bring the triac into conduction. Figure 7.7c and d show how negative gate turn-on current can be derived.

If electrical isolation between the control circuitry and the thyristor circuit is required, a simple triac opto-coupler can be employed as shown in figure 7.7e. The photo-triac is optically turned on which allows bidirectional main triac gate current to flow, the magnitude of which is controlled by the resistor R_g. If the main device is an scr, an opto-coupled scr can be used for isolation and uni-direction gate triggering current.

When suitable voltage rails are not available or isolation is required, a pulse transformer drive circuit can be employed as shown in figure 7.7f. The diode/Zener diode series combination across the pulse transformer primary provides a path for primary magnetising current decay at turn-off and prevents saturation. The resistor R limits the secondary current into the scr gate. This resistor can be placed in the pulse transformer primary or secondary by transforming the resistance in the turns ratio squared. If R is in the primary circuit and transformer saturation inadvertently occurs, the resistor R limits the current and protects the switching transistor T_s. The transformer secondary resistor R_2 is employed to decrease the gate to cathode impedance, thereby improving dv/dt capability, while the gate diode D_f prevents possible reverse gate voltage breakdown after T_s is turned off and the output voltage reverses during core reset. The transformer duty cycle must satisfy $t_{off} V_z \geq t_{on} V_s$, neglecting R.

7.2.2 Thyristor gate drive design

In order to design a gate interface circuit, both the logic and thyristor gate requirements must be specified.

Consider interfacing a typical ttl-compatible microprocessor peripheral which offers the following specification

$$I_{OH} = 0.3\text{mA} \ @ \ V_{OH} = 2.4\text{V}$$
$$I_{OL} = 1.8\text{mA} \ @ \ V_{OL} = 0.4\text{V}$$
$$V_{cc} = 5\text{V}$$

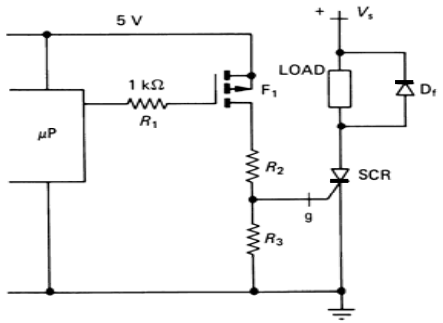


Figure 7.8. *Interfacing a microprocessor to a power thyristor.*

These specifications are inadequate for turning on a power thyristor or an optical interfacing device. If the power thyristor gate, worst case requirements are

$$I_{GT} = 75\text{ mA}, \ V_{GT} = 3\text{ V} \ @ \ -65°\text{C}$$

then a power interfacing circuit is necessary. Figure 7.8 shows an interfacing circuit utilising a p-channel MOSFET with the following characteristics

$$C_{gs} = 400\text{ pf}$$
$$V_{TH} = 3.0\text{V}$$
$$R_{ds(on)} = 10\text{ ohms}$$
$$I_d = 0.5\text{A}$$

The resistor R_1 limits the MOSFET C_{gs} capacitance-charging current and also specifies the MOSFET turn-on time. If the charging current is to be limited to 1.8 mA when V_{OL} = 0.4 V, then

$$R_1 = (V_{cc} - V_{OL}) / I_{OL} \quad \text{(ohms)}$$
$$= (5\text{V} - 0.4\text{V}) / 1.8\text{mA} = 2.7\text{ kilohms}$$

A smaller resistance could be used but this would not preserve the microprocessor low-voltage output level integrity if it were being used as input to ttl logic. The MOSFET will not turn on until C_{gs} has charged to 3 V or, with a 5 V rail, approximately one R-C time constant. That is

$$t_{delay} = R_1 C_{gs} \quad \text{(s)}$$
$$= 2.7\text{ kilohms} \times 400\text{ pF} = 1\ \mu\text{s}$$

The MOSFET must provide the thyristor gate current and the current through resistor R_3 when the gate is at 3 V.
The maximum value of resistor R_2 is when $R_3 = \infty$ and is given by

$$R_2 = \frac{V_{cc} - V_{GT} - I_{GT} \times R_{ds(on)}}{I_{GT}}$$

$$= \frac{5\text{V} - 3\text{V} - 75\text{ mA} \times 10\Omega}{75\text{ mA}} = 16.6 \text{ ohms}$$

Use R_2 = 10 ohms.
The resistor R_3 provides a low cathode-to-cathode impedance in the off-state, thus improving scr noise immunity. When V_{GT} = 3 V

$$I_d = \frac{V_{cc} - V_{GT}}{R_{ds(on)} + R_2} \quad \text{(A)}$$

$$= \frac{5\text{V}-3\text{V}}{10\Omega+10\Omega} = 100 \text{ mA}$$

of which 75 mA must flow into the gate, while 25 mA can flow through R_3. That is

$$R_3 = V_{GT}/(I_d - I_{GT}) \quad \text{(ohms)}$$

$$= 3 \text{ V}/25 \text{ mA} = 120 \text{ ohms}$$

After turn-on the gate voltage will be about 1 V, hence the MOSFET current will be 200 mA. Assuming 100 per cent on-state duty cycle, the I^2R power loss in the MOSFET and resistor R_2 will each be 0.4 W. A 1 W power dissipation 10 ohm resistor should be used for R_2.

Example 7.2: ***A light dimmer***
A diac with a breakdown voltage of ±30 V is used in a light dimming circuit as shown in figure 7.9. If R is variable from 1 kΩ to 22 kΩ and C = 47 nF, what are the maximum and minimum firing delays? What is the controllable output power range with a 10Ω load resistor?

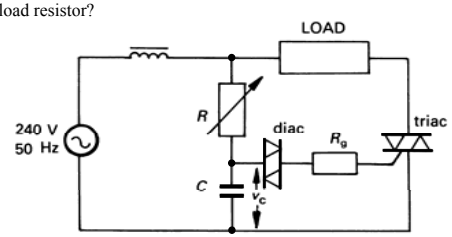


Figure 7.9. *Light dimmer.*

Solution
The capacitor voltage v_c is given by

$$v_c = \frac{-j/\omega C}{R - j/\omega C} \times 240\angle 0°$$

$$= \frac{1}{1 + j\omega CR} \times 240\angle 0°$$

i. For R = 1 kΩ
$v_c = 237.36 \angle -8.4°$
that is, $v_c = 335.8 \sin(\omega t - 8.4°)$
The diac conducts when v_c = 30V, that is
minimum delay = $\omega t = 8.4° + \sin^{-1}(30\text{V}/335.8\text{V}) = 13.5°$

ii. For R = 22 kΩ
$v_c = 70.6 \angle -72.8°$
that is, $v_c = 99.8.8 \sin(\omega t - 72.8°)$
The diac conducts when v_c = 30V, that is
minimum delay = $\omega t = 72.8° + \sin^{-1}(30\text{V}/99.8\text{V}) = 92°$

From equation (12.14), the output power for a resistive load is given by

$$P_o = \frac{V_{rms}^2}{R} = \frac{V^2}{R}\left\{1 - \frac{2\alpha - \sin 2\alpha}{2\pi}\right\} \quad \text{(W)}$$

Minimum power at α = 92° (1.6 rad) is $P_o = \frac{240^2}{10\Omega} \times \left\{1 - \frac{2\times 92° - \sin 2\times 92°}{2\pi}\right\} = 2862\text{W}$

Maximum power at α=13½° (0.24rad) is $P_o = \frac{240^2}{10\Omega} \times \left\{1 - \frac{2\times 13½° - \sin 2\times 13½°}{2\pi}\right\} = 5536\text{W}$

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7.3 Drive design for GTO thyristors

The gate turn-off thyristor is not only turned on from the gate but, as its name implies, is turned off from its gate with negative gate current. Basic GTO thyristor gate current requirements are very similar to those for the power bipolar transistor (now virtually obsolete) when reverse base current is used for fast turn-off.
Figure 7.10 shows a gate drive circuit for a GTO thyristor which is similar to that historically used for power bipolar junction transistor base drives. The inductor L, in figure 7.10, is the key turn-off component since it controls the di/dt of the reverse gate current. The smaller the value of L, the larger is the reverse di/dt and the shorter the turn-off time. But with a shorter turn-off time the turn-off gain decreases, eventually to unity. That is, if the GTO thyristor is switched off rapidly, the reverse gate current must be of the same magnitude as the anode current to be extinguished. A slowly applied

reverse gate current *di/dt* can produce a turn-off gain of over 20 but at the expense of increased turn-off switching losses. For the GTO thyristor L is finite to get a turn-off gain of more than one, while to achieve unity gain turn-off for the GCT, L is minimised.
The GTO thyristor cathode-to-gate breakdown voltage rating V_{RGM} specifies the maximum negative rail voltage level. A level of 15-20V is common, and for supply rail simplicity a ± 15 V rail may be selected.
Resistor R_4 limits the base current of T_t. If an open collector ttl driver is employed, the current through R_4 is given by

$$I_{OL} = (V_{cc} - V_{beT_t} - V_{Db} - V_{OL}) / R_4 \qquad \text{(A)}$$

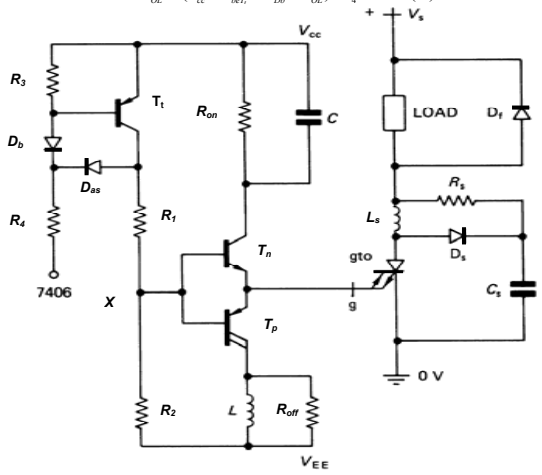

Figure 7.10. *Gate drive circuit and anode snubber circuits for a GTO thyristor.*

For open collector 74 ttl series, $I_{OL} = 40$ mA when V_{OL} - 0.5 V and therefore R_4 can be specified. The resistor R_3 speeds up turn-off of T_t. It is as large as possible to ensure that minimal base current is diverted from T_t. Diodes D_b and D_{as} form a Baker's clamp, preventing T_t from saturating thereby minimising its turn-off delay time.
The two driver transistor T_n and T_p should

- have high gains
- be fast switching
- have collector voltage ratings in excess of $V_{cc} + V_{EE}$.

The GTO thyristor gate turn-on current is determined by resistor R_{on}, which is specified by

$$R_{on} = \frac{V_{cc} - V_{ceT_n} - V_{GC}}{I_G} \qquad \text{(Ohms)}$$

The power rating of R_{on} is given by

$$P_{R_{on}} = \delta(V_{cc} - V_{ceT_n} - V_{GC}) I_G \qquad \text{(W)}$$

where δ is the maximum on-state duty cycle. The capacitor C_{on}, in parallel with R_{on}, provides a short current boost at turn-on, thereby speeding up turn-on, increasing turn-on initial *di/dt* capability, and reducing turn-on losses.
The series resistors R_1 and R_2 bias the bases of the totem pole level shift driver and, for an on-condition, the potential of point X in figure 7.10 is given by

$$V_X = V_{beT_n} + V_{GC} \qquad \text{(V)}$$

The total current flow through R_1 is made up of the transistor T_n base current and that current flowing through R_2, that is

$$I_{R1} = \frac{I_G}{\beta_{T_n}} + \frac{V_X + V_{EE}}{R_2} \qquad \text{(A)}$$

from which

$$R_1 = (V_{cc} - V_X) / I_{R1} \qquad \text{(ohms)}$$

The power rating of R_1 is

$$P_{R_1} = \delta(V_{cc} - V_X) I_{R_1} \qquad \text{(W)}$$

For fast turn-off, if the reverse gate current at turn-off is to be of the same magnitude as the maximum anode current, then R_2 must allow sufficient base current to drive T_p. That is

$$R_2 = \frac{V_X + V_{beT_p}}{I_c / \beta\beta_p} \qquad \text{(ohms)}$$

Once the gate-to-cathode junction of the GTO has recovered, the reverse gate current falls to the leakage level. The power rating of R_2 can be low at lower switching frequencies.
The small inductor L in the turn-off circuit is of the order of microhenrys and it limits the rate of rise of reverse gate current, while R_{off} damps any inductor current oscillation.
The turn-on and turn-off BJT circuits can be replaced by a suitable n-channel MOSFET circuit in high power GTO and GCT applications. In high power IGCT applications, MOSFET and rail decoupling electrolytic capacitors are extensively parallel connected. Typically 21 capacitors and 42 MOSFETs are parallel connected to provide a low impedance path for anode current extraction from the GCT gate. The gate inductance (including the GCT internal package inductance) is minimised, whence L is zero.

Table 7.3 Gate drive isolation technique summary

Technique	data transfer	power transfer	comments
Transformer	direct signal coupling	direct magnetic transfer	duty cycle limited corona breakdown limit
optocoupler	slow, with capacitive effects	n/a	voltage and *dv/dt* limit
fibre optics	fast, virtually no voltage limit	n/a	best signal transmission at MV and HV
charge couple	n/a	requires switching	induced effects between ground level and gate level, LV application
bootstrap	n/a	requires switching	

Reading list

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HDB-5, 1987.

Peter, J. M., *The Power Transistor in its Environment,*
Thomson-CSF, Sescosem, 1978.

Siliconix Inc., *Mospower Design Catalog,*
January 1983.

Graffiam, D. R. *et al., SCR Manual,*
General Electric Company, 6th Edition, 1979.

Problems

7.1. Calculate suitable resistor values for the triac gate drive circuit in figure 7.7a, assuming a minimum gate current requirement of 50 mA and the gain of Q1 is 50 at 50 mA.

7.2. Repeat problem 7.1 for the circuits in figures

- 7.7b
- 7.7c
- 7.7d.

8

Protecting Diodes, Transistors, and Thyristors

All power switching devices attain better switching performance if some form of switching aid circuit, called snubber, is employed. Snubber activation may be either passive or active which involves extra power switches. Only passive snubbers, which are based on passive electrical components, are considered in this chapter, while active snubbers are considered in Chapter 9. Fundamentally, the MOSFET and IGBT do not require switching aid circuits, but circuit imperfections, such as stray inductance and diode recovery, can necessitate the need for some form of switch snubber protection.
Protection in the form of switching aid circuits performs two main functions:

- Divert switching losses from the switch thereby allowing a lower operating temperature, or higher electrical operating conditions for a given junction temperature.
- Prevent transient electrical stressing that may exceed *I-V* ratings thereby causing device failure.

Every switching device can benefit from switching protection circuits, but extra circuit component costs and physical constraints may dictate otherwise.
The diode suffers from reverse recovery current and voltage snap which induces high but short duration circuit voltages. These voltage transients may cause interference to the associated circuit and to nearby equipment. A simple series *R-C* circuit connected in parallel to the stressed device is often used to help suppress the voltage oscillation at diode turn-off. Such a suppression circuit can be used on simple mains rectifying circuits when rectification causes conducted and radiated interference.
Although the MOSFET and IGBT can usually be reliably and safely operated without external protection circuitry, stringent application emission restrictions may dictate the use of snubbers. In specific applications, the IGBT is extensively current derated as its operating frequency increases. In order to attain better device current utilization, at higher frequencies, various forms of switching aid circuits can be used to divert switching losses from the stressed switch.
Generally, all thyristor devices benefit from a turn-on switching aid circuit, which is based on a series connected inductor that is active at thyristor turn-on. Such an

inductive turn-on snubber is obligatory for the high-power GTO thyristor and GCT. In order to fully utilise the GTO thyristor, it is usually used in conjunction with a parallel-connected capacitive turn-off snubber, which decreases device stressing during the turn-off transient. Triacs and rectifying grade SCRs and diodes tend to use a simple *R-C* snubber connected in parallel to the switch to reduce interference. The design procedure of the *R-C* snubber for a diode is different to that for the *R-C* snubber design for a thyristor device, because the protection objectives and initial conditions are different. In the case of a thyristor or rectifying diode, the objective is to control both the voltage rise at turn-off and recovery overshoot effects. For the fast recovery diode or any high-speed switch, the principal objectives are to control the voltage overshoot magnitude at diode snap recovery or at turn-off respectively, which are both exacerbated because of stray circuit inductance carrying current.

8.1 The *R-C* snubber

The series *R-C* snubber is the simplest switching aid circuit and is connected in parallel to the device being aided. It is characterized by having low series inductance and a high transient current rating. These requirements necessitate carbon type resistors for low inductance, below a few watts, and metal film resistors at higher powers. The high current and low inductance requirements are also provided by using metallised, polypropylene capacitors with high *dv/dt* ratings of typically hundreds of V/µs.
Theoretically a purely capacitive snubber would achieve the required protection objectives, but series resistance is added to decrease the current magnitude when the capacitor is discharging and to damp any oscillation by dissipating the oscillatory energy generated at turn-off when an over-voltage tends to occur.

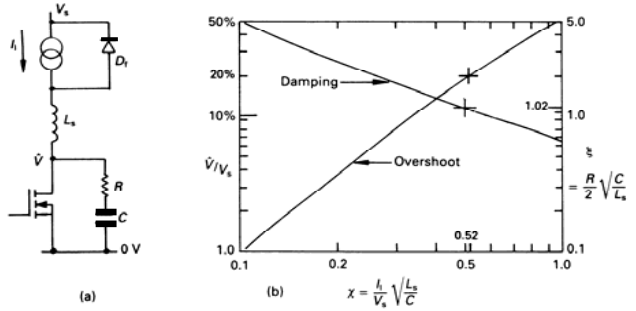


Figure 8.1. *MOSFET drain to source R-C snubber protection: (a) MOSFET circuit showing stray inductance, L_s, and R-C protection circuit and (b) R-C snubber optimal design curves.*

8.1.1 R-C switching aid circuit for the MOSFET and the diode

In figure 8.1a, at switch turn-off stray inductance L_s unclamped by the load freewheel diode, D_f, produces an over voltage $\hat{V}$ on the MOSFET or IGBT. The energy associated with the inductor can be absorbed in the shown drain to source *R-C* circuit, thereby containing the voltage overshoot to a safe level. Such an *R-C* snubber circuit is used extensively in thyristor circuits, 8.1.2, for *dv/dt* protection, but in such cases the initial current in the stray inductance is assumed zero. Here the initial inductor current is equal to the maximum load current magnitude, I_ℓ. The design curves in figure 8.1b allow selection of *R* and *C* values based on the maximum voltage overshoot $\hat{V}$ and an initial current factor χ, defined in figure 8.1b. The *C* and *R* values are given by

$$C = L_s\,(I_\ell/\chi V_s)^2 \qquad \text{(F)} \qquad (8.1)$$

$$R = 2\xi V_s \chi / I_\ell \qquad (\Omega) \qquad (8.2)$$

If the *R-C* circuit time constant, $\tau=RC$, is significantly less than the MOSFET voltage rise and fall times, t_{rv} and t_{fv}, at reset, a portion of the capacitor energy $\frac{1}{2}CV_s^2$, is dissipated in the switch, as well as in *R*. The switch appears as a variable resistor in series with the *R-C* snubber. Under these conditions (t_{fv} and $t_{rv} > RC$) the resistor power loss is approximately by

$$P_R = P_{Ron} + P_{Roff}$$

$$= \frac{\tau}{\tau + t_{fv}} P_{C0} + \frac{\tau}{\tau + t_{rv}}(P_{C0} + P_{L0}) \qquad \text{(W)} \qquad (8.3)$$

where $P_{C0} = \frac{1}{2}CV_s^2 f_s$ and $P_{L0} = \frac{1}{2}L_s I_\ell^2 f_s$

otherwise (t_{fv} and $t_{rv} < RC$) the resistor losses are the energy to charge and discharge the snubber capacitor, plus the energy stored in the stray inductance, that is $2P_{C0}+P_{L0}$.
Note the total losses are independent of snubber resistance. The snubber resistor determines the time over which the energy is dissipated.
When the *R-C* snubber is employed across a fast recovery diode, the peak reverse recovery current is used for I_ℓ in the design procedure.

Example 8.1: ***R-C snubber design for MOSFETs***
A MOSFET switches a 40 A inductive load on a 200 V dc rail, at 10 kHz. The unclamped drain circuit inductance is 20 nH and the MOSFET voltage rise and fall times are both 100 ns. Design a suitable *R-C* snubber if the MOSFET voltage overshoot is to be restricted to 240 V (that is, 40V overshoot, viz. 20%).

Solution
From figure 8.1b, for 20 per cent voltage overshoot

$$\xi = 1.02,\ \chi = 0.52$$

Using equations (8.1) and (8.2) for evaluating *C* and *R* respectively,

$$C = L_s\,(I_\ell/\chi V_s)^2 = 20\text{nH}\left(\frac{40\text{A}}{0.52\times 200\text{V}}\right)^2 = 3\text{nF}$$

$$R = 2\xi V_s \chi / I_\ell = 2\times 1.02\times\frac{0.52\times 200\text{V}}{40\text{A}} = 5.3\Omega$$

Use *C*=3.3 nF, 450V dc, metallised polypropylene capacitor and *R*=5.6 Ω.
Since the *RC* time constant, 18.5ns, is short compared with the MOSFET voltage transient times, 100ns, the resistor power rating is given by equation (8.3).

$$P_{C0} = \tfrac{1}{2}CV_s^2 f_s = \tfrac{1}{2}\times 3.3\text{nF}\times 200^2\times 10\text{kHz} = 2.64\text{W}$$

$$P_{L0} = \tfrac{1}{2}L_s I_\ell^2 f_s = \tfrac{1}{2}\times 20\text{nH}\times 40^2\times 10\text{kHz} = 0.16\text{W}$$

$$P_R = \frac{18.5}{100+18.5}\times 2.64\text{W} + \frac{18.5}{100+18.5}\times(2.64\text{W} + 0.16\text{W}) = 0.85\text{W}$$

Use a 5.6 Ω, 1 W carbon composition resistor for low self inductance, with a working voltage of at least 250V dc. Parallel connection of two ½W, carbon composition resistors may be necessary since resistance values below 10Ω are uncommon.
The MOSFET switching losses are increased by $2W_{C0} + P_{L0} - 0.85\text{W} = 4.95\text{W}$.

♣

8.1.2 R-C snubber circuit for a converter grade thyristor and a triac

The snubber circuit for a low switching frequency thyristor is an anode-to-cathode parallel connected *R-C* series circuit for off-state voltage transient suppression. Series inductance may be necessary (forming a turn-on snubber) to control anode *di/dt* at turn-on. This inductive snubber is essential for the GTO thyristor and the GCT, and will be considered in section 8.3.3.

Off-state dv/dt suppression snubber
Thyristors, other than the GTO thyristor, normally employ a simple *R-C* snubber circuit as shown in figure 8.2. The purpose of the *R-C* snubber circuit is not primarily to reduce turn-off switching loss but rather to prevent false triggering from applied or reapplied anode *dv/dt*, when the switch is in the off-state.
Any thyristor rate of rise of forward-voltage anode *dv/dt* produces a central junction charging current which may cause the thyristor to inadvertently turn on. The critical *dv/dt* is defined as the minimum value of *dv/dt* which will cause switching from the off-state to the on-state. In applications as shown in figure 8.2, an occasional false turn-on is generally not harmful to the triac or the load, since the device and the load only have to survive the surge associated with a half-a-cycle of the ac mains supply.
In other applications, such as reversible converters, a false *dv/dt* turn-on may prove catastrophic. A correctly designed snubber circuit is therefore essential to control the rate of rise of anode voltage.

The action of this *R-C* snubber circuit relies on the presence of inductance in the main current path. Zero inductor current is the initial condition, since the device is in the off-state when experiencing the anode positive *dv/dt*. The inductance may be stray, from transformer leakage or a supply, or deliberately introduced. Analysis is based on the response of the *R-C* portion of an *L-C-R* circuit with a step input voltage and zero initial inductor current. Figure 8.3 shows an *L-C-R* circuit with a step input voltage and the typical resultant voltage across the SCR or *R-C* components. The circuit resistor *R* damps (by dissipating power) any oscillation and limits the capacitor discharge current through the SCR at subsequent device turn-on from the gate.

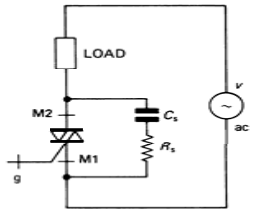


Figure 8.2. *Thyristor (triac) ac circuit with an R-C snubber circuit.*

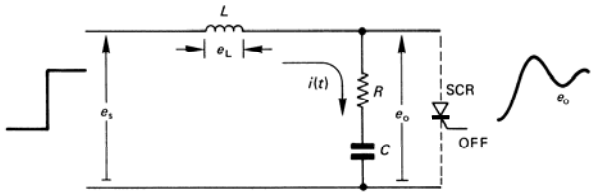


Figure 8.3. *R-C snubber equivalent circuit showing the second-order output response e_o to a step input voltage e_s.*

Based on the snubber circuit analysis presented in the appendix in section 8.5 at the end of this chapter, the maximum *dv/dt*, $\hat{S}$, which is usually specified for a given device, seen by the SCR for a step input of magnitude e_s, is given by

$$\hat{S} = e_s R / L \qquad \text{(V/s)} \tag{8.4}$$

for a damping factor of $\xi > ½$. That is, after rearranging, the snubber resistance is given by

$$R = L\hat{S}/e_s \qquad \text{(ohms)} \tag{8.5}$$

while the snubber capacitance is given by

$$C = \frac{4\xi^2 e_s}{R\hat{S}} \qquad \text{(F)} \tag{8.6}$$

and the peak snubber current is approximated by

$$\hat{I} = \frac{e_s}{R}\frac{2\xi}{\sqrt{1-\xi^2}} \qquad \text{(A)} \qquad \text{for } \xi < 1. \tag{8.7}$$

Figure 8.4 shows the variation of the various normalised design factors, with damping factor ξ.

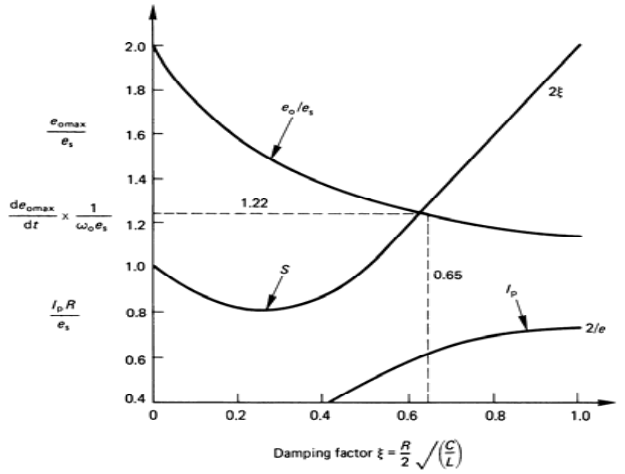


Figure 8.4. *Variation of snubber peak voltage, e_o, maximum de_o/dt, $\hat{S}$; and peak current, I_p; with L-C-R damping factor ξ.*

Example 8.2: ***R-C snubber design for a converter grade thyristor***

Design an *R-C* snubber for the SCRs in a cycloconverter circuit where the SCRs experience an induced *dv/dt* due to a complementary SCR turning on, given

- peak switching voltage, $e_s = 200$ V
- operating frequency, $f_s = 1$ kHz
- *dv/dt* limit, $S = 200$ V/μs.

Assume

- stray circuit $L = 10$ μH
- 22 per cent voltage overshoot across the SCR
- an *L-C-R* snubber is appropriate.

Solution

From equation (8.5) the snubber resistance is given by

$$R = L\hat{S}/e_s$$
$$= \frac{10\mu\text{H}\times 200\text{V}/\mu\text{s}}{200\text{V}} = 10\Omega$$

At turn-on the additional anode current from the snubber capacitor will be 200V/10Ω = 20A, which decays exponentially to zero, with a 1.8μs (10Ω×180nF) *RC* time constant. Figure 8.4 shows the *R-C* snubber circuit overshoot magnitude, $\hat{e}_0/e_s$ for a range of damping factors ξ. The normal range of damping factors is between 0.5 and 1. Thus from figure 8.4, allowing 22 per cent overshoot, implies $\xi = 0.65$. From equation (8.6)

$$C = \frac{4\xi^2 e_s}{R\hat{S}} = \frac{4\times(0.65)^2\times 200\text{V}}{10\Omega\times 200\times 10^6}$$

$$= 180 \text{ nF (preferred value) rated at 244 V peak.}$$

From equation (8.7) the peak snubber current during the applied *dv/dt* is

$$\hat{I} = \frac{e_s}{R}\frac{2\xi}{\sqrt{1-\xi^2}}$$
$$= \frac{200\text{V}}{10\Omega}\frac{2\times 0.65}{\sqrt{1\text{-}0.65^2}} = 34 \text{ A}$$

The 10 ohm snubber resistor losses are given by

$$P_{10\Omega} = Ce_0^2 f_s$$
$$= 180\times 10^{-9}\times 244^2\times 1\times 10^3 = 11\text{W}$$

The resistor carries current to both charge (maximum 34A) and discharge (initially 20A) the capacitor. The necessary 10Ω, 11W resistor must have lower inductance, hence two 22 Ω, 7W, 500V dc working voltage, metal oxide film resistors can be parallel connected to achieve the necessary ratings.

♣

Variations of the basic snubber circuit are shown in figure 8.5. These circuits use extra components in an attempt to control SCR initial *di/dt* arising from snubber discharge through R_L at turn-on.

An *R-C* snubber can be used across a diode in order to control voltage overshoot at diode snap-off during reverse recovery, as a result of stray circuit inductance, as considered in 8.1.1.

The *R-C* snubber can provide decoupling and transient overvoltage protection on both ac and dc supply rails, although other forms of *R-C* snubber circuit may be more applicable, specifically the soft voltage clamp.

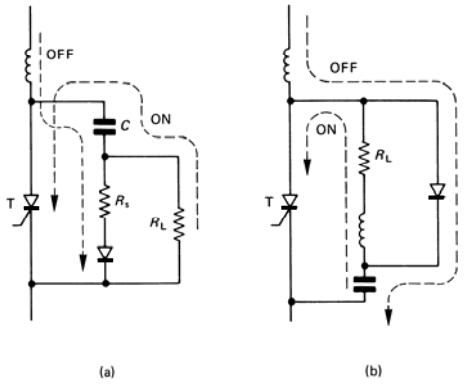


Figure 8.5. *Variations of the basic thyristor R-C snubber: (a) R_s<<R_L and (b) transistor-type R-C-D snubber, R_s = 0.*

8.2 The soft voltage clamp

A primary function of the basic *R-C* snubber is to suppress voltage overshoot levels. The *R-C* snubber commences its clamping action from zero volts even though the objective is to clamp the switch voltage to the supply voltage level, V_s. Any clamping action below V_s involves the unnecessary transfer of energy. The soft voltage clamp reduces energy involvement since it commences clamping action once the switch voltage has reached the supply voltage V_s, and the voltage overshoot commences.

The basic *R-C-D* soft voltage clamp is shown in figure 8.6a, with resistor *R* parasitic inductance, L_R, and stray or deliberately introduced unclamped inductance *L*, shown.
The voltage clamp functions at switch turn-off once the switch voltage exceeds V_s. The capacitor voltage does not fall below the supply rail voltage V_s. Due to the stored energy in *L*, the capacitor *C* charges above the rail voltage and *R* limits current magnitudes as the excess capacitor charge discharges through *R* in to V_s. All the energy stored in *L*, $\frac{1}{2}LI_m^2$, is dissipated in *R*. The inductor current i_L and capacitor voltage V_c waveforms are shown in figure 8.6b.
At switch turn-on, the diode D blocks, preventing discharge of C which remains charged to V_s.

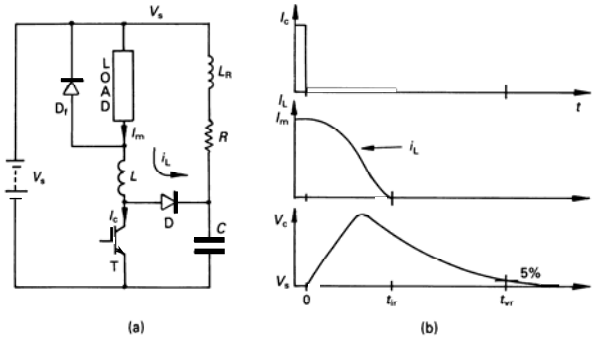


Figure 8.6. *Soft voltage clamp:*
(a) circuit diagram and (b) turn-on inductor current, I_L, and capacitor voltage, V_c, at switch turn-off.

The energy drawn from the supply V_s as the capacitor overcharges, is returned to the supply as the capacitor discharges through *R* into the supply. The net effect is that only the energy in *L*, $\frac{1}{2}LI_m^2$, is dissipated in *R*.
Analysis is simplified if the resistor inductance L_R is assumed zero. The inductor current decreases from I_m to 0 according to

$$i_L(\omega t) = I_m \omega_0/\omega e^{-\alpha t}\cos(\omega t - \phi) \qquad \text{(A)} \qquad (8.8)$$

where $\alpha = \frac{1}{2}RC$ (s) $\omega_0 = 1/\sqrt{LC}$ (rad/s)
$\omega = \sqrt{\omega_0^2 - \alpha^2}$ (rad/s) $\phi = \tan^{-1}\alpha/\omega$ (rad)

The inductor current reaches zero, termed the current reset time, t_{ir}, in time

$$t_{ir} = (\tfrac{1}{2}\pi + \phi)/\omega \qquad \text{(s)} \qquad (8.9)$$

which must be shorter than the switch minimum off-time, $\check{t}_{off}$. The capacitor charges from V_s according to

$$V_C(\omega t) = V_s + \frac{I_m}{\omega C}e^{-\alpha t}\sin\omega t \qquad \text{(V)} \qquad (8.10)$$

The maximum capacitor voltage, hence maximum switch voltage, occurs for large *R*

$$\hat{V}_C = V_s + I_m\sqrt{\frac{L}{C}} \qquad \text{(V)} \qquad (8.11)$$

Once the current in *L* has reduced to zero the capacitor discharges to V_s exponentially, with a time constant *RC*.
The practical *R-C* circuit, which includes the stray inductance L_R, must be over-damped, that is

$$R > 2\sqrt{\frac{L_R}{C}} \qquad (\Omega) \qquad (8.12)$$

The capacitor voltage reset time t_{vr} is the time for the capacitor to discharge to within 5 per cent of V_s, as shown in figure 8.6b.
The stray inductance L_R increases the peak capacitor voltage and increases the voltage reset time. Design of the voltage clamp, including the effects of L_R, is possible with the aid of figure 8.7. Design is based on specifying the maximum voltage overshoot, V_{cp} and minimizing the voltage reset time, t_{vr}, which limits the upper switching frequency, f_s, where $f_s \le 1/t_{vr}$ such that $\check{t}_{off} \ge t_{ir}$.

Example 8.3: ***Soft voltage clamp design***
A 5 µH inductor turn-on snubber is used to control diode reverse recovery current and switch turn-on loss, as shown in figure 8.6a. The maximum collector current is 25 A, while the minimum off-time is 5 µs and the maximum operating frequency is 50 kHz.

i. Assuming an independent *L-C* resonant transfer from *L* to *C* and a subsequent *R-C* discharge cycle, calculate soft voltage clamp *R* and *C* requirements.
ii. Use figure 8.7 to determine the voltage clamp requirements if the discharge (reset) resistor inductance L_R is
    (a) 0
    (b) 1.0µH.

In each case, the maximum switch overshoot is to be restricted to 50 V.

Solution
i. Assuming all the inductor energy is transferred to the clamp capacitor, before any discharge through R occurs, then from equation (8.11), for a 50 V capacitor voltage rise

$$50 = I_m\sqrt{L/C}$$

that is, $C = 5\ \mu H/(50V/25A)^2 = 1.25\ \mu F$ (use 1.2 µF).

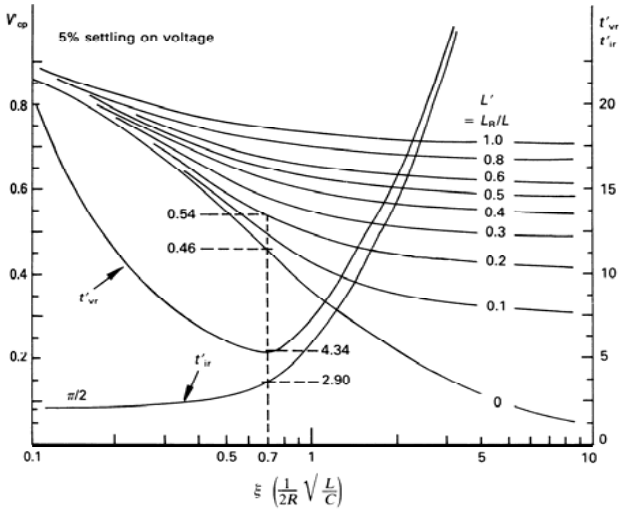


Figure 8.7. *Voltage clamp capacitor normalised peak over-voltage, V'_{Cp}, versus damping factor, ξ, for different resistor normalised inductances, L′, and voltage and current normalised settling times, t'_{vr}, $t'_{ir} = V_{cp}/\{I_m\sqrt{L/C}\}$, $t'_{vr} = t_{rv}/\omega_0$, $t'_{ir} = t_{ir}/\omega_0$.*

From equation (8.9), for $R = 0$, the energy transfer time (from L to C) is

$$t_{ir} = \tfrac{1}{2}\pi\sqrt{LC} = \tfrac{1}{2}\pi\sqrt{5\mu H \times 1.25\mu F} = 4\mu s$$

which is less than the switch minimum off-time of 5 μs.
If the maximum operating frequency is 50 kHz, the capacitor must discharge in 20 - 4 = 16 μs. Assuming five RC time constants for capacitor discharge

$$5 \times RC = 16\mu s$$

$$R = 16\mu s/(5\times 1.2\mu F) = 2\tfrac{2}{3}\Omega \quad \text{(use 2.4}\Omega\text{)}$$

The resistor power rating is

$$P_R = \tfrac{1}{2}LI_m^2 f_s = \tfrac{1}{2}\times 5\mu H \times 25^2 \times 50kHz = 78W$$

Obviously with a 2.4 Ω discharge resistor and 50V overshoot, discharge current would flow as the capacitor charges above the voltage rail. A smaller value of C could be used. A more accurate estimate of C and R values is possible, as follows.

ii. (a) $L_R = 0$, $L' = 0$
From figure 8.7, for the minimum voltage reset time

$$V'_{cp} = 0.46, \quad t'_{ir} = 2.90, \quad t'_{rv} 4.34, \quad \text{and} \quad \xi = 0.70$$

From $V'_{cp} = V_{cp}/I_m\sqrt{L/C}$

$$0.46 = 50V/25A\sqrt{5\mu H/C} \text{ gives } C = 0.27\mu F$$

From $\xi = \frac{1}{2R}\sqrt{L/C}$, $R = \frac{1}{2\xi}\sqrt{L/C} = \frac{1}{2\times 0.7}\sqrt{5\mu H/0.27\mu F} = 3.2\Omega$

(Use 3.3 Ω, 78 W)
The reset times are given by

$$t_{vr} = t'_{vr}\sqrt{LC} = 4.34 \times 1.16 = 5\mu s \quad (<20\mu s)$$

$$t_{ir} = t'_{ir}\sqrt{LC} = 2.9 \times 1.16 = 3.4\mu s \quad (<5\mu s)$$

It is seen that smaller capacitance (1.2 μF *vs* 0.27 μF) can be employed if simultaneous L-C transfer and R-C discharge are accounted for. The stray inductance of the resistor discharge path has been neglected. Any inductance decreases the effectiveness of the R-C discharge. Larger C than 0.27 μF and $R < 3.3\Omega$ are needed, as is now shown.
ii. (b) $L_R = 1\mu H$, $L' = L_R/L = 0.2$
In figure 8.7, for a minimum voltage reset time, $\xi = 0.7$, $V'_{cp} = 0.54$ when the L'=0.2 curve is used. The normalised reset times are unchanged, that is $t'_{ir} = 2.9$ and $t'_{vr} = 4.34$. Using the same procedure as in part b(i)

$$0.54 = 50V/25A\sqrt{5\mu H/C} \text{ gives } C = 0.37\mu F \text{ (use 0.39}\mu F\text{)}$$

$$R = \frac{1}{2\xi}\sqrt{L/C} = \frac{1}{2\times 0.7}\sqrt{5\mu H/0.39\mu F} = 2.6\Omega \quad \text{(use 2.7}\Omega\text{, 78W)}$$

Since resistor inductance has been accounted for, parallel connection of four 10Ω, 25W wire-wound aluminium clad resistors can be used.

$$t_{vr} = 4.34\times 1.4 = 6\mu s \quad (< 20\mu s)$$

$$t_{ir} = 2.90\times 1.4 = 4\mu s \quad (< 5\mu s)$$

Note that circuit supply voltage V_s is not a necessary design parameter, other than to specify the capacitor absolute dc voltage rating.

♣

8.3 Switching-aid circuits

Optimal gate drive electrical conditions minimize collector (or drain or anode) switching times, thus minimizing switch electrical stresses and power losses. Proper gate drive techniques greatly enhance the switching robustness and reliability of a power switching device. Switching-aid circuits, commonly called *snubber circuits,* can

be employed to further reduce device switching stresses and losses. Optimal gate drive conditions minimise the amount of snubbering needed.

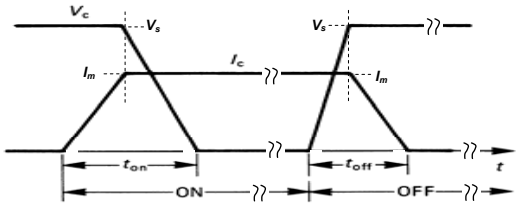


Figure 8.8. *Idealised collector switching waveforms for an inductive load.*

During both the switch-on and the switch-off intervals, for an inductive load as considered in chapter 6.2, an instant exists when the switch simultaneously supports the supply voltage V_s and conducts the full load current I_m, as shown in figure 8.8. The gate drive conditions cannot alter this peak power loss but can vary the duration of the switching periods (t_{on} and t_{off}). From chapter 6, the switching losses, W, dissipated as heat in the switch, are given by

for turn-on $W_{on} = \frac{1}{2} V_s I_m t_{on}$ (J) (8.13)

for turn-off $W_{off} = \frac{1}{2} V_s I_m t_{off}$ (J) (8.14)

In order to reduce switching losses, two snubber circuits can be employed on a power switching device, one operational during switch turn-on, the other effective during turn-off. In the case of the turn-off snubber, energy is diverted from the switch turning off into a parallel capacitor as shown in figure 8.9a. The turn-on snubber utilises an inductor in series with the collector as shown in figure 8.9b in order to control the rate of rise of anode current during the collector voltage fall time. For both snubbers, the *I-V* SOA trajectory is modified to be within that area shown in figure 6.8.

- *An **inductive turn-on snubber*** is essential for the GTO thyristor and the GCT in order to control the initial *di/dt* current to safe levels at switch turn-on. In large area thyristor devices, the inductor controlled current increase at turn-on allows sufficient time for the silicon active area to spread uniformly so as to conduct safely the prospective load current. Special thyristor gate structures such as the amplifying gate, as shown in figure 3.23, allow initial anode *di/dt* values of up to 1000 A/us. Use of a turn-on snubber with the MOSFET and the IGBT is limited but may be used because of freewheel diode imposed limitations rather than an intrinsic need by the switch.
- *The **capacitive turn-off snubber*** is used extensively on the GTO thyristor. The *R-D-C* circuit is necessary to ensure that GTO turn-off occurs at a low anode-to-cathode voltage, preventing excessive power loss at the central GTO junction during reverse recovery. Larger area GTOs employ 1 to 8 µF in an *R-D-C* turn-off snubber and at high voltages and frequencies the associated losses, $\frac{1}{2} C_s V_s^2 f_s$, tend to be high. To reduce this loss, GTOs with an increased SOA, namely GCTs, for use without a turn-off snubber are available. These devices under utilise their voltage and current density capabilities as compared with when a turn-off snubber is used.

While the switching performance of IGBTs and MOSFETs can be enhanced by using the turn-off snubber, it is not a prerequisite for safe, reliable switch operation.

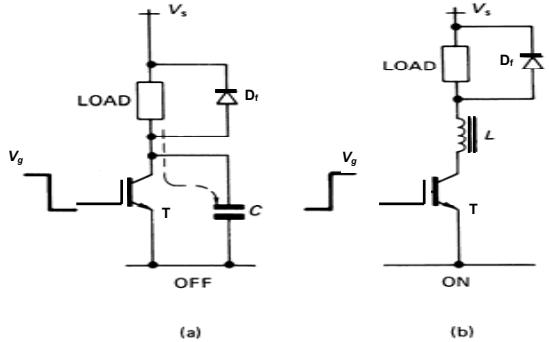


Figure 8.9. *Basic switching-aid circuits comprising:*
(a) a capacitor for current shunting at switch turn-off and
(b) an inductor for limiting the rate of rise of principal current at turn-on.

8.3.1 The turn-off snubber circuit - assuming a linear current fall

Figure 8.10 shows a complete turn-off snubber circuit comprising a capacitor-diode plus resistor combination across the anode-to-cathode/collector-to-emitter terminals of the switching device. At switch turn-off, load current is diverted into the snubber capacitor C via the diode D, while the switch principal current decreases. The anode/collector voltage is clamped to the capacitor voltage, which is initially zero. The larger the capacitor, the slower the anode/collector voltage rises for a given load current and, most importantly, turn-off occurs without a condition of simultaneous supply voltage and maximum load current (V_s,I_m). Figure 8.11 shows the anode/collector turn-off waveforms for different magnitudes of snubber capacitance. The GTO/IGBT tail current has been neglected, thus the switching device is analysed without any tail current. For clarity the terminology to be henceforth used, refers to an IGBT, viz., collector, emitter, and gate.

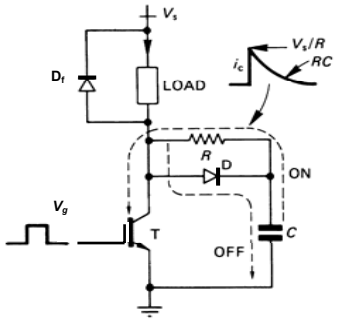


Figure 8.10. *Practical capacitive turn-off snubber showing capacitor charging and discharging paths during device switching.*

Figure 8.11a shows turn-off waveforms for a switch without a snubber, where it has been assumed that the collector voltage rise time is short compared with the collector current fall time, which is given by $i_c(t) = I_m(1 - t/t_{fi})$. For low capacitance values, the snubber capacitor (whence collector) may charge to the rail voltage before the collector current has fallen to zero, as seen in figure 8.11b. For larger capacitance, the collector current reaches zero before the capacitor (whence collector) has charged to the rail voltage level, as shown in figure 8.11c.

For analysis, the collector voltage rise time for an unaided switch is assumed zero. The device switch-off energy losses without a snubber, as shown in figure 8.11a, are given by

$$W = \tfrac{1}{2} V_s I_m t_{fi} \quad \text{(J)} \qquad (8.15)$$

With a snubber circuit, switch losses are decreased as shown in figure 8.11d, but snubber (resistor) losses are incurred. After turn-off the capacitor is charged to the rail voltage. This stored energy, $\tfrac{1}{2} C_s V_s^2$, is subsequently dissipated as heat in the snubber circuit resistor at subsequent switch turn-on, when an *R*-*C* discharge occurs. If the snubber *RC* time constant is significantly shorter than the switch voltage fall time at turn-on, the capacitor energy dissipated in the resistor is less than $\tfrac{1}{2} C_s V_s^2$ and switch losses are increased as considered in 8.1.1. A range of capacitance values exists where the total losses - snubber plus switch - are less than those losses incurred if the same device is switched unaided, when losses as given by equation (8.14) result. Two distinct snubber design cases exist, as indicated by figures 8.11b and 8.11c.

If the snubber capacitor charges fully before the collector current has reached zero then the switch losses are given by

$$W_t = \tfrac{1}{2} V_s I_m t_{fi} \left(1 - \tfrac{1}{3} k + \tfrac{1}{2} k^2\right) \quad \text{(J)} \qquad (8.16)$$

for $k \le 1$, where $k = \tau/t_{fi}$, as defined in figures 8.11b and 8.12.

Alternatively, with larger capacitance, if the snubber capacitor does not charge fully to V_s until after the collector current reaches zero, that is $k \ge 1$, then the switch losses are given by

$$W_t = \tfrac{1}{2} V_s I_m t_{fi} \; \frac{1}{6(2k-1)} \quad \text{(J)} \qquad (8.17)$$

for $k \ge 1$ as defined in figures 8.11c and 8.12. Initially the capacitor voltage increase is quadratic, then when the collector current reaches the load current level, the capacitor voltage increase becomes linear.

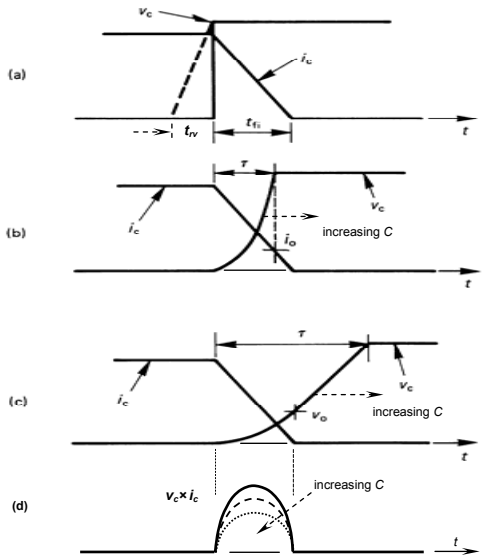


Figure 8.11. *Switch turn-off waveforms:*
(a) unaided turn-off; (b) turn off with small snubber capacitance; (c) turn-off with large snubber capacitance; (d) and reset power losses.

These losses, normalised with respect to the unaided switch losses given by equation (8.15), are plotted in figure 8.12. The switch and capacitor components contributing to the total losses are also shown. A number of important points arise concerning turn-off snubbers and snubber losses.

(a) Because of current tailing, voltage overshoot, and the assumption that the voltage rise time t_{rv} is insignificantly short, practical unaided switch losses, equation (8.14), are approximately twice those indicated by equation (8.15).

(b) As the snubber capacitance increases, that is, k increases, the switch loss is progressively reduced but at the expense of increased snubber associated loss.

(c) If $k \leq 1.41$ the total losses are less than those for an unaided switch. In the practical case $k \leq 2.70$ would yield the same condition.

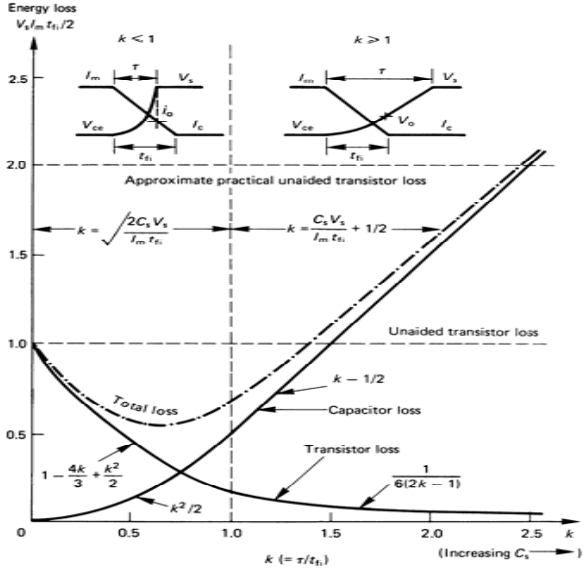


Figure 8.12. *Loss components for a switch at turn-off when employing a capacitance-type snubber and assuming the collector current falls according to* $i_C = I_m(1 - t/t_{fi})$.

(d) A minimum total loss (switch plus capacitor) condition exists. When $k = 2/3$ the total losses are only $5/9$ those of an unaided switch. The snubber capacitance for this condition is given by

$$C_s = \frac{2}{9}\frac{I_m t_{fi}}{V_s} \quad \text{(F)} \tag{8.18}$$

(e) Losses are usually minimised at the maximum loss condition, that is maximum load current I_m. At lower currents, the capacitor charging time is increased.

(f) Snubbers not only reduce total losses, but because the loss is distributed between the switch and resistor, more effective heat dispersion can be achieved.

(g) High switch current occurs at turn-on and incorporates the load current I_m, the snubber capacitor exponential discharge $\frac{V_s}{R}\left(1 - e^{-t/CR}\right)$, and any freewheel diode reverse recovery current.

The capacitor energy $\frac{1}{2}C_s V_s^2$ is removed at turn-on and is exponentially dissipated mainly in the snubber circuit resistor. The power rating of this resistor is dependent on the maximum switching frequency and is given by

$$P_{R_s} = \tfrac{1}{2}C_s V_s^2 f_s \quad \text{(W)} \tag{8.19}$$

Two factors specify the snubber circuit resistance value.

- The snubber circuit RC time constant period must ensure that after turn-on the capacitor discharges before the next turn-off is required. If t'_{on} is the minimum switch on-time, then $t_{on} = 5R_s C_s$, is sufficient to ensure the correct snubber circuit initial conditions, namely, zero capacitor volts.

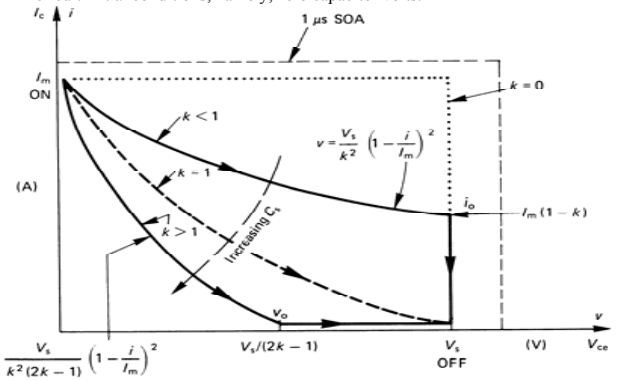


Figure 8.13. *The collector I-V trajectory at turn-off with a switching-aid circuit.*

- The resistor initial current at capacitor discharge is V_s / R_s. This component is added to the load current at switch turn-on, hence adding to the turn-on stresses. The maximum collector current rating must not be exceeded. In order to reduce the initial discharge current, a low valued inductor can be added in series with the resistor, (or a wire-wound resistor used), thus producing an overdamped *L-C-R* discharge current oscillation at turn-on.

As a result of utilising a turn-off snubber the collector trajectory across the SOA is modified as shown in figure 8.13. It is seen that the undesired unaided condition of simultaneous supply voltage V_s and load current I_m is avoided. Typical trajectory conditions for a turn-off snubbered device are shown for three situations, depending on the relative magnitudes of t_{fi} and τ. A brief mathematical derivation describing the turn-off switching-aid circuit action is presented in the appendix in section 8.6 at the end of this chapter.

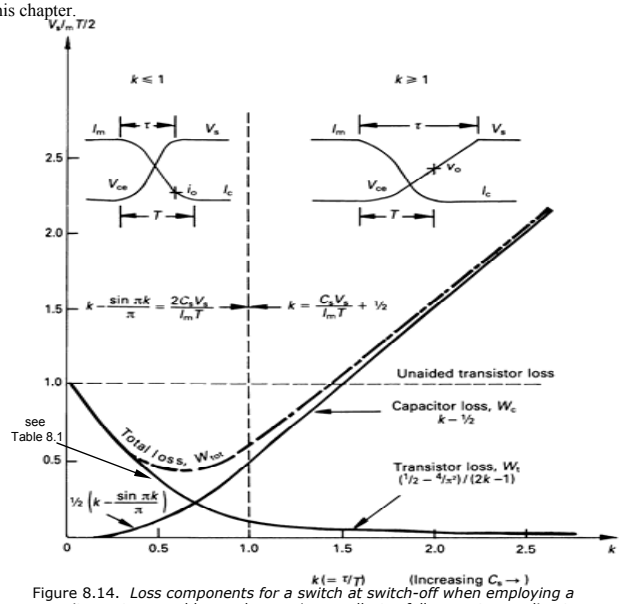


Figure 8.14. *Loss components for a switch at switch-off when employing a capacitance-type snubber and assuming a collector fall current according to* $i_c = \frac{1}{2}I_m\{1 + \cos(\pi t/T)\}$.

Table 8.1. Normalised switching loss components at turn-off with a cosinusoidal current fall of half period T

$\times V_s I_m T/2$	$k = \tau/T \leqslant 1$	$k = \tau/T \geqslant 1$
Switch W_t	$\frac{k^2}{2} + \frac{2}{\pi^2}(\cos \pi k - 1) + \frac{k}{\pi} \sin \pi k - \frac{\sin^2 \pi k}{2\pi^2}$	$\frac{\frac{1}{2} - \frac{4}{\pi^2}}{2k - 1}$
Resistor W_c	$\left(k - \frac{\sin \pi k}{\pi}\right)$ $+ 1 - k - \frac{\sin \pi k}{\pi}$ $\left(k - \frac{\sin \pi k}{\pi}\right)/2$	$k - \frac{1}{2}$
W_{tot}	$W_t + W_c$	$\left(k - \frac{1}{2}\right) + \left(\frac{1}{4} - \frac{2}{\pi^2}\right) / \left(k - \frac{1}{2}\right)$

8.3.2 The turn-off snubber circuit - assuming a cosinusoidal current fall

As an alternative to a linear current fall at turn-off, it may be more realistic to assume that the current falls cosinusoidally according to

$$i_c(t) = \tfrac{1}{2} I_m (1 + \cos \pi t / T) \quad \text{(A)} \qquad (8.20)$$

for $0 \le t \le T$, as shown in figure 8.14.

As with a linear current fall, two cases exist.

(i) $\tau \le T$ ($k \le 1$), that is the snubber capacitor charges to V_s in time τ, before the switch current reaches zero, at time T.

(ii) $\tau \ge T$ ($k \ge 1$), that is the snubber capacitor charges to the supply V_s after the switch current has fallen to zero.

These two cases are shown in figure 8.14 where k is defined as τ / T. Using a similar analysis as presented in the appendix (section 8.6), expressions can be derived for switch and snubber resistor losses. These and the total losses for each case are summarised in table 8.1.

Figure 8.14 shows that a minimum total loss occurs, namely

$$W_{total} = 0.41 \times \tfrac{1}{2} V_s I_m T \quad \text{at} \quad k = 0.62$$

when

$$C_s = 0.16 \frac{I_m T}{V_s} \quad \text{(F)} \qquad (8.21)$$

For $t_{fi} < 0.85T$, a cosinusoidal fall current predicts lower total losses than a linear fall current, with losses shown in figure 8.12.

Example 8.4: ***Turn-off snubber design***

A 600V, 100A machine field winding is switched at 10kHz. The switch operates with an on-state duty cycle ranging between 5% and 95% ($5\% \le \delta \le 95\%$) and has a turn-off linear current fall time of 100ns, that is, $i_c(t) = 100 \times (1 - t/100\text{ns})$.

i. Estimate the turn-off losses in the switch.

ii. Design a capacitive turn-off snubber using the dimensionally correct identity $i=Cdv/dt$. What is the capacitor voltage when the current reaches zero.

iii. Design a capacitive turn-off snubber such that the switch voltage reaches 600V as its conducting current reaches zero.

In each case calculate the percentage decrease in switch turn-off power dissipation.

Solution

i. The switch un-aided turn-off losses are given by equation (8.14). The turn-off time is greater than the current fall time (since the voltage rise time t_{rv} has been neglected), thus the turn-off switching losses will be greater than

$$W_{off} = \tfrac{1}{2} V_s I_m t_{off} = \tfrac{1}{2} \times 600\text{V} \times 100\text{A} \times 100\text{ns} = 3\text{mJ}$$

$$P_{off} = W_{off} \times f_s = 3\text{mJ} \times 10\text{kHz} = 30\text{W}$$

ii. Use of the equation $i=Cdv/dt$ results in a switch voltage that reaches the rail voltage after the collector current has fallen to zero. From $k = \tfrac{1}{2} + C V_s / I_m t_{fi}$ in figure 8.12, k=3/2 satisfies the dimensionally correct capacitor charging equation. Substitution into $i=Cdv/dt$ gives the necessary snubber capacitance

$$100\text{A} = C \frac{600\text{V}}{100\text{ns}}$$

$$\text{that is} \quad C = 16\tfrac{2}{3}\text{nF}$$

Use an 18nF, 1000V dc, metallised polypropylene, high dv/dt capacitor.

The snubber capacitor discharges at switch turn-on, and must discharge during the minimum on-time. That is

$$t_{on} = 5\,CR$$

$$5\% \text{ of } 1/10\text{kHz} = 5 \times R \times 18\text{nF}$$

$$\text{that is} \quad R = 55.5\Omega \quad \text{Use } 56\Omega$$

The discharge resistor power rating is independent of resistance and is given by

$$P_{56\Omega} = \tfrac{1}{2} C V_s^2 f_s$$

$$= \tfrac{1}{2} \times 18\text{nF} \times 600\text{V}^2 \times 10\text{kHz} = 32.4\text{W} \quad \text{Use 50W.}$$

The resistor can be wire-wound, the internal inductance of which reduces the initial peak current when the capacitor discharges at switch turn-on. The maximum discharge current in to the switch during reset, which is added to the 100A load current, is

$$I_{56\Omega} = V_s / R = 600\text{V} / 56\Omega = 10.7\text{A}$$

which decays exponential to zero in five time constants, 5µs. The peak switch current (neglecting freewheel diode recovery) is 100A+10.7A=110.7A, at turn-on.

At switch turn-off, when the switch current reduces to zero, the snubber capacitor has charged to a voltage less than the 600V rail voltage, specifically

$$v_0 = \frac{1}{C} \int i_{cap}\, dt$$

$$= \frac{1}{18\text{nF}} \int_0^{100ns} 100\text{A} \times \left(\frac{t}{100\text{ns}} \right) dt = 277\text{V} \quad (300\text{V with } 16\tfrac{2}{3}\text{nF})$$

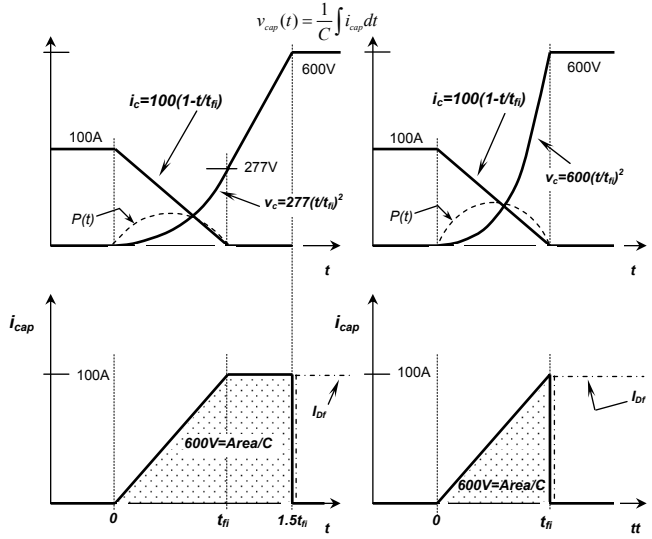
The switch turn-off losses are reduced from 30W to

$$P_{off} = f_s \int_0^{100\text{ns}} i_c v_{ce}\, dt = f_s \int_0^{100\text{ns}} I_m \left(1 - \frac{t}{100\,\text{ns}} \right) \times v_0 \left(\frac{t}{100\text{ns}} \right)^2 dt$$

$$= f_s \int_0^{100\text{ns}} 100\text{A} \left(1 - \frac{t}{100\,\text{ns}} \right) \times 277\text{V} \left(\frac{t}{100\text{ns}} \right)^2 dt = 2.3\text{W}$$

The total turn-off losses (switch plus snubber resistor) are 2.3W+32.4W=34.7W, which is more than the 30W for the unaided switch. Since the voltage rise time has been neglected in calculating the un-aided losses, 34.7W would be expected to be less than the practical un-aided switch losses. The switch losses have been reduced by 92⅓%.

iii. As the current in the switch falls linearly to zero, the capacitor current increases linearly to 100A (k = 1), such that the load current remains constant, 100A. The capacitor voltage increases in a quadratic function according to



Example 8.4. part (b) ***Example 8.4. part (c)***

The capacitor charges quadratically to 600V in 100ns, as its current increases linearly from zero to 100A, that is

$$600\text{V} = \frac{1}{C}\int_0^{100ns} 100\frac{t}{100\text{ns}}dt$$

that is $C = 8\frac{1}{3}$nF

Use a 10nF, 1000V dc, metallised polypropylene, high *dv/dt* capacitor.

The necessary reset resistance to discharge the 10nF capacitor in 5μs is

$$5\mu\text{s} = 5 \times R \times 10\text{nF}$$

that is $R = 100\Omega$

The power dissipated in the reset resistor is

$$P_{100\Omega} = \tfrac{1}{2}CV_s^2 f_s$$
$$= \tfrac{1}{2} \times 10\text{nF} \times 600\text{V}^2 \times 10\text{kHz} = 18\text{W}$$

Use a 100Ω, 25W, wire-wound, 600V dc withstand voltage, metal clad resistor.

The resistance determines the current magnitude and the period over which the capacitor energy is dissipated. The resistance does not determine the amount of energy dissipated. The capacitor exponentially discharges with an initial current of 600V/100Ω = 6A, which adds to the 100A load current at switch turn-on. The peak switch current is therefore 100A+6A = 106A, at turn-on.

The energy dissipated in the switch at turn-off is reduced from 30W when un-aided to

$$P_{off} = f_s \int_0^{100\text{ns}} i_c v_c dt = f_s \int_0^{100\text{ns}} I_m\left(1-\frac{t}{100\text{ns}}\right) \times V_s\left(\frac{t}{100\text{ns}}\right)^2 dt$$
$$= f_s \int_0^{100\text{ns}} 100\text{A}\left(1-\frac{t}{100\text{ns}}\right) \times 600\text{V}\left(\frac{t}{100\text{ns}}\right)^2 dt = 5\text{W}$$

The total losses (switch plus snubber resistor) with a turn-off snubber are 5W+18W =23W, which is less than the 30W for the unaided switch. The switch losses have been decreased by 83⅓%.

Note that the losses predicted by the equations in figure 8.12 amount to 5W+15W =20W. The discrepancy is due to the fact that the preferred value of 10nF (rather that the calculated 8½nF, k =1.2) has been used for the resistor loss calculation.

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8.3.3 The turn-on snubber circuit - with non-saturable (air-core) inductance

A turn-on snubber comprises an inductor-diode combination in the collector circuit as shown in figure 8.15. At turn-on the inductor controls the rate of rise of collector current and supports a portion of the supply voltage while the collector voltage falls. At switch turn-off the energy stored in the inductor, $\frac{1}{2}L_s I_m^2$, is transferred by current through the diode and dissipated in the diode D_s and in the resistance of the inductor.

Figure 8.16 shows collector turn-on waveforms with and without a turn-on snubber circuit. The turn-on losses associated with an unaided switch, figure 8.16a, neglecting the current rise time, are given by

$$W = \tfrac{1}{2}V_s I_m t_{fv} \quad \text{(J)} \qquad (8.22)$$

where it is assumed that the collector current rise time is zero and that the collector voltage falls linearly, according to $v_c(t) = V_s(1 - t/t_{fv})$.

When an inductive turn-on snubber circuit is employed, collector waveforms as in figure 8.16b or 8.16c result. For low inductance the collector current reaches its maximum value I_m before the collector voltage has reached zero. As shown in figure 8.16b, the collector current increases quadratically $i_c(t)=I_m(t/\tau)^2$ and the total turn-on losses (switch plus snubber resistor) are given by

$$W_t = \tfrac{1}{2} V_s I_m t_{fv} \left(k^2 - \tfrac{4}{3}k + 1\right) \quad \text{(J)} \qquad (8.23)$$

for $k \leq 1$, where $k = \tau/t_{fv}$ as defined in figure 8.16. These losses include both switch losses and stored inductor energy subsequently dissipated. For higher snubber inductance, the collector voltage reaches zero before the collector current reaches the load current level. Initially the inductor current increases quadratically $i_{Ls}(t)=i_0(t/t_{fv})^2$, then when the collector voltage has reached zero, the current increases linearly. The total losses are given by

$$W_t = \tfrac{1}{2} V_s I_m t_{fv} \left(k^2 - k + \tfrac{1}{3}\right) \Big/ \left(k - \tfrac{1}{2}\right) \quad \text{(J)} \qquad (8.24)$$

Note that these equations are similar to those for the turn-off snubber, except that the current fall time is replace by the voltage fall time. The normalised loss components for the capacitive snubber in figure 8.12 are valid for the inductive turn-on snubber. Minimum total turn-on losses of 5/9 those of the un-aided case, occur at $k = \tfrac{2}{3}$ when

$$L_s = \frac{2}{9}\frac{V_s t_{fv}}{I_m} \quad \text{(H)} \qquad (8.25)$$

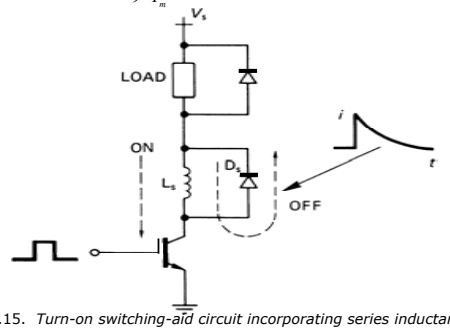


Figure 8.15. *Turn-on switching-aid circuit incorporating series inductance, L_s.*

At switch turn-off, the snubber inductance stored energy is dissipated as heat in the snubber freewheeling diode path. The maximum power loss magnitude is dependent on the operating frequency and is given by

$$P_{L_s} = \tfrac{1}{2} L_s I_m^2 f_s \quad \text{(W)} \qquad (8.26)$$

This power is dissipated in both the inductor winding resistance and freewheeling diode D_s. The resistance in this loop is usually low and therefore a long L/R dissipating time constant may result. The time constant is designed such that $\breve{t}_{off} = 5L_s / R$ where $\breve{t}_{off}$ is the minimum device off-time. The time constant can be reduced either by adding series resistance or a Zener diode as shown in figure 8.17.

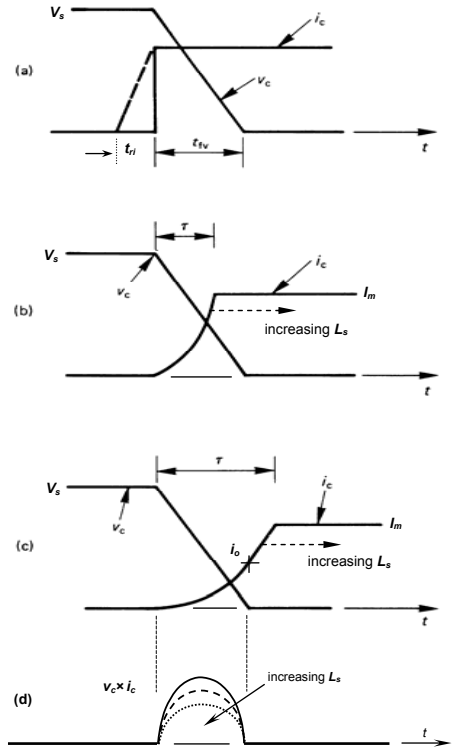


Figure 8.16. *Switch voltage and current collector waveforms at turn-on: (a) without a snubber; (b) and (c) with an inductive snubber; and (d) switch power losses.*

A disadvantage of adding series resistance R as in figure 8.17a is that the switch collector voltage at turn-off is increased from V_s to $V_s + I_m R$. The resistor must also have low self-inductance in order to allow the collector current to rapidly transfer from the switch to the resistor/diode reset circuit. The advantage of using a Zener diode as in figure 8.17b is that the maximum overvoltage is fixed, independent of the load current magnitude. For a given overvoltage, the Zener diode absorbs the inductor-stored energy quicker than would a resistor (see example 6.3 and problem 8.9). The advantages of using resistive dissipation are lower costs and more robust heat dissipation properties.

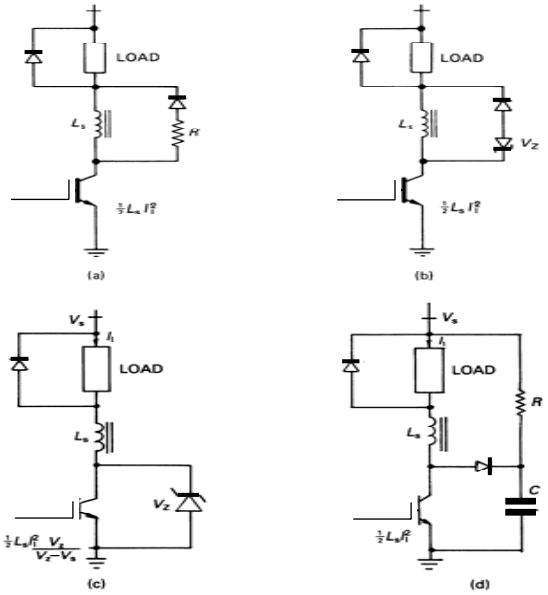


Figure 8.17. *Four turn-on snubber modifications for increasing the rate of release of inductor L_s stored energy: (a) using a power resistor; (b) using a power Zener diode; (c) parallel switch Zener diode, $V_Z > V_s$; and (d) using a soft voltage clamp.*

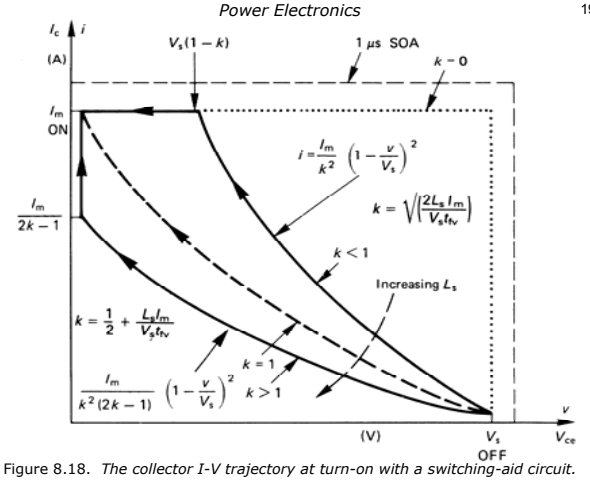


Figure 8.18. *The collector I-V trajectory at turn-on with a switching-aid circuit.*

Alternatively the Zener diode can be placed across the switch as shown in figure 8.17c. The power dissipated is increased because of the energy drawn from the supply, through the inductor, during reset. At higher power, the soft voltage clamp shown in figure 8.17d, and considered in section 8.2, can be used. At switch turn-off, the energy stored in L_s, along with energy from the supply, is transferred and stored in a clamp capacitor. Simultaneously energy is dissipated in R and returned to the supply as the capacitor voltage rises. The advantage of this circuit is that the capacitor affords protection directly across the switch, but with lower loss than a Zener diode as in figure 8.17c. The energy loss equation for each circuit is also shown in figure 8.17. Figure 8.18 shows how a switch turn-on snubber circuit modifies the SOA trajectory during switch-on, avoiding a condition of simultaneous maximum voltage V_s and current I_m.

Example 8.5: ***Turn-on air-core inductor snubber design***

A 600V, 100A machine field winding is switched at 10kHz. The switch operates with an on-state duty cycle between 5% and 95% ($5\% \le \delta \le 95\%$) and has a turn-on voltage fall time of 100ns, that is, $v_c(t) = 600\text{V}(1 - t/100\text{ns})$.

i. Estimate the turn-on losses of the switch.

ii. Design an inductive turn-on snubber using the dimensionally correct identity $v=Ldi/dt$. What is the current magnitude in the turn-on inductor when the switch voltage reaches zero.

iii. Design an inductive turn-on snubber such that the switch current reaches 100A as its supported voltage reaches zero.

In each snubber case, using first a resistor and second a Zener diode for inductor reset, calculate the percentage decrease in switch power dissipation at turn-on.

Solution

i. The switch un-aided turn-on losses are given by equation (8.13). The turn-on time is greater than the voltage fall time (since the current rise time t_{ri} has been neglected), thus the turn-on switching losses will be greater than

$$W_{on} = ½V_s I_m t_{on} = ½ \times 600\text{V} \times 100\text{A} \times 100\text{ns} = 3\text{mJ}$$

$$P_{on} = W_{on} \times f_s = 3\text{mJ} \times 10\text{kHz} = 30\text{W}$$

ii. Use of the equation $v=Ldi/dt$ results in a switch current that reaches the load current magnitude after the collector voltage has fallen to zero. From $k = ½ + L_s I_m / V_s t_{fs}$ in figure 8.18, k=3/2 satisfies the dimensionally correct inductor equation. Substitution into $v=Ldi/dt$ gives the necessary snubber inductance

$$600\text{V} = L\frac{100\text{A}}{100\text{ns}}$$

$$\text{that is} \quad L = 600\text{ nH}$$

The snubber inductor releases its stored energy at switch turn-off, and must discharge during the switch minimum off-time, $\check{t}_{off}$. That is

$$\check{t}_{off} = 5L / R$$

$$5\% \text{ of } 1/10\text{kHz} = 5 \times 0.6\mu\text{H} / R$$

$$\text{that is } R = 0.6\ \Omega$$

Use the preferred value 0.68Ω, which reduces the L/R time constant.

The discharge resistor power rating is independent of resistance and is given by

$$P_{0.68\Omega} = ½LI_m^2 f_s$$

$$= ½ \times 600\text{nH} \times 100\text{A}^2 \times 10\text{kHz} = 30\text{W}$$

The resistor in the circuit in figure 8.17a must have low inductance to minimise voltage overshoot at switch turn-off. Parallel connection of metal oxide resistors may be necessary to fulfil both resistance and power rating requirements. The maximum switch over-voltage at turn-off, (assuming zero resistor inductance), at the commencement of core reset, which is added to the supply voltage, 600V, is

$$V_{0.68\Omega} = I_m R = 100\text{A} \times 0.68\Omega = 68\text{V}$$

which decays exponential to zero volts in five time constants, 5µs. The maximum switch voltage is 600V+68V=668V, at turn-off. The reset resistor should be rated at 0.68Ω, 30W, metal film, 750V dc working voltage.

A Zener diode, as in figure 8.17b, of $V_z = L I_m / \check{t}_{off} = 0.6\mu\text{H} \times 100\text{A}/5\mu\text{s} = 12\text{V}$, will reset the inductor in the same time as 5 L/R time constants. The switch voltage is clamped to 612V during the 5µs inductor reset time at turn-off.

At turn-on when the switch voltage reduces to zero, the snubber inductor current (hence switch current) is less than the load current, 100A, specifically

$$i_0 = \frac{1}{L}\int v_{ind}\,dt$$

$$= \frac{1}{600\text{nH}} \int_0^{100\text{ns}} 600\text{V} \times \left(\frac{t}{100\text{ns}}\right) dt = 50\text{A}$$

The switch turn-on losses are reduced from 30W to

$$P_{on} = f_s \int_0^{100\text{ns}} i_c v_c\,dt = f_s \int_0^{100\text{ns}} V_s \left(1 - \frac{t}{100\,\text{ns}}\right) \times i_0 \left(\frac{t}{100\text{ns}}\right)^2 dt$$

$$= f_s \int_0^{100\text{ns}} 600\text{V} \left(1 - \frac{t}{100\,\text{ns}}\right) \times 50\text{A} \left(\frac{t}{100\text{ns}}\right)^2 dt = 2.5\text{W}$$

The total turn-on losses (switch plus snubber resistor) are 2.5W + 30W = 32.5W, which is more than the 30W for the unaided switch. Since the current rise time t_{ri} has been neglected in calculating the 30W un-aided turn-on losses, it would be expected that 32.5W would be less than the practical un-aided case. The switch losses are decreased by 92⅔%, from 30W down to 2.5W.

iii. As the voltage across the switch falls linearly to zero from 600V, the series inductor voltage increases linearly to 600V (k=1), such that the voltage sum of each component amounts to 600V. The inductor current increases in a quadratic function according to

$$i_{ind}(t) = \frac{1}{L}\int v_{ind}\,dt$$

The inductor current increases quadratically to 100A in 100ns, as its voltage increases linearly from zero to 600V, that is

$$100\text{A} = \frac{1}{L} \int_0^{100ns} 600\text{V} \ \ t/100\text{ns}\,dt$$

$$\text{that is L} = 300\text{nH}$$

The necessary reset resistance to reduce the 300nH inductor current to zero in 5µs is

$$\check{t}_{off} = 5\mu\text{s} = 5 \times 0.3\mu\text{H} / R$$

$$\text{that is } R = 0.3\Omega$$

Use the preferred value 0.33Ω in order to reduce the time constant.

The power dissipated in the 0.33Ω reset resistor is

$$P_{0.33\Omega} = ½LI_m^2 f_s$$

$$= ½ \times 300\text{nH} \times 100\text{A}^2 \times 10\text{kHz} = 15\text{W}$$

The resistance determines the voltage magnitude and the period over which the inductor energy is dissipated, not the amount of inductor energy to be dissipated. The inductor peak reset voltage is 100A×0.33Ω=33V, which is added to the supply voltage

of 600V, giving 633V across the switch at turn-off. That is, use an 0.33Ω, 15W metal film, 750V dc working voltage resistor.

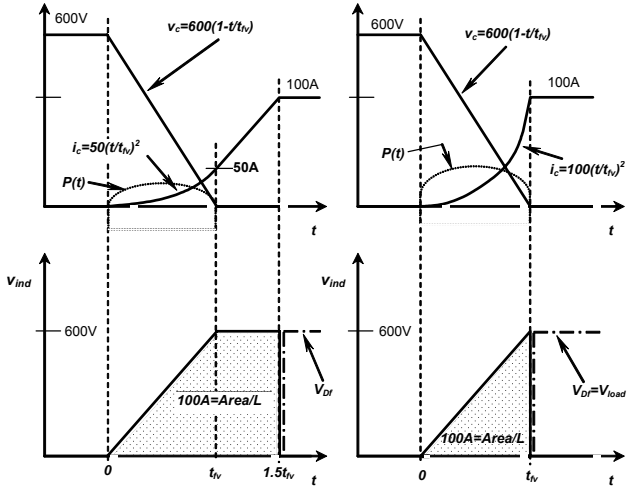
A Zener diode, as in figure 8.17b, of $V_z = L I_m / \breve{t}_{off} = 0.3\mu H \times 100A/5\mu s = 6V$ (use 6.8V), will reset the inductor in the same time as 5 L/R time constants. The switch voltage is clamped to 606.8V during the $\breve{t}_{off} = 5\mu s$ inductor reset time at turn-off.

The energy dissipated in the switch at turn-on is reduced from 30W to

$$P_{on} = f_s \int_0^{100ns} i_c v_c dt = f_s \int_0^{100ns} V_s \left(1 - \frac{t}{100ns}\right) \times I_m \left(\frac{t}{100ns}\right)^2 dt$$

$$= f_s \int_0^{100ns} 600V \left(1 - \frac{t}{100ns}\right) \times 100A \left(\frac{t}{100ns}\right)^2 dt = 5W$$

The total turn-on snubber losses (switch plus snubber resistor) are 5W+15W=20W, which is less than the 30W for the unaided switch. The switch losses, with an inductive turn-on snubber, are decreased by 83⅓%, from 30W to 5W.



Example 8.5. part (b) *Example 8.5. part (c)*

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8.3.4 The turn-on snubber circuit - with saturable ferrite inductance

The purpose of a turn-on snubber circuit is to allow the switch collector voltage to fall to zero while the collector current is low. Device turn-on losses are thus reduced, particularly for inductive loads, where during switching the locus point (V_s, I_m) occurs. This turn-on loss reduction effect can be achieved with a saturable inductor in the circuit shown in figure 8.19a, rather than using a non-saturable (air core) inductor as previously considered in section 8.3.3. The saturable inductor in the snubber circuit is designed to saturate after the collector voltage has fallen to zero, at point **Y** in figure 8.19. Before saturation the saturable inductor presents high reactance and only a low magnetising current flows. From Faraday's equation, assuming the collector voltage fall to be linear, $V_s\left(1 - t/t_{fv}\right)$, the saturable inductor ℓ_s must satisfy

$$v_\ell = N \frac{d\phi}{dt} = NA \frac{dB}{dt} \tag{8.27}$$

Rearranging, using an inductor voltage $v_\ell(t) = V_s - v_c(t) = V_s\, t / t_{fv}$, and integrating gives

$$B_s = \frac{1}{NA} \int_0^{t_{fv}} v_\ell(t)\, dt = \frac{1}{NA} \int_0^{t_{fv}} V_s \frac{t}{t_{fv}} dt \tag{8.28}$$

which yields the following identity

$$V_s = \frac{2NA\, B_s}{t_{fv}} \qquad \text{(V)} \tag{8.29}$$

where N is the number of turns,
A is the core area, and
B_s is the core ferro-magnetic material saturation flux density.

The inductor magnetising current I_M should be much less than the load current magnitude I_m, $I_M << I_m$, and the magnetising current at saturation is given by

$$I_M = H_s L_{eff} / N \qquad \text{(A)} \tag{8.30}$$

where L_{eff} is the core effective flux path length and H_s is the magnetic flux intensity at the onset of saturation. Before core saturation the inductance is given by

$$L = N\Phi / I = N^2 / \Re = \mu_0 \mu_r A N^2 / L_{eff} \qquad \text{(H)} \tag{8.31}$$

When the core saturates the inductance falls to that of an air core inductor (μ_r=1) of the same turns and dimensions, that is, the incremental inductance is

$$L_{sat} = \mu_0 A N^2 / L_{eff} \qquad \text{(H)} \tag{8.32}$$

The energy stored in the inductor core is related to the *B-H* area shown in figure 8.19c and magnetic volume, and is approximated by

$$W_{\ell_s} = ½ B_s H_s A L_{eff} = ½ L I_M^2 \qquad \text{(J)} \tag{8.33}$$

The collector turn-on waveforms are shown in figure 8.19b, while the corresponding *B-H* curve in figure 8.19b that little device turn-on electrical stressing occurs.and SOA trajectories are illustrated in figure 8.19 parts c and d. It will be seen

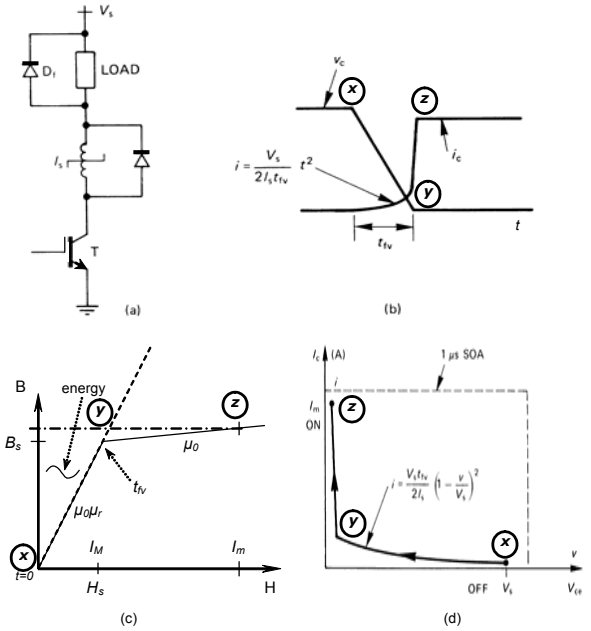


Figure 8.19. *Switch turn-on characteristics when a saturable inductor is used in the turn-on snubber: (a) circuit diagram; (b) collector voltage and current waveforms; (c) magnetic core B-H curve trajectory; and (d) safe operating area I-V turn-on trajectory.*

Example 8.6: ***Turn-on ferrite-core inductor snubber design***

A 600V, 100A machine field winding is switched at 10kHz. The switch operates with an on-state duty cycle between 5% and 95% ($5\% \le \delta \le 95\%$) and has a turn-on voltage fall time of t_{fv}=100ns, that is, $v_c(t) = 600\text{V}(1 - t/100\text{ns})$.

i. Design a saturable inductor turn-on snubber that saturates as the collector voltage reaches zero, using a ferrite core with the following parameters.
   - A = 0.4 sq cm
   - L = 4cm

   - B_s = 0.4T
   - H_s = 100At/m

ii. Calculate the switch losses at turn-on when using the saturable reactor. What is the percentage reduction in switch turn-on losses?

iii. If an air cored inductor is used to give the same switch turn-on loss, what are the losses at reset?

Solution

From *example 8.5*, the unaided switch turn-on loss is 30W.

i. From equation (8.29) the number of turns is

$$N = \tfrac{1}{2} V_s t_{fv} / AB_s$$
$$= \tfrac{1}{2} \times 600\text{V} \times 0.1\mu\text{s} / 0.4 \times 10^{-4} \times 0.4\text{T} \approx 2 \text{ turns}$$

The magnetising current I_M at saturation, that is, when the collector voltages reaches zero, is given by equation (8.30)

$$I_M = H_s L_{eff} / N$$
$$= 100\text{At/m} \times 0.04 / 2 = 2\text{A}$$

Since $I_M << I_m$, (2A<<100A), this core with 2 turns produces satisfactory turn-on snubber action, resulting in greatly reduced switch losses at turn-on.

From equation (8.31) the inductance before saturation is

$$L = NAB_s / I_M$$
$$= 2 \times 0.4 \times 10^{-4} \times 0.4\text{T} / 2\text{A} = 16\mu\text{H}$$

The incremental inductance after saturation, from equation (8.32), is given by

$$L_{sat} = N^2 A \mu_0 / L_{eff}$$
$$= 2^2 \times 0.4 \times 10^{-4} \times 4\pi \times 10^{-7} / 0.04 = 50\text{nH}$$

From equation (8.33) the energy stored in the core and released as heat in the reset resistor is

$$W_L = \tfrac{1}{2} L I_M^2 \quad \left(= \tfrac{1}{2} B_s H_s L_{eff} A\right)$$
$$= \tfrac{1}{2} \times 16\mu\text{H} \times 2^2 = 32\mu\text{J}$$
$$P_L = W_L \times f_s = 32\mu\text{J} \times 10\text{kHz} = 0.32\text{W}$$

The time $\check{t}_{off}$ for core reset via the resistor in five L/R time constants, is dominated by the 16μH section (the pre-saturation section) of the *B-H* curve, thus

$$\check{t}_{off} = 5\mu\text{s} = 5 \times 16\mu\text{H} / R$$

that is $R = 16\Omega$

Use a 15Ω, 1W, carbon composition resistor, for low inductance.

This resistance results in a switch voltage increase above 600V of 15Ω×100A=1500V at turn-off. This high-voltage may be impractical in terms of the switch and resistor voltage ratings.

Alternatively, the Zener diode clamps shown in figures 8.17 b or c, may be suitable to dissipate the 0.32W of stored magnetic energy. The Zener voltage is determined by assuming that a fixed Zener voltage results in a linear decrease in current from 2A to zero in 5µs. That is

$$W_L = V_Z \int_0^{\breve{t}_{off}} i_{ind}\,dt \quad \left(= \tfrac{1}{2} L I_M^2\right)$$

$$32\mu\text{J} = \tfrac{1}{2} \times V_Z \times 2\text{A} \times 5\mu\text{s}$$

$$\text{that is } V_Z = 6.4\text{V}$$

Use a 6.8V, 1W Zener diode.

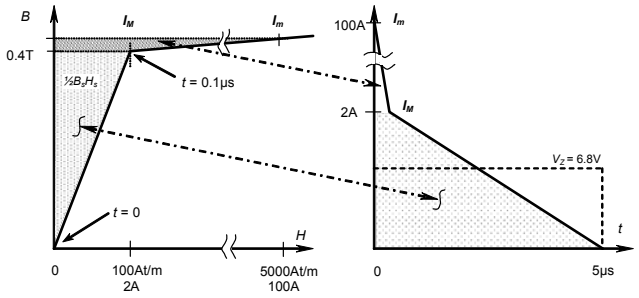
Series connected Zener diodes in parallel with the switch would need to dissipate 30W. The energy associated with saturation is small and is released in an insignificant time compared to the 5µs minimum off-time. The advantage of the Zener diode clamping approach, as opposed to using a resistor, is that the maximum switch voltage is clamped to 606.8V, even during the short, low energy period when the inductor current falls from 100A to 2A.

ii. The switch turn-on losses with the saturable reactor are given by

$$P_{on} = f_s \int_0^{100\text{ns}} i_c v_c\,dt = f_s \int_0^{100\text{ns}} V_s \left(1 - \frac{t}{100\text{ns}}\right) \times I_M \left(\frac{t}{100\text{ns}}\right)^2 dt$$

$$= f_s \int_0^{100\text{ns}} 600\text{V} \left(1 - \frac{t}{100\text{ns}}\right) \times 2\text{A} \left(\frac{t}{100\text{ns}}\right)^2 dt = 0.1\text{W}$$

The switch losses at turn-on have been reduced from 30W to 0.1W, a 99⅔% decrease in losses. The total losses (switch plus Zener diode) are 0.1W+0.32W=0.42W, which is significantly less than the 30W in the un-aided case.



Example 8.6

iii. If an air core inductor of 16µH were to replace the saturable reactor, the stored energy released would give losses

$$W = \tfrac{1}{2} L I_m^2$$

$$= \tfrac{1}{2} \times 16\mu\text{H} \times 100^2 = 80\text{mJ}$$

$$P = W \times f_s = 80\text{mJ} \times 10\text{kHz} = 800\text{W}$$

Clearly the use of an air cored inductor rather than a saturable reactor, to achieve the same switch loss of 0.1W at turn-on, is impractical.

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8.3.5 The unified snubber circuit

Figure 8.20 shows a switching circuit which incorporates both a turn-on and turn-off snubber circuit. Both C_s and L_s are dimensioned by the analysis outlined in sections 8.3.1 and 8.3.3, respectively. The power rating of the dissipating resistor R incorporates a contribution from both the turn-on inductor L_s and turn-off capacitor C_s, according to

$$P_{R_s} = \tfrac{1}{2}\left(L_s I_m^2 + C_s V_s^2\right) f_s \qquad \text{(W)} \qquad (8.34)$$

Calculated resistance values to satisfy minimum off and on time reset according to $\breve{t}_{on} \geq 5 R_s C_s$ and $\breve{t}_{off} \geq 5 L_s / R_s$, may result in irreconcilable resistance requirements. The snubber capacitor discharges at turn-on via an *L-C-R* circuit rather than the usual *R-C* circuit, hence reducing the turn-on current stressing of the switch.

An important by-product from using a turn-on snubber circuit is that the inductor controls the reverse recovery process of the load freewheeling diode at switch turn-on.

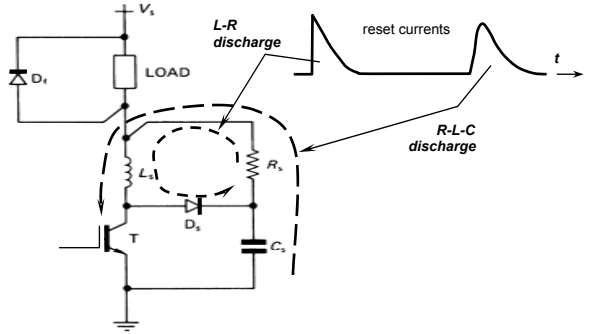

Figure 8.20. *Unified snubber incorporating both a turn-on and a turn-off circuit which share the one dissipation reset resistor.*

8.4 Snubbers for bridge legs

Figure 8.21 shows three typical switch bridge leg configurations used in inverters as shown in figures 14.1 and 14.3. The inductive turn-on snubber L and capacitive turn-off snubber C_s are incorporated into the bridge legs as shown in each circuit in figure 8.21.

The combinational snubber circuit in figure 8.21a can be used to minimise the number of snubber components. The turn-on snubber inductance L_s, reset resistor R, and snubber capacitor C_{sc}, are common to any number of bridge legs. The major disadvantage of this circuit is that turn-off snubber action associated with the lower switch is indirect, relying on low inductance decoupling through C_s and C_{sc}.

With an inductive load, unwanted turn-off snubber action occurs during the switch modulation sequence as shown in figures 8.21b and 8.21c. When the upper switch T_u is turned off as in figure 8.21b the load current I_m is diverted to the freewheel diode D_f. While D_f conducts the capacitor C, discharges to zero through the resistor R, as shown, dissipating energy $\frac{1}{2}C_sV_s^2$. When the switch T_u is turned on, the load current is provided via the switch T_u and the snubber capacitor C_s is charged through the series turn-on snubber inductance, as shown in figure 8.21c. A lightly damped L-C oscillation occurs and C_s is over charged. Advantageously, the recovery voltage of the freewheel diode D_f is controlled by the capacitor voltage rise.

The unwanted snubber action across the non-power conducting switch can be avoided in some applications by using a series blocking diode as shown in figure 8.21d. The diode D_b prevents C_s from discharging into the load as occurs with the lower switch in figure 8.21b. A blocking diode can be used to effectively disable the internal parasitic diode of the MOSFET. Adversely, the blocking diode increases the on-state losses.

In reactive load applications, bridge legs are operated with one switch on, with only a short underlap when both switches are off. Thus although the snubber capacitor cannot discharge into the load in figure 8.21d, it always discharges through the switch T, regardless of load current flow through the switch.

In IGBT and MOSFET applications, the conventional R-C-D turn-off snubber is not usually required. But because of diode recovery limitations, a turn-on snubber may be necessary. In low frequency applications, a single turn-on snubber inductor can be used in the dc link as shown in figure 8.22a. Snubber circuit design is based on the turn-on snubber presented in 8.3.3. The circuit in figure 8.22b is based on the conventional turn-on snubber being incorporated within the bridge leg. Figures 8.22c and d show turn-on snubbers which use the soft voltage clamp, presented in 8.2, to reset the snubber inductor current to zero at turn-off.

In each circuit at switch turn-off, t_3, the energy $\frac{1}{2}LI_m^2$ stored in the turn-on snubber inductor is dissipated in the resistor of the discharge circuit. The energy $\frac{1}{2}LI_{rm}^2$ in L, due to diode recovery, is dissipated in the resistor at time t_1, in circuits (a), (b) and (c). In figure 8.22d the energy in excess of that associated with the load, $\frac{1}{2}LI_m^2$, due to diode recovery, is dissipated in the switch and its parallel connected diode. At time t_1

$$W = \tfrac{1}{2}LI_{rm}^2 + \frac{V_{ce}}{V_{ce}+V_{Df}}LI_{rm}I_m \tag{8.35}$$

is dissipated in the two semiconductor components. Since the energy is released into a low voltage $v_{ce} + v_{Df}$, the reset time $t_2 - t_1$ is large.

Coupling of the inductors in figures 8.22c and d does not result in any net energy savings.

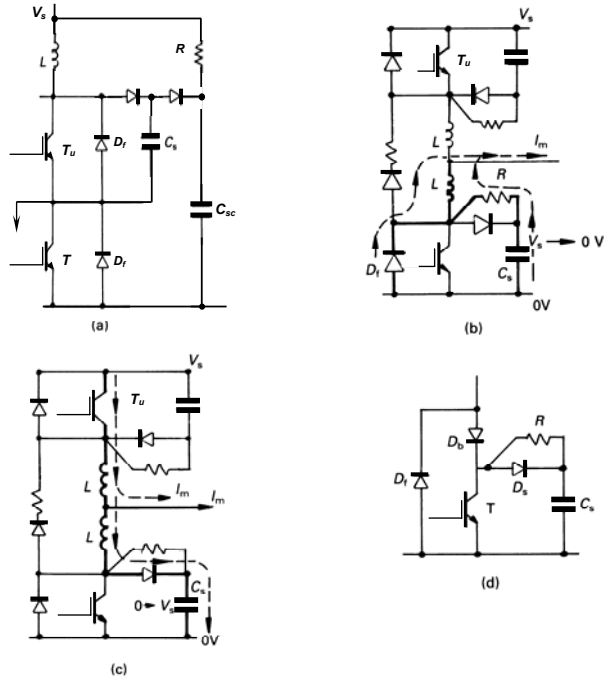

Figure 8.21. *Bridge leg configurations: (a) Undeland leg snubber circuit; (b) leg with turn-on snubber and turn-off snubber C_s discharge path shown; (c) L-C oscillation at switch-on; and (d) blocking circuit to prevent snubber capacitor discharge when D_f conducts.*

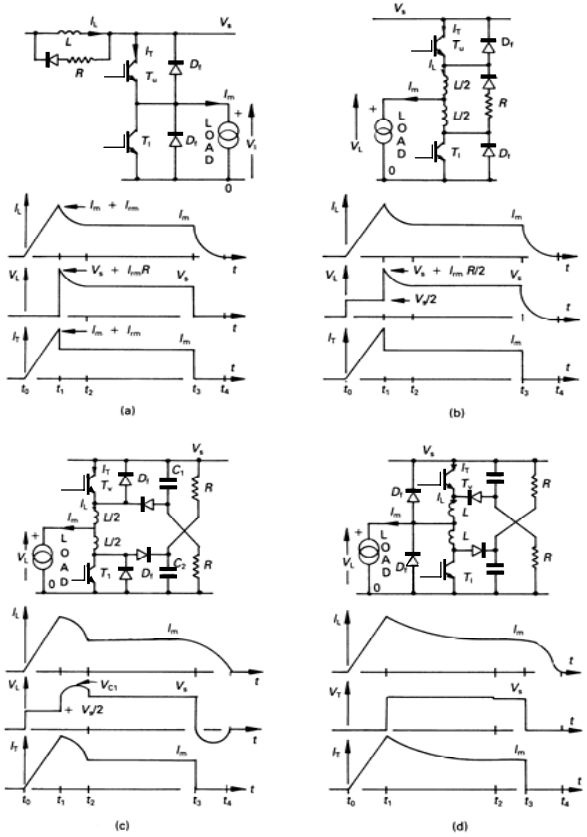

Figure 8.22. *Turn-on snubbers for bridge legs: (a) single inductor in dc link; (b) unified L-R-D snubber; (c) soft voltage clamp; and (d) soft voltage clamp with load clamped.*

8.5 Appendix: Turn-off *R-C* snubber circuit analysis

When a step input voltage is applied to the *L-C-R* circuit in figure 8.3, a ramped voltage appears across the *R-C* part of the circuit. If this *dv/dt* is too large, a thyristor in the off-state will turn on as a result of the induced central junction displacement current, which causes injection from the outer junctions.
The differential equations describing circuit current operation are

$$(D^2 + 2\xi_0 D + \omega_0^2)\, I = 0 \qquad (8.36)$$

and

$$(\tau D + 1)I = CDe_0 \qquad (8.37)$$

where D = differential operator = d/dt
and ξ = damping ratio = $\frac{1}{2}R\sqrt{C/L}$
ω_0 = natural frequency = $1/\sqrt{LC}$
ω = oscillation frequency = $\omega_0\sqrt{1-\xi^2}$

Solution of equations (8.36) and (8.37), for $I_o = 0$, leads to
(a) The snubber current

$$I(t) = \frac{e_s}{R}\frac{2\xi}{\sqrt{1-\xi^2}}\, e^{-\xi\omega_0 t} \sin \omega t \quad \text{(A)} \qquad (8.38)$$

(b) The rate of change of snubber current

$$\frac{dI}{dt} = \frac{e_s}{L}\, e^{-\xi\omega_0 t}\left(\cos \omega t - \frac{\xi}{\sqrt{1-\xi^2}} \sin \omega t\right) \quad \text{(A/s)} \qquad (8.39)$$

(c) Snubber *R-C* voltage

$$e_0 = e_s\left(1 - e^{-\xi\omega_0 t} \cos \omega t - \frac{\xi}{\sqrt{1-\xi^2}} \sin \omega t\right) \quad \text{(V)} \qquad (8.40)$$

(d) The rate of change of *R-C* voltage

$$\frac{de_0}{dt} = \omega_0 e_s\, e^{-\xi\omega_0 t}\left(2\xi \cos \omega t + \frac{1-2\xi}{\sqrt{1-\xi^2}} \sin \omega t\right) \quad \text{(V/s)} \qquad (8.41)$$

The maximum value expressions for each equation can be found by differentiation
(a) Maximum snubber current

$$I_p = \frac{e_s}{R}\, 2\xi\, e^{\left(-\xi\cos^{-1}\xi/\sqrt{1-\xi^2}\right)} \quad \text{(A)} \qquad (8.42)$$

when $\cos \omega t = \xi$

(b) The maximum snubber *di/dt* is given by

$$\frac{dI_p}{dt} = \frac{e_s - e_0}{L} \quad \text{(A/s)} \qquad (8.43)$$

(c) Maximum *R-C* voltage

$$\hat{e}_o = e_s\left(1 + e^{\left(-\xi\cos^{-1}\xi \Big/ \sqrt{1-\xi^2}\right)}\right) \quad \text{(V)} \qquad (8.44)$$

when $\cos \omega t = 2\xi^2 - 1$

(d) Maximum slew rate, $\frac{de_0}{dt} = \hat{S}$

for $\xi < ½$

$$\hat{S} = e_0\omega_0 e^{\left(-\xi\cos^{-1}\xi\left(3-4\xi^2\right) \Big/ \sqrt{1-\xi^2}\right)} \quad \text{(V/s)} \qquad (8.45)$$

when $\cos \omega = \xi(3-4\xi^2)$

for $\xi > ½$

$$\hat{S} = 2\xi e_s w_0 \quad (= e_s R/L) \quad \text{(V/s)} \qquad (8.46)$$

when $t = 0$

Equations (8.42) to (8.46), after normalisation are shown plotted in figure 8.4 as a function of the snubber circuit damping factor ξ. The power dissipated in the resistor is approximately $Ce_s^2 f_s$.

8.6 Appendix: Turn-off *R-C-D* switching aid circuit analysis

Switch turn-off losses for an unaided switch, assuming the collector voltage rise time is negligible compared with the collector current fall time, are

$$W = ½V_s I_m t_{fi} \qquad (8.47)$$

If τ is the time in figure 8.11 for the snubber capacitor C_s to charge to the supply V_s, and t_{fi} is the switch collector current fall time, assumed linear such that $i_c(t) = I_m(1-t/t_{fi})$, then two capacitor charging conditions can exist

- $\tau \le t_{fi}$
- $\tau \ge t_{fi}$

Let $k = \tau/t_{fi}$ and electrical energy $W = \int_0^t vi\,dt$

Case 1: $\tau \le t_{fi}$, $k \le 1$

Figure 8.11b shows ideal collector voltage and current waveforms during aided turn-off for the condition $t \le t_{fi}$. If, assuming constant maximum load current, I_m, the collector current falls linearly, then the load deficit, $I_m t/t_{fi}$, charges the capacitor C_s, whose voltage therefore increases quadratically. The collector voltage v_c and current i_c are

given by

$$\begin{bmatrix} i_c(t) = I_m(1-\frac{t}{t_{fi}}) \\ v_c(t) = V_s\left(\frac{t}{\tau}\right)^2 \end{bmatrix},\ 0 \le t \le \tau \quad \text{and} \quad \begin{bmatrix} i_c(t) = I_m(1-\frac{t}{t_{fi}}) \\ v_c(t) = V_s \end{bmatrix},\ 0 \le t \le t_{fi} \qquad (8.48)$$

The final capacitor charge is given by

$$Q = C_s V_s = \int_0^\tau (I_m - i_c(t))dt = ½I_m t_{fi} k^2 \quad \text{(C)} \qquad (8.49)$$

The energy stored by the capacitor, W_c, and lost in the switch, W_t, are given by

$$\begin{aligned} W_c &= ½C_s V_s^2 \quad (= ½QV_s) \\ &= ½V_s I_m t_{fi} \times ½k^2 \quad \text{(J)} \end{aligned} \qquad (8.50)$$

$$\begin{aligned} W_t &= \int_0^\tau V_s I_m(t/\tau)dt + \int_0^{t_{fi}} V_s I_m(1-t/t_{fi})dt \\ &= ½V_s I_m t_{fi}\left(1 - ⅔k + ½k^2\right) \quad \text{(J)} \end{aligned} \qquad (8.51)$$

Case 2: $\tau \ge t_{fi}$, $k \ge 1$

Figure 8.11c shows the ideal collector voltage and current switch-off waveforms for the case when $k \ge 1$. When the collector current falls to zero the snubber capacitor has charged to a voltage, v_0, where

$$\begin{aligned} v_o &= \frac{1}{C_s}\int_0^{t_{fi}} i\,dt \\ &= \frac{1}{C_s} \times ½I_m t_{fi} \quad \text{(V)} \end{aligned} \qquad (8.52)$$

The collector voltage v_c and current i_c are given by

$$\begin{bmatrix} i_c(t) = I_m(1-\frac{t}{t_{fi}}) \\ v_c(t) = V_s\left(\frac{t}{t_{fi}}\right)^2 \end{bmatrix},\ 0 \le t \le t_{fi} \text{ and } \begin{bmatrix} i_c(t) = 0 \\ v_c(t) = \frac{1}{t_{fi}}\frac{(V_s - v_0)t}{k-1} + \frac{kv_0 - V_s}{k-1} \end{bmatrix},\ t_{fi} \le t \le \tau \qquad (8.53)$$

The final capacitor charge is given by

$$\begin{aligned} Q = C_s V_s &= \int_0^{t_{fi}} (I_m - i_c(t))dt + \int_{t_{fi}}^\tau I_m\,dt \\ &= I_m t_{fi}\left(k - ½\right) \quad \text{(C)} \end{aligned} \qquad (8.54)$$

The energy stored by the capacitor W_c, and lost in the switch W_t, are given by

$$\begin{aligned} W_c &= \tfrac{1}{2}C_s V_s^2 \quad (=\tfrac{1}{2}QV_s) \\ &= \tfrac{1}{2}V_s I_m t_{fi} \times (k - \tfrac{1}{2}) \quad \text{(J)} \\ W_t &= \int_0^{t_{fi}} v_0 I_m (1 - t/t_{fi})(t/t_{fi})^2 \, dt \\ &= \tfrac{1}{12} v_0 I_m t_{fi} \quad \text{(J)} \end{aligned} \tag{8.55}$$

Using equations (8.52) and (8.54) to eliminate v_0 yields

$$W_t = \tfrac{1}{2}V_s I_m t_{fi} \times \frac{1}{6(2k-1)} \quad \text{(J)} \tag{8.56}$$

The total circuit losses W_{tot}, are

$$\begin{aligned} W_{total} &= W_t + W_c \\ W_{total} &= \tfrac{1}{2}V_s I_m t_{fi} \times (1 - \tfrac{1}{3}k + \tfrac{1}{2}k^2), \ k \le 1 \quad \text{(J)} \\ W_{total} &= \tfrac{1}{2}V_s I_m t_{fi} \times \frac{(k^2 - k + \tfrac{1}{3})}{(k - \tfrac{1}{2})}, \quad k \ge 1 \quad \text{(J)} \end{aligned} \tag{8.57}$$

The equations (8.50), (8.51), and (8.55) to (8.57) have been plotted, normalised, in figure 8.12.

Reading list

International Rectifier, *HEXFET Data Book,*
HDB-5, 1987.

Peter, J. M., *The Power Transistor in its Environment,*
Thomson-CSF, Sescosem, 1978.

Siliconix Inc., *Mospower Design Catalog,*
January 1983.

Graffiam, D. R. *et al., SCR Manual,*
General Electric Company, 6th Edition, 1979.

Problems

8.1. The figure 8.23 shows GTO thyristor turn-off anode *I-V* characteristics. Calculate

i. turn-off power loss at 1 kHz. What percentage of the total loss does the tail current account for?

ii. losses when a capacitive turn-off snubber is used and the anode voltage rises quadratically to 600V in 0.5µs. What percentage of the total losses does the tail current account for? What is the necessary capacitance?

iii. losses when a capacitive turn-off snubber is used and the anode voltage rises quadratically to 600V in 2µs. What percentage of the total losses does the tail current account for? What is the necessary capacitance?

[10.5 W]

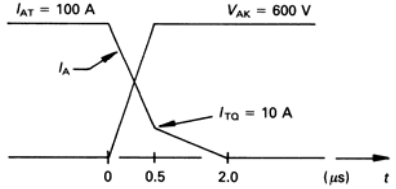

Figure 8.23. *Problem 8.1, GTO thyristor tail current characteristics.*

8.2. Prove that the minimum total losses (switch plus snubber resistor), associated with a switch which utilises a capacitive turn-off switching-aid circuit, occur if the snubber capacitor is fully charged when the collector current has fallen to ⅓ its original value. Derive an expression for this optimal snubber capacitance.

$$C_s = \tfrac{2}{9}\frac{I_m t_{fi}}{V_s} \quad \text{(F)}$$

8.3. Derive an expression for the optimal turn-on switching-aid circuit inductance, assuming the collector current rise time in the unaided circuit is very short compared with the collector voltage fall time.

$$L_s = \tfrac{2}{9}\frac{V_s t_{fv}}{I_m} \quad \text{(H)}$$

8.4. A ferrite toroid has *B-H* characteristics as shown in figure 8.24 and a cross-sectional area, *A,* of 10 mm^2 and effective length, L_{eff} of 50 mm.

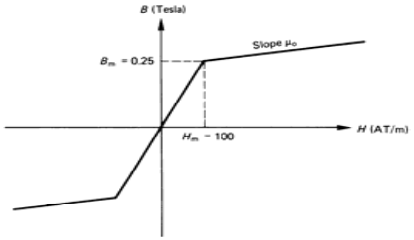

Figure 8.24. *Problem 8.4, B-H characteristics.*

A number of such toroid cores are to be stacked to form a core for a saturable inductor turn-on snubber in a switching circuit. The circuit supply voltage is V and the switch voltage fall time at turn-on is t_{fv}. Assume t_{fv} is independent of supply voltage and falls linearly from V to 0 V.

i. Using Faraday's Law, show that if the ferrite inductor is to saturate just as the switch collector voltage falls to zero at turn-on, then the number of turns N for n cores is given by

$$N = \frac{Vt_{fv}}{2B_m An}$$

ii. Derive an expression for the inductance before saturation.

iii. It is required that the maximum magnetising current before saturation does not exceed 1 A. If only 10 turns can be accommodated through the core window, what is the minimum number of cores required if V = 200 V and t_{fv} = 1 μs?

iv. How many cores are required if the supply V is increased to the peak voltage of the three-phase rectified 415 V ac mains, and the load power requirements are the same as in part (c)?

v. Calculate the percentage change in the non-saturated inductance between parts iii and iv.

vi. What are the advantages of saturable inductance over linear non-saturable inductance in turn-on snubber applications? What happens to the inductance and stored energy after saturation?

[$\ell = N^2/R$, n =5, n =4, 1:9]

8.5. Prove, for an inductive turn-on snubber, where the voltage fall is assumed linear with time, that

$$k = \sqrt{\frac{2L_s I_m}{V_s t_{fv}}} \quad \text{for } k \geq 1$$

$$k = \frac{L_s I_m}{V_s t_{fv}} + \tfrac{1}{2} \quad \text{for } k \leq 1$$

where $k = t_{fv}/\tau$ (see figures 8.16 and 8.18).

8.6. Derive the expressions in table 8.1 for a turn-off snubber assuming a cosinusoidal current fall. Prove equation (8.21), the optimal capacitance value.

8.7 Show that when designing a capacitive turn-off snubber using the dimensionally correct equation $i = Cdv/dt$, as in example 8.4b, the capacitor charges to $\frac{1}{2}V_s$ when the switch current reaches zero.

8.8 Show that when designing an inductive turn-on snubber using the dimensionally correct equation $v = Ldi/dt$, as in example 8.5b, the inductor current reaches $\frac{1}{2}I_m$ when the switch voltage reaches zero.

8.9 Reset of inductive turn-on snubber energy $\frac{1}{2}L_s I_m^2$ can be effected through a resistor, R, as in figure 8.17a or through a Zener diode, D_z, as in figure 8.17b.
Show that for the same reset voltage, namely $V_z = I_m R$, in each case, Zener diode reset is n times faster the resistor reset when $nR_s C_s \leq \check{t}_{on}$.

9

Switching-aid Circuits with Energy Recovery

Turn-on and turn-off snubber circuits for the IGBT transistor and the GTO thyristor have been considered in chapter 7. These snubber circuits modify the device *I-V* switching trajectory and in so doing reduce the device transient losses. Snubber circuit action involves temporary energy stored in either an inductor or capacitor. In resetting these passive components it is usual to dissipate the stored energy in a resistor as heat. At high frequencies these losses may become a limiting factor because of the difficulties associated with equipment cooling. Instead of dissipating the switching-aid circuit stored energy, it may be viable to recover the energy either back into the supply or into the load. Two classifications of energy recovery circuits exist, either passive or active. A passive recovery circuit involves only passive components such as *L* and *C* while active recovery techniques involve switching devices, as in a switched-mode power supply.

9.1 Energy recovery for turn-on snubber circuits

Figure 9.1 shows the conventional turn-on snubber circuit for a simple IGBT transistor switching circuit. Equally the switch may be a GTO thyristor or a GCT, for which an inductive turn-on snubber is mandatory.
At switch turn-on the snubber inductance controls the rate of rise of current as the collector voltage falls to zero. The switch turns on without the stressful condition of simultaneous maximum voltage and current being experienced. At turn-off the inductor current is diverted through the diode and resistor network and the stored inductor energy $\frac{1}{2}LI^2$ is dissipated in the resistance of the *L-R-D* circuit as heat. The power loss is determined by the switching frequency and is given by $\frac{1}{2}LI^2f_s$. Full design and operational aspects have been considered in section 8.3.3.

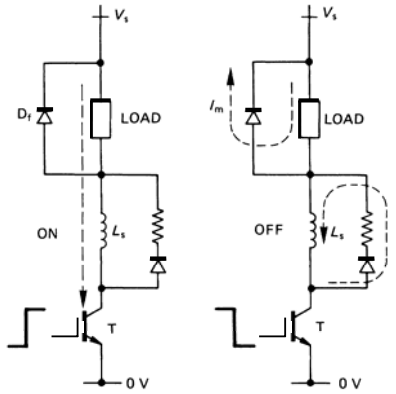

Figure 9.1. *Conventional inductive turn-on snubber principal currents at: (a) turn-on and (b) turn-off.*

9.1.1 Passive recovery

Figure 9.2 shows a simple passive technique for recovering the turn-on snubber stored energy back into the supply. The inductor is bifilar-wound with a catch winding. The primary winding is designed to give the required inductance based on core dimensions, properties, and number of turns. At switch turn-off the current in the coupled inductor primary is diverted to the secondary so as to maintain core flux. The windings are arranged so that the transferred current flows back into the supply via a diode which prevents reverse current flow.
The operating principles of this turn-on snubber recovery scheme are simple but a number of important circuit characteristics are exhibited. Let the coupled inductor have a primary-to-secondary turns ratio of 1:*N*. At turn-off the catch winding conducts and is thereby clamped to the supply rail V_s. The primary winding therefore has an induced voltage specified by the turns ratio. That is

$$V_{tp} = \frac{1}{N}V_s \quad \text{(V)} \tag{9.1}$$

The switch collector voltage at turn-off is increased by this component, to

$$V_c = \left(1+\frac{1}{N}\right)V_s \quad \text{(V)} \tag{9.2}$$

The turns ratio *N* should be large so as to minimise the switch voltage rating.

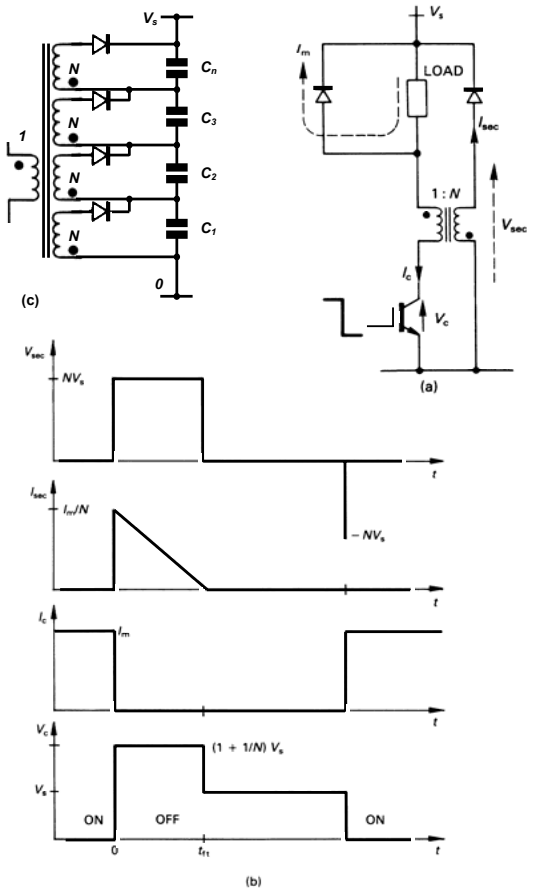

Figure 9.2. *Turn-on snubber with snubber energy recovery via a catch winding: (a) circuit diagram; (b) circuit waveforms; and (c) multilevel recovery.*

At turn-on the inductor supports the full rail voltage and, by transformer action, the induced secondary voltage is NV_s. The reverse-blocking voltage seen by the secondary blocking diode is

$$V_c = (1+N)V_s \quad \text{(V)} \qquad (9.3)$$

Thus by decreasing the switch voltage requirement with large N, the blocking diode reverse voltage rating is increased, and vice versa when N is decreased.

One further design compromise involving the turns ratio is necessary. The higher the effective pull-down voltage, the quicker the stored energy is returned to the supply. The secondary voltage during the recovery is fixed at V_s; hence from $v = L\,di/dt$ the current will decrease linearly from I_m/N to zero in time t_{fi}. By equating the magnetically stored energy with the energy pumped back to the rail

$$\tfrac{1}{2}L_p I_m^2 = V_s \frac{I_m}{N} \tfrac{1}{2} t_{fi} \quad \text{(J)} \qquad (9.4)$$

the core reset time, that is the time for the core energy to be returned to the supply, is given by

$$t_{fi} = L_p \frac{I_m}{V_s} N \quad \text{(s)} \qquad (9.5)$$

Thus the lower the turns ratio N, the shorter the core reset time and the higher the upper switching frequency limit. This analysis assumes that the collector current fall time is short compared with the core reset time.

Primary leakage inductance results in a small portion of the core stored energy remaining at turn-off. This energy, in the form of primary current, can usually be absorbed by the turn-off snubber circuit across the switch.

Figure 11.2c shows a recovery arrangement with multiple secondary windings, for a multilevel inverter. The reflected voltage, $(1+N/n)V_s$, on to the switch is significantly reduced as the number of secondary windings, n, increases. Auto balancing and regulation of the capacitor voltages is achieved since only the lowest charged capacitor has energy transferred to it.

9.1.2 Active recovery

Figure 9.3 shows an inductive turn-on snubber energy recovery scheme which utilises a switched-mode power supply (smps) based on the boost converter in 15.4, as shown in figure 9.4a.

At switch turn-off the energy stored in the snubber inductor L_s is transferred to the storage capacitor C via the blocking diode, D_b. The smps is then used to convert the relatively low capacitor voltage into a higher voltage suitable for feeding energy back into a supply. The capacitor charging rate is dependent on load current magnitude. The smps can be controlled so as to maintain the capacitor voltage constant, thereby fixing the maximum switch collector off-state voltage, or varied with current so as to maintain a constant snubber inductor reset time. One smps and storage capacitor can be utilised by a number of switching circuits, each with a blocking diode as indicated in figure 9.3. The diode and switch are rated at $V_s + V_{Co}$.

If the load and turn-on snubber are re-arranged to be in the cathode circuit, then the smps in figure 9.4b can be used to recover the snubber energy from capacitor C_o.

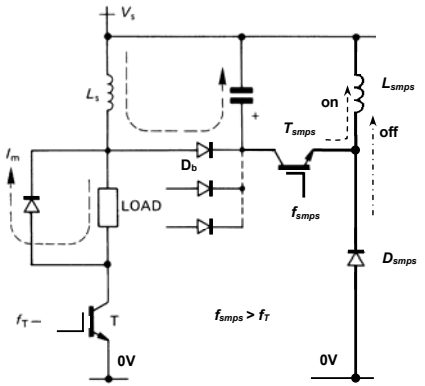

Figure 9.3. *Turn-on snubber with active snubber inductor energy recovery.*

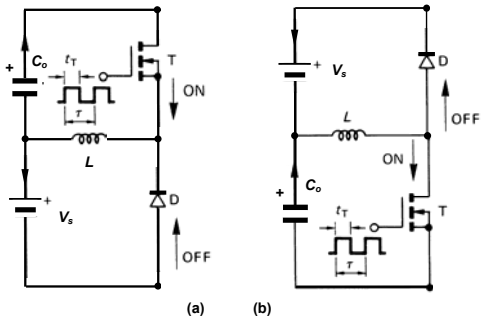

Figure 9.4. *Underlying energy recovery circuits for when energy in C_o is stored: (a) above V_s and (b) below 0V.*

9.2 Energy recovery for turn-off snubber circuits

Figure 9.5 shows the conventional turn-off snubber circuit used with both the GTO thyristor and the IGBT transistor. At turn-off, collector current is diverted into the snubber capacitor *C* via D. The switch turns off clamped to the capacitor voltage which increases quadratically from zero. At the subsequent switch turn-on the energy stored in *C*, $\frac{1}{2}CV_s^2$ is dissipated as heat, mainly in the resistor *R*. A full functional description and design procedure for the turn-off snubber circuit is to be found in section 8.3.1.

At high voltages and switching frequencies, with slow switching devices, snubber losses ($\frac{1}{2}CV_s^2 f_s$) may be too high to be dissipated easily. An alternative is to recover this energy, using either passive or active recovery techniques.

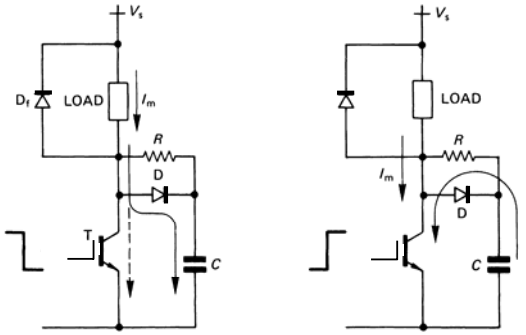

Figure 9.5. *Conventional capacitive turn-off snubber showing currents at: (a) turn-off and (b) IGBT transistor turn-on.*

9.2.1 Passive recovery

Figure 9.6 illustrates a passive, lossless, turn-off snubber energy recovery scheme which dumps the snubber energy, $\frac{1}{2}CV_s^2 f_s$, into the load. The turn-off protection is that of the conventional capacitive snubber circuit. At turn-off the snubber capacitor C_s charges to the voltage rail V_s as shown in figure 9.7a.

At subsequent switch turn-on, the load current diverts from the freewheeling diode to the switch. Simultaneously the snubber capacitor resonates its charge to capacitor C_o through the path shown in figure 9.7b.

When the switch next turns off, the snubber capacitor C_s charges and the capacitor C_o discharges into the load. When C_o is discharged the freewheeling diode conducts. During turn-off C_o and C_s act effectively in parallel across the switching device.

A convenient starting point for the analysis of the recovery scheme is at switch turn-on when snubber energy is transferred from C_s to C_o. The active portions of figure 9.7b are shown in figure 9.8a.

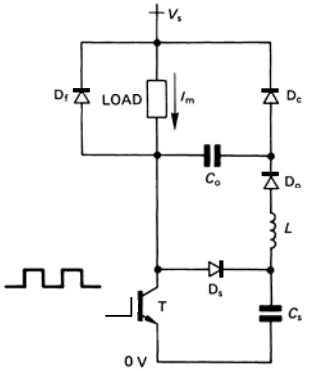

Figure 9.6. *A capacitive turn-off snubber with passive capacitor energy recovery into the load.*

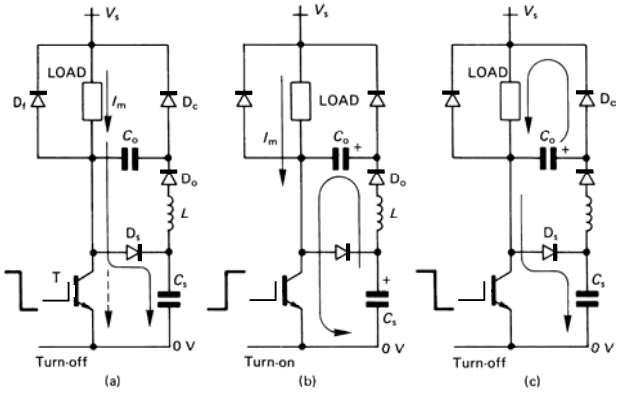

Figure 9.7. *Energy recovery turn-off snubber showing the energy recovery stages: (a) conventional snubber action at turn-off; (b) intermediate energy transfer at subsequent switch turn-on; and (c) transferred energy dumped into the load at subsequent switch turn-off.*

Analysis of the *L-C* resonant circuit with the initial conditions shown yields the following capacitor voltage and current equations. The resonant current is given by

$$i(\omega t) = \frac{V_s}{Z}\sin\omega t \quad \text{(A)} \tag{9.6}$$

where $Z = \omega L = Z_o\sqrt{1 + 1/n}$ (ohms)

$\omega = \omega_o\sqrt{1 + 1/n}$ (rad/s)

$\omega_o = 1/\sqrt{LC_o}$ (rad/s)

$n = C_s/C_o$

$Z_o = \sqrt{L/C_o}$ (ohms)

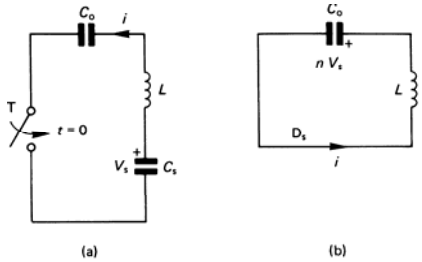

Figure 9.8. *Equivalent circuit for the intermediate energy transfer phase of snubber energy recover, occurring via: (a) the main switch T and (b) then via the snubber diode D_s.*

The snubber capacitor voltage decreases according to

$$V_{Cs} = V_s\left\{1 - \frac{1}{1+n}\cos\omega t\right\} \quad \text{(V)} \tag{9.7}$$

while the transfer capacitor voltage charges according to

$$V_{Co} = V_s\frac{n}{1+n}\left(1 + \cos\omega t\right) \quad \text{(V)} \tag{9.8}$$

Examination of equation (9.7) shows that if $n > 1$, the final snubber capacitor voltage at $\omega t = \pi$ will be positive. It is required that C_s retains no charge, ready for subsequent switch turn-off; thus $n \le 1$, that is $C_o \ge C_s$. If C_o is greater than C_s equation (9.7) predicts C_s will retain a negative voltage. Within the practical circuit of figure 9.6, C_s will be clamped to zero volts by diode D_s conducting and allowing the stored energy in L to be transferred to C_o. The new equivalent circuit for $\omega t = \cos^{-1}(-n)$ is shown in figure 9.8b. The resonant current is given by

$$i(\omega t) = \frac{V_s}{Z}\sin\left(\omega_s t + \phi\right) \quad \text{(A)} \tag{9.9}$$

where $t \geq 0$ and $\phi = -\tan^{-1}\sqrt{\frac{1-n^2}{n}}$.

The final voltage on C_o is $\sqrt{n}\,V_s$ and C_s retains no charge. The voltage and current waveforms for the resonant energy transfer stage are shown in figure 9.9.

Energy dumping from C_o into the load and snubber action occur in parallel and commence when the switch is turned off. As the collector current falls to zero in time t_{fi} a number of serial phases occur. These phases, depicted by capacitor voltage and current waveforms, are shown in figure 9.10.

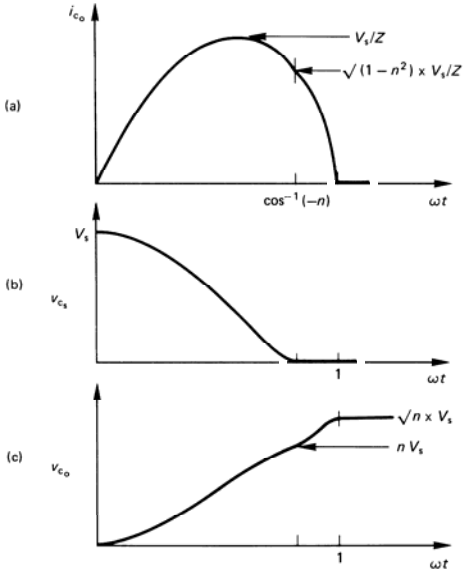

Figure 9.9. *Circuit waveforms during intermediate energy transfer phase of snubber energy recovery: (a) transfer capacitor C_o current; (b) snubber capacitor voltage; and (c) transfer capacitor voltage.*

Phase one

Capacitor C_o is charged to $\sqrt{n}\,V_s$, so until the snubber capacitor C_s charges to $\left(1-\sqrt{n}\right)V_s$, C_o takes no part. Conventional snubber turn-off action occurs as discussed in section 8.3.1. The snubber capacitor voltage increases according to

$$V_{Cs} = \tfrac{1}{2}\frac{I_m}{C_s t_{fi}} t^2 \qquad \text{(V)} \qquad (9.10)$$

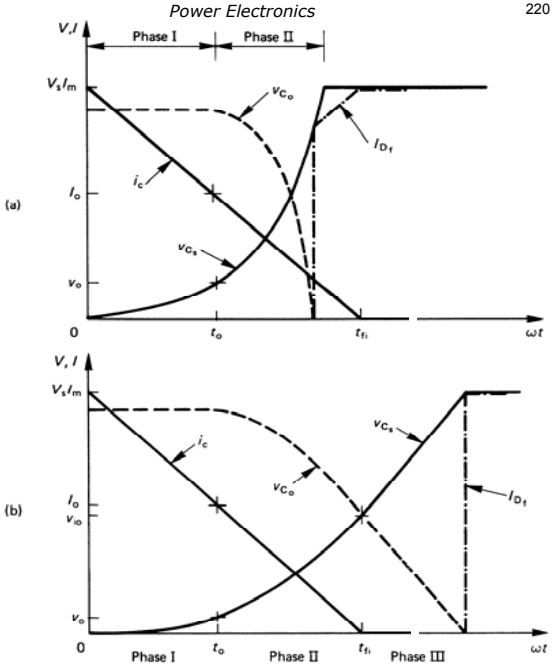

Figure 9.10. *Circuit waveforms at switch turn-off with turn-off snubber energy recovery when: (a) the snubber C_s is fully charged before the switch current at turn-off reaches zero and (b) the switch collector current has fallen to zero before the snubber capacitor has charged to the rail voltage.*

while C_o remains charged with a constant voltage of $\sqrt{n}\,V_s$. This first phase is complete at t_o when

$$V_{Cs} = v_o = \tfrac{1}{2}\frac{I_m t_o^2}{C_s t_{fi}} = \left(1-\sqrt{n}\right)V_s \qquad \text{(V)} \qquad (9.11)$$

whence

$$t_o = \sqrt{\frac{2\left(1-\sqrt{n}V_s C_s t_{fi}\right)}{I_m}} \qquad \text{(s)} \qquad (9.12)$$

and the collector current

$$I_o = \mathrm{I_m}\left(1-{}^{t_o}\!/_{t_{fi}}\right) \qquad \text{(A)} \qquad (9.13)$$

Phase two

When C_s charges to $\left(1-\sqrt{n}\right)V_s$, the capacitor C_o begins to discharge into the load. The equivalent circuit is shown in figure 9.11a, where the load current is assumed constant while the collector current fall is assumed linear. The following conditions must be satisfied

$$V_s = V_{Cs} + V_{Co} \qquad \text{(V)} \qquad (9.14)$$

$$I_m = i_{Co} + i_{Cs} + I_o(1 - t/t_{fi}) \qquad \text{(A)} \qquad (9.15)$$

for $0 \le t \le t_{fi} - t_o$

Under these conditions, the snubber capacitor voltage increases according to

$$V_{Cs} = \frac{n}{1+n}\frac{1}{C_s}\left[\left(I_m - I_o\right)t + \tfrac{1}{2}t^2/t_o\right] + \left(1-\sqrt{n}\right)V_s \qquad \text{(V)} \qquad (9.16)$$

with a current

$$i_{Cs} = \frac{1}{1+n}\left\{I_m - I_o(1 - t/t_o)\right\} \qquad \text{(A)} \qquad (9.17)$$

The transfer dump capacitor C_o discharges with a current given by

$$i_{Co} = i_{Cs}/n \qquad (9.18)$$

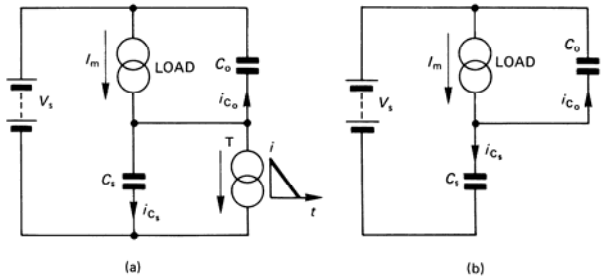

Figure 9.11. *Turn-off snubber equivalent circuit during energy recovery into the load when: (a) C_o begins to conduct and (b) after the switch has turned off.*

Phase three

If the snubber capacitor has not charged to the supply rail voltage before the switch collector current has reached zero, phase three will occur as shown in figure 9.10b. The equivalent circuit to be analysed is shown in figure 9.11b. The Kirchhoff equations describing this phase are similar to equations (9.14) and (9.15) except that in equation (9.15) the component $I_o(1- t/t_0)$ is zero.

The capacitor C_s, charging current is given by

$$i_{Cs} = \frac{n}{1+n}I_m \qquad \text{(A)} \qquad (9.19)$$

while the dumping capacitor C_o current is

$$i_{Co} = i_{Cs}/n \qquad \text{(A)} \qquad (9.20)$$

The snubber capacitor charges linearly, according to

$$V_{Cs} = v_{so} + \frac{n}{1+n}\frac{I_m}{C_s}t \qquad \text{(V)} \qquad (9.21)$$

When C_s is charged to the rail voltage V_s, C_o is discharged and the load freewheeling diode conducts the full load current I_m.

Since the snubber capacitor energy is recovered there is no energy loss penalty for using a large snubber capacitance and the larger the capacitance, the lower the switch turn-off switching loss. The energy to be recovered into the load is fixed, $\frac{1}{2}C_sV_s^2$ and at low load current levels the long discharge time of C_o may inhibit proper snubber circuit action. This is generally not critical since switching losses are small at low load current levels.

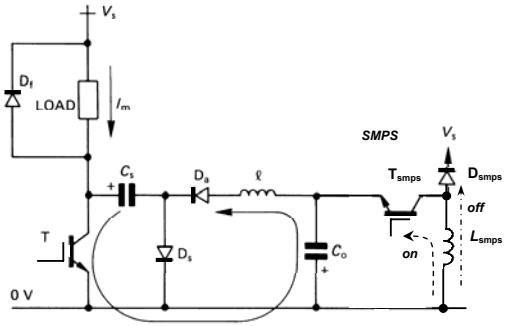

Figure 9.12. *Switching circuit for recovering turn-off snubber capacitor energy, and for providing either a negative voltage rail or transferring to V_s, via an smps.*

9.2.2 Active recovery

Active energy recovery methods for the turn-off snubber are simpler than the technique needed for active recovery of turn-on snubber circuit stored energy. The energy to be recovered from the turn-off snubber is fixed at $\frac{1}{2}C_sV_s^2$ and is independent of load current. In the case of the turn-on snubber, the energy to be recovered is load current magnitude dependent (αI_L^2) which complicates active recovery.

At turn-on the snubber capacitor stored energy is resonated into a large intermediate storage capacitor C_o as shown in figure 9.12. It is possible to use the energy in C_o as a negative low-voltage rail supply. This passive recovery technique

suffers from the problem that energy $\frac{1}{2}C_sV_s^2$ may represent more energy than the low-voltage supply requires. An smps can convert energy stored in C_o to a more useful voltage level.
It may be noticed that the 'Cuk' converter is in fact the snubber energy recovery circuit in figure 9.12, controlled in a different mode.

9.3 Unified turn-on and turn-off snubber circuit energy recovery

9.3.1 Passive recovery

Conventional turn on and turn off snubber circuits can be incorporated on a switching device as shown in figure 8.20. The stored energy is dissipated as heat in the reset resistor. Figure 9.13 shows turn-on and turn-off snubber circuits which allow energy recovery for both the snubber capacitor and inductor.
The snubber capacitor energy is recovered by the transfer process outlined in section 9.2.1. Figure 9.13a shows the energy transfer paths at switch turn-off. The capacitor C_o and inductor ℓ_s transfer their stored energy to the load in parallel, such that the inductor voltage is clamped to the capacitor voltage V_{Co}.

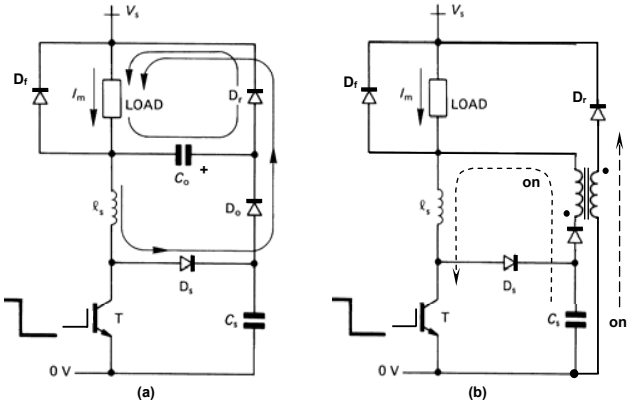

Figure 9.13. *Switching circuits incorporating unified turn-on and turn-off snubber, showing recovery path of energy (a) in C_o and ℓ_s and (b) in C_s and ℓ_s through D_r.*

As C_o discharges, the voltage across ℓ_s decreases to zero, at which time the load freewheel diode conducts. Any remaining inductor energy is dissipated as unwanted heat in circuit resistance. Proper selection of ℓ_s and C_s ($\frac{1}{2}L_sI_m^2 \leq \frac{1}{2}C_sV_s^2$) can minimise the energy that is lost although all the snubber capacitor energy is recovered, neglecting diode and stray resistance losses.

Aspects of the mathematical analysis of this unified recovery circuit are derived in the answer to the problem set at the end of this chapter.
Figure 9.13b shows a dual snubber energy recovery technique where resonance energy is transferred back to the supply at switch turn-on, through a coupled circuit.
Figure 9.14 shows an inverter bridge leg where both switches have turn-on and turn-off snubbers and passive recovery circuits. The circuit also recovers the energy associated with freewheel diode reverse recovery. Both the turn-on energy and turn-off energy are recovered back into the dc supply, V_s. Although this decreases the energy transfer efficiency, recovery into the load gives poor regulation at low load current levels where the capacitor turn-off energy, which is fixed, may exceed the load requirements. Energy recovery involves a coupled circuit which can induce high voltage stresses. Such conditions can be readily avoided if a split capacitor (multilevel) voltage rail is used, as shown in figure 9.2c.

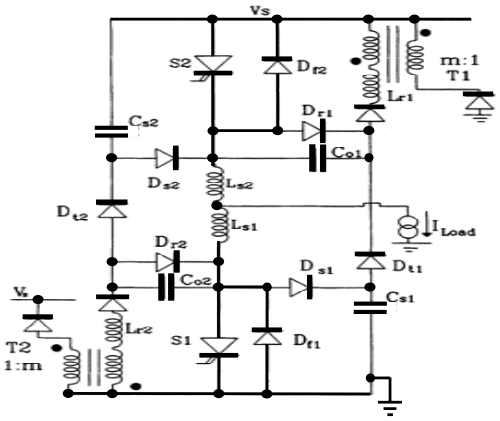

Figure 9.14. *Unified, passive snubber energy recovery circuit for inverter bridge legs.*

9.3.2 Active recovery

Figure 9.15 shows two similar turn-on and turn-off snubber, active energy recovery circuits, which are particularly suitable for bridge leg configurations. In figure 9.15a the turn-on snubber section is similar in operation to that shown in figure 9.3 while the turn-off snubber section is similar in operation to that shown in figure 9.12. A common smps is used for each turn-on and turn-off snubber pair. This arrangement is particularly useful when the two power switches and associated freewheel diodes are available in a single isolated package.

The active recovery circuit in figure 9.15b shows the turn-on snubbers relocated. The smps inputs are cross-coupled, serving the turn-on snubber of one switch and the turn-off snubber of the other switch.
The interaction of turn-off snubbers in both circuits can create high *L-C* resonant currents as discussed in section 8.4. In each case two smps can serve numerous bridge legs. The circuit in figure 9.15a is readily reduced for single-ended operation.

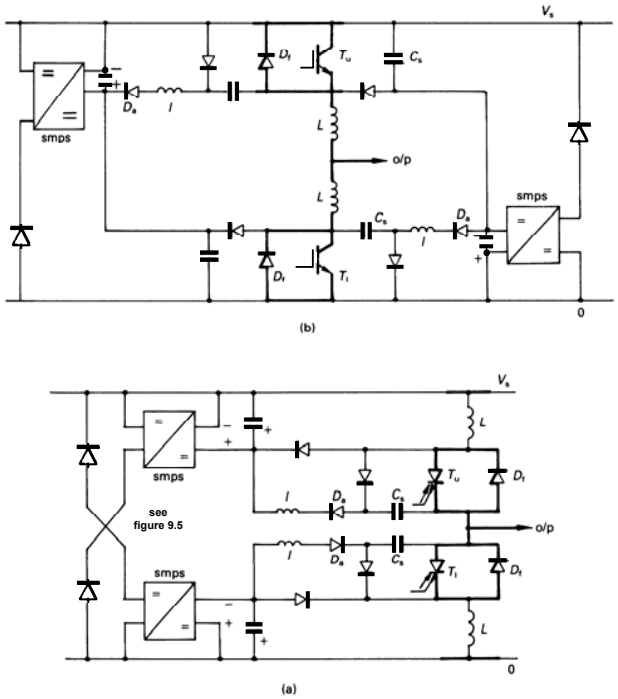

Figure 9.15. *Unified, active snubber energy recovery circuits:*
(a) multiple single-ended circuit and (b) cross-coupled high frequency circuit.

Reading list

Boehringer, A. *et al.,* 'Transistorschatter im Bereich hoher Leistungen und Frequenzen', *ETZ,* Bd. 100 (1979) pp. 664-670.

Peter, J. M., *The Power Transistor in its Environment,* Thomson-CSF, Sescosem, 1978.

Williams, B. W., *et al*., (2000) 'Passive snubber energy recovery for a GTO thyristor inverter bridge leg', *Trans. IE lEEE,* Vol. 47, No. 1, Feb. (2000) pp. 2-8.

Problems

9.1. Derive expressions for the snubber capacitor C_s and transfer capacitor C_o voltage and currents at switch turn-off for the unified snubber circuit energy recovery scheme shown in figure 9.13. The energy transfer process from C_s to C_o at switch turn-on is identical to that in the recovery scheme shown in figure 9.6 and analysed in section 9.2.1.
During recovery, the inductor current is of the form

$$i_l = a - bt + c\sin(\omega t + \phi)$$

9.2. For the circuit in Figure 9.13a show that the upper current limit for total energy recovery is given by $\frac{1}{2}L_s I_m^2 \le \frac{1}{2}C_s V_s^2$.

9.3. Derive capacitor C_s voltage and current equations which describe the operation of the turn-off snubber energy recovery circuit in figure 9.12. Assume the storage capacitor C_o to be an ideal voltage source with polarity as shown.

10

Series and Parallel Device Operation and Protection

This chapter considers various areas of power device application that are often overlooked. Such areas include parallel and series device utilisation, overcurrent and overvoltage protection, radio frequency interference (rfi) noise, filtering, and interactive noise effects.

10.1 Parallel and series operation of power devices

The power-handling capabilities of power devices are generally limited by device area utilisation, encapsulation, and cooling efficiency. Many high-power applications exist where a single device is inadequate and, in order to increase power capability, devices are paralleled to increase current capability or series-connected to increase voltage ratings. Extensive series connection of devices is utilised in HVDC transmission thyristor and IGBT modules while extensive paralleling of IGBTs is common in inverter applications.
When devices are connected in series for high-voltage operation, both steady-state and transient voltages must be shared equally by each individual series device. If power devices are connected in parallel to obtain higher current capability, the current sharing during both switching and conduction is achieved either by matching appropriate device electrical and thermal characteristics or by using external forced sharing techniques.

10.1.1 Series operation

Owing to variations in blocking currents, junction capacitances, delay times, on-state voltage drops, and reverse recovery for individual power devices, external voltage equalisation networks and special gate circuits are required if devices are to be reliably connected and operated in series.

10.1.1i - Steady-state voltage sharing

Figure 10.1 shows the forward off-state voltage-current characteristics of two typical power switching devices, such as SCRs or IGBTs. Both series devices conduct the same off-state leakage current but, as shown, each supports a different voltage. The total voltage blocked is $V_1 + V_2$ which can be significantly less than the sum of the individual capabilities. Forced voltage sharing can be achieved by connecting a resistor of suitable value in parallel with each series device as shown in figure 10.2.

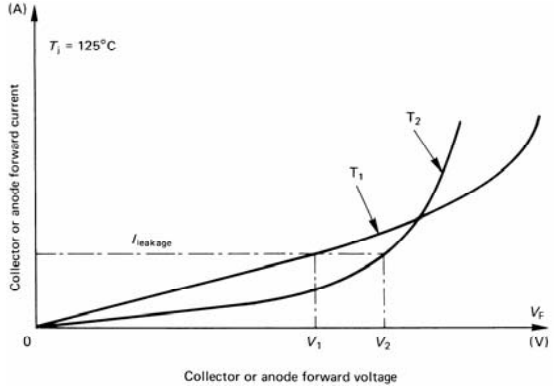

Figure 10.1. *Collector (transistor) or anode (thyristor) forward blocking I-V characteristics showing voltage sharing imbalance for two devices in series.*

These equal value sharing resistors will consume power and it is therefore desirable to use as large a resistance as possible. For worst case analysis consider *n* cells in series, where all the cells pass the maximum leakage current except cell D_1 which has the lowest leakage. Cell D_1 will support a larger blocking voltage than the remaining *n* - 1 which share voltage equally.
Let V_D be the maximum blocking voltage for any cell which in the worst case analysis is supported by D_1. If the range of maximum rated leakage or blocking currents is from $\hat{I}_b$ to $\check{I}_b$ then the maximum imbalance occurs when member D_1 has a leakage current of $\check{I}_b$ whilst all the remainder conduct $\hat{I}_b$. From figure 10.2, Kirchhoff's current law gives

$$\Delta I = \hat{I}_b - \check{I}_b \quad \text{(A)} \tag{10.1}$$

$$= I_1 - I_2 \quad \text{(A)} \tag{10.2}$$

where $I_1 > I_2$. The voltage across cell D_1 is

$$V_D = I_1 R \quad \text{(V)} \tag{10.3}$$

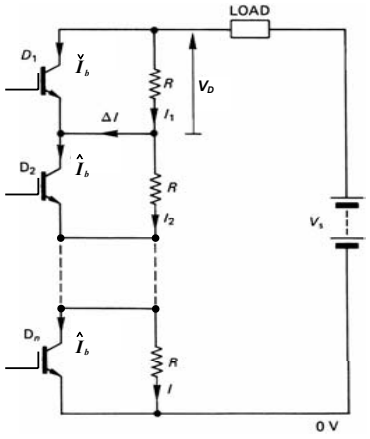

Figure 10.2. *Series IGBT string with resistive shunting for sustaining voltage equalisation in the off-state.*

By symmetry and Kirchhoff's voltage law, the total string voltage to be supported, V_s, is given by

$$V_s = (n - 1) I_2 R + V_D \quad \text{(V)} \tag{10.4}$$

Eliminating ΔI, I_1, and I_2 from equations (10.1) to (10.4) yields

$$\hat{R} \le \frac{nV_D - V_s}{(n-1)\left(\hat{I}_b - \check{I}_b\right)} \quad \text{(ohms)} \tag{10.5}$$

for $n \ge 2$.

Generally only the maximum leakage current at rated voltage and maximum junction temperature is specified. By assuming $\check{I}_b = 0$, a conservative value of the maximum allowable resistance is obtained, namely

$$\hat{R} \le \frac{nV_D - V_s}{(n-1)\hat{I}_b} = \frac{n(1-k_s)V_D}{(n-1)\hat{I}_b} \quad \text{(ohms)} \tag{10.6}$$

The extent to which nV_D is greater than V_s, is termed the voltage sharing factor, namely

$$k_s = V_s / nV_D \le 1 \tag{10.7}$$

As the number of devices is minimized the sharing factor approaches one, but equation (10.5) shows that undesirably the resistance for sharing decreases, hence losses increase.

The power dissipation of the resistor experiencing the highest voltage is given by

$$\hat{P}_d = V_D^2 / \hat{R} \quad \text{(W)} \tag{10.8}$$

If resistors of ± l00a per cent resistance tolerance are used, the worst case occurs when cell D_1 has a parallel resistance at the upper tolerance while all the others have parallel resistance at the lower limit. After using $V_D=(1+a)I_1R$ and $V_s=(n-1)(1-a)I_2R+V_D$ for equations (10.3) and (10.4), the maximum resistance is given by

$$\hat{R} \le \frac{n(1 - a)V_D - (1 + a)V_s}{(n - 1)\left(1 - a^2\right)\hat{I}_b} \quad \text{(ohms)} \tag{10.9}$$

for $n \ge 2$.

The maximum loss in a resistor is

$$\hat{P}_D = V_D^2 / \hat{R}(1 - a) \tag{10.10}$$

If the supply toleration is incorporated, then V_s in equations (10.6) and (10.9) is replaced by $(1+b)\times V_s$ where 100b is the supply percentage upper tolerance. This leads to a decreased resistance requirement, hence increased resistor power losses.

$$\hat{R} \le \frac{n(1-a)V_D - (1+a)(1+b)V_s}{(n - 1)\left(1 - a^2\right)\hat{I}_b} \quad \text{(ohms)} \tag{10.11}$$

The effects and importance of just a few per cent resistance or supply voltage tolerance on the maximum value for the sharing resistors and their power losses, are illustrated by the following example.

Example 10.1: ***Series device connection – static balancing***

Ten, 200 V reverse-blocking, ultra fast 35 ns reverse recovery diodes are to be employed in series in a 1500 V peak, string voltage application. If the maximum device reverse leakage current is 10 mA calculate the sharing factor, and for worst case conditions, the maximum value of sharing resistance and power dissipation.

- If 10 per cent tolerance resistors are employed, what is the maximum sharing resistance and its associated power rating?
- If a further allowance for supply voltage tolerance of ±5% is incorporated, what is the maximum sharing resistance and its associated power rating?

Solution

When n = 10, V_D = 200 V, V_s = 1500 V, and $\hat{I}_b$ = 10 mA, the sharing factor is k_s = 1500V/10×200V = 0.75. Equation (10.6) yields the maximum allowable sharing resistance

$$\hat{R} \le \frac{nV_D - V_s}{(n-1)\hat{I}_b} = \frac{10\times 200\text{V} - 1500\text{V}}{(10\text{-}1)\times 10\text{mA}} = 5.55\text{k}\Omega$$

The nearest (lower) preferred value, 4.7 kilohms, would be used.

Maximum resistor power losses occur when the diodes are continuously blocking. The maximum individual supporting voltage appears across the diode which conducts the least leakage current. Under worst case conditions this diode therefore supports voltage V_D, hence maximum power loss $\hat{P}_D$ is

$$\hat{P}_D = V_D^2 / \hat{R}$$
$$= 200^2/4700\Omega = 8.5\text{ W}$$

Since the worse device, (in terms of sharing has lowest leakage current), is randomly located in the string, each resistor must be capable of dissipating 8.5W.
The maximum 1500V supply leakage current is 42.5mA (10mA+1500V/10×4.7kΩ) giving 63.8W total losses (1500V×42.5mA), of which 15W (10mA×1500V) is lost in the diodes.
If resistance tolerance is incorporated, equation (10.9) is employed with a = 0.1, that is

$$\hat{R} \le \frac{n(1 - a)V_D - (1 + a)V_s}{(n - 1)\left(1 - a^2\right)\hat{I}_b}$$

$$\hat{R} \le \frac{10 \times (10 - 0.1) \times 200\text{V} - (1 + 0.1) \times 1500\text{V}}{(10 - 1) \times \left(1 - 0.1^2\right) \times 10\text{mA}}$$

$$= 2.13\ \text{k}\Omega$$

The nearest (lower) preferred value is 1.8 kilohms, which is much lower resistance (higher losses) than if matched resistors were to be used.
Worst case resistor power dissipation is

$$\hat{P}_D = V_D^2 / \hat{R}(1 - a)$$

$$= 200^2 / 1800\Omega \times (1 - 0.1)$$

$$= 27.7\ \text{W}$$

The maximum total module losses are 165W (1500V×103mA) arising from 103 mA (10mA + 1500V/1.8kΩ×(1- 0.1)) of leakage current.
If the device with the lowest leakage is associated with the worse case resistance (upper tolerance band limit), and simultaneously the supply is at its upper tolerance limit, then worse case resistance is given by equation (10.11), that is

$$\hat{R} \le \frac{n(1-a)V_D - (1+a)(1+b)V_s}{(n - 1)\left(1 - a^2\right)\hat{I}_b}$$

$$= \frac{10 \times (1 - 0.1) \times 200\text{V} - (1 + 0.1) \times (1 + 0.05) \times 1500\text{V}}{(10 - 1) \times \left(1 - 0.1^2\right) \times 10\text{mA}} = 758\Omega$$

Each resistor (preferred value 680Ω) needs to be rated at

$$200^2 / 680\Omega \times (1 - 0.1) = 68.6\ \text{W}$$

♣

When resistance tolerances are considered, sharing resistors of lower value must be used and the wider the tolerance, the lower will be the resistance and the higher the power losses. A number of solutions exist for reducing power losses and economic considerations dictate the acceptable trade-off level. Matched devices would allow a minimum number of string devices (sharing factor $k_s \rightarrow 1$) or, for a given string device number, a maximum value of sharing resistance (lowest losses). But matching is complicated by the fact that leakage current varies significantly with temperature. Alternatively, by increasing the string device number (decreasing the sharing factor k_s) the sharing resistance is increased, thereby decreasing losses. By increasing the string device number from 10 (k_s = ¾)

to 11 (k_s = 0.68) in the previous example, the sharing resistance requirement increases from 4.7 kilohms to 6.8 kilohms and resistor losses are reduced from a total of 50.8 W to 31 W. Another method of minimising sharing resistance losses is to minimise resistance tolerances. A tolerance reduction from 10 per cent to 5 per cent in the previous example increases the sharing resistance requirements from 1.8 kilohms to 3.9 kilohms, while power losses are reduced from 140 W to 64 W. These worse case losses assume a 100% on-state duty cycle.

10.1.1ii - Transient voltage sharing

During steady-state or at very low frequencies, sharing resistors as shown in figure 10.2 are sufficient to prevent individual device overvoltage. Mismatching of turn-on delay times of thyristors and transistors can be minimised by supplying high enough turn-on drive with very fast rise times. A higher initial *di/dt* is allowable.
Before a conducting string of diodes or thyristors can reverse-block, reverse recovery charge must flow. Those elements with least recovery charge requirements recover first and support the reverse bias. The un-recovered devices recover slowly, since recovery now occurs as a result of the low leakage current though the recovered devices, and natural recombination.
The reverse-blocking voltage can be shared more equally by placing capacitance across each string element as shown in figure 10.3. The capacitor action is to provide a transient current path bypassing a recovered device to allow a slower device to recover and to support volts. In the case of thyristors, low value resistance is connected in series with each capacitor to avoid high capacitor discharge through the thyristors at turn-on. Figure 10.4 shows the *I-V* characteristics of two unmatched thyristors or diodes during reverse recovery.
The worst case assumptions for the analysis of figure 10.3 are that element D_1 has minimum stored charged $\check{Q}$ while all other devices have the maximum requirement, $\hat{Q}$. The charge difference is

$$\Delta Q = \hat{Q} - \check{Q} \quad \text{(C)} \qquad (10.12)$$

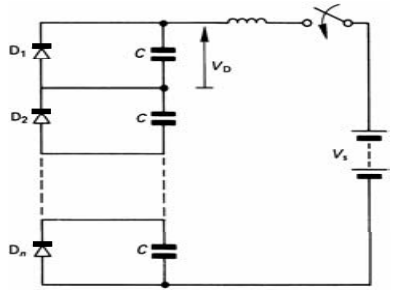

Figure 10.3. *A series diode string with shunting capacitance for transient reverse blocking voltage sharing.*

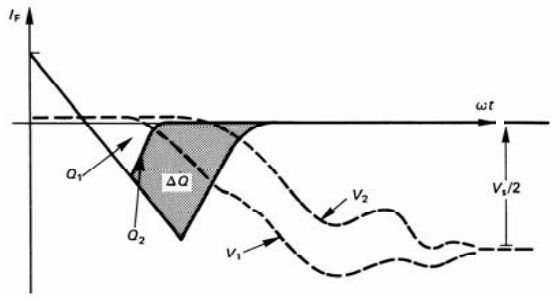

Figure 10.4. *Reverse recovery current and voltage for two mismatched series connected diodes.*

The total string voltage V_s, comprises the voltage across the fast-recovery device V_D plus the sum of the voltages across the slow n - 1 devices, V_{slow}. That is

$$V_s = V_D + (n - 1)V_{slow} \quad \text{(V)} \qquad (10.13)$$

The voltage across the slow devices is given by

$$V_{slow} = \frac{1}{n}\left(V_s - \Delta\hat{V}\right) \quad \text{(V)} \qquad (10.14)$$

where $\Delta\hat{V} = \Delta\hat{Q}/C$.

Eliminating V_{slow} from equations (10.13) and (10.14) yields

$$\breve{C} \geq \frac{(n-1)\Delta Q}{nV_D - V_s} = \frac{(n-1)\Delta Q}{n(1-k_s)V_D} \quad \text{(F)} \qquad (10.15)$$

This equation shows that as the number of devices is minimized, the sharing factor, k_s, which is in the denominator of equation (10.15), tends to one and the capacitance requirement undesirably increases.

Manufacturers do not specify the minimum reverse recovery charge but specify the maximum reverse recovery charge for a given initial forward current, reverse recovery *di/dt,* and temperature. For worst case design, assume $\breve{Q}$ = 0, thus

$$\breve{C} \geq \frac{(n-1)\hat{Q}}{nV_D - V_s} \quad \text{(F)} \qquad (10.16)$$

Sharing circuit design is complicated if the effects of reverse steady-state leakage current in ac thyristor blocking are taken into account.

Supply and sharing capacitance tolerances significantly affect the minimum capacitance requirement. Worst case assumptions for capacitance tolerances involve the case when the fastest recovering diode is in parallel with capacitance at its lower tolerance limit while all the other sharing capacitances are at their upper tolerance limit. Assuming the minimum reverse recovery charge is zero, then the minimum sharing capacitance requirement is

$$\breve{C} \geq \frac{(n-1)\hat{Q}}{(1-a)(nV_D - V_s)} \quad \text{(F)} \qquad (10.17)$$

where -100a is the capacitor negative percentage tolerance and $n \geq 2$. Voltage sharing resistors help minimise capacitor static voltage variation due to capacitance variations.

If the supply tolerance is incorporated, then V_s in equations (10.16) and (10.17) are replaced by $(1+b)\times V_s$ where +100b is the supply percentage upper tolerance. This leads to an increased capacitance requirement, hence increased energy losses, $\frac{1}{2}CV_D^2$.

$$\breve{C} \geq \frac{(n-1)\hat{Q}}{(1-a)(nV_D - (1+b)V_s)} \quad \text{(F)} \qquad (10.18)$$

Example 10.2: ***Series device connection – dynamic balancing***

The string of ten, 200 V diodes in worked example 10.1 is to incorporate capacitive reverse recovery transient sharing. Using the data in chapter 5, figure 5.9, specify a suitable sharing capacitance based on zero capacitance and supply tolerances (a = b = 0), ± 10 per cent capacitance tolerances (a = 0.1, b = 0), ± 5 per cent supply tolerance (a = 0, b = 0.05), then both tolerances (a = 0.1, b = 0.05). Estimate in each case the energy loss due to capacitor discharge.

Solution

Figure 5.9 shows that worst case reverse recovery conditions occur at maximum junction temperature, *di/dt,* and I_F, and a value of $\hat{Q}$ =6μC is appropriate.

The minimum possible sharing capacitance occurs when the capacitance and dc rail voltage are tightly specified. From equation (10.16)

$$\breve{C} \geq \frac{(n-1)\hat{Q}}{nV_D - V_s} = \frac{(10\text{-}1)\times 6\mu C}{10\times 200 - 1500V} = 108nF$$

The sharing capacitance requirement with 10% tolerance capacitors, is given by equation (10.17),

$$\breve{C} \geq \frac{(n-1)\hat{Q}}{(1-a)(nV_D - V_s)} = \frac{(10 - 1)\times 6\mu C}{(1 - 0.1)\times(10\times 200V - 1500V)} = 0.12\mu F \text{ @ } 200Vdc$$

A further increase in capacitance requirements results if the upper tolerance dc rail voltage is used. From equation (10.18)

$$\breve{C} \geq \frac{(n-1)\hat{Q}}{(1-a)(nV_D - (1+b)V_s)}$$

$$= \frac{(10 - 1)\times 6\mu C}{(1 - 0.1)\times(10\times 200V - (1+0.05)\times 1500V)} = 0.14\mu F \text{ @ } 200Vdc$$

In each tolerance case the next larger preferred capacitance value should be used, namely, 120nF, 120nF, and 150nF respectively.

The total series capacitance, using the upper tolerance limit is

$$C_T = \frac{(1+a)\overset{\vee}{C}}{n}$$

The stored energy with a 1500V dc rail in the 10 series connect 120nF capacitors, and subsequently loss when the string voltages reduces to zero at diode forward bias, is therefore

$$W_T = ½C_T\hat{V}_s^2 = ½\frac{(1+a)\overset{\vee}{C}}{n}V_s^2(1+b)^2$$

$$= ½\frac{(1+0.1)\times 120\text{nF}}{10}\times 1500^2\times(1+0.05)^2 = 16.4\text{mJ}$$

The energy stored in the 10 series connect 150nF capacitors, and subsequently loss when the string voltages reduces to zero at diode forward bias, is

$$W_T = ½\times\frac{(1+0.1)\times 150\text{nF}}{10}\times 1500^2\times(1+0.05)^2 = 20.5\text{mJ}$$

♣

When capacitive sharing is used with switching devices, at turn-on the transient sharing capacitor discharges into the switching device. The discharge current magnitude is controlled by the turn-on voltage fall characteristics. If a linear voltage fall at turn-on is assumed, then the transient sharing capacitor maximum discharge current i_{dis} is a constant current pulse for the fall duration of magnitude

$$i_{dis} = C\frac{V_D}{t_{tv}} \quad \text{(A)} \qquad (10.19)$$

The discharge current can be of the order of hundreds of amperes, incurring initial *di/dt* values beyond the capabilities of the switching device. In example 10.2 the discharge current for a switch rather than a diode is approximately 150nF×200V/1μs =30A, assuming a 1μs voltage fall time. This 30A may not be insignificant compared to the switches current rating. But, advantageously, the sharing capacitors do act as turn-off snubbers, reducing switch turn-off stressing.

In the case of the thyristor, the addition of low-valued resistance in series with the transient capacitor can control the capacitor discharge current, yet not significantly affect the transient sharing properties. The resultant *R-C* discharge current can provide thyristor latching current while still offering transient recovery sharing, *dv/dt,* and voltage spike suppression. Thyristor snubber operation and design have been considered in section 8.1.2.

Figure 10.5 shows the complete steady-state and transient-sharing networks used for diodes, thyristors, and transistors. Transient voltage sharing for transistors involves the use of the conventional *R-D-C* snubber shown in figure 10.5c and considered in chapter 8. The series inductor used with thyristor and transistor strings provides transient turn-on voltage protection. The inductor supports the main voltage while each individual element switches on. Such an inductive turn-on snubber is mandatory for the GTO thyristor and the GCT. No one device is voltage-stressed as a consequence of having a longer turn-on delay time, although gate overdrive at turn-on minimises delay variations.

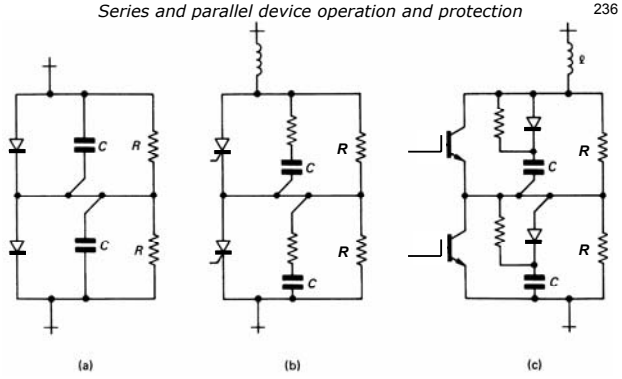

Figure 10.5. *Transient and steady-state voltage sharing circuits for series connected: (a) diodes; (b) thyristors; and (c) igbt transistors.*

10.1.2 Parallel operation

It is common practice to parallel devices in order to achieve higher current ratings or lower conducting voltages than are attainable with a single device. Although devices in parallel complicate layout and interconnections, better cooling distribution is obtained. Also, built-in redundancy can give improved equipment reliability. A cost saving may arise with smaller, cheaper, high production volume, devices.

The main design consideration for parallel device operation is that all devices share both the steady-state and transient currents. Any bipolar device carrying a disproportionately high current will heat up and conduct more current, eventually leading to thermal runaway as considered in section 4.1.

The problem of current sharing is less severe with diodes because diode characteristics are more uniform (because of their simpler structure and manufacturing) than those of thyristors and transistors. Two basic sharing solutions exist

- matched devices
- external forced current sharing.

10.1.2i - Matched devices

Figure 10.6 shows the static *I-V* on-state characteristics of two SCR's. If these two devices are connected in parallel, for the same on-state voltage, the resultant current flow is $I_1 + I_2$ where I_1 and I_2 can be very different in value. The total current rating of the pair is not the sum of the maximum current rating for each but rather a value which can be just larger than the rating of one device alone. The percentage parallel derating *pd* for *n* parallel connected devices is defined as

$$pd = \left(1 - \frac{I_T}{nI_m}\right) \times 100 \quad = \left(1 - k_p\right) \times 100 \quad \text{per cent} \qquad (10.20)$$

where I_T = total current through the parallel arrangement
I_m = maximum allowable single device current rating
n = number of parallel devices
k_p = parallel sharing factor $= I_T/nI_m$

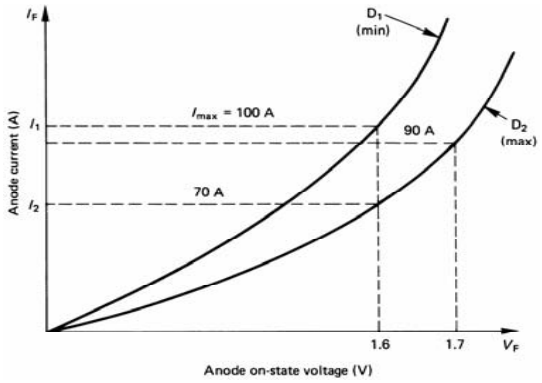

Figure 10.6. *Forward conduction characteristics of two unmatched devices.*

10.1.2ii - External forced current sharing

Derating does not account for effects such as layout and electrical and thermal impedance imbalance. The amount of derating is traded off against the extra cost involved in selecting devices with closer (matched) static characteristics.
Forced current sharing is applicable to both steady-state and transient conditions. For a current derating of less than 5 per cent it is usually cheaper to use forced sharing techniques rather than matched devices.
Figure 10.6 shows the maximum variation of *I-V* characteristics in devices of the same type. When parallel connected the maximum current is restricted to I_m+I_2, (= 100A+70A = 170A). The maximum current rating for each device is I_m, (100A); hence with suitable forced sharing a combination in excess of I_m+I_2 should be possible. The resistive network in figure 10.7 is used for current sharing and in example 10.3 it is required that I_m, 100A, flows through D_1 and $(1-2\times pd)\times I_m > I_2$, (90A) flows through D_2, for a *pd* (5%) overall derating.
From Kirchhoff's voltage law in figure 10.7

$$\begin{aligned} V_1 + V_3 &= V_2 + V_4 \\ V_{D_1} + I_m R &= V_{D_2} + \left(I_T - I_m\right) R \end{aligned} \qquad (10.21)$$

From equation (10.20), rearranged for two devices, $n = 2$

$$I_T = 2 \times (1 - pd) I_m$$

Substituting for I_T in equation (10.21) gives

$$R = \frac{V_{D_2} - V_{D_1}}{2\ pd\ I_m} \quad \text{(ohms)} \qquad (10.22)$$

For n devices connected in parallel, equation (10.21) becomes

$$V_{D_1} + I_m R = V_{D_2} + \frac{\left(I_T - I_m\right)}{n-1} R \qquad (10.23)$$

which after substituting for I_T from equation (10.20), for maximum device voltage variation, gives

$$R = \frac{\hat{V}_D - \check{V}_D}{I_m} \frac{(n-1)}{n \times pd} \quad \text{(ohms)} \qquad (10.24)$$

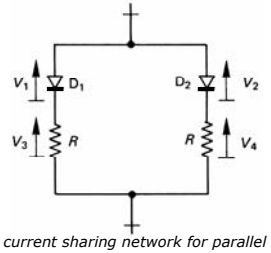

Figure 10.7. *Forced current sharing network for parallel connected devices.*

Although steady-state sharing is effective, sharing resistor losses can be high. The resistor losses in general terms for n parallel connected devices and a conduction duty cycle δ, are given by

$$P_r = \delta \left\{1 + \left(1 - \frac{n}{n-1} \times pd\right)^2\right\} I_m^2 R \quad \text{(W)} \qquad (10.25)$$

Example 10.3: ***Resistive parallel current sharing - static balancing***
For the two diodes shown in figure 10.6, with $\hat{I} = 100\text{A}$, what derating result when they are parallel connected, without any external sharing circuits?
The maximum current rating for each device is I_m, 100A; hence with suitable forced sharing a 190A combination should be possible. Using the network in figure 10.7 for current sharing, it is required that 100A flows through D_1 and 90A through D_2. Specify the per cent overall derating, the necessary sharing resistors and their worse case losses.

Solution
The derating for the parallel situation depicted in figure 10.6, without external sharing, is

$$pd = \left(1 - \frac{170\text{A}}{2\times 100\text{A}}\right)\times 100 = 15 \text{ per cent} \qquad (k_p = 0.85)$$

With forced resistive sharing, the objective derating is reduced from 15% to

$$pd = \left(1 - \frac{190\text{A}}{2\times 100\text{A}}\right)\times 100 = 5 \text{ per cent} \qquad (k_p = 0.95)$$

From figure 10.6

$$1.6\text{V} + 100\text{A}\times R = 1.7\text{V} + 90\text{A}\times R$$

that is

$$R = 10 \text{ milliohm}$$

Equation (10.22), being based on the same procedure, gives the same result. The cell voltage drop is increased to $1.6\text{V}+100\text{A}\times 0.01\Omega = 1.7\text{V}+90\text{A}\times 0.01\Omega = 2.6\text{V}$.

For $\delta = ½$

$$\bar{I}_{D1} = \delta \times I_{D1} = ½\times 100\text{A} = 50\text{A} \qquad \bar{I}_{D2} = \delta \times I_{D2} = ½\times 90\text{A} = 45\text{A}$$

$$I_{D1^{rms}} = \sqrt{\delta}\times I_{D1} = \sqrt{½}\times 100\text{A} = 70.7\text{A} \qquad \bar{I}_{D2^{rms}} = \sqrt{\delta}\times I_{D2} = \sqrt{½}\times 90\text{A} = 63.6\text{A}$$

$$I_{D1^{ac}} = \sqrt{I_{D1rms}^2 - \bar{I}_{D1}^2} \qquad I_{D2^{ac}} = \sqrt{I_{D2rms}^2 - \bar{I}_{D2}^2}$$

$$= \sqrt{70.7^2 - 50^2} = 50\text{A} \qquad = \sqrt{63.6^2 - 45^2} = 45\text{A}$$

$$P_{R1} = I_{D1rms}^2 R_1 = 70.7^2 \times 0.01\text{m}\Omega = 50\text{W} \qquad P_{R2} = I_{D2rms}^2 R_2 = 63.6^2 \times 0.01\text{m}\Omega = 40.5\text{W}$$

$$P_{D1} = \bar{I}_{D1} V_{D1} = 50\text{A}\times 1.6\text{V} = 80\text{W} \qquad P_{R2} = \bar{I}_{D2} V_{D2} = 45\text{A}\times 1.7\text{V} = 76.5\text{W}$$

$$P_{total} = P_R + P_D = (50\text{W} + 40.5\text{W}) + (80\text{W} + 76.5\text{W}) = 90.5\text{W} + 156.5\text{W} = 247\text{W}$$

For worse case losses, $\delta \rightarrow 1$

$$\bar{I}_{D1} = \delta \times I_{D1} = 1\times 100\text{A} = 100\text{A} \qquad \bar{I}_{D2} = \delta \times I_{D2} = 1\times 90\text{A} = 90\text{A}$$

$$I_{D1^{rms}} = \sqrt{\delta}\times I_{D1} = \sqrt{1}\times 100\text{A} = 100\text{A} \qquad \bar{I}_{D2^{rms}} = \sqrt{\delta}\times I_{D2} = \sqrt{1}\times 90\text{A} = 90\text{A}$$

$$I_{D1^{ac}} = \sqrt{I_{D1rms}^2 - \bar{I}_{D1}^2} \qquad I_{D2^{ac}} = \sqrt{I_{D2rms}^2 - \bar{I}_{D2}^2}$$

$$= \sqrt{100^2 - 100^2} = 0\text{A} \qquad = \sqrt{90^2 - 90^2} = 05\text{A}$$

$$P_{R1} = I_{D1rms}^2 R_1 = 100^2 \times 0.01\text{m}\Omega = 100\text{W} \qquad P_{R2} = I_{D2rms}^2 R_2 = 90^2 \times 0.01\text{m}\Omega = 81\text{W}$$

$$P_{D1} = \bar{I}_{D1} V_{D1} = 100\text{A}\times 1.6\text{V} = 160\text{W} \qquad P_{R2} = \bar{I}_{D2} V_{D2} = 90\text{A}\times 1.7\text{V} = 153\text{W}$$

$$P_{total} = P_R + P_D = (100\text{W} + 81\text{W}) + (160\text{W} + 153\text{W}) = 181\text{W}+313\text{W} = 494\text{W}$$

The general form in equation (10.25) gives the same total losses in each duty case.

♣

A more efficient method of current sharing is to use coupled reactors as shown in figure 10.8. In this feedback arrangement, in figure 10.8a, if the current in D_1 tends to increase above that through D_2, the voltage across L_1 increases to oppose current flow through D_1. Simultaneously a negative voltage is induced across L_2 thereby increasing the voltage across D_2 thus its current. This technique is most effective in ac circuits where the core is more readily designed to not saturate.

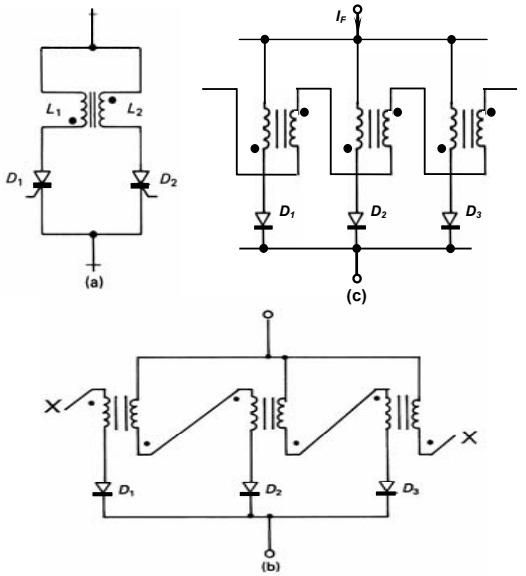

Figure 10.8. *External forced current sharing network using cross-coupled reactors: (a) for two devices; and (b) and (c) for many devices.*

Equalising reactor arrangements are possible for any number of devices in parallel, as shown in figure 10.8b and c, but size and cost become limiting constraints. The technique is applicable to steady-state and transient sharing. At high current densities, the forward *I-V* characteristic of diodes and thyristors has a positive temperature dependence which provides feedback aiding sharing.

The mean current in the device with the highest current, therefore lowest voltage, of *n* parallel connected devices, is given by

$$\bar{I}_F = \frac{I_F}{n} + \Delta I_F = \frac{I_F}{n} + \frac{n}{n-1}\frac{\tau^2}{2TL_M}\Delta V_F \qquad (10.26)$$

where ΔV_F is the maximum on-state voltage drop difference
L_M is the self-inductance (magnetising inductance) of the coupled inductor
T is the cycle period, $1/f_s$ and
τ is the conduction period

Consider two thyristors ($n = 2$) connected in parallel as show in figure 10.9. The coupled circuit magnetising current is modelled by the magnetising inductor L_M. The transformer turns ratio is 1:1, hence the winding voltages and currents are equal, taking into account the relative winding flux orientation shown by the dots.

From Kirchhoff's voltage law

$$v_{T1} + v_1 = v_{T2} - v_1 \tag{10.27}$$

That is

$$v_1 = ½ \times \left(v_{T1} - v_{T2}\right) = ½ \times \Delta v \tag{10.28}$$

From Kirchhoff's current law

$$I_M = i_1 - i_2 \tag{10.29}$$

From Faraday's equation

$$v_1 = L_M \frac{dI_M}{dt} \tag{10.30}$$

which after integrating both sides gives

$$\begin{aligned} I_M &= \frac{1}{L_M}\int_0^\tau v_1 dt \\ &= ½ \frac{1}{L_M} \Delta V_F \tau \end{aligned} \tag{10.31}$$

As a worst case condition it is assumed that the voltage difference Δv does not decrease as the operating point moves along the *I-V* characteristics, that is $\Delta v = \Delta V_F$. Specifically D1 moves further up the *I-V* characteristic with time as it conducts more current while D2 moves towards the origin.

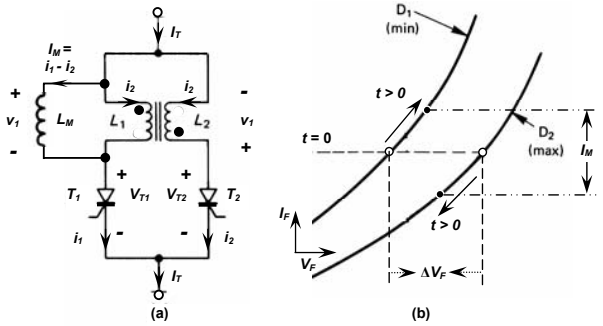

Figure 10.9. *External forced current sharing network using cross-coupled reactors: (a) circuit for two devices and (b) I-V operating points.*

Example 10.4: ***Transformer current sharing – static and dynamic balancing***

Two thyristors with the same forward conduction characteristics as the diodes in figure 10.6 are parallel connected using the coupled circuit arrangement in figure 10.8a.

The maximum current rating for each device is I_m, 100A; hence with suitable forced sharing a 190A combination should be possible. Using the network in figure 10.9a for current sharing, it is required that no more than rated current flow through the lower conducting voltage device, D_1. Specify the per cent overall derating and the necessary sharing transformer properties assuming a half-wave, 180º conduction, phase-controlled, 50Hz, highly inductive load application.
What are the transformer core reset requirements?

Solution

As in example 10.3, the derating for the parallel situation depicted in figure 10.6, without external sharing, is

$$pd = \left(1 - \frac{170\text{A}}{2\times 100\text{A}}\right)\times 100 = 15 \text{ per cent}$$

With forced transformer sharing, the objective derating is reduced from 15% to

$$pd = \left(1 - \frac{190\text{A}}{2\times 100\text{A}}\right)\times 100 = 5 \text{ per cent}$$

When the two thyristors are turned on, the magnetizing current is assumed zero and transformer action will force each device to conduct 95A, giving 190A in total. From figure 10.6, the voltage difference between the thyristors, ΔV_F is about 0.1V, thus the transformer winding voltages will be 0.05V each, with polarities as shown in figure 10.9a. In time the magnetizing current increases and the current in T1 increases above 95A due to the increasing magnetizing current, while the current in T2 decreases below 95A, such that the total load current is maintained at 190A.
The worse case conduction period, giving maximum magnetising current, is for 180º conduction, that is, 10ms. Thus it is required that T1 current rises to 100A and T2 current falls to 90A after 10ms, that is, the magnetising current is 100A-90A = 10A.
Substitution into equation (10.31) gives

$$L_M = ½ \frac{1}{I_M}\int_0^{10\text{ms}} \Delta v dt = ½ \times \frac{1}{10\text{A}} \times 0.1\text{V} \times 10\text{ms} = 50\mu\text{H}$$

where it is assuming that the voltage differential ΔV_F between the two devices is constant during the conduction period. In fact figure 10.9b shows that the voltage difference decreases, so assuming a constant value gives an over-estimate of requirements.
The core volt-µs during conduction is 0.05V×10ms = 500 V-µs. That is, during core reset the reverse voltage time integral must be at least 500 V-µs to ensure the core flux is reset, (magnetising current reduced to zero).

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10.2 Protection

A fault can be caused by a device failure or noise which causes undesired device turn-on. This will cause semiconductor device and equipment failure unless protective measures are utilised.
Protection against fault current effects usually involves fuses which clear in time

to protect endangered devices, or voltage transient absorption devices which absorb spike energy and clamp the equipment voltage to a safe level. The crowbar fault protection technique can be employed to divert the fault from sensitive components to the crowbar which is a robust circuit. The crowbar clamps the sensitive circuits to zero volts and initiates an isolation breaker or fuse action.

10.2.1 Overcurrent

It is not economical to design a circuit where fault overloads are catered for by using devices and components which will withstand worst case faults. A fuse link is normally used for circuit fault current protection. A fuse link protecting a semiconductor is required to carry normal and overload currents but to open the circuit under fault conditions before the semiconductor is damaged. The resultant circuit induced arcing voltage must not cause damage to the circuit. Other fuse links or circuit breakers should be unaffected when the defective cell is disconnected. This non-interaction property is termed *discrimination.*

The fuse element is one or more parallel conductors of pure silver rolled into thin bands, 0.04-0.25 mm thick. Each silver band has a number of traverse rows of punched holes (or notches) as shown in figure 10.10. The area between the holes determines the pre-arcing I^2t integral of the fuse and, along with thermal aspects, is related to the fuse current rating. The number of rows of holes determines the fuse voltage rating. When fusing occurs the current is shared between the holes (the necks), while the arcing voltage is supported between the series of rows of holes. The arcing characteristics are enhanced by packing the silver element in sand or glassed sand. The sand and silver element are contained in a ceramic body and the end connector plates are copper flashed and tinned.

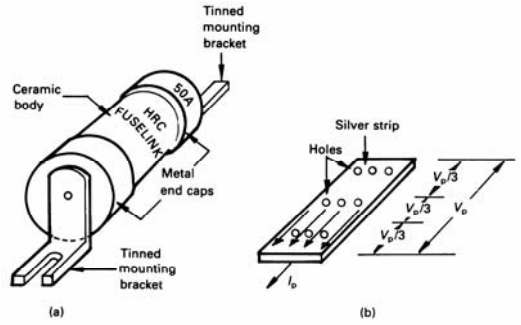

Figure 10.10. *The current fuse link:*
(a) a 50 A 660 V ac fuse link and (b) a silver fuse link element.

The action of a typical fuse link is shown in figure 10.11. Owing to the *prospective fault current* I_a the fuse melts at point A, time t_m. Depending on the fuse design and the circuit, the current may continue to rise further to point B, termed the *peak let-through current* I_p. Beyond this point the impedance of the arcing fuse forces the fault current down to zero at the point C. Thus *fuse-clearing* or *total interrupting time* t_c consists of a *melting time* t_m and an *arcing time* t_a.

The load fault energy, for a fuse link resistance R, is

$$W_{tot} = \int_0^{t_c} i^2 R \, dt \qquad \text{(J)}$$

If the load current, shown in figure 10.l0a, during fuse action is assumed to be triangular, then the clearing integral of the fuse is

$$W_c = \tfrac{1}{3} I_p^2 t_c R \qquad \text{(J)} \qquad (10.32)$$

If the resistance R is assumed constant (because of its low resistivity temperature co-efficient), the value of I^2t ($\frac{1}{3}I_p^2t_c$) is proportional to the energy fed to the protected circuit. The I^2t term is called the *total let-through energy* or the *virtual clearing integral* of the fuse. The energy which melts the fuse is proportional to $\frac{1}{3}I_p^2t_m$ and is termed the *pre-arcing* or *melting* I^2t.

10.2.1i - Pre-arcing I^2t

Before a fuse melts, the fuse is affected only by the current flowing. The pre-arcing or melting I^2t characteristics of fuse links are therefore only a function of prospective fault current and are independent of voltage. For melting times longer than 5-10 ms, the time-current characteristics are usually used for design. Typical time-current characteristics for four different current rated fuses are shown in figure 10.12. For times less than a millisecond, the melting I^2t reduces to a minimum and the pre-arcing I^2t characteristics shown in figure 10.13 are most useful.

The peak let-through current I_p, is a function of prospective fault current I_a for a given supply voltage. Typical current cut-off characteristics are shown in figure 10.14.

10.2.1ii - Total I^2t let-through

For fuse operating times of less than about 10 milliseconds the arcing I^2t can be considerably larger than the pre-arcing I^2t and it varies considerably with system voltage, fault level, power factor, and the point on the wave when the fault is initiated. The higher the voltage the more onerous is the duty of the fuse link because of the increase in energy absorbed by the fuse link during the arcing process. Under short-circuit conditions this leads to an increase in I^2t let-through with voltage. The I^2t let-through will decrease with increased supply frequency whereas the cut-off current will increase.

The peak arc voltage after melting is usually specified for a given fuse link type and is a function of supply voltage, as indicated by the typical arcing voltage characteristics in figure 10.15. The faster the fault is cleared, the higher the arc voltage V_p. Typical total I^2t let-through values for total operating times of less than 10 ms, at a given voltage, are shown in figure 10.16. Derating factors are shown in figure 10.17.

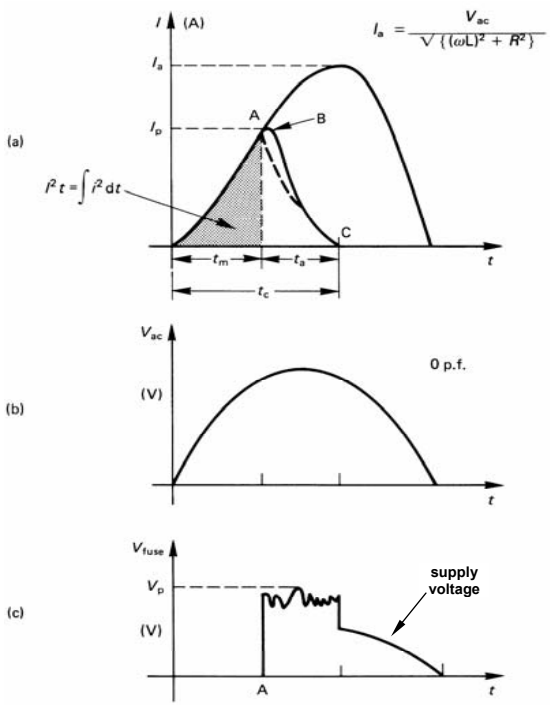

Figure 10.11. *Parameters of a fuse link operating: (a) current waveforms; (b) supply voltage; and (c) fuse arcing voltage.*

10.2.1iii - Fuse link and semiconductor I^2t co-ordination

Difficulties arise in matching fuses with semiconductors because each has very different thermal and electrical properties.

Semiconductor manufacturers publish (mainly for diodes and thyristors) I^2t withstand values for their devices for times less than 10 ms. To ensure fuse link protection the total I^2t let-through by the fuse link under appropriate circuit conditions should be less than the I^2t withstand ability of the semiconductor.

Fuse link manufacturers usually give the data shown in figures 10.12-10.17. In ac applications the parameters on which the semiconductor withstand capability is normally compared to the fuse link are

- Peak let-through current versus clearing time or clearing I^2t
- Applied voltage
- Power factor.

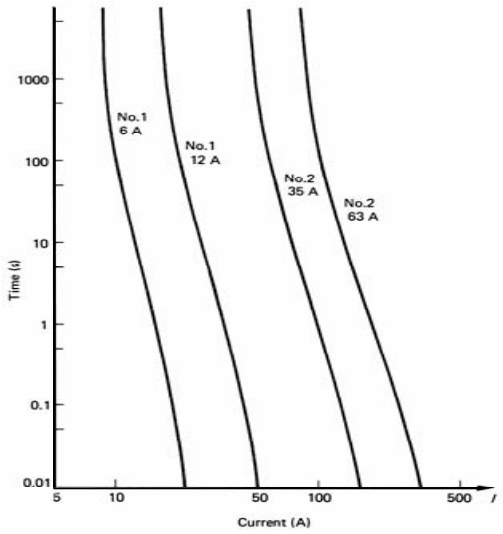

Figure 10.12. *Fuse-link time-current characteristics for four fuses and symmetrical sinusoidal 50 Hz currents.*

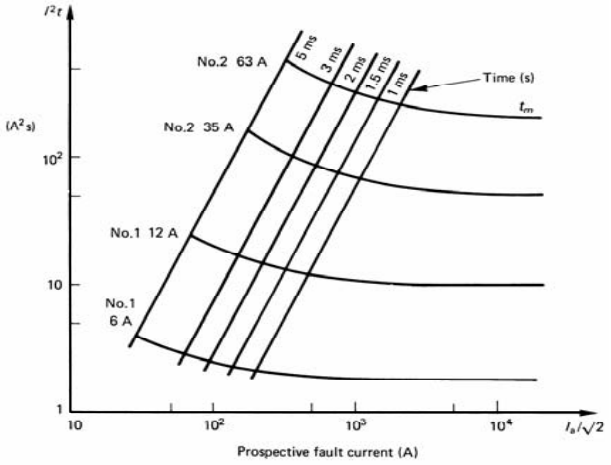

Figure 10.13. *Pre-arcing I^2t characteristics of four fuse links.*

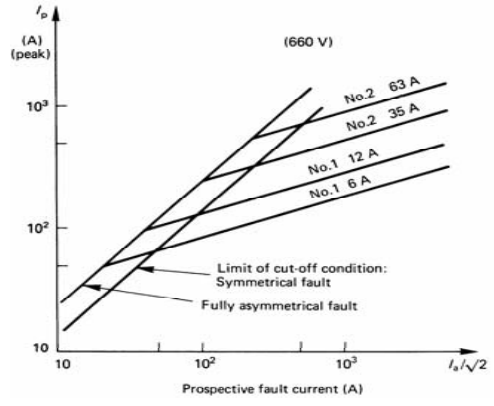

Figure 10.14. *Fuse-link cut-off characteristics at 660 V rms.*

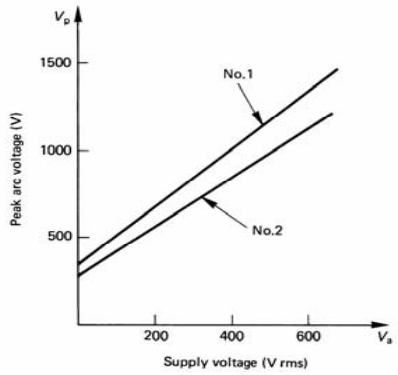

Figure 10.15. *Typical peak arc voltage for two different fuse-link types.*

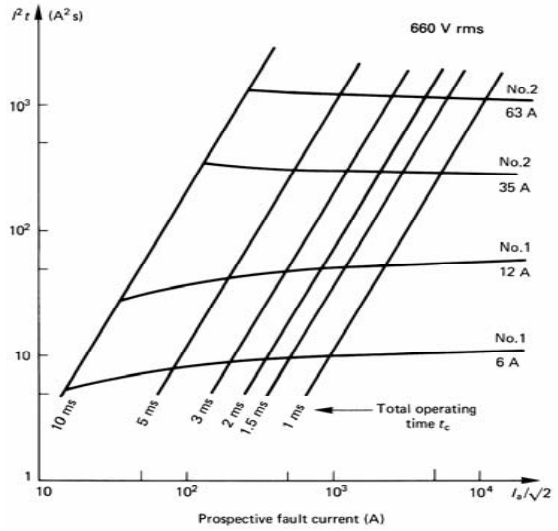

Figure 10.16. *Total let-through current for total fuse-link operating times of less than 10 ms and at 660 V rms.*

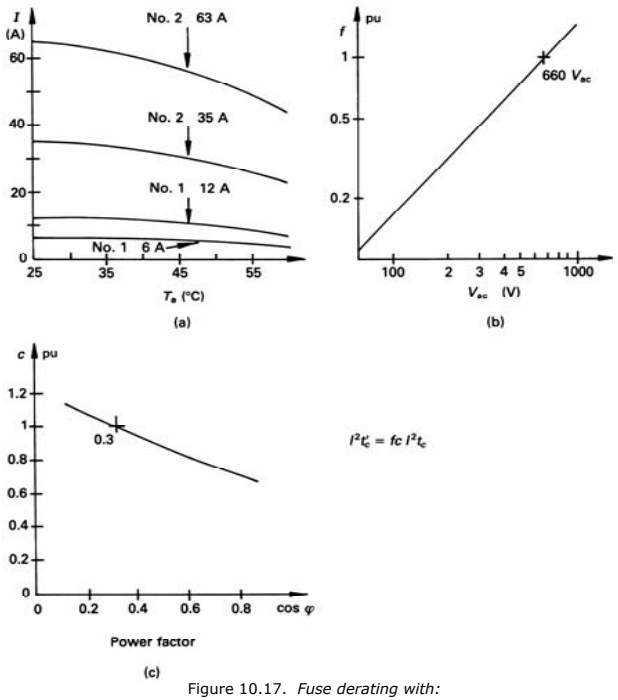

Figure 10.17. *Fuse derating with:*
(a) ambient temperature; (b) ac supply voltage; and (c) power factor.

Fuse protection in dc circuits represents greater difficulty than for ac circuits. No natural ac period current zeros exist and faults can result in continuous arcing, depending on the circuit L/R time constant, prospective fault, and supply voltage. Thus in dc applications the essential parameters are

- Peak let through current versus clearing time or clearing I^2t
- Applied voltage
- Prospective fault *di/dt*
- Time constant.

It may be possible in some applications to use an ac fuse in a dc circuit, before the rectification stage. Generally low voltage fuses are more effective than high voltage fuses. In high voltage transformer applications satisfactory protection may be afforded by transferring the fuse to the low voltage side. The fuse I^2t rating is transferred as with impedance transferring, that is, in the turns ratio squared.

$$I^2t_{fuse}^{primary} = \left(\frac{V_s}{V_p}\right)^2 \times I^2t_{semiconductor}^{secondary} \qquad (10.33)$$

Alternatively an mcb (miniature circuit breaker) may offer better protection in cases when the fault is more of an overload such that the current magnitude is limited. On overload, the mcb takes a longer time to clear than a fuse, thus the mcb is less prone to nuisance tripping.
Fuse protection is mainly applicable to more robust devices such as thyristors and diodes. Transistors (MOSFETs more readily than IGBTs) usually fail as a result of overcurrent before any fuse link can clear the fault.

Example 10.5: ***AC circuit fuse design***

A fast acting fuse is connected in series with a thyristor in a 415 V ac, 50 Hz ac application. The average current in the thyristor is 30 A at a maximum ambient temperature of 45°C. The ratings of the thyristor are

$I_{T(AV)}$ = 45 A @ T_c = 85°C
I_{TRMS} = 80 A
I^2t = 5 k A^{2}s for 10 ms @ 125°C
I^2t = 20 k A$^2\sqrt{}$s
I_{TSM} = 1000 A for 10 ms @ 125°C and V_{RRM} = 0

The fault circuit inductance is 1.32 mH and the resistance is negligible. Using the figures 10.12 to 10.17, select a suitable fuse.

Solution

From figure 10.17a, the 35 A rms No. 2 fuse is rated at 30 A rms in a 45°C ambient.
From figure 10.15 the peak arc voltage for a type No. 2 fuse will be less than 1200 V, hence the thyristor voltage rating must be greater than 1200 V.
The short circuit or prospective rms symmetrical fault current is

$$I_{sc} = \frac{I_a}{\sqrt{2}} = \frac{V_s}{X_L} = \frac{415\text{V}}{2\pi \times 50\text{Hz} \times 1.32\text{mH}} = 100\text{A}$$

Figure 10.13 gives a fuse peak let through current of 500 A, which is less than the thyristor peak current rating of 1 kA.
Figure 10.16 gives the fuse total I^2t of 300 A^{2}s and the total clearing time of t_c =3.5 ms. Since the fuse clears in less than 10 ms (½ ac cycle), the thyristor re-applied V_{RRM} will be zero and an I_{TSM} = 1000 A rating is applicable. The total I^2t is corrected for voltage (415V ac) and power factor (0 pu) with f = 0.6 and c = 1.2 from figures 10.17b and c.

$$I^2t' = f \times c \times I^2t = 0.6 \times 1.2 \times 300\ \text{A}^2\text{s} = 216\ \text{A}^2\text{s}$$

which is significantly less than the thyristor I^2t rating of 5 kA^{2}s.
Since t_c is less than 10 ms, the $I^2\sqrt{t}$ rating of the thyristor is used.

$$I^2t'' = (I^2\sqrt{t})\sqrt{t_c}$$
$$= 20\ \text{kA}^2\sqrt{\text{s}} \times \sqrt{3.5\ \text{ms}} = 1.18\ \text{kA}^2\text{s}$$

which is significantly greater than the I^2t (216 A^2s) of the fuse.
Since the fuse peak let through current (500 A) is less than the thyristor peak surge current rating (1000 A), and the fuse I^2t rating (216 A^2s) is significantly less than that for the thyristor (1180 A^2s), the proposed 35 A fast acting fuse should afford adequate protection for the thyristor.
Generally, if the rms current rating of the fuse is less than the average current rating of the thyristor or diode, the fuse will provide adequate protection under fault conditions.

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10.2.2 Overvoltage

Voltage transients in electrical circuits result from the sudden release of previously stored energy, such as insulation breakdown arcing, fuses, contactors, freewheeling diode current snap, switches, and transformer energising and de--energising. These induced transients may be repetitive or random impulses. Repetitive voltage spikes are observable but random transients are elusively, unpredictable in time and location. A spike is usually brief but may result in high instantaneous power dissipation. A voltage spike in excess of a semiconductor rating for just a few microseconds usually results in catastrophic device failure. Extensive noise may be injected into low-level control logic causing spurious faults. Generally, high-frequency noise components can be filtered, but low-frequency noise is difficult to attenuate.
Effective transient overvoltage protection requires that the impulse energy be dissipated in the added transient absorption circuit at a voltage low enough to afford circuit survival.

10.2.2i - Transient voltage suppression devices

Two types of voltage transient suppression techniques can be employed.

- **Transient voltage attenuation**
  Low pass filters, such as an *L-C* filter, can be used to attenuate high frequencies and allow the low-frequency power to flow.
- **Diverter (to limit the residual voltage)**
  Voltage clamps such as crowbars or snubbers are usually slow to respond. The crowbar will be considered in section 10.2.3 while the snubber, which is for low-energy applications, has been considered in section 8.2.

The voltage-limiting function may be performed by a number of non-linear impedance devices such as reverse selenium rectifiers, avalanche (commonly called Zener) diodes, and varistors made of various materials such as silicon carbide or zinc oxide.

The relationship between the current in the non-linear device, *I,* and the voltage across its terminals, *V,* is typically described by the power law

$$I = kV^{\alpha} \quad \text{(A)} \qquad (10.34)$$

k is an element constant dependent on device geometry in the case of the varistor, and the non-linear exponent α is defined as

$$\alpha = \frac{\log I_2 - \log I_1}{\log V_2 - \log V_1} = \frac{\log I_2/I_1}{\log V_2/V_1} \qquad (10.35)$$

where I_1 and I_2 are taken a decade apart. The term alpha (α) represents the degree of non-linearity of the conduction. The higher the value of alpha, the better the clamp and therefore alpha may be used as a figure of merit. A linear resistance has an alpha of 1 ($I = \frac{1}{R}V^{+1}$).
The voltage-dependent resistance is given by

$$R = V/I = V/kV^{\alpha} = \tfrac{1}{k}V^{1-\alpha} \quad (\Omega) \qquad (10.36)$$

and the power dissipation is

$$P = VI = V\,kV^{\alpha} = kV^{\alpha+1} \quad \text{(W)} \qquad (10.37)$$

The most useful transient suppressors are the Zener diode and the varistor. They are compact devices which offer nanosecond response time and high energy capability.

1 - The Zener diode is a very effective clamp and comes the closest to being a constant voltage clamp, having an alpha of 35. Since the avalanche junction area is small and not highly uniform, substantial heating occurs in a small volume. The energy dissipation of the Zener diode is limited, although transient absorption Zener devices with peak instantaneous powers of 50 kW are available. These peak power levels are obtained by:

- Using diffusion technology, which leads to low metallisation contact resistance, narrow base width, and minimises the temperature coefficient.
- Achieving void-free soldering and thermal matching of the chip and the large area electrodes of copper or silver. Molybdenum buffer electrodes are used.
- Using bulk silicon compatible glass passivation which is alkali metal contamination free, and is cut without glass cracking.

Voltage ratings are currently limited to 280 V but devices can be series connected for higher voltage application. This high-voltage clamping function is unipolar and back-to-back series connected Zener diodes can provide high-voltage bipolar clamping.

2 - The varistor is a ceramic, bipolar, non-linear semiconductor utilising silicon carbide for continuous transient suppression or sintered zinc oxide for intermittent dissipation. Approximately 90 per cent by weight of zinc oxide and suitable additives such as oxides of bismuth, cobalt, and manganese, can give varistors with alphas better than 25. The structure of the plate capacitor like body consists of a matrix of conductive zinc oxide grains separated by grain boundaries, providing pn junction semiconductor-type characteristics. The grain sizes vary from

approximately 100 μm for low-voltage varistors down to 20 μm for high voltage components. The junctions block conduction at low voltage and provide non-linear electrical characteristics at high voltage. Effectively pn junctions are distributed throughout the structure volume, giving more uniformly distributed heat dissipation than the plane structure Zener diode. The diameter determines current capability, hence maximum power dissipation, while thickness specifies voltage. The structure gives high terminal capacitance values depending on area, thickness, and material processing. The varistor may therefore be limited in high-frequency applications. Functionally the varistor is similar to two Zener diodes connected back-to-back, in series.

10.2.2ii - Comparison between Zener diodes and varistors

Figure 10.18a illustrates the *I-V* characteristics of various voltage clamping devices suitable for 240 V ac application. The resistor with alpha equal to 1 is shown for reference. It is seen that the higher the exponent alpha, the nearer an ideal constant voltage characteristic is attained, and that the Zener diode performs best on these grounds. When considering device energy absorption and peak current and voltage clamping level capabilities, the Zener diode loses significant ground to the varistor.

The higher the alpha, the lower will be the standby power dissipated. Figure 10.18b shows the dependence of standby power dissipation variation on withstand voltage for various transient absorbers. A small increase in Zener diode withstand voltage produces a very large increase in standby power dissipation. Various device compromises are borne out by the comparison in table 10.1.

The current, power, and energy ratings of varistors are, typically, rated values up to 85°C, then linearly derated to zero at a case temperature of 125°C. Voltage-limiting diodes are typically linearly derated from rated values at 75°C to zero at 175°C. Reliability depends on the ambient temperature and applied voltage, and lifetime decreases with increased voltage or temperature. In the case of the varistor, an 8 per cent increase in applied voltage halves the mean time between failure, mtbf, for applied voltages less than 0.71 times the nominal voltage. Below 40°C ambient, the mtbf for a varistor is better than 7×10^8 hours.

The voltage temperature coefficient for the varistor is - 0.05 per cent/K while +0.1 per cent/K is typical for the power Zener.

The following design points will specify whether a Zener diode or varistor clamp is applicable and the characteristics of the required device.

- Determine the necessary steady-state voltage rating.
- Establish the transient energy to be absorbed by the clamp.
- Calculate the peak transient current through the clamp.
- Determine power dissipation requirements.
- Determine the clamping voltage to which the transient is to be suppressed.
- Estimate the number of fault cycles during the lifetime.

In order to meet higher power ratings, higher voltage levels or intermediate voltage levels, Zener diodes or varistors can be series-connected. The only requirement is

that each series device has the same peak current rating. In the case of the varistor this implies the same disc diameter. Then the *I-V* characteristics, energy rating, and maximum clamping voltages are all determined by summing the respective characteristics and ratings of the individual devices.

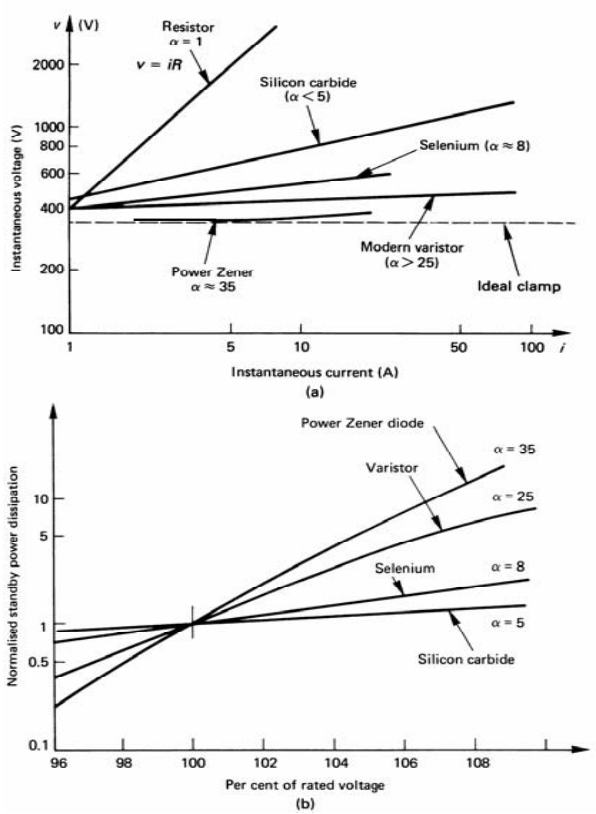

Figure 10.18. *(a) The I—V characteristics of four transient voltage suppressor devices, with resistance characteristics for reference and (b) standby power dissipation characteristics showing the higher the alpha the lower the standby power dissipation.*

Parallel operation is difficult and matched *I-V* characteristics are necessary. A feature of varistors often overlooked is deterioration. Figure 10.19a shows that at relatively low energy levels an infinite number of transients can be absorbed, while at rated absorbed energy only one fault is allowed. This single fault, lifetime, is defined as that energy level that causes a 10 per cent increase in clamping voltage level, for a specified current density.

Figure 10.19b shows that very high currents can be tolerated for short intervals. The lower the pulse number, the higher the allowable current.

The failure mode of the Zener diode and varistor is a short circuit. Subsequent high current flow may cause an explosion and disintegration of contacts, forming an open circuit. This catastrophic condition can be avoided by fuse protection.

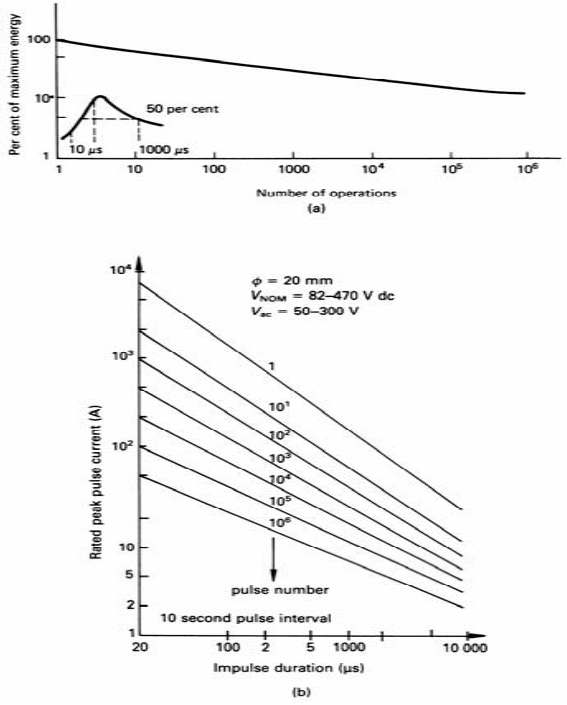

Figure 10.19. *Pulse lifetime ratings for a Zinc oxide varistor: (a) lifetime for fixed 10/100μs pulses and (b) lifetime number for variable-duration square-wave pulses.*

Table 10.1 A comparison of typical voltage transient suppressor characteristics

Suppressor type	Standby current (mA)	Peak current at 1 ms exp. (A)	Peak power at 1 ms (kW)	Peak energy (J)	Voltage clamping ratio at 10 A	Voltage range dc	Capacitance at 1 MHz (nF)
Silicon carbide varistor	5	-	-	50	4.6	15–300	-
Selenium	12	30	9	9	2.3	35–700	-
Metal oxide varistor	1	120	40	70	1.7	14–1200	2
Zener diode (5 W)	0.005	5.5	1.5	2	1.4	1.8–280	1

Example 10.6: ***Non-linear voltage clamp***

Evaluate the current of a 1mA @ 250 V Zener diode when used to clamp at 340V dc. Calculate the percentage decrease in voltage-dependent resistance and the per unit increase in power dissipation, assuming $\alpha = 30$.

Solution

From $I = kV^{\alpha}$, equation (10.34)

i. $I_2 = I_1(V_2/V_1)^{\alpha} = 1\text{ mA}\,(340\text{V}/250\text{V})^{30} = 10.14\text{ A}$
The Zener diode will conduct 10.14A when clamping at 340 V (a 10,140 increase on the standby current of 1mA)

ii. From equation (10.36), $R = V^{1-\alpha}/k$ therefore

$$1-\frac{R_2}{R_1} = 1-\left(\frac{V_2}{V_1}\right)^{1-\alpha} = 1-\left(\frac{340\text{V}}{250\text{V}}\right)^{-29} = 0.99987$$

The percentage decrease in resistance is 99.987 per cent.
The dynamic resistance decreases from (250 V / 1 mA) 250 kΩ to (340 V / 10.1 A) 33.5Ω. The incremental resistance (dv/di) reduces 10,000 to 1.

iii. $P = kV^{\alpha+1}$ (equation (10.37))

$$\frac{P_2}{P_1}-1 = \left(\frac{V2}{V1}\right)^{31} - 1 = \left(\frac{340\text{V}}{250\text{V}}\right)^{31} - 1 = 13793.5$$

The per unit power increase is 13,800.
The power increases from (250 V × 1 mA) 0.2 W at standby to (340 V × 10.14A) 3447.6 W when clamping at 340 V dc.

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10.2.3 Crowbar

A *crowbar* can be used for overvoltage and/or overcurrent protection in both ac and dc circuits. Figure 10.20 illustrates how an SCR can be used to provide fault protection for sensitive dc power electronic circuits and loads. Whenever a fault condition occurs the crowbar SCR is triggered, shorting the supply. The resultant high supply current flowing blows the fuse, or initiates a fast-acting circuit breaker/mcb, thereby isolating the load from the supply. The diode D_c provides a current path for inductive load energy.

The load current is measured by the voltage across the sense resistor *R.* When this voltage reaches a preset limit, that is the load current has reached the fault level, the SCR is triggered. The load or dc link voltage is measured from the resistor divider R_2-R_3. When this voltage exceeds the pre-determined limit the SCR is triggered and the fuse is blown by the crowbar short-circuit current, isolating the sensitive load from the supply.

A judiciously selected crowbar SCR can conduct many times its average current rating. For the few milliseconds in which the fuse is isolating, the SCR I^2t surge current feature can be exploited. The SCR I^2t rating must be larger than the fuse total I^2t rating. If the SCR crowbar is fuse-link protected then the total I^2t of the dc-link fuse link must be less than the pre-arcing I^2t of the SCR crowbar fuse link.

An ac crowbar can comprise two antiparallel-connected SCR's across the fuse-protected ac line, or alternatively one SCR in a four diode rectifying bridge.

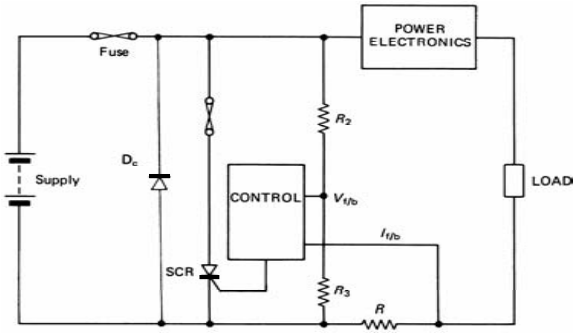


Figure 10.20. *An SCR crowbar for overvoltage and over-current protection.*

10.2.4 Noise

RFI noise (electromagnetic interference, EMI) and the resultant equipment interaction is an area of power electronic design that is often overlooked.

EMI is due to the effects of undesired energy transfer caused by radiated electromagnetic fields or conducted voltages and currents. The interference is

produced by a source emitter and is detected by a susceptible victim via a coupling path. The source itself may be a self-inflicted victim. The effects of this interference can vary from simple intermittent reset conditions to a catastrophic failure.

The coupling path may involve one or more of the following coupling mechanisms.

- *Conduction* - electric current
- *Radiation* - electromagnetic field
- *Capacitive coupling* - electric field
- *Inductive coupling* - magnetic field

10.2.4i - Conducted noise is coupled between components through interconnecting wiring such as through power supply (both ac and dc supplies) and ground wiring. This common impedance coupling is caused when currents from two or more circuits flow through the same wiring impedance. Coupling can also result because of common mode and differential currents, which are illustrated in figure 10.21.

10.2.4ii - Radiated electromagnetic field coupling can be considered as two cases, namely

- near field, $r \ll \lambda / 2\pi$, where radiation due to electric fields, *E*, and magnetic fields, *H*, are considered separate
- far field, $r \gg \lambda / 2\pi$, where the coupling is treated as a plane wave.

The boundary between the near and far field is given by $r = \lambda / 2\pi$ where λ is the noise wavelength and *r* is distance from the source.

In the far field, the characteristic impedance of free space Z_o, given by E / H, is constant, $\sqrt{\mu_o / \varepsilon_o} = 120\pi = 377\Omega$.

In the *near field* region, r^{-3} (as opposed to $r^{-2}$and r^{-1}) terms dominate field strength.

- A wire currying current produces $E \alpha r^{-3}$and $H \alpha r^{-2}$,
  - thus the electric field *E* dominates and the wave impedance $Z > Z_o$.
- A wire loop carrying current produces $H \alpha r^{-3}$and $E \alpha r^{-2}$,
  - thus the magnetic field *H* dominates and the wave impedance $Z < Z_o$.

In the near field, interference is dominated by the effective input impedance, Z_{in}, of the susceptible equipment and the source impedance R_s of its input drive.

- Electric coupling increases with increased input impedance, while
- magnetic coupling decreases with increased input impedance.

That is, electric fields, *E*, are a problem with high input impedance (because the induced current results in a high voltage similar to that given by equation (10.38)),

$$v = i_c \times R_s // Z_{in} = C_c \, dv / dt \times R_s // Z_{in} \qquad (10.38)$$

while magnetic fields, *H*, are a problem with low input impedance (because the induced voltage results in a high current similar to that given by equation (10.39)).

$$i = v_c / R_s // Z_{in} = M \, di / dt / R_s // Z_{in} \qquad (10.39)$$

In the *far field* the r^{-1} term dominates.

In the far field region both the *E* and *H* fields are in phase and at right angles. Importantly their magnitudes both decrease, inversely proportionally with distance *r*, so their magnitude ratio remains constant. That is, the characteristic impedance is $Z_o = \sqrt{\mu_o / \varepsilon_o} = 120\pi = 377\Omega$. The far field radiation wave with this constant

impedance is termed a plane wave. The electric field component of the plane wave tends to dominate interface problems in the far field region.

10.2.4iii - Electric field coupling is caused by changing voltage differences, *dv/dt*, between conductors. This coupling is usually modelled by capacitance.
The changing electric field produces a current according to $i = C_c dv/dt$, where coupling capacitance C_c is dependant distance of separation, area, and the permittivity of the media. The effect of the produced current is dependant on the source impedance R_s and the effective input impedance, Z_{in}, of the victim equipment as given by equation (10.38).

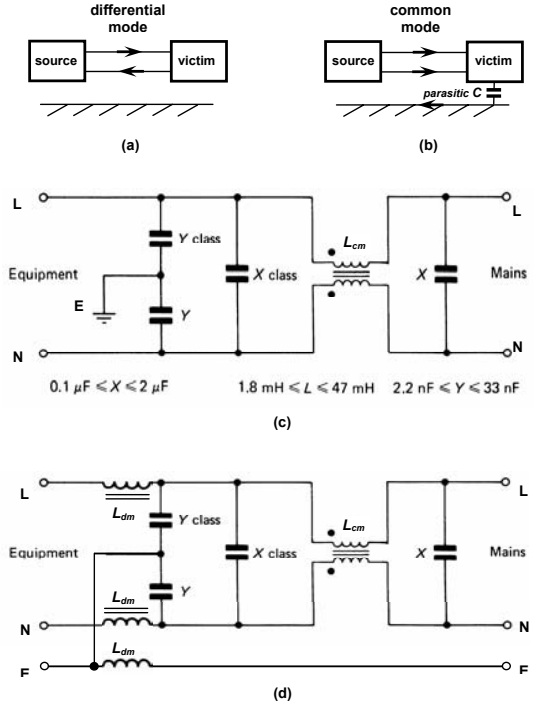


Figure 10.21. *Common mode and differential mode mains supply noise filtering: (a) differential mode noise paths; (b) common mode noise paths; (c) simple L-C mains filter; and (d) high specification mains filter.*

10.2.4iv - Magnetic field coupling is due to changing currents, *di/dt*, flowing in conductors. This coupling mechanism is usually modelled by a coupled circuit, or a transformer, according to $v=Mdi/dt$, where the resultant current is given by equation (10.39). The mutual inductance M is related to loop area, orientation, separation distance, and screening and its permeability. This induced voltage is independent of any ground connection or electrical connection between the coupled circuits. Magnetic field problems tend to be at low frequencies. Below 100kHz effective screen materials are steel, mu-metal (μ_r = 20,000), and permalloy, while at higher frequencies the good electrical conduction properties of copper and aluminium are more effective despite there much lower permeabilities.

10.2.5 Mains filters

The conducted ac mains borne noise can be attenuated to safe levels by filtering. The simplest type of filter is an inductor in series with the load in order to reduce any current *di/dt* changes. It is usual practice to use *L-C* filtering, which gives second-order attenuation. The typical circuit diagram of a mains voltage filter, with common mode noise filtering, is shown in figure 10.21c. The core inductance is only presented to any ampere turn imbalance (common mode current), not the much larger principle throughput (go and return) ac current, hence the core dimensional requirements can be modest. Extra non-coupled inductance is needed for differential mode filtering, as shown in figure 10.21d. Only the higher frequency noise components can be effectively attenuated since the filter must not attenuate the 50 Hz mains component.

10.2.6 Noise filtering precautions

For power electronics, circuit noise suppression and interaction is ultimately based on try-it and see. Logic does not necessarily prevail. The noise reduction precautions to follow are orientated towards power electronics applications.
Good circuit layout and construction (incorporated at the initial design stage) can greatly reduce the radiated noise, both transmitted and received. Obvious starting points are minimising wire loop lengths, using ground planes, capacitor decoupling, twisted wire pairs, and judicious placement of magnetic components. Use opto-couplers, not only to isolate signals but to allow flexible grounding that can bypass ground power noise around sensitive circuitry. Sensitive electronic circuitry should be rfi radiation protected by copper (electric and high frequency magnetic) or mild steel (low frequency magnetic) sheeting, depending on the type of radiation and frequency. Shielding, including isolated heatsinks, should be connected to a point that minimises interference. This may involve connection to supply rails (positive, zero, negative) or ground.
An *R-C* snubber across a diode decreases *dv/dt* while a series inductive snubber will limit *di/dt*. Mains series input inductors for bridge rectifiers (plus diode *R-C* snubbers) decrease the amount of diode recovery noise injected back into the mains and into the equipment. In ac circuit applications, zero-voltage turn-on and zero-current turn-off minimise any rapid changes in current, thus reducing radiation. To minimise diode recovery noise, slow down switch turn-on.

To minimise interactive noise effects, high noise immune circuit designs can be employed which utilise mos technology. The high-voltage input thresholds of cmos logic (4000 series), 74AC (not ACT) logic series, and power MOSFETs (high gate threshold and capacitance), offer circuit noise immunity. Since noise possesses both magnitude and duration, the much slower response times (but with high input thresholds) of 4000 HEF series cmos may result in better noise immunity in applications requiring clock frequencies below a few megahertz.
DSP core operating voltages below a few volts have necessitate: the use of a multilayer pcbs with ground planes, carefully layout separating of analogue and digital circuitry, low inductance ceramic chip decoupling, watchdog circuitry, etc.

Reading list

General Electric Company, *Transient Voltage Suppression,*
400.3, 1982.

Grafham, D.R. *et al., SCR Manual,*
General Electric Company, 6th Edition, 1979.

Williams, T., *EMC for Product Designers*,
Newnes, 2nd Edition, 1998.

Problems

10.1. Derive an expression for the worst case maximum allowable voltage-sharing resistance for n series devices each of voltage rating V_D and maximum leakage I_m across a supply V_s. The resistance tolerance is ± 100a per cent and the supply tolerance is ± 100b per cent.
If V_s = 1500 V, V_D = 200 V, I_m = 10 mA, n = 10 and tolerances are ±10 per cent, calculate resistance and maximum total power losses if

i. tolerances are neglected
ii. only one tolerance is considered
iii. both tolerances are included.

[i. R <5.5 kΩ, 63.8 W; ii. R <2.1 kΩ, 185 W; R <3.9 kΩ, 91 W; iii. R <280 Ω, 1234 W].

10.2. Derive a power loss expression for a voltage-sharing resistance network in which both supply and resistance tolerances are included. Assume a dc reverse bias of duty cycle δ.

10.3. Derive the power loss expression for an SCR string with voltage-sharing resistance and an ac supply.

10.4. Two diodes modelled as in figure 2.4a having characteristics approximated in the forward direction by

Diode D_1: $V_F = 1.0 + 0.01\ I_F$ (V)
Diode D_2: $V_F = 0.95 + 0.011\ I_F$ (V)

are connected in parallel. Derive general expressions for the voltage across and the current in each diode if the total current is 200 A.
At what total current and voltage will the diodes equally share?
[102.4 A, 97.6 A, 2.02 V; 100 A, 1.5 V]

10.5. In problem 10.4, what single value of resistance in series with each parallel connected diode match the currents to within 1 per cent of equal sharing? Calculate the resistor maximum power loss.
How will the current share at I_T = 100 A & I_T = 500A with the balancing resistors.
[14.5 mΩ, 148 W; 50 A, 50 A; 254 A, 246 A]

10.6. A Zener diode has an I-V characteristic described by $I = kV^{30}$. What percentage increase in voltage will increase the power dissipation by a factor of 1000? [25 per cent]

10.7. What is the percentage decrease in the dynamic resistance of the Zener diode in question 10.6? [99.845 per cent]

10.8. A string of three 2,600 V thyristors connected in series is designed to withstand an off-state voltage of 7.2 kV. If the compensating circuit consists of a series 33 Ω, 0.01 μF snubber in parallel with a 24 kΩ resistor, across each thyristor, and the leakage currents for the thyristors are 20 mA, 25 mA, and 15 mA, at 125°C, calculate the voltage across each thyristor, then the discharge current of each capacitor at turn-on.
[2400 V, 2280 V, 2520 V, 72.73 A, 69.09 A, 76.36 A]

10.9. The reverse leakage current characteristics of two series connected diodes are

Diode D_1: $I_1 = -10^{-4}\ V_1 + 0.14$ (A) for $V_1 < -1400$ V
Diode D_2: $I_2 = -10^{-4}\ V_2 + 0.16$ (A) for $V_2 < -1600$V

If the resistance across diode D_1 is 100 kΩ and $V_{D1} = V_{D2} = -2000$ V, what is the leakage current in each diode and what resistance is required across diode D_2?
[0.34 mA, 0.36 mA, ∞]

10.10. Two high voltage diodes are connected in series as shown in figure 10.5a. The dc input voltage is 5 kV and 10 kΩ dc sharing resistors are used. If the reverse leakage current of each diode is 25mA and 75mA respectively, determine the voltage across each diode and the resistor power loss.
[2750 V, 2250 V, 756.25 W, 506.25 W]

10.11. The forward characteristics of two parallel connected diodes are

Diode D_1: $I_1 = 200\ V_1 - 100$ (A) for $V_1 \geq 0.5$ V

Diode D_2: $I_2 = 200\ V_2 - 200$ (A) for $V_2 \geq 1$V

If the forward voltage of the parallel combination is 1.5V, determine the forward current through each diode. [200 A, 100 A]

10.12. Two diodes are connected in parallel and with current sharing resistances as shown in figure 10.7. The forward *I-V* characteristics are as given in problem 10.11. The voltage across the parallel combination is 2V and the balancing resistors are equal in value. Calculate each diode voltage and current. Calculate resistor maximum power loss. Let $I_{tot} = 400$ A.

11

Naturally Commutating Converters

The converter circuits considered in this chapter have in common an ac supply input and a dc load. The function of the converter circuit is to convert the ac source into controlled dc load power, mainly for high inductive loads. Turn-off of converter semiconductor devices is brought about by the ac supply reversal, a process called *line commutation* or *natural commutation.*

Converter circuits employing only diodes are termed *uncontrolled* while the incorporation of only thyristors results in a *controlled converter.* The functional difference is that the diode conducts when forward-biased whereas the turn-on of the forward-biased thyristor can be controlled from the gate. An uncontrolled converter provides a fixed output voltage for a given ac supply.

Converter circuits employing a combination of both diodes and thyristors are generally termed *half-controlled.* Both fully controlled and half-controlled converters allow an adjustable output voltage by controlling the phase angle at which the forward biased thyristors are turned on. The polarity of the load voltage of a fully controlled converter can reverse, allowing power flow into the supply, a process called *inversion.* Thus a fully controlled converter can be described as a *bidirectional converter* as it facilitates power flow in either direction.

The half-controlled converter, as well as the uncontrolled converter, contains diodes which prevent the output voltage from going negative. Such converters only allow power flow from the supply to the load, termed *rectification,* and can therefore be described as *unidirectional converters.*

Although all these converter types provide a dc output, they differ in characteristics such as output ripple and mean voltage as well as efficiency and supply harmonics. Another converter characteristic is that of pulse number, which is defined as the repetition rate in the direct output voltage during one complete cycle of the input ac supply.

The general analysis in this chapter is concerned with single and three-phase supplies feeding inductive loads. A load back emf is used in modelling the dc machine.

11.1 Single-phase uncontrolled converter circuits

11.1.1 Half-wave circuit with an R-L load

A simple half-wave diode rectifying circuit is shown in figure 11.la, while various circuit electrical waveforms are shown in figure 11.lb. Load current starts to flow when the supply goes positive at $\omega t = 0$. It will be seen that load current flows not only during the positive part of the supply voltage, $0 \leq \omega t \leq \pi$, but also during a portion of the negative supply voltage, $\pi \leq \omega t \leq \beta$. The load inductor stored energy maintains the load current and the inductor's terminal voltage reverses so as to overcome the negative supply and keep the diode forward-biased and conducting. This current continues until all the inductor energy, $\frac{1}{2}Li^2$, is released ($i = 0$) at the *current extinction angle, $\omega t = \beta$.*

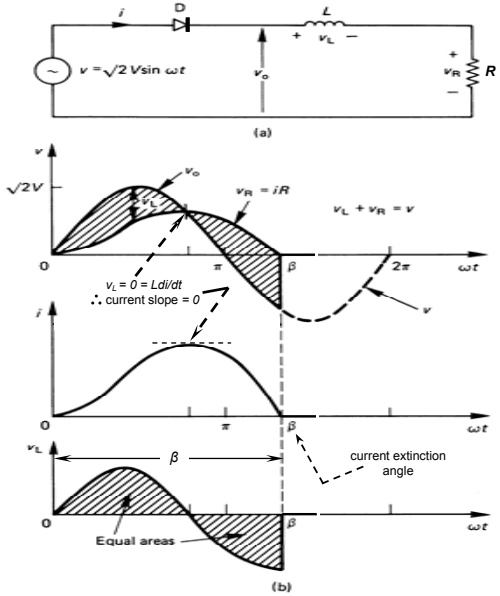


Figure 11.1. *Half-wave rectifier with an R-L load: (a) circuit diagram and (b) waveforms, illustrating the equal area and zero current slope criteria.*

During diode conduction the circuit is defined by the Kirchhoff voltage equation

$$L\frac{di}{dt} + Ri = \sqrt{2}\,V \sin \omega t \quad \text{(V)} \qquad (11.1)$$

where V is the rms ac supply voltage. Solving equation (11.1) yields the load current

$$i(\omega t) = \frac{\sqrt{2}V}{Z}\left\{\sin(\omega t - \phi) + \sin\phi\, e^{-\omega t/\tan\phi}\right\} \quad \text{(A)} \qquad (11.2)$$

$$0 \le \omega t \le \beta \quad \text{(rad)}$$

where $Z = \sqrt{(R^2 + \omega^2 L^2)}$ (ohms)

$\tan\phi = \omega L / R$

$$i(\omega t) = 0 \quad \text{(A)} \qquad (11.3)$$

$$\beta \le \omega t \le 2\pi \quad \text{(rad)}$$

The current extinction angle β is determined by the load impedance Z and can be solved from equation (11.2) when $i = 0$ with $\omega t = \beta$, such that $\beta > 0$, that is

$$\sin(\beta - \phi) + \sin\phi\, e^{-\beta/\tan\phi} = 0 \qquad (11.4)$$

This is a transcendental equation which can be solved by iterative techniques. Figure 11.2a can be used to determine the extinction angle β, given any load impedance angle $\phi = \tan^{-1}\omega L / R$.

The mean value of the rectified current, $\overline{I_o}$, is given by integration of equation (11.2)

$$\overline{I_o} = \frac{1}{2\pi}\int_0^{\beta} i(\omega t)\, d\omega t \quad \text{(A)} \qquad (11.5)$$

$$\overline{I_o} = \frac{\sqrt{2}V}{2\pi R}(1 - \cos\beta) \quad \text{(A)}$$

while the mean output voltage V_o is given by

$$V_o = \overline{I_o}R = \frac{\sqrt{2}V}{2\pi}(1 - \cos\beta) \quad \text{(V)} \qquad (11.6)$$

since the mean voltage across the load inductance is zero (see the equal area criterion below). Figure 11.2b shows the normalised output voltage V_o / V as a function of $\omega L/R$. The rms output voltage is given by

$$V_{rms} = \left[\tfrac{1}{2\pi}\int_0^{\beta}\left(\sqrt{2}\,V\right)^2 \sin^2\omega t\, d\omega t\right]^{\frac{1}{2}} = \frac{\sqrt{2}\,V}{2}\left[\tfrac{1}{\pi}\{\beta - \tfrac{1}{2}\sin 2\beta\}\right]^{\frac{1}{2}} \qquad (11.7)$$

11.1.1i - Equal area criterion

The average output voltage V_o, given by equation (11.6), is based on the fact that the average voltage across the load inductance, in steady state, is zero. The inductor voltage is given by

$$v_L = L\,di/dt \quad \text{(V)}$$

which for the circuit in figure 11.1a can be expressed as

$$\int_0^{\beta/\omega} v_L(t)\, dt = \int_{i_o}^{i_\beta} L\, di = L(i_\beta - i_0) \qquad (11.8)$$

If the load current is in steady state then $i_\beta = i_o$, which is zero here, and in general

$$\int v_L\, dt = 0 \quad \text{(Vs)} \qquad (11.9)$$

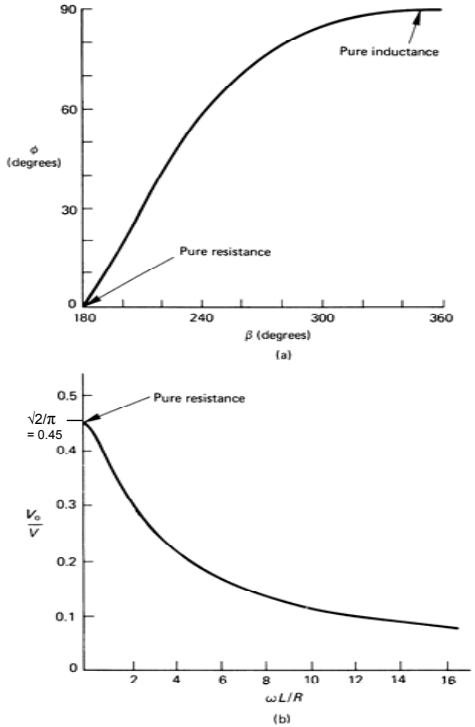


Figure 11.2. *Single-phase half-wave converter characteristics: (a) load impedance angle ø versus current extinction angle β and (b) variation in normalised mean output voltage V_o/V versus ωL/R.*

The inductor voltage waveform for the circuit in figure 11.la is shown in the last plot in figure 11.lb. The equal area criterion implies that the shaded positive area must equal the shaded negative area, in order to satisfy equation (11.9). The net inductor energy is zero. This is a useful aid in predicting and drawing the load current waveform.
It is useful to superimpose the supply voltage v, the load voltage v_o, and the resistor voltage v_R waveforms on the same time axis, ωt. The load resistor voltage, $v_R = Ri$, is directly related to the load current, i. The inductor voltage v_L will be the difference between the load voltage and the resistor voltage and this bounded area must be zero. The equal voltage areas associated with the load inductance are shown shaded in two plots in figure 11.1b.

11.1.1ii - Load current zero slope criterion

The load inductance voltage polarity changes from positive to negative as energy initially transferred into the inductor, is released. The stored energy in the inductor allows current to flow after the input ac voltage has reversed. At the instant when the inductor voltage reverses, its terminal voltage is zero, that is

$$v_L = L di/dt = 0$$
$$\text{that is} \quad di/dt = 0 \tag{11.10}$$

The current slope changes from positive to negative, whence the voltage across the load resistance ceases to increase and starts to decrease, as shown in figure 11.1b. That is, the Ri waveform crosses the supply voltage waveform with zero slope, whence when the inductor voltage is zero, the current begins to decrease. The fact that the resistor voltage slope is zero when v_L=0, aids prediction and sketching of the various circuit waveforms in figure 11.1b, and subsequent waveforms in this chapter.

11.1.2 Half-wave circuit with an R-L load and freewheel diode

The circuit in figure 11.1a, which has an *R-L* load, is characterised by discontinuous (i = 0) and high ripple current. Continuous load current can result when a diode is added across the load as shown in figure 11.3a. This freewheel diode prevents the voltage across the load from reversing during the negative half-cycle of the supply voltage. The stored energy in the inductor cannot reduce to zero instantaneously, so the current is forced to find an alternative path whilst decreasing towards zero. When diode D_1 ceases to conduct at zero volts it blocks, and diode D_f provides an alternative load current freewheeling path, as indicated by the waveforms in figure 11.3b.
The output voltage is the positive half of the sinusoidal input voltage. The mean output voltage is

$$V_o = \frac{1}{2\pi}\int_0^{\pi}\sqrt{2}V \sin\omega t \, d\omega t$$
$$V_o = \sqrt{2}V/\pi \quad = \quad 0.45\,V \qquad \text{(V)} \tag{11.11}$$

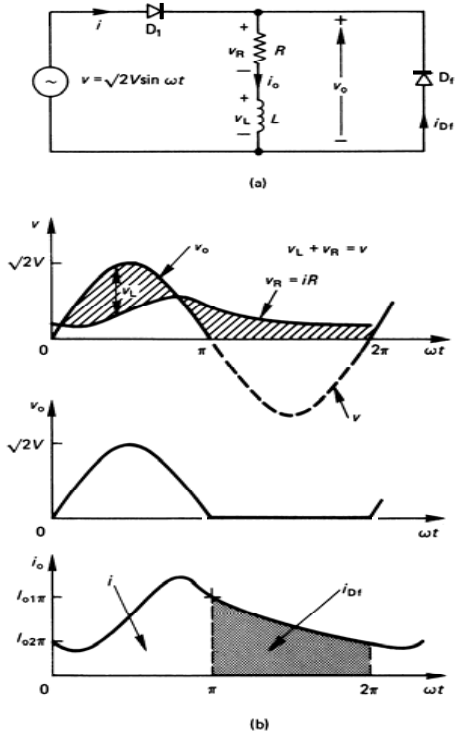


Figure 11.3. *Half-wave rectifier with a freewheel diode and an R-L load: (a) circuit diagram and parameters and (b) circuit waveforms.*

The rms value of the load circuit voltage v_0 is given by

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{\pi}\left(\sqrt{2}V\sin\omega t\right)^2 d\omega t}$$
$$= \sqrt{2}V/2 = 0.71V \qquad \text{(V)} \tag{11.12}$$

The output ripple voltage is defined as

$$V_{RI} \triangleq \sqrt{V_{rms}^2 - V_o^2} = \sqrt{\left(\sqrt{2}V/2\right)^2 - \left(\sqrt{2}V/\pi\right)^2} = 0.545\,V \quad (11.13)$$

hence the voltage ripple factor is defined as

$$K_v \triangleq V_{RI}/V_o = \sqrt{\left(\frac{V_{rms}}{V_o}\right)^2 - 1} = \sqrt{¼\pi^2 - 1} = 1.211 \quad (11.14)$$

After a large number of ac supply cycles, steady-state load current conditions are established, and the load current is defined by

$$L\frac{di}{dt} + Ri = \sqrt{2}\,V\sin\omega t \qquad \text{(A)} \qquad 0 \le \omega t \le \pi \quad (11.15)$$

and when the freewheel diode conducts

$$L\frac{di}{dt} + Ri = 0 \qquad \text{(A)} \qquad \pi \le \omega t \le 2\pi \quad (11.16)$$

During the period $0 \le \omega t \le \pi$, when the freewheel diode current is given by $i_{Df} = 0$, the supply current and load current are given by

$$i(\omega t) = i_o(\omega t) = \sqrt{2}V/Z\sin(\omega t - \phi) + (I_{o2\pi} + \sqrt{2}V/Z\sin\phi)e^{-\omega t/\tan\phi} \qquad \text{(A)} \quad (11.17)$$
$$0 \le \omega t \le \pi$$

for

$$I_{o2\pi} = \sqrt{2}V/Z\sin\phi\,\frac{1+e^{-\pi/\tan\phi}}{e^{\pi/\tan\phi} - e^{-\pi/\tan\phi}} \qquad \text{(A)}$$

where $Z = \sqrt{R^2 + (\omega L)^2}$ (ohms)

$\tan\phi = \omega L/R$

During the period $\pi \le \omega t \le 2\pi$, when the supply current $i = 0$, the diode current and hence load current is given by

$$i_o(\omega t) = i_{Dy}(\omega t) = I_{o1\pi}e^{-(\omega t - \pi)/\tan\phi} \qquad \text{(A)} \qquad \pi \le \omega t \le 2\pi \quad (11.18)$$

for

$$I_{o1\pi} = I_{o2\pi}e^{\pi/\tan\phi} \qquad \text{(A)}$$

In figure 11.3b it will be seen that although the load current is continuous, the supply current is discontinuous and therefore has a high harmonic content.

Example 11.1: ***Half wave rectifier***

In the circuit of figure 11.3 the source voltage is $240\sqrt{2}\sin(2\pi\,50t)$ V, R = 10 ohms, and L = 50 mH. Calculate

i. the mean and rms values of the load voltage, V_o and V_{rms}
ii. the mean value of the load current, $\overline{I}_o$
iii. the current boundary conditions, namely $I_{o1\pi}$ and $I_{o2\pi}$.

Solution

i. From equation (11.11), the mean output voltage is given by

$$V_o = \sqrt{2}V/\pi = \sqrt{2}\times 240/\pi = 108\text{V}$$

From equation (11.12) the load rms voltage is

$$V_{rms} = \sqrt{2}V/2 = 240/\sqrt{2} = 169.7\text{V}$$

ii. The mean output current, equation (11.5), is

$$\overline{I}_o = V_o/R = \sqrt{2}V/\pi R = \sqrt{2}\times 240/\pi\times 10 = 10.8\text{A}$$

iii. The load impedance is characterised by

$$Z = \sqrt{R^2 + (\omega L)^2} = \sqrt{10^2 + (2\pi\times 50\times 0.05)^2} = 18.62\text{ohms}$$

$$\tan\phi = \omega L/R = 2\pi\times 50\times 0.05/10 = 1.57\text{rad} \text{ or } \phi = 57.5°$$

From section 11.1.2, equation (11.17)

$$I_{o2\pi} = \sqrt{2}V/Z\sin\phi\,\frac{1+e^{-\pi/\tan\phi}}{e^{\pi/\tan\phi} - e^{-\pi/\tan\phi}}$$

$$I_{o2\pi} = \sqrt{2}\times 240/18.62\times\sin(\tan^{-1}1.57)\times\frac{1+e^{-\pi/1.57}}{e^{\pi/1.57} - e^{-\pi/1.57}} = 3.41\text{A}$$

Hence, from equation (11.18)

$$I_{o1\pi} = I_{o2\pi}e^{\pi/\tan\phi} = 3.41\times e^{\pi/1.57} = 25.22\text{A}$$

♣

11.1.3 Full-wave bridge circuit

Single-phase uncontrolled full-wave bridge circuits are shown in figures 11.4a and 11.4b. Figures 11.4a and b appear identical as far as the load is concerned. It will be seen in part b that two fewer diodes can be employed but this requires a centre-tapped secondary transformer where each secondary has only a 50% copper utilisation factor. For the same output voltage, each of the secondary windings in figure 11.4b must have the same rms voltage rating as the single secondary winding of the transformer in figure 11.4a. The rectifying diodes in figure 11.4b experience twice the reverse voltage, as that experienced by each of the four diodes in the circuit of figure 11.4a. The use of a centre tapped transformer secondary, halves the copper utilisation factor.

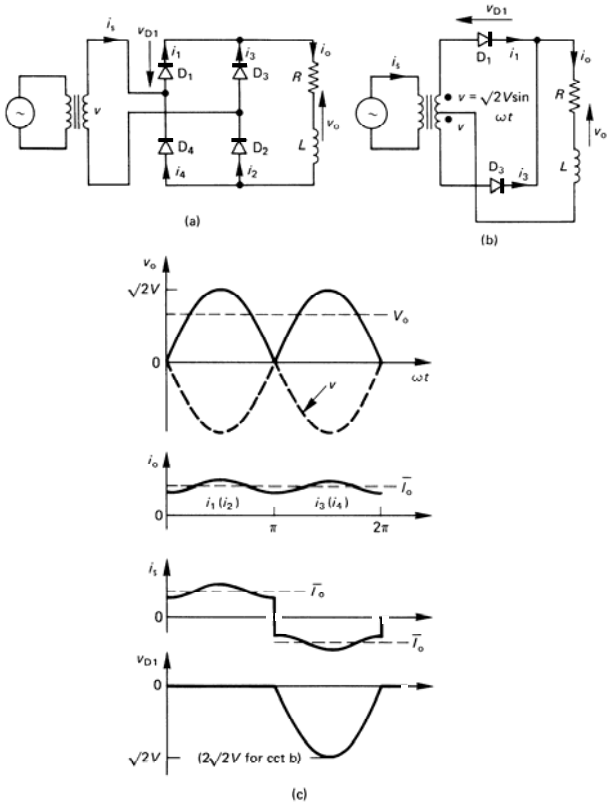


Figure 11.4. *Single-phase full-wave rectifier bridge: (a) circuit with four rectifying diodes; (b) circuit with two rectifying diodes; and (c) circuit waveforms.*

Figure 11.4c shows bridge circuit voltage and current waveforms. The load experiences the transformer secondary rectified voltage which has a mean voltage of

$$V_o = \frac{1}{\pi}\int_0^{\pi} \sqrt{2}V \sin\omega t \, d\omega t$$
$$\bar{V}_o = \bar{I}_o R = 2\sqrt{2}V/\pi = 0.90V \quad \text{(V)} \tag{11.19}$$

The rms value of the load circuit voltage v_0 is

$$V_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} \left(\sqrt{2}V \sin\omega t\right)^2 d\omega t}$$
$$V_{rms} = V \quad \text{(V)} \tag{11.20}$$

The ripple voltage is

$$V_{RI} \triangleq \sqrt{V_{rms}^2 - V_o^2}$$
$$= \sqrt{V^2 - \left(2\sqrt{2}/\pi\right)^2 V^2} = 0.435V \quad \text{(V)} \tag{11.21}$$

hence the voltage ripple factor is

$$K_v \triangleq V_{RI}/V_o$$
$$K_v = \sqrt{1 - \left(2\sqrt{2}/\pi\right)^2} \;/\; 2\sqrt{2}/\pi = 0.483 \tag{11.22}$$

which is significantly less than the half-wave rectified value of 1.211 from equation (11.14).

With a highly inductive load, which is the usual practical case, virtually constant load current flows, as shown dashed in figure 11.4c. The bridge diode currents are then square wave blocks of current of magnitude $\bar{I}_o$. The diode current ratings can now be specified and depend on the pulse number *n*. For this full-wave single-phase application each input cycle comprises two output current pulses, hence $n = 2$.

The mean current in each diode is

$$\bar{I}_D = 1/n \, \bar{I}_o = 1/2 \, \bar{I}_o \quad \text{(A)} \tag{11.23}$$

and the rms current in each diode is

$$I_D = 1/\sqrt{n} \, \bar{I}_o = \bar{I}_o/\sqrt{2} \quad \text{(A)} \tag{11.24}$$

whence the diode current form factor is

$$K_{ID} = I_D/\bar{I}_D = \sqrt{n} = \sqrt{2} \tag{11.25}$$

Since the current is approximately constant, power delivered to the load is

$$P_o \approx V_o \bar{I}_o = 8/\pi^2 \times V^2/R \quad \text{(W)} \tag{11.26}$$

11.2 Single-phase full-wave half-controlled converter

When a converter contains both diodes and thyristors, for example as shown in figure 11.5 parts a, b, and c, the converter is termed half-controlled. These three circuits produce identical load waveforms neglecting any differences in the number and type of semiconductor voltage drops. The power to the load is varied by controlling the angle α, shown in figure 11.5d, at which the bridge thyristors are triggered. The circuit diodes prevent the load voltage from going negative, extend the conduction period, and reduce the ac ripple.

The particular application will determine which one of the three circuits should be employed. For example, circuit figure 11.5a contains five devices of which four are thyristors, whereas the other two circuits contain four devices, of which only two are thyristors. The thyristor triggering requirements of the circuit in figure 11.5b are simple since both thyristors have a common cathode connection.

Figure 11.5b may suffer from prolonged shut-down times with highly inductive loads. The diode in the freewheeling path will hold on the freewheeling thyristor, allowing conduction during that thyristors next positive cycle without any gate drive present. This does not occur in circuits 11.5a and c since freewheeling does not occur through the circuit thyristors, hence they will drop out of conduction at converter shut-down. The table in figure 11.5d shows which semiconductors are active in each circuit during the various periods of the load cycle.

Various circuit waveforms are shown in figure 11.5d.

The mean output voltage and current are

$$V_o = \bar{I}_o R = \frac{1}{\pi}\int_{\alpha}^{\pi} \sqrt{2}\, V \sin(\omega t)\; d\omega t$$

$$= \frac{\sqrt{2}\, V}{\pi}(1+\cos\alpha) \qquad \text{(V)} \qquad (11.27)$$

$$\bar{I}_o = {}^{V_o}\!/_{R} = \frac{\sqrt{2}\, V}{\pi R}(1+\cos\alpha) \qquad \text{(A)}$$

where α is the delay angle from the point at which the associated thyristor first becomes forward-biased and is therefore able to be turned on. The maximum mean output voltage, $\hat{V}_o = 2\sqrt{2}V/\pi$ (also predicted by equation 11.16), occurs at $\alpha = 0$. The normalised mean output voltage V_n is

$$V_n = V_o/\hat{V}_o = \tfrac{1}{2}(1+\cos\alpha) \qquad (11.28)$$

Equation (11.27) shows that the load voltage is independent of the load (because the diodes clamp the load to zero volts thereby preventing the load from going negative), and is a function only of the phase delay angle for a given supply voltage.

The rms value of the load circuit voltage v_o is

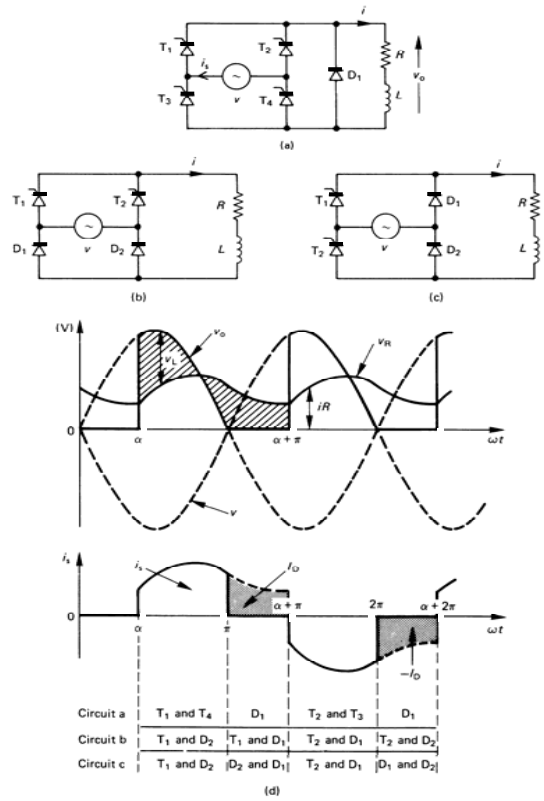


Figure 11.5. *Full-wave half-controlled converter with freewheel diodes: (a), (b) and (c) different circuit configurations producing the same output; and (d) circuit voltage and current waveforms and device conduction table.*

$$V_{rms} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\pi}\left(\sqrt{2}V\sin\omega t\right)^2 d\omega t} = V\sqrt{\frac{\pi-\alpha+\tfrac{1}{2}\sin 2\alpha}{\pi}} \quad \text{(V)} \tag{11.29}$$

Equations (11.27) and (11.29) can be used to evaluate the load ripple voltage, defined by equation (11.13), and load voltage ripple factor, defined by equations (11.14).

11.2i - Discontinuous load current, with $\alpha < \pi$ and $\beta - \alpha < \pi$, the load current (and supply current) is based on equation (11.1) which gives

$$i(\omega t) = i_s(\omega t) = \sqrt{2}V/Z\left(\sin(\omega t-\phi) - \sin(\alpha-\phi)e^{-\omega t+\alpha/\tan\phi}\right) \quad \text{(A)} \qquad \alpha \le \omega t \le \pi \tag{11.30}$$

After $\omega t = \pi$ the load current decreases exponentially to zero through the freewheel diode according to

$$i(\omega t) = i_{Df}(\omega t) = I_{01\pi}e^{-\omega t/\tan\phi} \quad \text{(A)} \qquad 0 \le \omega t \le \alpha \tag{11.31}$$

where for $\omega t = \pi$ in equation (11.30)

$$I_{o1\pi} = \sqrt{2}V/Z\,\sin(\phi-\alpha)(1-e^{-\pi/\tan\phi})$$

11.2ii - Continuous load current, with $\alpha < \phi$ and $\beta - \alpha \ge \pi$, the load current is given by equations similar to equations (11.17) and (11.18), specifically

$$i(\omega t) = i_s(\omega t) = \sqrt{2}V/Z\left(\sin(\omega t-\phi) + \left(\frac{\sin\phi\, e^{-\alpha/\tan\phi} - \sin(\alpha-\phi)}{1-e^{-\pi/\tan\phi}}\right)e^{-\omega t+\alpha/\tan\phi}\right) \qquad \alpha \le \omega t \le \pi \quad \text{(A)} \tag{11.32}$$

While the load current when the freewheel diode conducts is

$$i(\omega t) = i_{Df}(\omega t) = I_{01\pi}e^{-\omega t/\tan\phi} \quad \text{(A)} \qquad 0 \le \omega t \le \alpha \tag{11.33}$$

where, when $\omega t = \pi$ in equation (11.32)

$$I_{01\pi} = \sqrt{2}V/Z\;\frac{\sin\phi - \sin(\alpha-\phi)e^{-\pi+\alpha/\tan\phi}}{1-e^{-\pi/\tan\phi}} \quad \text{(A)}$$

The critical inductance, to prevent the current falling to zero, is given by

$$\frac{\omega L_{crit}}{R} = \theta - \alpha - \tfrac{1}{2}\pi + \frac{\alpha + \sin\alpha + \pi\cos\theta}{1+\cos\alpha} \tag{11.34}$$

for $\alpha \le \theta$ where

$$\theta = \sin^{-1}\frac{V_o}{\sqrt{2}V} = \sin^{-1}\frac{1+\cos\alpha}{\pi} \tag{11.35}$$

The minimum current occurs at the angle θ, where the mean output voltage V_o equals the instantaneous load voltage, v_o. When phase delay angle α is greater than the critical angle θ, $\theta = \alpha$ in equation (11.35) yields

$$\frac{\omega L_{crit}}{R} = -\tfrac{1}{2}\pi + \frac{\alpha + \sin\alpha + \pi\cos\alpha}{1+\cos\alpha} \tag{11.36}$$

It is important to note that converter circuits employing diodes cannot be used when inversion is required. Since the converter diodes prevent the output voltage from being negative, regeneration from the load into the supply is not achievable.
Figure 11.5a is a fully controlled converter with an *R-L* load and freewheel diode. In single-phase circuits, this converter essentially behaves as a half-controlled converter.

11.3 Single-phase controlled thyristor converter circuits

11.3.1 Half-wave circuit with an R-L load

The diode in the circuit of figure 11.1 can be replaced by a thyristor as shown in figure 11.6a to form a half-wave controlled rectifier circuit with an *R-L* load. The output voltage is now controlled by the thyristor trigger angle, α. The output voltage ripple is at the supply frequency. Circuit waveforms are shown in figure 11.6b.
The output current, hence output voltage, for the circuit is given by

$$L\frac{di}{dt} + Ri = \sqrt{2}V\sin\omega t \quad \text{(V)} \qquad \alpha \le \omega t \le \beta \quad \text{(rad)} \tag{11.37}$$

where phase delay angle α and current extinction angle β are shown in the waveform in figure 11.6b and are the zero load current points.

Solving equation (11.37) yields the load and supply current

$$i(\omega t) = \frac{\sqrt{2}\,V}{Z}\left\{\sin(\omega t - \phi) - \sin(\alpha - \phi)e^{(\alpha - \omega t)/\tan\phi}\right\} \quad \text{(A)}$$

$$\text{where } Z = \sqrt{R^2 + (\omega L)^2} \quad \text{(ohms)} \qquad \tan\phi = \omega L/R \qquad \alpha \le \omega t \le \beta \tag{11.38}$$

The current extinction angle β is dependent on the load impedance and trigger angle α, and can be determined by solving equation (11.38) with $\omega t = \beta$ when $i(\beta) = 0$, that is

$$\sin(\beta - \phi) = \sin(\alpha - \phi)\,e^{(\alpha-\beta)/\tan\phi} \tag{11.39}$$

This is a transcendental equation. A family of curves of current conduction angle versus delay angle, that is $\beta - \alpha$ versus α, is shown in figure 11.7. The plot for $\phi = \tfrac{1}{2}\pi$ is for a purely inductive load, whereas $\phi = 0$ is a purely resistive load.

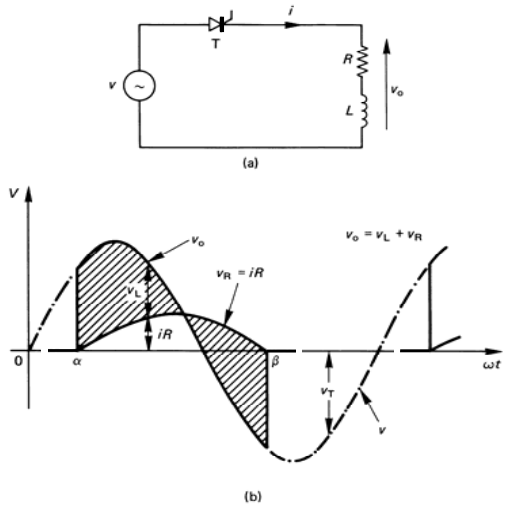


Figure 11.6. *Single-phase half-wave controlled converter: (a) circuit diagram and (b) circuit waveforms for an inductive load.*

The mean load voltage, whence the mean load current, is given by

$$V_o = \frac{1}{2\pi}\int_{\alpha}^{\beta}\sqrt{2}V\sin\omega t\, d\omega t$$

$$V_o = \bar{I}_o R = \frac{\sqrt{2}V}{2\pi}(\cos\alpha - \cos\beta) \qquad \text{(V)} \tag{11.40}$$

where the angle β can be extracted from figure 11.7.
The rms load voltage is

$$V_{rms} = \left[\tfrac{1}{2\pi}\int_{\alpha}^{\beta}\left(\sqrt{2}V\right)^2\sin^2\omega t\, d\omega t\right]^{\frac{1}{2}}$$

$$= \sqrt{2}V\Big/2\left[\tfrac{1}{\pi}\left\{(\beta-\alpha)-\tfrac{1}{2}(\sin 2\beta - \sin 2\alpha)\right\}\right]^{\frac{1}{2}} \tag{11.41}$$

The rms current involves integration of equation (11.38), giving equation (11.60)/√2. Iterative solutions to equation (11.39) are shown in of figure 11.7a, where it is seen that two straight-line relationships exist between α and β-α. Exact solutions to equation

(11.39) exist for these two cases. That is, exact solutions exist for the purely resistive load and the purely inductive load.

11.3.1i - Case 1: Purely resistive load. From equation (11.38), $Z = R$, $\phi = 0$, and the current is given by

$$i(\omega t) = \frac{\sqrt{2}\,V}{R}\sin(\omega t) \qquad \text{(A)} \tag{11.42}$$

$$\alpha \le \omega t \le \pi \text{ and } \beta = \pi \;\; \forall\alpha$$

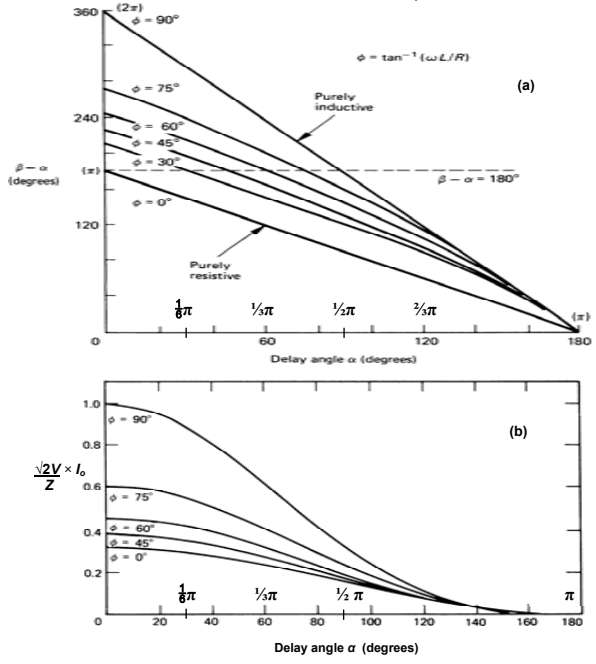


Figure 11.7. *Half-wave, controlled converter thyristor trigger delay angle α versus: (a) thyristor conduction angle, β-α, and (b) normalised mean load current.*

The average load voltage, hence average load current, is

$$V_o = \frac{1}{2\pi}\int_{\alpha}^{\pi} \sqrt{2}V \sin\omega t \, d\omega t$$
$$V_o = \bar{I}_o R = \frac{\sqrt{2}V}{2\pi}(1+\cos\alpha) \qquad \text{(V)} \tag{11.43}$$

The rms output voltage is

$$V_{rms} = \left[\tfrac{1}{2}\pi \int_{\alpha}^{\pi} \left(\sqrt{2}V\right)^2 \sin^2 \omega t \, d\omega t \right]^{\frac{1}{2}}$$
$$= \sqrt{2}V \Big/ 2 \left[\tfrac{1}{2}\pi \left\{ (\pi - \alpha) + \tfrac{1}{2}\sin 2\alpha) \right\} \right]^{\frac{1}{2}} \tag{11.44}$$

Since the load is purely resistive, $I_{rms} = V_{rms}/R$ and the power delivered to the load is $P_o = I_{rms}^2 R$.

11.3.1ii - Case 2: Purely inductive load. From equation (11.38), $Z = \omega L$, $\phi = \tfrac{1}{2}\pi$, and the current is given by

$$i(\omega t) = \frac{\sqrt{2}\ V}{\omega L}\ \left(\sin(\omega t - \tfrac{1}{2}\pi)\ - \sin\left(\alpha - \tfrac{1}{2}\pi\right)\right) \quad \text{(A)}$$
$$= \frac{\sqrt{2}\ V}{\omega L}\ \left(\cos\alpha\ - \cos\omega t\right) \tag{11.45}$$
$$\alpha \le \omega t \le \beta \text{ and } \beta = 2\pi - \alpha$$

The average load voltage, based on the equal area criterion, is zero

$$V_o = \frac{1}{2\pi}\int_{\alpha}^{2\pi-\alpha} \sqrt{2}V \sin\omega t \, d\omega t = 0 \tag{11.46}$$

The average output current is

$$\bar{I}_o = \tfrac{1}{2}\pi \int_{\alpha}^{2\pi-\alpha} \frac{\sqrt{2}\ V}{\omega L}\ \{\cos\alpha\ -\ \cos\omega t\}\, d\omega t$$
$$= \frac{\sqrt{2}\ V}{\pi\omega L}\left[(\pi - \alpha)\cos\alpha + \sin\alpha\ \right] \tag{11.47}$$

The rms output current is derived from

$$I_{rms} = \frac{\sqrt{2}\ V}{\omega L}\ \left[\tfrac{1}{2}\pi \int_{\alpha}^{2\pi-\alpha} \left(\cos\alpha\ - \cos\omega t\right)^2 d\omega t \right]^{\frac{1}{2}} \tag{11.48}$$

The rms output voltage is

$$V_{rms} = \left[\tfrac{1}{2}\pi \int_{\alpha}^{2\pi-\alpha} \left(\sqrt{2}V\right)^2 \sin^2 \omega t \, d\omega t \right]^{\frac{1}{2}}$$
$$= \sqrt{2}V \left[\tfrac{1}{2}\pi \left\{ (\pi - \alpha) + \tfrac{1}{2}\sin 2\alpha) \right\} \right]^{\frac{1}{2}} \tag{11.49}$$

Since the load is purely inductive load, $P_o = 0$.

By setting $\alpha = 0$, the equations (11.42) to (11.49) are valid for the uncontrolled rectifier considered in section 11.1.1, for a purely resistive and purely inductive load.

Example 11.2: ***Half-wave controlled rectifier***

The ac supply of the half-wave controlled single-phase converter in figure 11.6a is $v = \sqrt{2}\ 240 \sin\omega t$. For the following loads

Load 1: $R = 10\Omega$, $\omega L = 0\ \Omega$
Load 2: $R = 0\ \Omega$, $\omega L = 10\Omega$
Load 3: $R = 7.1\Omega$, $\omega L = 7.1\Omega$

determining in each load case, for a firing delay angle $\alpha = \pi/6$

- the conduction angle γ, hence the current extinction angle β
- the dc output voltage and the average output current
- the power dissipated in the load for the first two loads

Solution

Load 1: $R = 10\Omega$, $\omega L = 0\ \Omega$

From equation (11.38), $Z = 10\Omega$ and $\phi = 0°$.
From equation (11.42), $\beta = \pi$ for all α, thus for $\alpha = \pi/6$, $\gamma = \beta - \alpha = 5\pi/6$.
From equation (11.43)

$$V_o = \bar{I}_o R = \frac{\sqrt{2}V}{2\pi}(1+\cos\alpha)$$
$$= \frac{\sqrt{2}V}{2\pi}(1+\cos\pi/6) = 100.9\text{V}$$

The average load current is

$$\bar{I}_o = V_o/R = \frac{\sqrt{2}V}{2\pi R}(1+\cos\alpha) = 100.9\text{V}/10\Omega = 10.1\text{A}.$$

The rms load current is given by equation (11.44), that is

$$V_{rms} = \sqrt{2}V \Big/ 2 \left[\tfrac{1}{2}\pi \left\{ (\pi - \alpha) - \tfrac{1}{2}\sin 2\alpha) \right\} \right]^{\frac{1}{2}}$$
$$= \sqrt{2}\times 240 \Big/ 2 \times \left[\tfrac{1}{2}\pi \left\{ (\pi - \pi/6) + \tfrac{1}{2}\sin\pi/3) \right\} \right]^{\frac{1}{2}} = 200\text{V}$$

Since the load is purely resistive the power delivered to the load is

$$P_o = I_{rms}^2 R = V_{rms}^2/R$$
$$= 100\text{V}^2/10\Omega = 1000\text{W}$$

Load 2: $R = 0\ \Omega$, $\omega L = 10\Omega$

From equation (11.38), $Z = 10\Omega$ and $\phi = \tfrac{1}{2}\pi$.
From equation (11.45), which is based on the equal area criterion, $\beta = 2\pi - \alpha$, thus for $\alpha = \pi/6$, $\beta = 11\pi/6$ whence the conduction period is $\gamma = \beta - \alpha = 5\pi/3$.
From equation (11.46)

$$V_o = 0\text{V}$$

The average load current is

$$\bar{I}_o = \frac{\sqrt{2}\,V}{\pi\omega L}\left[(\pi-\alpha)\cos\alpha + \sin\alpha\right]$$

$$= \frac{\sqrt{2}\ 240}{\pi\times 10}\times\left[(5\pi/6)\cos\pi/6 + \sin\pi/6\right] = 14.9\text{A}$$

Since the load is purely inductive the power delivered to the load is zero.

Load 3: $R = 7.1\Omega$, $\omega L = 7.1\Omega$

From equation (11.38), $Z = 10\Omega$ and $\phi = ¼\pi$.

From figure 11.7a, for $\phi = ¼\pi$ and $\alpha = \pi/6$, $\gamma = \beta - \alpha$ =195° whence β = 225°.

From equation (11.40)

$$V_o = \bar{I}_o R = \frac{\sqrt{2}V}{2\pi}(\cos\alpha - \sin\beta)$$

$$= \frac{\sqrt{2}\times 240}{2\pi}(\cos 30° - \sin 200°) = 60.8\text{V}$$

The average load current is

$$\bar{I}_o = V_o / R$$

$$= 60.8\text{V}/7.1\Omega = 8.6\text{A}$$

Alternatively, the average current can be extract from figure 11.7b, which for $\phi = ¼\pi$ and $\alpha = \pi/6$ gives the normalised current as 0.35, thus

$$\bar{I}_o = \sqrt{2}V\big/Z \times 0.35$$

$$= \sqrt{2}\times 240\text{V}\big/10\Omega \times 0.35 = 11.9\text{A}$$

♣

11.3.2 Half-wave half-controlled

The half-wave controlled converter waveform in figure 11.6b shows that when $\alpha < \omega t < \pi$, during the positive half of the supply cycle, energy is delivered to the load. But when $\pi < \omega t < 2\pi+\alpha$, the supply reverses and some energy is returned to the supply. More energy can be retained by the load if the load voltage is prevented from reversing. A load freewheel diode can facilitate this objective.

The single-phase half-wave converter can be controlled when a load commutating diode is incorporated as shown in figure 11.8a. The diode will prevent the instantaneous load voltage v_0 from going negative, as with the single-phase half-controlled converters shown in figure 11.5.

The load current is defined by equations (11.15) for $\alpha \le \omega t \le \pi$ and equation (11.16) for $\pi \le \omega t \le 2\pi + \alpha$, namely:

$$\begin{aligned} L\frac{di}{dt} + Ri &= \sqrt{2}V\sin\omega t \qquad \text{(A)} \qquad \alpha \le \omega t \le \pi \\ L\frac{di}{dt} + Ri &= 0 \qquad\qquad\quad \text{(A)} \qquad \pi \le \omega t \le 2\pi + \alpha \end{aligned} \tag{11.50}$$

At $\omega t = \pi$ the thyristor is commutated and the load current, and hence diode current, is of the form of equation (11.18). As shown in figure 11.8b, depending on the delay angle α and *R-L* load time constant, the load current may fall to zero, producing discontinuous load current.

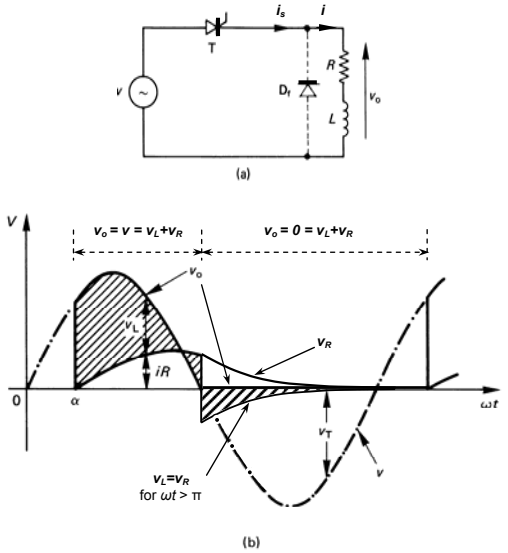


Figure 11.8. *Half-wave half-controlled converter: (a) circuit diagram and (b) circuit waveforms for an inductive load.*

11.3.2i - For **discontinuous conduction** the load current is defined by

$$i(\omega t) = i_s(\omega t) = \sqrt{2}V/Z\left(\sin(\omega t-\phi)-\sin(\alpha-\phi)\,e^{-\omega t+\alpha/\tan\phi}\right) \quad \text{(A)}$$

$$\alpha \le \omega t \le \pi$$

$$i(\omega t) = i_{Df}(\omega t) = I_{01\pi}e^{-\omega t/\tan\phi} \qquad (11.51)$$

$$= \left\{\sqrt{2}V/Z\,\sin(\phi-\alpha)(1-e^{-\pi/\tan\phi})\right\}e^{-\omega t+\pi/\tan\phi} \quad \text{(A)}$$

$$\pi \le \omega t \le 2\pi+\alpha$$

11.3.2ii - For **continuous conduction** the load current is defined by

$$i(\omega t) = i_s(\omega t) = \frac{\sqrt{2}V}{Z}\left(\sin(\omega t-\phi)+\left(\frac{\sin\phi\;e^{-\alpha/\tan\phi}-\sin(\alpha-\phi)}{1-e^{-2\pi/\tan\phi}}\right)e^{-\omega t+\alpha/\tan\phi}\right)$$

$$\alpha \le \omega t \le \pi \quad \text{(A)}$$

$$i(\omega t) = i_{Df}(\omega t) = I_{01\pi}e^{-\omega t/\tan\phi} \qquad (11.52)$$

$$= \left\{\sqrt{2}V/Z\;\frac{\sin\phi-\sin(\alpha-\phi)e^{-\pi-\alpha/\tan\phi}}{1-e^{-\pi/\tan\phi}}\right\}e^{-\omega t+\pi/\tan\phi} \quad \text{(A)}$$

$$\pi \le \omega t \le 2\pi+\alpha$$

The mean load voltage (hence mean output current) for all conduction cases is

$$V_o = \frac{1}{2\pi}\int_\alpha^\pi \sqrt{2}V\sin\omega t\;\;d\omega t$$

$$V_o = \bar{I}_o R = \frac{\sqrt{2}V}{2\pi}(1+\cos\alpha) \quad \text{(V)} \qquad (11.53)$$

which is half the mean voltage for a single-phase half-controlled converter, given by equation (11.27). The maximum mean output voltage, $\hat{V}_o = \sqrt{2}V/\pi$ (equation (11.11)), occurs at $\alpha = 0$. The normalised mean output voltage V_n is

$$V_n = V_o/\hat{V}_o = ½(1+\cos\alpha) \qquad (11.54)$$

The rms output voltage for both continuous and discontinuous load current is

$$V_{rms} = \left[½\pi\int_\alpha^\pi\left(\sqrt{2}V\right)^2\sin^2\omega t\,d\omega t\right]^{½}$$

$$= \sqrt{2}V/2\left[½\pi\left\{(\pi-\alpha)+½\sin 2\alpha\right\}\right]^{½} \qquad (11.55)$$

The advantages of incorporating a load freewheel diode are

- the input power factor is improved and
- the load waveform is improved giving a better load performance

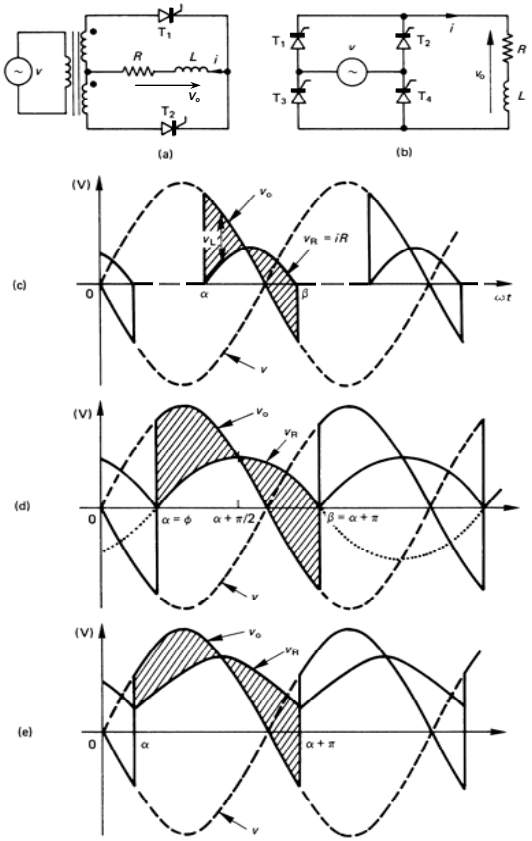


Figure 11.9. *Full-wave controlled converter: (a) and (b) circuit diagrams; (c) discontinuous load current; (d) verge of continuous load current, when α = ø; and (e) continuous load current.*

11.3.3 Full-wave circuit with an R-L load

Full-wave voltage control is possible with the circuits shown in figures 11.9a and b. The circuit in figure 11.9a uses a centre-tapped transformer and two thyristors which experience a reverse bias of twice the supply. At high powers where a transformer may not be applicable, a four-thyristor configuration as in figure 11.9b is suitable. The voltage ratings of the thyristors in figure 11.9b are half those of the devices in figure 11.9a, for a given input voltage.

Load voltage and current waveforms are shown in figure 11.9 parts c, d, and e for three different phase control angle conditions.

The load current waveform becomes continuous when the phase control angle α is given by

$$\alpha = \tan^{-1}\omega L/R = \phi \qquad \text{(rad)} \tag{11.56}$$

at which angle the output current is a rectified sine wave. For $\alpha > \phi$, discontinuous load current flows as shown in figure 11.9c. At $\alpha = \phi$ the load current becomes continuous as shown in figure 11.9d, whence $\beta = \alpha + \pi$. Further decrease in α, that is $\alpha < \phi$, results in continuous load current that is always greater than zero, as shown in figure 11.9e.

11.3.3i - *$\alpha > \phi$, $\beta - \alpha < \pi$, discontinuous load current*

The load current waveform is the same as for the half-wave situation considered in section 11.3.1, given by equation (11.38). That is

$$i(\omega t) = \frac{\sqrt{2}V}{Z}\left[\sin(\omega t - \phi) - \sin(\alpha - \phi)\, e^{\{(\alpha - \omega t)/\tan\phi\}}\right] \qquad \text{(A)}$$
$$\alpha \le \omega t < \pi + \alpha \qquad \text{(rad)} \tag{11.57}$$

The mean output voltage for this full-wave circuit will be twice that of the half-wave case in section 11.3.1, given by equation (11.40). That is

$$V_o = \bar{I}_o R = \frac{1}{\pi}\int_\alpha^\beta \sqrt{2}V \sin\omega t\, d\omega t$$
$$= \frac{\sqrt{2}V}{\pi}(\cos\alpha - \cos\beta) \qquad \text{(V)} \tag{11.58}$$

where β can be extracted from figure 11.7. The average output current is given $\bar{I}_o = V_o/R$.

The rms load voltage is

$$V_{rms} = \sqrt{2}V\left[\frac{1}{\pi}\int_\alpha^\beta \sin^2\omega t\, d\omega t\right]^{1/2}$$
$$= \sqrt{2}V\left[\frac{1}{2\pi}\{(\beta - \alpha) + \tfrac{1}{2}(\sin 2\beta - \sin 2\alpha)\}\right]^{1/2} \tag{11.59}$$

The rms load current is

$$I_{rms} = \frac{\sqrt{2}V}{2\pi R}\left[\cos\phi\cos(\beta - \alpha) - \sin\phi\cos(\alpha + \phi + \beta)\right]^{1/2} \tag{11.60}$$

The load power is therefore $P = I_{rms}^2 R$.

11.3.3ii - *$\alpha = \phi$, $\beta - \alpha = \pi$, verge of continuous load current*

When $\alpha = \phi = \tan^{-1}\omega L/R$, the load current given by equation (11.57) reduces to

$$i(\omega t) = \frac{\sqrt{2}V}{Z}\sin(\omega t - \phi) \qquad \text{(A)}$$
$$\text{for } \phi \le \omega t \le \phi + \pi \qquad \text{(rad)} \tag{11.61}$$

and the mean output voltage, on reducing equation (11.58) using $\beta = \alpha + \pi$, is given by

$$V_o = \frac{2\sqrt{2}V}{\pi}\cos\alpha \qquad \text{(V)} \tag{11.62}$$

which is dependent of the load such that $\alpha = \phi = \tan^{-1}\omega L/R$. From equation (11.59), with $\beta - \alpha = \pi$, the rms output voltage is V, $I = V/Z$, and power = $VI\cos\phi$.

11.3.3iii - *$\alpha > \phi$, $\beta - \pi = \alpha$, continuous load current*

Under this condition, a thyristor is still conducting when another is forward-biased and is turned on. The first device is instantaneously reverse-biased by the second device which has been turned on. The first device is commutated and load current is instantaneously transferred to the oncoming device.

The load current is given by

$$i(\omega t) = \frac{\sqrt{2}V}{Z}\left[\sin(\omega t - \phi) - \frac{2\sin(\alpha - \phi)}{1 - e^{-\pi/\tan\phi}}\, e^{\{(\alpha - \omega t)/\tan\phi\}}\right] \tag{11.63}$$

This equation reduces to equation (11.61) for $\alpha = \phi$.

The mean output voltage, whence mean output current, are defined by equation (11.62)

$$V_o = \bar{I}_o R = \frac{2\sqrt{2}V}{\pi}\cos\alpha \qquad \text{(V)}$$

which is uniquely defined by α. The maximum mean output voltage, $\hat{V}_o = 2\sqrt{2}V/\pi$ (equation (11.19)), occurs at α=0. The normalised mean output voltage V_n is

$$V_n = V_o/\hat{V}_o = \cos\alpha \tag{11.64}$$

The rms output voltage is equal to the rms input supply voltage and given by

$$V_{rms} = \sqrt{\frac{1}{\pi}\int_\alpha^{\pi+\alpha}\left(\sqrt{2}V\right)^2 \sin^2\omega t\, d\omega t} = V \tag{11.65}$$

The ac component harmonic magnitudes in the load, which are odd, are given by

$$\frac{V_n}{V_o} = \left(\frac{1}{(2n-1)^2} + \frac{1}{(2n+1)^2} - \frac{2\cos 2\alpha}{(2n-1)(2n+1)}\right) \tag{11.66}$$

for n = 1, 2, 3…
The critical inductance, to prevent the current falling to zero, is given by

$$\frac{\omega L_{crit}}{R} = \frac{\pi}{2\cos\alpha}\left(\cos\theta + \frac{2}{\pi}\sin\alpha - \frac{2}{\pi}\cos\alpha\left(½\pi + \alpha + \theta\right)\right) \qquad (11.67)$$

for $\alpha \le \theta$ where

$$\theta = \sin^{-1}\frac{V_o}{\sqrt{2}V} = \sin^{-1}\frac{2\cos\alpha}{\pi} \qquad (11.68)$$

The minimum current occurs at the angle θ, where the mean output voltage V_o equals the instantaneous load voltage, v_o. When phase delay angle α is greater than the critical angle θ, substituting $\alpha=\theta$ in equation (11.67) gives

$$\frac{\omega L_{crit}}{R} = -\tan\alpha \qquad (11.69)$$

11.3.4 Full-wave circuit with R-L and emf load

An emf source and *R-L* load can be encountered in dc machine modelling. The emf represents the machine speed back emf, defined by $E = k\phi\omega$. These machines can be controlled by a fully controlled converter configuration as shown in figure 11.10a.
If in each half sine period the thyristor firing delay angle occurs after the rectified sine supply has fallen below the emf level *E,* then no load current flows since the bridge thyristors will always be reverse-biased. Thus the zero current firing angle α_0, for $\alpha_0 >$ ½π is given by

$$\alpha_o = \sin^{-1}\left(E/\sqrt{2}V\right) \qquad \text{(rad)} \qquad (11.70)$$

where it has been assumed the emf has the polarity shown in figure 11.10a. Load current can flow with a firing angle defined by

$$0 \le \alpha \le \alpha_o \qquad \text{(rad)} \qquad (11.71)$$

whence $\hat{\alpha} = \pi - \alpha_o$.
The load circuit current can be evaluated by solving

$$\sqrt{2}V\sin\omega t = L\frac{di}{dt} + Ri + E \qquad \text{(V)} \qquad (11.72)$$

11.3.4i - Discontinuous load current
The load current is given by

$$i(\omega t) = \frac{\sqrt{2}V}{Z}\left[\sin(\omega t - \phi) - \frac{E}{\sqrt{2}V}/\cos\phi + \left\{\frac{E}{\sqrt{2}V}/\cos\phi - \sin(\alpha - \phi)\right\}e^{\{(\alpha-\omega t)/\tan\phi\}}\right] \qquad (11.73)$$

$$\alpha \le \omega t \le \beta < \pi + \alpha \qquad \text{(rad)}$$

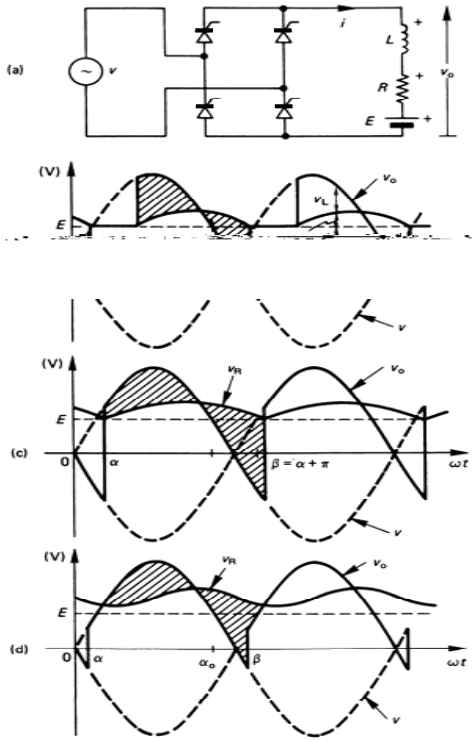


Figure 11.10. *A full-wave fully controlled converter with an inductive load which includes an emf source: (a) circuit diagram; (b) voltage waveforms with discontinuous load current; (c) verge of continuous load current; and (d) continuous load current.*

For discontinuous load current conduction, the current extinction angle β, shown on figure 11.10b, is solved by iterative techniques. The mean output voltage can be obtained from equation (11.31), which is valid for E= 0. For non-zero E

$$V_o = \frac{1}{2\pi}\int_{\alpha}^{\beta}\left(\sqrt{2}V\sin\omega t + E\right)d\omega t$$

$$V_o = \frac{\sqrt{2}V}{\pi}\left(\cos\alpha - \cos\beta + (\pi+\alpha-\beta)\frac{E}{\sqrt{2}V}\right) \quad \text{(V)} \qquad (11.74)$$

$$0 < \beta - \alpha < \pi \quad \text{(rad)}$$

The current extinction angle β is load-dependent, being a function of α, Z, and E. Since $V_o = E + \bar{I}_o R$, the mean load current is given by

$$\bar{I}_o = \frac{V_o - E}{R} = \frac{\sqrt{2}V}{\pi R}\left(\cos\alpha - \cos\beta - \frac{E}{\sqrt{2}V}(\beta-\alpha)\right) \quad \text{(A)} \qquad (11.75)$$

$$0 < \beta - \alpha < \pi \quad \text{(rad)}$$

The rms output voltage is given by

$$V_{rms} = \left(V^2\frac{\beta-\alpha}{\pi} + E^2\left(1-\frac{\beta-\alpha}{\pi}\right) - \frac{V^2}{2\pi}(\sin 2\beta - \sin 2\alpha)\right)^{1/2} \quad \text{(V)} \qquad (11.76)$$

The rms voltage across the *R-L* part of the load is given by

$$V_{RLrms} = \sqrt{V_{rms}^2 - E^2} \qquad (11.77)$$

11.3.4ii - Continuous load current

The load current is given by

$$i(\omega t) = \frac{\sqrt{2}V}{Z}\left[\sin(\omega t - \phi) - E/\sqrt{2}V/\cos\phi + 2\frac{\sin(\alpha-\phi)}{e^{-\pi/\tan\phi}-1}e^{\{(\alpha-\omega t)/\tan\phi\}}\right] \qquad (11.78)$$

$$\alpha \le \omega t \le \pi + \alpha \quad \text{(rad)}$$

The minimum current is given by

$$\check{I} = \frac{\sqrt{2}V}{Z}\sin(\alpha-\phi)\frac{e^{-\pi/\tan\phi}+1}{e^{-\pi/\tan\phi}-1} - \frac{E}{\sqrt{2}V} \qquad (11.79)$$

For continuous load current conditions, as shown in figures 11.10c and 11.10d, the mean output voltage is given by equation (11.74) with $\beta = \pi - \alpha$

$$V_o = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha}\sqrt{2}V\sin\omega t\, d\omega t = \frac{2\sqrt{2}V}{\pi}\cos\alpha \quad \text{(V)} \qquad (11.80)$$

The average output voltage is dependent only on the phase delay angle α. The mean load current is given by

$$\bar{I}_o = \frac{V_o - E}{R} = \frac{\sqrt{2}V}{R}\left(\frac{2}{\pi}\cos\alpha - \frac{E}{\sqrt{2}V}\right) \quad \text{(A)} \qquad (11.81)$$

The load voltage harmonics for continuous conduction are given by equation (11.66). From equation (11.79) set to zero, the boundary between continuous and discontinuous inductor current must satisfy

$$\frac{R}{Z}\sin(\alpha-\phi)\frac{e^{-\pi/\tan\phi}+1}{e^{-\pi/\tan\phi}-1} > \frac{E}{\sqrt{2}V} \qquad (11.82)$$

If the polarity of E is reversed as shown in figure 11.11a, waveforms as in parts b and c of figure 11.11 result. The emf supply can provide a forward bias across the bridge thyristors even after the supply polarity has gone negative. The zero current angle α_0 now satisfies $\pi < \alpha_0 < 3\pi/2$, as given by equation (11.70). Thus load and supply current can flow

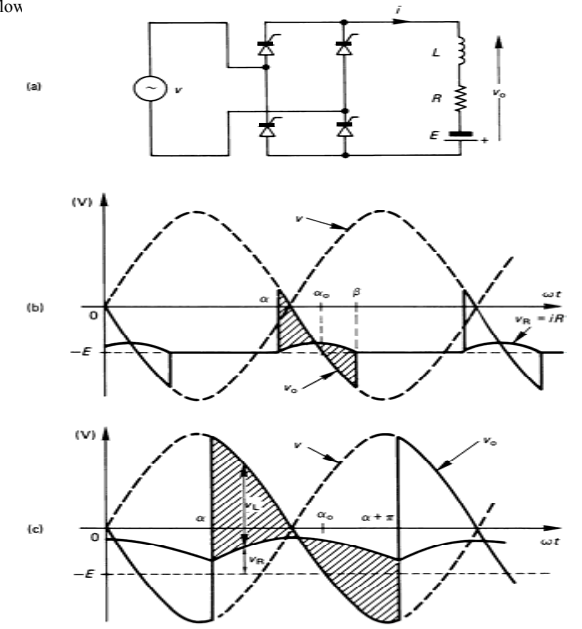


Figure 11.11. *A full-wave controlled converter with an inductive load and negative emf source: (a) circuit diagram; (b) voltage waveforms for discontinuous load current; and (c) continuous load current.*

The relationship between the mean output voltage and current is now given by

$$V_o = -E + \bar{I}_o R \tag{11.83}$$

That is, the emf term E in equations (11.70) to (11.81) is appropriately changed to $-E$. The load current flows from the emf source and the average load voltage is negative. Power is being delivered to the ac supply from the emf source in the load, which is an energy transfer process called *power inversion.*

11.4 Three-phase uncontrolled converter circuits

Single-phase supply circuits are adequate below a few kilowatts. At higher power levels, restrictions on unbalanced loading, line harmonics, current surge voltage dips, and filtering require the use of three-phase (or higher) converter circuits. Generally it will be assumed that the output current is both continuous and smooth. This assumption is based on the dc load being highly inductive.

11.4.1 Half-wave rectifier circuit with an inductive load

Figure 11.12 shows a half-wave, three-phase diode rectifier circuit along with various circuit voltage and current waveforms. A transformer having a star connected secondary is required for neutral access, N.
The diode with the highest potential with respect to the neutral conducts a rectangular current pulse. As the potential of another diode becomes the highest, load current is transferred to that device, and the previously conducting device is reverse-biased and naturally (line) commutated.
In general terms, for an n-phase system, the mean output voltage is given by

$$\begin{aligned} V_o &= \frac{\sqrt{2}V}{2\pi/n}\int_{-\pi/n}^{\pi/n} \cos\omega t \, d\omega t \qquad \text{(V)} \\ &= \sqrt{2}V\frac{\sin(\pi/n)}{\pi/n} \qquad \text{(V)} \end{aligned} \tag{11.84}$$

For a three-phase, half-wave circuit (n=3) the mean output voltage is

$$\begin{aligned} V_o &= \tfrac{1}{2\pi/3}\int_{\pi/6}^{5\pi/6} \sqrt{2}\,V \sin\omega t \, d\omega t \\ &= \sqrt{2}V\frac{\tfrac{1}{2}\sqrt{3}}{\pi/3} \qquad \text{(V)} \end{aligned} \tag{11.85}$$

The diode conduction angle is $2\pi/n$, namely $\frac{2}{3}\pi$. The peak diode reverse voltage is given by the maximum voltage between any two phases, $\sqrt{3}\sqrt{2}\,V = \sqrt{6}\,V$.
From equations (11.23), (11.24), and (11.25), the mean diode current is

$$\bar{I}_D = \tfrac{1}{n}\bar{I}_o = \tfrac{1}{3}\bar{I}_o \qquad \text{(A)} \tag{11.86}$$

and the rms diode current is

$$I_D = \tfrac{1}{\sqrt{n}}\bar{I}_o = \tfrac{1}{\sqrt{3}}\bar{I}_o \qquad \text{(A)} \tag{11.87}$$

The diode current form factor is

$$K_{ID} = I_D / \bar{I}_D = \sqrt{3} \tag{11.88}$$

The rms load voltage is

$$V_{rms} = \sqrt{\tfrac{1}{2\pi/3}\int_{\pi/6}^{5\pi/6} \left(\sqrt{2}V\right)^2 \sin^2\omega t \, d\omega t} \tag{11.89}$$

$$= 1.19V$$

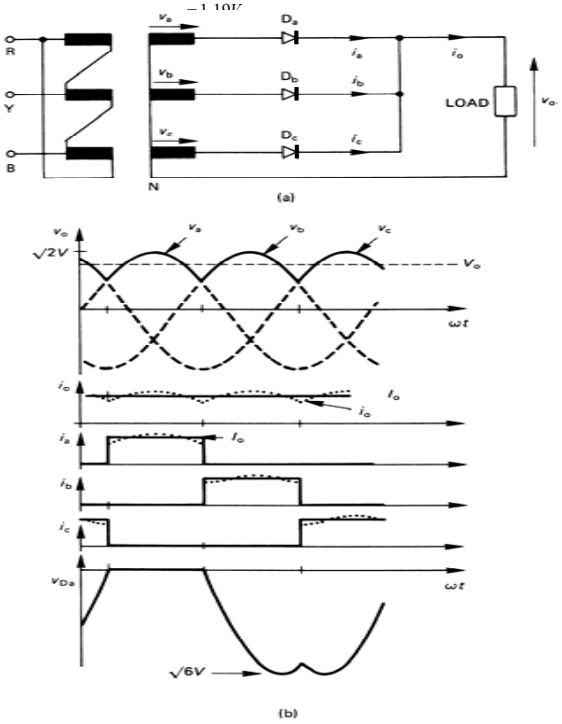


Figure 11.12. *Three-phase half-wave rectifier: (a) circuit diagram and (b) circuit voltage and current waveforms.*

The load form factor is

$$V_{FF} = V_{rms} \Big/ V = 1.19V / 1.17V = 1.01 \tag{11.90}$$

$$\text{The ripple factor} = \frac{\text{ac voltage at the load}}{\text{dc volatge at the load}}$$

$$= \sqrt{\left(\frac{V_{rms}}{V}\right)^2 - 1} = 0.185 \tag{11.91}$$

If neutral is available, a transformer is not necessary. The full load current is returned via the neutral supply. This neutral supply current is generally not acceptable other than at low power levels. The simple delta-star connection of the supply in figure 11.12a is not appropriate since the unidirectional current in each phase is transferred from the supply to the transformer. This may result in increased magnetising current and iron losses if dc magnetisation occurs. This problem is avoided in most cases by the special interconnected star winding, called zig-zag, shown in figure 11.13a. Each transformer limb has two equal voltage secondaries which are connected such that the magnetising forces balance. The resultant phasor diagram is shown in figure 11.13b.

As the number of phases increases, the windings become less utilised per cycle since the diode conduction angle decreases, from π for a single-phase circuit, to ⅔π for the three-phase case.

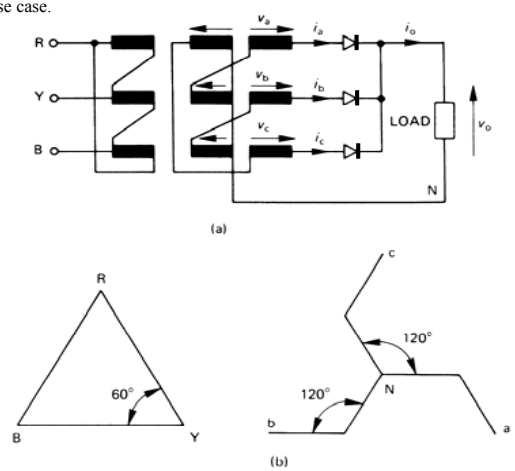


Figure 11.13. *Three-phase zig-zag interconnected star winding: (a) transformer connection and (b) phasor diagram of transformer voltages.*

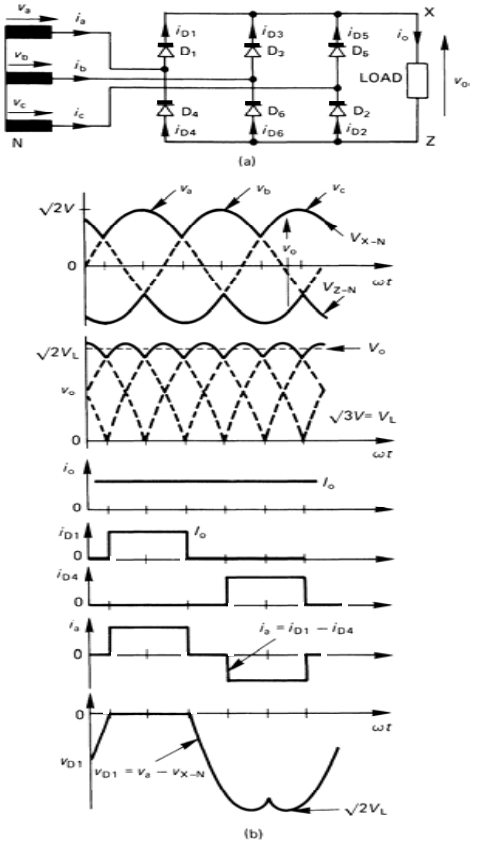


Figure 11.14. *Three-phase full-wave bridge rectifier: (a) circuit connection and (b) voltage and current waveforms.*

11.4.2 Full-wave rectifier circuit with an inductive load

Figure 11.14a shows a three-phase full-wave rectifier circuit where no neutral is necessary and it will be seen that two series diodes are always conducting. One diode can be considered as being in the feed circuit, while the other is in the return circuit. As such, the line-to-line voltage is impressed across the load. The rectifier circuit waveforms in figure 11.14b show that the load ripple frequency is six times the supply. Each diode conducts for ⅔π and experiences a reverse voltage of the peak line voltage.
The mean load voltage is given by twice equation (11.85), that is

$$V_o = \frac{1}{\pi/3}\int_{\pi/3}^{2\pi/3} \sqrt{2}\,V \sin\omega t\, d\omega t \qquad \text{(V)}$$
$$= \sqrt{2}V\frac{\sqrt{3}}{\pi/3} = \frac{3}{\pi}\sqrt{2}\,V_L = 1.36V_L \qquad (11.92)$$

where V_L is the line-to-line rms voltage.
The rms output voltage is given by

$$V_{rms} = \left(\frac{1}{2\pi/6}\int_{\pi/3}^{2\pi/3} \sqrt{2}V \sin^2\omega t\, d\omega t\right)^{\frac{1}{2}} = 1.352V \qquad (11.93)$$

The load form factor = 1.352/1.35=1.001 and the ripple factor = √form factor -1 = 0.06.

11.5 Three-phase half-controlled converter

Figure 11.15a illustrates a half-controlled converter where half the devices are thyristors, the remainder being diodes. As in the single-phase case, a freewheeling diode can be added across the load so as to allow the bridge thyristors to commutate. The output voltage expression consists of √2V 3√3/2π due to the uncontrolled half of the bridge and √2V 3√3 × cos α /2π due to the controlled half which is phase-controlled. The half-controlled bridge mean output is given by the sum, that is

$$V_o = \sqrt{2}\,V\frac{3\sqrt{3}}{2\pi}(1+\cos\alpha) = \sqrt{2}\,V_L\frac{3}{2\pi}(1+\cos\alpha)$$
$$= 2.34V(1+\cos\alpha) \qquad \text{(V)} \qquad (11.94)$$
$$0 \le \alpha \le \pi \qquad \text{(rad)}$$

At α = 0, $\hat{V}_o = \sqrt{2}\ V\ 3\sqrt{3}/\pi = 1.35\ V_L$, as in equation (11.46). The normalised mean output voltage V_n is

$$V_n = V_o/\hat{V}_o = ½(1+\cos\alpha) \qquad (11.95)$$

The diodes prevent any negative output, hence inversion cannot occur. Typical output voltage and current waveforms for an inductive load are shown in figure 11.15b.

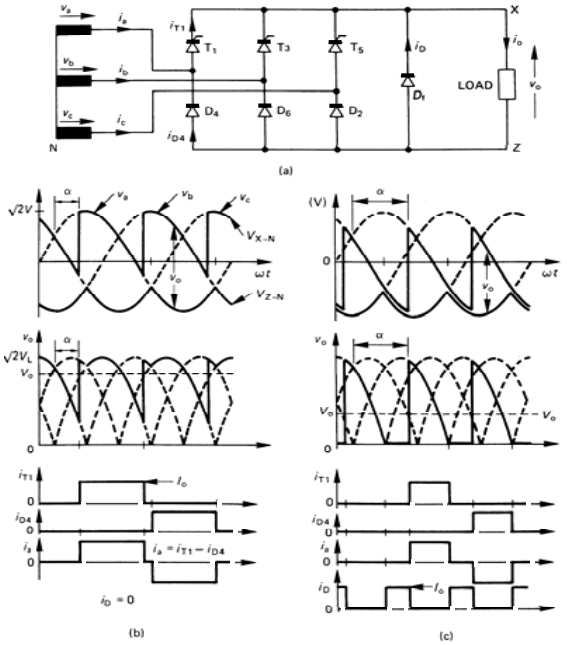


Figure 11.15. *Three-phase half-controlled bridge converter: (a) circuit connection; (b) voltage and current waveforms for a small firing delay angle α; and (c) waveforms for α large.*

11.5i - For $\alpha \le ⅓\pi$

When the delay angle is less than ⅓π the output waveform contains six pulses per cycle, of alternating controlled and uncontrolled phases, as shown in figure 11.15b. The output current is always continuous since no voltage zeros occur.
The rms output voltage is given by

$$V_{rms} = \sqrt{\frac{3}{2\pi}\int_{\alpha+\pi/6}^{\alpha+5\pi/6} 3\left(\sqrt{2}V\right)^2 \sin^2(\omega t - \pi/6)\, d\omega t}$$
$$= \sqrt{3}\sqrt{2}V\left(\frac{3}{4\pi}\left(\pi - \alpha + \tfrac{1}{2}\sin 2\alpha\right)\right)^{\frac{1}{2}} \qquad (11.96)$$
$$\text{for } \alpha \le \pi/3$$

11.5ii - For $\alpha \ge \frac{1}{3}\pi$

For delay angles greater than $\frac{1}{3}\pi$ the output voltage waveform is made up of three controlled pulses per cycle, as shown in figure 11.15c. Although output voltage zeros result, continuous load current can flow through a diode and the conducting thyristor, or through the commutating diode if employed. The rms output voltage is given by

$$V_{rms} = \sqrt{\frac{3}{2\pi}\int_{\alpha+\pi/6}^{7\pi/6} 3\left(\sqrt{2}V\right)^2 \sin^2(\omega t - \pi/6)\, d\omega t}$$
$$= \sqrt{3}\sqrt{2}V\left(\frac{3}{4\pi}\left(\pi - \alpha + \tfrac{1}{2}\sin 2\alpha\right)\right)^{\frac{1}{2}} \qquad (11.97)$$
$$\text{for } \alpha \ge \pi/3$$

11.6 Three-phase controlled thyristor converter circuits

11.6.1 Half-wave circuit with an inductive load

When the diodes in the circuit of figure 11.12 are replaced by thyristors, as in figure 11.16a, a fully controlled half-wave converter results. The output voltage is controlled by the delay angle α. This angle is specified from the thyristor commutation angle, which is the earliest point the associated thyristor becomes forward-biased, as shown in parts b, c, and d of figure 11.16. (The reference is not the phase zero voltage cross-over point). The thyristor with the highest instantaneous anode potential will conduct when fired and in turning on will reverse bias and turn off any previously conducting thyristor. The output voltage ripple is three times the supply frequency and the supply currents contain dc components. Each phase progressively conducts for periods of $\frac{1}{3}\pi$. The mean output for an n-phase half-wave controlled converter is given by (see example 11.2)

$$V_o = \frac{\sqrt{2}V}{2\pi/n}\int_{\alpha-\pi/n}^{\alpha+\pi/n} \cos\omega t\, d\omega t$$
$$= \sqrt{2}V\frac{\sin(\pi/n)}{\pi/n}\cos\alpha \qquad \text{(V)} \qquad (11.98)$$

which for the three-phase circuit considered with **continuous load current** gives

$$V_o = \bar{I}_o R = \frac{3\sqrt{3}}{2\pi}\sqrt{2}V\cos\alpha = 1.17V\cos\alpha \qquad \text{(V)} \qquad (11.99)$$
$$0 \le \alpha \le \pi/6$$

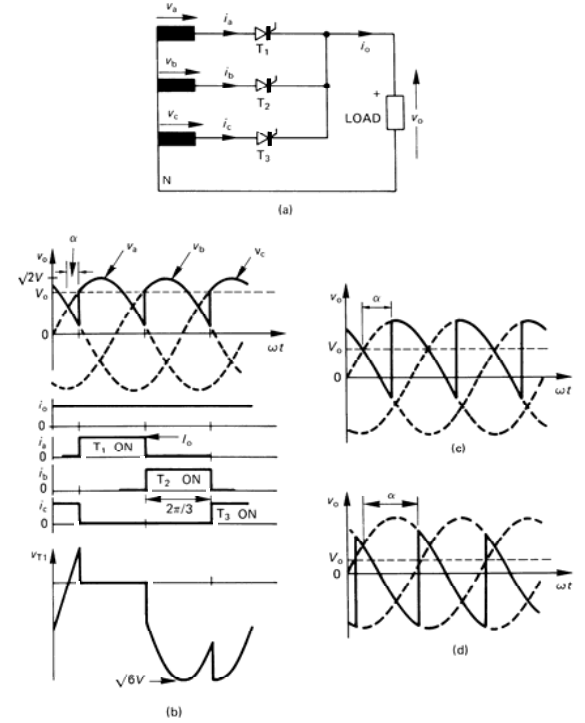


Figure 11.16. *Three-phase half-wave controlled converter: (a) circuit connection; (b) voltage and current waveforms for a small firing delay angle α; (c) and (d) load voltage waveforms for progressively larger delay angles.*

The maximum mean output voltage $\hat{V}_o = \sqrt{2}V\,3\sqrt{3}/2\pi$ occurs at $\alpha = 0$. The normalised mean output voltage V_n is

$$V_n = V_o/\hat{V}_o = \cos\alpha \qquad (11.100)$$

For **discontinuous conduction**, the mean output voltage is

$$V_o = \bar{I}_o R = \frac{3\sqrt{3}}{2\pi}\sqrt{2}V\left(1+\cos\left(\alpha+\pi/6\right)\right) \quad \text{(V)} \qquad (11.101)$$
$$\pi/6 \le \alpha \le 5\pi/6$$

The mean output voltage is zero for $\alpha = ½\pi$. For $0 < \alpha < \pi/6$, the instantaneous output voltage is always greater than zero. Negative average output voltage occurs when $\alpha > ½\pi$ as shown in figure 11.16d. Since the load current direction is unchanged, for $\alpha > ½\pi$, power reversal occurs, with energy feeding from the load into the ac supply. Power inversion assumes a load with an emf to assist the current flow, as in figure 11.11. If $\alpha > \pi$ no reverse bias exists for natural commutation and continuous load current will freewheel.

With an *R-L* load, at $V_o = 0$, the load current falls to zero. Thus for $\alpha > ½\pi$, continuous load current does not flow for an *R-L* load.

The rms output voltage is given by

$$V_{rms} = \sqrt{\frac{3}{2\pi}\int_{\alpha-\pi/3}^{\alpha+\pi/3}\left(\sqrt{2}V\right)^2\sin^2(\omega t)\,d\omega t}$$
$$= \sqrt{3}\sqrt{2}V\left(\frac{1}{6}+\frac{\sqrt{3}}{8\pi}\sin 2\alpha\right)^{½} \qquad (11.102)$$

11.6.2 Half-wave converter with freewheel diode

Figure 11.17 shows a three-phase, half-wave controlled rectifier converter circuit with a load freewheel diode. This diode prevents the load voltage from going negative, thus inversion is not possible.

***11.6.2i* - For $\alpha < \pi/6$** the output is as in figure 11.16b, with no voltage zeros occurring. The mean output is given by equation (11.99), that is

$$V_o = \bar{I}_o R = \frac{3\sqrt{3}}{2\pi}\sqrt{2}V\cos\alpha = 1.17V\cos\alpha \quad \text{(V)} \qquad (11.103)$$
$$0 \le \alpha \le \pi/6 \quad \text{(rad)}$$

The maximum mean output $V_o = \sqrt{2}V\,3\sqrt{3}/2\pi$ occurs at $\alpha = 0$. The normalised mean output voltage, V_n is given by

$$V_n = V_o/\hat{V}_o = \cos\alpha \qquad (11.104)$$

***11.6.2ii* - For $\alpha > \pi/6$**, voltage zeros occur and the negative portions in the waveforms in parts c and d of figure 11.16 do not occur. The mean output voltage is given by

$$V_o = \bar{I}_o R = \frac{\sqrt{2}V}{2\pi/3}\int_{\alpha-\pi/6}^{\pi}\sin\omega t\,d\omega t$$
$$= \frac{\sqrt{2}V}{2\pi/3}\left(1+\cos(\alpha+\pi/6)\right) \quad \text{(V)} \qquad (11.105)$$
$$\pi/6 \le \alpha \le 5\pi/6$$

The normalised mean output voltage V_n is

$$V_n = V_o/\hat{V}_o = [1 + \cos(\alpha+\pi/6)]/\sqrt{3} \qquad (11.106)$$

The average load current is given by

$$\bar{I}_o = \frac{V_o - E}{R} \qquad (11.107)$$

These equations assume continuous load current.

11.6.2i – For $\alpha > 5\pi/6$. A delay angle of greater than $5\pi/6$ would imply a negative output voltage, clearly not possible with a freewheel load diode.

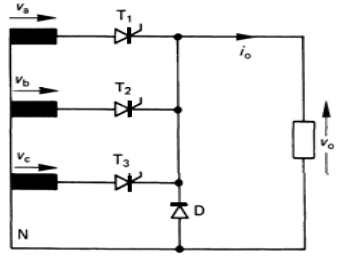


Figure 11.17. *A half-wave fully controlled three-phase converter with a load freewheel diode.*

11.6.3 Full-wave circuit with an inductive load

A three-phase bridge is fully controlled when all six bridge devices are thyristors, as shown in figure 11.18a. The frequency of the output ripple voltage is six times the supply frequency and each thyristor always conducts for ⅔π. Circuit waveforms are shown in figure 11.18b. The mean output voltage is given by

$$V_o = \frac{3}{\pi}\int_{\alpha+\pi/6}^{\alpha+\frac{1}{2}\pi} \sqrt{2}\sqrt{3}V\sin\left(\omega t+\pi/6\right)d\,\omega t$$

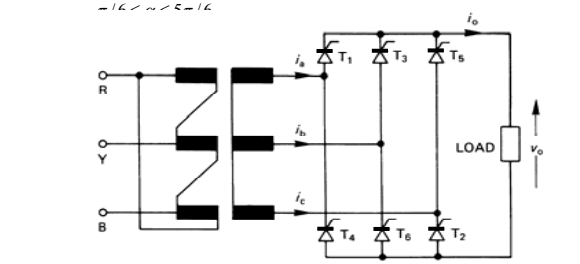
$$= \frac{3\sqrt{3}}{\pi}\sqrt{2}V\cos\alpha = 2.34V\cos\alpha \qquad \text{(V)} \qquad (11.108)$$

$$0 \le \alpha \le \pi/6$$

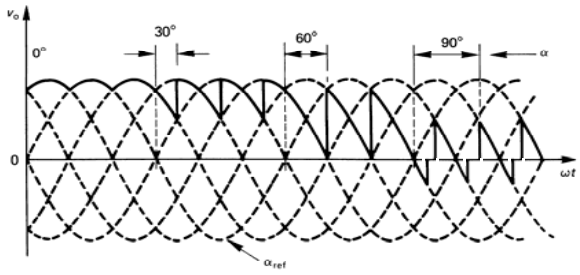
which is twice the voltage given by equation (11.99) for the half-wave circuit, and

$$V_o = \frac{3\sqrt{3}}{\pi}\sqrt{2}V\left[1+\cos\left(\alpha+\pi/6\right)\right] = 2.34V\cos\alpha \quad \text{(V)} \qquad (11.109)$$

$$\pi/6 \le \alpha \le 5\pi/6$$



(a)



(b)

Figure 11.18. *A three-phase fully controlled converter: (a) circuit connection and (b) load voltage waveform for four delay angles.*

The average output current is given by $\bar{I}_o = V_o / R$ in each case. If a load back emf exists the average current becomes

$$\bar{I}_o = \frac{V_o - E}{R} \qquad (11.110)$$

The maximum mean output voltage $\hat{V}_o = \sqrt{2}V\ 3\sqrt{3}/\pi$ occurs at $\alpha = 0$. The normalised mean output V_n is

$$V_n = V_o / \hat{V}_o = \cos\alpha \qquad (11.111)$$

For delay angles up to ⅓π, the output voltage is at all instances non-zero, hence the load current is continuous for any passive load. Beyond ⅓π the load current may be discontinuous. For $\alpha >$ ½π the current is always discontinuous for passive loads and the average output voltage is less than zero. With a load back emf the critical inductance for continuous load current must satisfy

$$\frac{R}{Z}\times\left[\sin\left(\alpha-\phi+\tfrac{1}{3}\pi\right)+\frac{\sin\left(\alpha-\phi\right)}{e^{-\pi/3\tan\phi}-1}\right] \ge \frac{E}{\sqrt{3}\sqrt{2}V} \qquad (11.112)$$

where $\tan\phi = \omega L / R$.

The rms value of the output voltage is given by

$$V_{rms} = \left(\frac{3}{\pi}\int_{\alpha-\pi/6}^{\alpha+\pi/2} 3\left(\sqrt{2}V\right)^2\sin^2(\omega t)\,d\,\omega t\right)^{\frac{1}{2}}$$

$$= \sqrt{3}\sqrt{2}V\left(1+\frac{3\sqrt{3}}{2\pi}\sin 2\alpha\right)^{\frac{1}{2}} \qquad (11.113)$$

The normalise voltage harmonic peaks magnitudes in the output voltage, with continuous load current, are

$$\frac{V_n}{V_o} = \left(\frac{1}{(6n-1)^2}+\frac{1}{(6n+1)^2}-\frac{2\cos 2\alpha}{(6n-1)(6n+1)}\right)^{\frac{1}{2}} \qquad (11.114)$$

for n = 1, 2, 3…

11.6.4 Full-wave converter with freewheel diode

Both half-controlled and fully controlled converters can employ a load freewheel diode. These circuits have the voltage output characteristic that the output voltage can never go negative, hence power inversion is not possible. Figure 11.19 shows a fully controlled three-phase converter with a freewheel diode D.

- The freewheel diode is active for $\alpha >$ ⅓π. The output is as in figure 11.18b for $\alpha <$ ⅓π. The mean output voltage is

$$V_o = \bar{I}_o R = \frac{3\sqrt{3}}{\pi}\sqrt{2}V\cos\alpha = 2.34V\cos\alpha \quad \text{(V)} \qquad (11.115)$$
$$0 \le \alpha \le \pi/3 \quad \text{(rad)}$$

The maximum mean output voltage $\hat{V}_o = \sqrt{2}V\,3\sqrt{3}/\pi$ occurs at $\alpha = 0$.
The normalised mean output voltage V_n is given by

$$V_n = V_o/\hat{V}_o = \cos\alpha \qquad (11.116)$$

- while

$$V_o = \bar{I}_o R = \frac{3\sqrt{3}}{\pi}\sqrt{2}V\left(1+\cos\left(\alpha+\pi/3\right)\right) \quad \text{(V)} \qquad (11.117)$$
$$\pi/3 \le \alpha \le 2\pi/3 \quad \text{(rad)}$$

The normalised mean output, V_n, is

$$V_n = V_o/\hat{V}_o = 1+\cos\left(\alpha+\pi/3\right) \qquad (11.118)$$

- while

$$V_o = 0 \quad \text{(V)} \qquad (11.119)$$
$$2\pi/3 \le \alpha \quad \text{(rad)}$$

In each case the average output current is given by $\bar{I}_o = V_o/R$, which can be modified to include any load back emf, that is, $\bar{I}_o = \left(V_o - E\right)/R$.

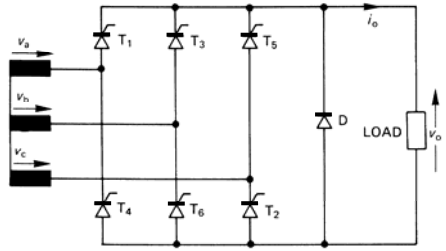


Figure 11.19. *A full-wave three-phase controlled converter with a load free-wheeling diode (half-controlled).*

Example 11.3: ***Converter average load voltage***

Derive a general expression for the average load voltage of an *n*-pulse controlled converter.

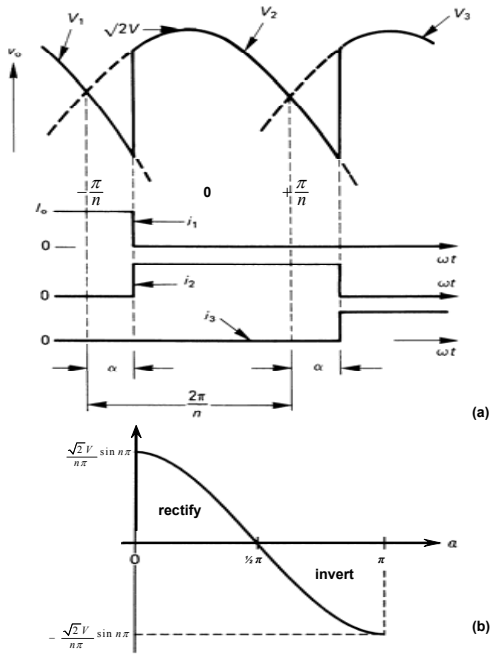


Figure 11.20. *A half-wave n-phase controlled converter: (a) output voltage and current waveform and (b) transfer function of voltage versus delay angle α.*

Solution

Figure 11.20 defines the general output voltage waveform where *n* is the output pulse number. From the output voltage waveform

$$V_o = \frac{1}{2\pi/n}\int_{-\pi/n+\alpha}^{\pi/n+\alpha}\sqrt{2}\,V\cos\omega t\; d\omega t$$
$$= \frac{\sqrt{2}\,V}{2\pi/n}\left(\sin(\alpha+\pi/n)-\sin(\alpha-\pi/n)\right)$$
$$= \frac{\sqrt{2}\,V}{2\pi/n}2\sin(\pi/n)\cos\alpha$$
$$V_o = \frac{\sqrt{2}\,V}{\pi/n}\sin(\pi/n)\cos\alpha$$
$$= \hat{V}_o\cos\alpha \qquad \text{(V)}$$

where

for $n = 2$ for the single-phase full-wave controlled converter in figure 11.9.
for $n = 3$ for the three-phase half-wave controlled converter in figure 11.16.
for $n = 6$ for the three-phase full-wave controlled converter in figure 11.18.

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11.7 Overlap

In the previous sections, impedance of the ac source has been neglected, such that current transfers or *commutates* instantly from one switch to the other with higher anode potential. However, in practice the source has inductive reactance X_c and current takes a finite time to fall in the device turning off and rise in the device turning on.

Consider the three-phase half-wave controlled rectifying converter in figure 11.16a, where it is assumed that a continuous dc load current, I_o, flows. When thyristor T_1 is conducting and T_2 is turned on after delay α, the equivalent circuit is shown in figure 11.21a. The source reactances X_1 and X_2 limit the rate of change of current in T_1 as i_1 decreases from I_o to 0 and in T_2 as i_2 increases from 0 to I_o. These current transitions in T_1 and T_2 are shown in the waveforms of figure 11.21d. A circulating current, i, flows between the two thyristors. If the line reactances are identical, the output voltage during commutation, v_γ, is mid-way between the conducting phase voltages v_1 and v_2, as shown in figure 12.21b. That is $v_\gamma = ½(v_1 + v_2)$, creating a series of notches in the output voltage waveform as shown in figure 11.21c. This interval during which both T_1 and T_2 conduct ($i \neq 0$) is termed the *overlap period* and is defined by the *overlap angle* γ. Ignoring thyristor voltage drops, the overlap angle is calculated as follows

$$v_2 - v_1 = 2L\,di/dt$$

With reference $t = 0$ when T_2 is triggered

$$v_2 - v_1 = v_L = \sqrt{3}\,v_{phase} = \sqrt{3}\sqrt{2}\,V\sin(\omega t + \alpha)$$

where V is the line to neutral rms voltage.

Equating these two equations

$$2L\,di/dt = \sqrt{3}\sqrt{2}\,V\sin(\omega t + \alpha)$$

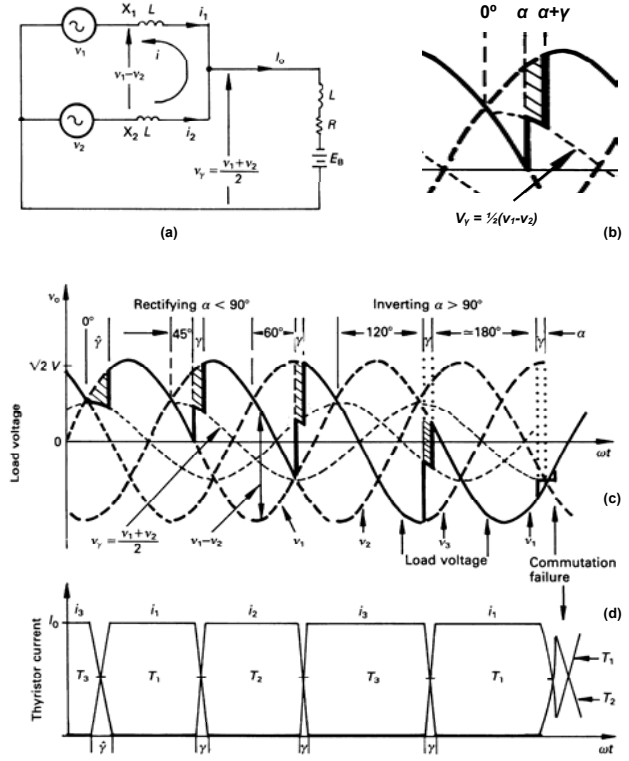

Figure 11.21. *Overlap: (a) equivalent circuit during overlap; (b) angle relationships; (c) load voltage for different delay angles α (hatched areas equal to I_oL; last overlap shows commutation failure); and (d) thyristor currents showing eventual failure.*

Rearranging and integrating gives

$$i(\omega t) = \frac{\sqrt{3}\sqrt{2}V}{2\omega L}\left(\cos\alpha - \cos\left(\omega t + \alpha\right)\right)$$

Commutation from T_1 to T_2 is complete when $i=I_o$, at $\omega t = \gamma$, that is

$$I_o = \frac{\sqrt{3}\sqrt{2}V}{2\omega L}\left(\cos\alpha - \cos\left(\gamma + \alpha\right)\right) \qquad \text{(A)} \qquad (11.120)$$

Figure 11.21b shows that the load voltage comprises the phase voltage v_2 when no source inductance exists minus the voltage due to circulating current v_γ (= ½(v_1 + v_2)) during commutation.

The mean output voltage V_o^γ is therefore

$$V_o^\gamma = V_o - \bar{v}_\gamma$$

$$= \frac{1}{2\pi/3}\left[\int_{\alpha+\pi/6}^{\alpha+5\pi/6} v_2\, d\omega t - \int_{\alpha+\pi/6}^{\gamma+\alpha+\pi/6} v_\gamma\, d\omega t \right]$$

where v_γ= ½(v_1 + v_2)

$$V_o^\gamma = \frac{3}{2\pi}\left[\int_{\alpha+\pi/6}^{\alpha+5\pi/6} \sqrt{2}\,V \sin\left(\omega t + \alpha\right) d\omega t - \int_{\alpha+\pi/6}^{\gamma+\alpha+\pi/6} \sqrt{2}\,V \left\{\sin\left(\omega t + 2\pi/3\right) + \sin\omega t\right\} d\omega t \right]$$

$$V_o^\gamma = \frac{3}{2\pi}\sqrt{3}\sqrt{2}V\cos\alpha - \frac{3}{2\pi}\frac{\sqrt{3}}{2}\sqrt{2}V\left(\cos\alpha - \cos\left(\alpha - \gamma\right)\right) \qquad (11.121)$$

$$V_o^\gamma = \frac{3\sqrt{3}}{4\pi}\sqrt{2}V\left[\cos\alpha + \cos\left(\alpha + \gamma\right)\right] \qquad (11.122)$$

which reduces to equation (11.99) when $\gamma = 0$. Substituting cos α - cos (α + γ) from equation (11.120) into equation (11.121) yields

$$V_o^\gamma = \frac{3\sqrt{3}}{2\pi}\sqrt{2}V\cos\alpha - \frac{3}{2\pi}\omega L I_o \qquad (11.123)$$

$$\text{that is} \quad V_o^\gamma = V_o - \frac{3}{2\pi}\omega L I_o \qquad (11.124)$$

The mean output voltage V_o is reduced or regulated by the commutation reactance X_c = ωL and varies with load current magnitude I_o. Converter semiconductor voltage drops also regulate the output voltage. The component $3\omega L/2\pi$ is called the *equivalent internal resistance.* Being an inductive phenomenon, it does not represent a power loss component.

The overlap occurs immediately after the delay α. The commutation voltage, v_2 - v_1, is $\sqrt{3}$ $\sqrt{2}$ V sin α. The commutation time is inversely proportional to the commutation

voltage v_2 - v_1. As α increases to π, the commutation voltage increases to a maximum and the overlap angle γ decreases to a minimum at ½π. From equation (11.120), with α = π

$$\gamma = arc\ \sin(2\omega L I_o / \sqrt{2}\sqrt{3}\ V)$$

The general expressions for the mean load voltage V_o^γ of a n-pulse, fully-controlled rectifier, with underlap, are given by

$$V_o^\gamma = \frac{\sqrt{2}V}{2\pi/n}\sin\pi/n\left[\cos\alpha + \cos\left(\alpha + \gamma\right)\right] \qquad (11.125)$$

and

$$V_o^\gamma = \frac{\sqrt{2}V}{\pi/n}\sin\pi/n\cos\alpha \quad - \quad nX_c I_o/2\pi \qquad (11.126)$$

where V is the line voltage for a full-wave converter and the phase voltage for a half-wave converter. Effectively, as shown in figure 11.22, overlap reduces the mean output voltage by $nfLI_0$ or as if α were increased. The supply voltage is effectively distorted and the harmonic content of the output is increased. Equating equations (11.125) and (11.126) gives the mean output current

$$I_o = \frac{\sqrt{2}V}{X_c}\sin\pi/n\left(\cos\alpha - \cos\left(\gamma + \alpha\right)\right) \qquad \text{(A)} \qquad (11.127)$$

which reduces to equation (11.120) when n = 3.

Harmonic input current magnitudes are decreased by a factor $\sin\left(½n\gamma\right)/½n\gamma$.

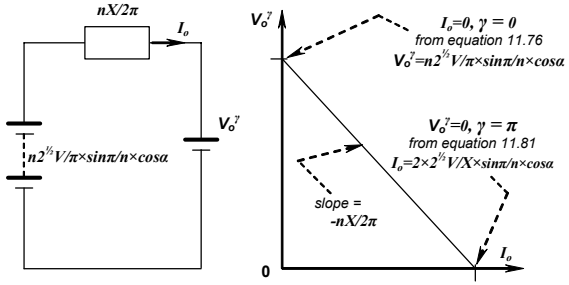

Figure 11.22. *Overlap regulation model:*
(a) equivalent circuit and (b) load plot of overlap model.

11.8 Overlap - inversion

A fully controlled converter operates in the inversion mode when $\alpha > 90°$ and the mean output voltage is negative and less than the load back emf shown in figure 11.21a. Since the direction of the load current I_o is from the supply and the output voltage is negative, energy is being returned, *regenerated* into the supply from the load. Figure 11.23 shows the power flow differences between rectification and inversion. As α decreases, the return energy magnitude increases. If α plus the overlap γ exceeds $\omega t = \pi$, commutation failures occurs. The output goes positive and the load current builds up uncontrolled. The last commutation with $\alpha \approx \pi$ in figures 11.21b and c results in a commutation failure of thyristor T_1. Before the circulating inductor current i has reduced to zero, the incoming thyristor T_2 experiences an anode potential which is less positive than that of the thyristor to be commutated T_1, $v_1 - v_2 < 0$. The incoming device T_2 fails to stay on and conduction continues through T_1, impressing positive supply cycles across the load. This positive converter voltage aids the load back emf and the load current builds up uncontrolled.

Equations (11.125) and (11.126) are valid provided a commutation failure does not occur. The controllable delay angle range is curtailed to

$$0 \le \alpha \le \pi - \gamma$$

The maximum allowable delay angle $\hat{\alpha}$ occurs when $\hat{\alpha} + \gamma = \pi$ and from equations (11.125) and (11.126) with $\alpha + \gamma = \pi$ gives

$$\hat{\alpha} = \cos^{-1}\left\{\frac{XI_o}{\sqrt{2}V \sin \pi/n} - 1\right\} < \pi \qquad \text{(rad)} \qquad (11.128)$$

In practice commutation must be complete δ rad before $\omega t = \pi$, in order to allow the outgoing thyristor to regain a forward blocking state. That is $\alpha + \gamma + \delta < \pi$. δ is known as the *recovery* or *extinction angle.*

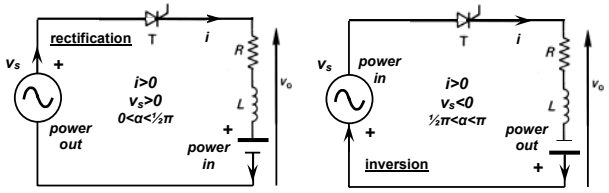

Figure 11.23. Controlled converter model showing: *(a) rectification and (b) inversion.*

Example 11.4: ***Converter overlap***

A three-phase full-wave converter is supplied from the 415 V ac, 50 Hz mains with phase source inductance of 0.1 mH. If the average load current is 100 A continuous, determine the supply reactance voltage drop, the overlap angle, and mean output voltage for phase delay angles of (i) 0º and (ii) 60º

Ignoring thyristor forward blocking time requirements, determine the maximum allowable delay angle.

Solution

Using equations (11.125) and (11.126) with $n = 6$ and $V = 415$ V ac, the mean supply reactance voltage

$$\bar{v}_\gamma = \frac{n}{2\pi} 2\pi f L I_o = \frac{6}{2\pi} \times 2\pi 50 \times 10^{-4} \times 10^2$$
$$= 3\text{V}$$

i. $\alpha = 0°$ - as for uncontrolled rectifiers. From equation (11.126), the maximum output voltage is

$$V_o^\gamma = \frac{\sqrt{2}V}{2\pi/n} \sin \pi/n \cos\alpha - nX_c I_o / 2\pi$$
$$= \frac{\sqrt{2} \times 415}{2\pi/6} \sin \pi/6 \times \cos 0 - 3\text{V} = 557.44\text{V}$$

From equation (11.125)

$$V_o^\gamma = \frac{\sqrt{2}V}{2\pi/n} \sin \pi/n \left[\cos\alpha + \cos(\alpha + \gamma)\right]$$
$$557.44 = \frac{\sqrt{2} \times 415}{2\pi/6} \times \sin \pi/6 \times \left[1 + \cos\gamma\right]$$

that is $\gamma = 8.4°$

ii. $\alpha = 60º$

$$V_o^\gamma = \frac{\sqrt{2}V}{2\pi/n} \sin \pi/n \cos\alpha + nX_c I_o / 2\pi$$
$$= \frac{\sqrt{2} \times 415}{2\pi/6} \sin \pi/6 \times \cos 60° - 3\text{V} = 277.22\text{V}$$

$$V_o^{\gamma} = \frac{\sqrt{2}V}{2\pi/n}\sin\pi/n\left[\cos\alpha+\cos(\alpha+\gamma)\right]$$

$$277.22 = \frac{\sqrt{2}\times 415}{2\pi/6}\times ½\times\left[\cos 60°+\cos(60°+\gamma)\right]$$

that is $\gamma = 0.71°$

Equation (11.128) gives the maximum allowable delay angle as

$$\hat{\alpha} = \cos^{-1}\left\{\frac{X I_o}{\sqrt{2}V\sin\pi/n}-1\right\}$$

$$= \cos^{-1}\left\{\frac{2\pi 50\times 10^{-4}\times 10^{2}}{\sqrt{2}\times 415\times ½}-1\right\}$$

$$= 171.56° \text{ and } V_o^{\gamma} = -557.41\text{V}$$

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11.9 Summary

General expressions for n-phase converter mean output voltage, V_o

(i) Half-wave and full-wave, fully-controlled converter

$$V_o = \sqrt{2}V\,\frac{\sin(\pi/n)}{\pi/n}\cos\alpha$$

where V is
the rms line voltage for a full-wave converter or
the rms phase voltage for a half-wave converter.
$\cos\alpha = \cos\psi$, the supply displacement factor

(ii) Full-wave, half-controlled converter

$$V_o = \sqrt{2}V\,\frac{\sin(\pi/n)}{\pi/n}\left(1+\cos\alpha\right)$$

where V is
the rms line voltage.

(iii) Half-wave and full-wave controlled converter with load freewheel diode

$$V_o = \sqrt{2}V\,\frac{\sin(\pi/n)}{\pi/n}\cos\alpha \qquad 0 < \alpha < ½\pi - \pi/n$$

$$V_o = \sqrt{2}V\,\frac{1+\cos(\alpha+½\pi-\pi/n)}{2\pi/n} \qquad ½\pi-\pi/n < \alpha < ½\pi+\pi/n$$

the output rms voltage is given by

$$V_{rms} = \sqrt{2}V\sqrt{½+\frac{\cos 2\alpha\sin 2\pi/n}{4\pi/n}} \qquad \alpha+\pi/n \le ½\pi$$

$$V_{rms} = \sqrt{2}V\sqrt{¼+\frac{n}{8}-\frac{\alpha}{4\pi/n}-\frac{\cos(2\alpha-2\pi/n)}{8\pi/n}} \qquad \alpha+\pi/n > ½\pi$$

where V is
the rms line voltage for a full-wave converter or
the rms phase voltage for a half-wave converter.
$n = 0$ for single-phase and three-phase half-controlled converters
$= \frac{1}{6}\pi$ for three-phase half-wave converters
$= ⅓\pi$ for three-phase fully controlled converters

These voltage output characteristics are shown in figure 11.24 and the main converter circuit characteristics are shown in table 11.1.

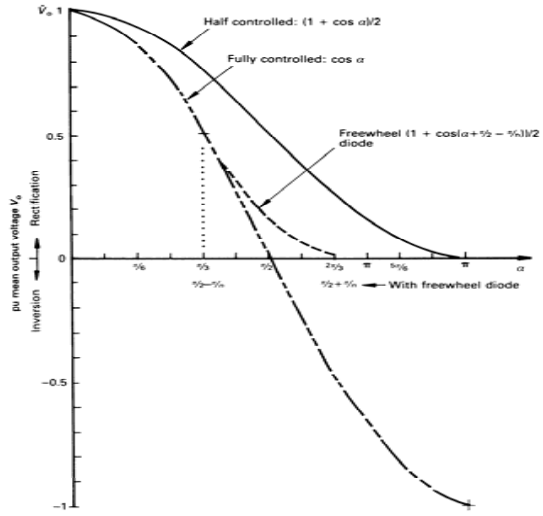

Figure 11.24. *Converter normalised output voltage characteristics as a function of firing delay angle α.*

11.10 Definitions

V_o average output voltage $\quad \bar{I}_o$ average output current

V_{rms} rms output voltage $\quad I_{rms}$ rms output current

Load voltage form factor = $FF_v = V_{rms} / V_o$

Load current form factor = $FF_i = I_{rms} / \bar{I}_o$

$$\text{Rectification efficiency} = \eta = \frac{\text{dc load power}}{\text{ac load power + rectifier losses}} = \frac{V_o I_o}{V_{rms} I_{rms} + \text{Loss}_{\text{rectifier}}}$$

$$\text{Waveform smoothness} = \text{Ripple factor} = K_v = \frac{\text{effective values of ac } V \text{ (or } I\text{)}}{\text{average value of } V \text{ (or } I\text{)}} = \frac{V_{Rv}}{V_o} = \sqrt{\frac{V_{rms}^2 - V_o^2}{V_o^2}} = \sqrt{FF_v^2 - 1}$$

where $V_{Rv} = \left[\sum_{n=1}^{\infty} \tfrac{1}{2}\left(v_{an}^2 + v_{bn}^2\right)\right]^{1/2}$

similarly the current ripple factor is $K_i = \frac{I_{Ri}}{\bar{I}_o} = \sqrt{FF_i^2 - 1}$

$K_i = K_v$ for a resistive load

Reading list

Dewan, S. B. and Straughen, A., *Power Semiconductor Circuits,* John Wiley and Sons, New York, 1975.

Sen, P.C., *Power Electronics*, McGraw-Hill, 5th reprint, 1992.

Shepherd, W *et al*. *Power Electronics and motor control*, Cambridge University Press, Second Edition 1995.

http://www.ipes.ethz.ch/

Table 11.1 Main characteristics of converter circuits

Ouput phase number n and ripple frequency (xf_s):	*1*	*2*				*3*	*6*	
Type of controlled circuit:		*Single-phase bridge*					*Three-phase bridge*	
	Single-phase half-wave 11.6	*Two-phase half-wave 11.9a*	*Fully controlled 11.9b*	*Half controlled 11.5b*	*Three-phase half-wave 11.16*	*Fully controlled 11.18*	*Half controlled 11.15*
Text figure number:							
Maximum output voltage $\hat{V}_o$ (α = 0 or diode bridge V is rms phase voltage	$\sqrt{2}\,V/\pi$ (0.45 V)	$2\sqrt{2}\,V/\pi$ (0.9 V)			$3\sqrt{3}\,\sqrt{2}\,V/2\pi$ (1.17 V)	$3\sqrt{3}\sqrt{2}\,V/\pi$ (2.33 V)		
Mean output voltage: Normalised controlled mean output voltage $V_o/\hat{V}_o$ — Pure resistive load or with freewheel diode D_f	$\frac{1+\cos\alpha}{2}$	$\frac{1+\cos\alpha}{2}$			$0 \leqslant \alpha \leqslant \pi/6$: $\cos\alpha$; $\pi/6 < \alpha \leqslant 5\pi/6$: $\frac{1+\cos(\alpha+\pi/6)}{\sqrt{3}}$	$0 \leqslant \alpha \leqslant \pi/3$: $\cos\alpha$; $\pi/3 < \alpha < 2\pi/3$: $1+\cos(\alpha+\pi/3)$	$\frac{1+\cos\alpha}{2}$	
Inductive load without D_f		$\cos\alpha$	$\frac{1+\cos\alpha}{2}$		$\cos\alpha$	$\cos\alpha$	$\frac{1+\cos\alpha}{2}$	

Equivalent internal resistance $i\ nX/2\pi \quad X = \omega L$		0.318X	0.637X		0.477X	0.955X	
Output voltage ripple ratio (per cent) ($\alpha = 0$, $\gamma = 0$)	121	48			19	4.2	
Rectifying device — Average current I_o/n	I_o	$I_o/2$			$I_o/3$	$I_o/3$	
Rectifying device — Peak voltage, $\times V$	$\sqrt{2}$	$2\sqrt{2}$			$\sqrt{3}\sqrt{2}$	$\sqrt{3}\sqrt{2}$	
Supply rms currents — Fundamental I_1			$2\sqrt{2}\,I_o/\pi$	$\frac{2\sqrt{2}\,I_o}{\pi}\cos\alpha/2$		$\sqrt{6}\,I_o/\pi$	
Supply rms currents — Total I_s			I_o	$I_o\sqrt{1-\alpha/\pi}$		$\sqrt{\frac{2}{3}}\,I_o$	
Supply factors — Harmonic factor ρ			$\sqrt{\frac{\pi^2}{8}-1}$	$\sqrt{\frac{\pi(\pi-\alpha)}{4(1+\cos\alpha)}-1}$		$\sqrt{\left(\frac{\pi}{3}\right)^2-1}$	
Supply factors — Displacement factor, $\cos\psi$			$\cos-\alpha$	$\cos-\alpha/2$		$\cos-\alpha$	
Supply factors — Power factor λ			$\frac{2\sqrt{2}}{\pi}\cos\alpha$	$\frac{\sqrt{2}(1+\cos\alpha)}{\sqrt{\pi(\pi-\alpha)}}$		$\frac{3}{\pi}\cos\alpha$	

Problems

11.1. For the circuit shown in figure 11.25, if the thyristor is fired at $\alpha = \frac{1}{3}\pi$
- i. derive an expression for the load current, i
- ii. determine the current extinction angle, β
- iii. determine the peak value and the time at which it occurs
- iv. sketch to scale on the same ωt axis the supply voltage, load voltage, thyristor voltage, and load current

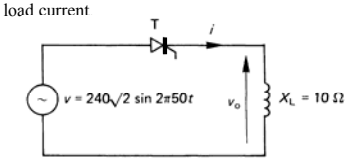

Figure 11.25. *Problem 11.1.*

11.2. For the circuit shown in figure 11.26, if the thyristor is fired at $\alpha=\frac{1}{4}\pi$ determine
- i. the current extinction angle, β
- ii. the mean and rms values of the output current
- iii. the power delivered to the source E.

Sketch the load current and load voltage v_0.

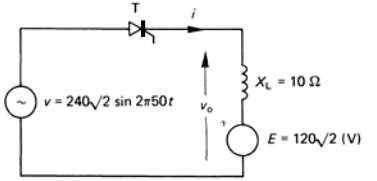

Figure 11.26. *Problem 11.2.*

11.3. Derive equations (11.17) and (11.18) for the circuit in figure 11.3.

11.4. Assuming a constant load current derive an expression for the mean and rms device current and the device form factor, for the circuits in figures 11.4 and 11.5.

11.5. Plot load ripple voltage K_{RI} and load voltage ripple factor K_v, against the thyristor phase delay angle α for the circuit in figure 11.5.

11.6. Show that the average output voltage of a *n*-phase half-wave controlled converter with a freewheel diode is characterised by

$$V_o = \sqrt{2}\,V\,\frac{\sin(\pi/n)}{\pi/n}\cos\alpha \qquad \text{(V)}$$

$$0 < \alpha < \tfrac{1}{2}\pi - \pi/n$$

$$V_o = \sqrt{2}\,V\,\frac{1+\cos\alpha+\tfrac{1}{2}\pi-\tfrac{1}{n}\pi}{2\pi/n} \qquad \text{(V)}$$

$$\tfrac{1}{2}\pi - \tfrac{1}{n}\pi < \alpha < \tfrac{1}{2}\pi + \tfrac{1}{n}\pi$$

11.7. Show that the average output voltage of a single-phase fully controlled converter is given by

$$V_o = \frac{2\sqrt{2}\,V}{\pi}\cos\alpha$$

Assume that the output current I_o is constant.
Prove that the supply current Fourier coefficients are given by

$$a_n = -\frac{4I_o}{n\pi}\sin n\alpha$$

$$b_n = \frac{4I_o}{n\pi}\cos n\alpha$$

for *n* odd.
Hence or otherwise determine (see section 12.6)

i. the displacement factor, cos ψ
ii. the distortion factor, μ
iii. the total supply power factor λ.

Determine the supply harmonic factor, ρ, if

$$\rho = I_h / I_\ell$$

where I_h is the total harmonic current and I_ℓ is the fundamental current.

11.8. Show that the average output voltage of a single-phase half-controlled converter is given by

$$v_o = \frac{\sqrt{2}\,V}{\pi}\left(1+\cos\alpha\right)$$

Assume that the output current I_o is constant.
Determine

i. the displacement factor, cos ψ
ii. the distortion factor, μ
iii. the total supply power factor, λ.

Show that the supply harmonic factor, ρ (see problem 11.7), is given by

$$\rho = \sqrt{\left[\frac{\pi(\pi-\alpha)}{4(1+\cos\alpha)} - 1\right]}$$

11.9. Draw the load voltage and current waveforms for the circuit in figure 11.8a when a freewheel diode is connected across the load. Specify the load rms voltage.

11.10. A centre tapped transformer, single-phase, full-wave converter (figure 11.9a) with a load freewheel diode is supplied from the 240 V ac, 50 Hz supply with source inductance of 0.25 mH. The continuous load current is 5 A. Find the overlap angles for

i. the transfer of current form a conducting thyristor to the load freewheel diode and
ii. from the freewheel diode to a thyristor when the delay angle α is 30°.

$$\gamma_{t-d} = \cos^{-1}\left\{1 - \frac{\omega L I_o}{\sqrt{2}\,V}\right\} = 2.76°;$$

$$\gamma_{t-d} = \cos^{-1}\left\{\cos\alpha - \frac{\omega L I_o}{\sqrt{2}\,V}\right\} - \alpha = 0.13°$$

11.11. The circuit in figure 11.6a, with $v = \sqrt{2}\,V\sin(\omega t + \alpha)$, has a steady-state time response of

$$i(\omega t) = \frac{\sqrt{2}\,V}{Z}\left\{\sin(\omega t + \alpha - \phi) - \sin(\alpha - \phi)e^{-Rt/L}\right\}$$

where α is the trigger phase delay angle after voltage crossover, and
$\phi = \tan^{-1}(\omega L / R)$
Sketch the current waveform for $\alpha = \frac{1}{4}\pi$ and Z with

i. $R >> \omega L$
ii. $R = \omega L$
iii. $R << \omega L$.

[$(\sqrt{2}\,V/R)\sin(\omega t + \frac{1}{4}\pi)$; $(V/R)\sin\omega t$; $(V/\omega L)(\sin\omega t - \cos\omega t + 1)$]

11.12. A three-phase, fully-controlled converter is connected to the 415 V supply, which has a reactance of 0.25 Ω/phase and resistance of 0.05 Ω/phase. The converter is operating in the inverter mode with α = 150º and a continuous 50 A load current. Assuming a thyristor voltage drop of 1.5 V at 50 A, determine the mean output voltage, overlap angle, and available recovery angle.
[-485.36 V -3 V -5 V -11.94 V = -505.3 V; 6.7°; 23.3°]

11.13. For the converter system in problem 11.12, what is the maximum dc current that can be accommodated at a phase delay of 165°, allowing for a recovery angle of 5°?
[35.53 A]

11.14. The single-phase half-wave controlled converter in figure 11.6 is operated from the 240 V, 50 Hz supply and a 10 Ω resistive load. If the mean load voltage is 50 per cent of the maximum mean voltage, determine the (a) delay angle, α, (b) mean and rms load current, and (c) the input power factor.

11.15. The converter in figure 11.8a, with a freewheel diode, is operated from the 240 V, 50 Hz supply. The load consists of, series connected, a 10 Ω resister, a 5 mH inductor and a 40 V battery. Derive the load voltage expression in the form of a Fourier series. Determine the rms value of the fundamental of the load current.

11.16. The converter in figure 11.5a is operated from the 240 V, 50 Hz supply with a load consisting of the series connection of a 10 Ω resistor, a 5 mH inductor, and a 40 V battery. Derive the load voltage expression in the form of a Fourier series. Determine the rms value of the fundamental of the load current.

11.17. The converter in figure 11.17 is operated from a Y-connected, 415 V, 50 Hz supply. If the load is 100 A continuous with a phase delay angle of π/6, calculate the (a) harmonic factor of the supply current, (b) displacement factor cos ψ, and (c) supply power factor, λ.

11.18. The converter in figure 11.17 is operated from the 415 V line-to-line voltage, 50 Hz supply, with a series load of 10 Ω + 5 mH + 40 V battery. Derive the load voltage expression in terms of a Fourier series. Determine the rms value of the fundamental of the load current.

11.19. Repeat problem 11.18 for the three-phase, half-controlled converter in figure 11.15.

11.20. Repeat problem 11.18 for the three-phase, fully-controlled converter in figure 11.18.

11.21. The three-phase, half-controlled converter in figure 11.15 is operated from the 415 V, 50 Hz supply, with a 100 A continuous load current. If the line inductance is 0.5 mH/phase, determine the overlap angle γ if (a) $\alpha = \pi/6$,,and,(b) $\alpha = ⅔\pi$.

11.22. Repeat *example 11.1* using a 100Vac 60Hz supply.

12

AC Voltage Regulators

AC voltage regulators have a constant voltage ac supply input and incorporate semiconductor switches which vary the rms voltage impressed across the ac load. These regulators fall into the category of naturally commutating converters since their thyristor switches are commutated by the alternating supply. This converter turn-off process is termed *line commutation*.

The regulator output current, hence supply current, may be discontinuous or non-sinusoidal and as a consequence input power factor correction and harmonic reduction are usually necessary, particularly at low output voltage levels.

A feature of direction conversion of ac to ac is the absence of any intermediate energy stage, such as a dc link. Therefore ac to ac converters are potentially more efficient but usually involve a larger number of switching devices and output is lost if the input supply is temporarily lost.

There are three basic ac regulator categories, depending on the relationship between the input supply frequency f_s, which is usually assume single frequency sinusoidal, and the output frequency f_o. Without the use of transformers, the output voltage rms magnitude V_{Orms} is less than or equal to the input voltage rms magnitude V_s , $V_{Orms} \leq V_s$.

- output frequency increased, $f_o > f_s$
- output frequency decreased, $f_o < f_s$
- output frequency fundamental = supply frequency, $f_o = f_s$

12.1 Single-phase ac regulator

Figure 12.la shows a single-phase thyristor regulator supplying an *L-R* load. The two thyristors can be replaced by any of the bidirectional conducting and blocking switch arrangements shown in figure 6.11. Equally, in low power applications the two thyristors are usually replaced by a triac. The thyristor gate trigger delay angle is α, as indicated in figure 12.lb. The fundamental of the output frequency is the same as the input frequency, $\omega = 2\pi f_s$. The thyristor current, shown in figure 12.lb, is defined by equation (11.33); that is

$$L\frac{di}{dt} + Ri = \sqrt{2}V \sin \omega t \quad \text{(V)} \qquad \alpha \leq \omega t \leq \beta \quad \text{(rad)}$$
$$= 0 \qquad \text{otherwise} \qquad (12.1)$$

The solution to this first order differential equation has two solutions, depending on the delay angle α relative to the load natural power factor angle, $\phi = \tan^{-1} \omega L/R$.

Because of symmetry around the time axis, the mean supply and load, voltages and currents, are zero.

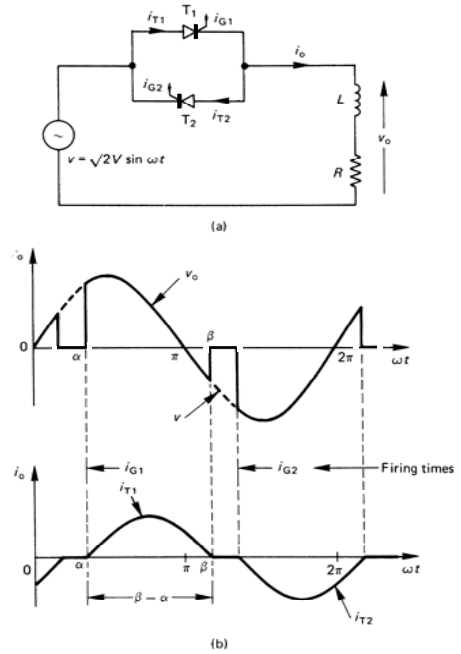

Figure 12.1. *Single-phase full-wave thyristor ac regulator with an R-L load: (a) circuit connection and (b) load current and voltage waveforms.*

12.1i - Case 1: $\alpha > \phi$

When the delay angle exceeds the power factor angle the load current always reaches zero, thus the differential equation boundary conditions are zero. The solution for *i* is

$$i(\omega t) = \frac{\sqrt{2}V}{Z}\left\{\sin\ (\omega t - \phi) - \sin(\alpha - \phi)\ e^{-\omega t + \alpha / \tan\phi}\right\} \quad \text{(A)} \qquad \alpha \le \omega t \le \beta \quad \text{(rad)} \tag{12.2}$$

$$i(\omega t) = 0 \quad \text{(A)} \qquad \pi \le \beta \le \omega t \le \pi + \alpha \quad \text{(rad)} \tag{12.3}$$

where $Z = \sqrt{(R^2 + \omega^2 L^2)}$ (ohms) and $\tan\phi = \omega L / R$

Provided $\alpha > \phi$ both regulator thyristors will conduct and load current flows symmetrically as shown in figure 12.lb.

The thyristor current extinction angle β for discontinuous load current can be determined with the aid of figure 11.7a, but with the restriction that $\beta - \alpha \le \pi$ or by solving equation 11.39, that is:

$$\sin(\beta - \phi) = \sin(\alpha - \phi)\ e^{(\alpha - \beta)/\tan\phi}$$

From figure 12.lb the rms output voltage is

$$V_{rms} = \left[\tfrac{1}{2\pi}\int_{\alpha}^{\beta}\left(\sqrt{2}\,V\right)^2 \sin^2 \omega t\ d\omega t\right]^{\frac{1}{2}} = \sqrt{2}\,V\left[\tfrac{1}{2\pi}\int_{\alpha}^{\beta}(1 - \cos 2\omega t)\,d\omega t\right]^{\frac{1}{2}}$$
$$= V\left[\tfrac{1}{2\pi}\left\{(\beta - \alpha) - \tfrac{1}{2}(\sin 2\beta - \sin 2\alpha)\right\}\right]^{\frac{1}{2}} \tag{12.4}$$

12.1ii - Case 2: $\alpha \le \phi$

When $\alpha \le \phi$, a pure sinusoidal load current flows, and substitution of $\alpha = \phi$ in equation (12.2) results in

$$i(\omega t) = \frac{\sqrt{2}V}{Z}\sin\ (\omega t - \phi) \quad \text{(A)} \qquad \alpha \le \phi \quad \text{(rad)} \tag{12.5}$$

The rms output voltage is *V,* the sinusoidal supply voltage rms value.

The power delivered to the load is therefore

$$P_o = I_{rms}^2 R = \frac{V^2}{Z}\cos\phi \tag{12.6}$$

If a short duration gate trigger pulse is used and $\alpha < \phi$, unidirectional load current will result. The device to be turned on is reverse-biased by the conducting device. Thus if the gate pulse ceases before the load current has fallen to zero, only one device conducts. It is therefore usual to employ a continuous gate pulse, or stream of pulses, from α until π, then for $\alpha < \phi$ a sine wave output current results.

In both load angle cases, the following equations are valid, except $\beta = \pi + \alpha$ is used for case 2, when $\alpha \le \phi$.

The rectified mean voltage can be used to determine the thyristor mean current rating.

$$\overline{V}_o = \tfrac{1}{2\pi}\int_{\alpha}^{\beta}\sqrt{2}\,V\sin\omega t\ d\omega t$$
$$= \sqrt{2}\,V\left[\tfrac{1}{2\pi}\{\cos\alpha - \cos\beta\}\right] \quad \text{(V)} \tag{12.7}$$

The mean thyristor current $\overline{I}_{Th} = \tfrac{1}{2}\overline{I}_o = \tfrac{1}{2}\overline{V}_o / R$, that is

$$\overline{I}_{Th} = \frac{\tfrac{1}{2}\overline{V}_o}{R} = \frac{\sqrt{2}\,V}{2R}\left[\tfrac{1}{2\pi}\{\cos\alpha - \cos\beta\}\right] \quad \text{(A)} \tag{12.8}$$

The maximum mean thyristor current is for a resistive load, $\alpha = 0$, and $\beta = \pi$, that is

$$\hat{\overline{I}}_{Th} = \sqrt{2}V \Big/ \pi R \tag{12.9}$$

The rms load current is found by the appropriate integration of equation (12.2), namely

$$I_{rms} = \left[\tfrac{1}{2\pi}\int_{\alpha}^{\beta}\left(\frac{\sqrt{2}V}{Z}\right)^2\left\{\sin\ (\omega t - \phi) - \sin(\alpha - \phi)\ e^{-\omega t + \alpha/\tan\phi}\right\}^2 d\omega t\right]^{\frac{1}{2}}$$
$$= \frac{V}{Z}\left[\tfrac{1}{2\pi}\left(\beta - \alpha - \frac{\sin(\beta - \alpha)}{\cos\phi}\cos(\beta + \alpha + \phi)\right)\right]^{\frac{1}{2}} \tag{12.10}$$

The thyristor maximum rms current is given by $I_{Th_{rms}} = I_{Orms} / \sqrt{2}$ when $\alpha \le \phi$, that is

$$\hat{I}_{Th\ rms} = V \Big/ \sqrt{2}Z \tag{12.11}$$

The thyristor forward and reverse voltage blocking ratings are both $\sqrt{2}V$.

The fundamental load voltage components are

$$a_1 = \frac{\sqrt{2}\,V}{2\pi}\{\cos 2\alpha - \cos 2\beta\}$$
$$b_1 = \frac{\sqrt{2}\,V}{2\pi}\{2(\beta - \alpha) - \sin 2\beta - \sin 2\alpha\} \tag{12.12}$$

If $\alpha \le \phi$, then continuous load current flows, and equation (12.12) reduces to $a_1 = 0$ and $b_1 = \sqrt{2}V$, when $\beta = \alpha + \pi$ is substituted.

12.1.1 Resistive Load

For a purely resistive load, the load voltage and current are related according to

$$i_o(\omega t) = v_o(\omega t) \Big/ R = \sqrt{2}V\sin(\omega t) \Big/ R \qquad \alpha \le \omega t \le \pi, \quad \alpha + \pi \le \omega t \le 2\pi$$
$$= 0 \qquad \text{otherwise}$$

The equations (12.1) to (12.6) can be simplified if the load is purely resistive. Continuous output current only flows for $\alpha = 0$, since $\phi = \tan^{-1} 0 = 0°$. Therefore the output equations are derived from the discontinuous equations (12.2) to (12.4).

The mean half-cycle output voltage, used to determine the thyristor mean current

rating, is found by integrating the supply voltage over the interval α to π, ($\beta = \pi$).

$$V_o = \tfrac{1}{2\pi}\int_{\alpha}^{\pi}\sqrt{2}V\sin\omega t\, d\omega t$$
$$= \tfrac{\sqrt{2}V}{2\pi}(1+\cos\alpha) \quad \text{(V)}$$
$$\bar{I}_o = V_o / R = \tfrac{\sqrt{2}V}{2\pi}(1+\cos\alpha) \quad \text{(A)}$$
$$\bar{I}_{Th} = \tfrac{1}{2}\bar{I}_o$$

From equation (12.4) the rms output voltage for a delay angle α is

$$V_{rms} = \sqrt{\tfrac{1}{2\pi}\int_{\alpha}^{\pi}\left(\sqrt{2}V\sin\omega t\right)^2 d\omega t} \qquad (12.13)$$
$$= \sqrt{2}V\sqrt{\tfrac{2(\pi-\alpha)+\sin 2\alpha}{4\pi}} \quad \text{(V)}$$

Therefore the output power is

$$P_o = \frac{V_{rms}^2}{R} = \frac{V^2}{R}\left\{1 - \tfrac{2\alpha-\sin 2\alpha}{2\pi}\right\} \quad \text{(W)} \qquad (12.14)$$

The rms output current and supply current from $P_o = I_{rms}^2 R$ is

$$I_{rms} = \frac{V_{rms}}{R} = \frac{V}{R}\sqrt{1 - \tfrac{2\alpha-\sin 2\alpha}{2\pi}} \quad \text{(A)}$$

and

$$I_{Trms} = I_{rms}/\sqrt{2}$$

The supply power factor λ is defined as the ratio of the real power to the apparent power, that is

$$\lambda = \frac{P_o}{S} = \frac{V_{rms}I}{V\,I} = \frac{V_{rms}}{V} = \sqrt{\frac{2(\pi-\alpha)+\sin 2\alpha}{4\pi}}$$

Example 12.1a: ***single-phase ac regulator - 1***

If the load of the 50 Hz 240V ac voltage regulator shown in figure 12.1 is Z = 7.1+j7.1 Ω, calculate the load natural power factor angle, ϕ. Then calculate

(a) the rms output voltage, and hence
(b) the output power and rms current, whence input power factor

for

i. $\alpha = \frac{1}{6}\pi$
ii. $\alpha = \frac{1}{3}\pi$

Solution

From equation (12.3) the load natural power factor angle is

$$\phi = \tan^{-1}\omega L/R = \tan^{-1}X_L/R$$
$$= \tan^{-1}7.1/7.1 = \tfrac{1}{4}\pi \text{ (rad)}$$
$$Z = \sqrt{R^2 + (\omega L)^2}$$
$$= \sqrt{7.1^2 + 7.1^2} = 10\Omega$$

i. $\alpha = \frac{1}{6}\pi$

(a) Since $\alpha = \pi/6 < \phi = \pi/4$, the load current is continuous. The rms load voltage is 240V.

(b) From equation (12.6) the power delivered to the load is

$$P_o = I_{rms}^2 R = \frac{V^2}{Z}\cos\phi$$
$$= \frac{240^2}{10}\cos\tfrac{1}{4}\pi = 4.07\text{kW}$$

The rms output current and supply current are both given by

$$I_{rms} = \sqrt{P_o/R}$$
$$= \sqrt{4.07\text{kW}/7.1\Omega} = 23.8\text{A}$$

The input power factor is the load natural power factor, that is

$$pf = \frac{P_o}{S} = \frac{4.07\text{kW}}{240\text{V}\times 23.8\text{A}} = 0.70$$

ii. $\alpha = \frac{1}{3}\pi$

(a) Since $\alpha = \pi/3 > \phi = \frac{1}{4}\pi$, the load hence supply current is discontinuous. For $\alpha = \pi/3 > \phi = \frac{1}{4}\pi$ the extinction angle $\beta = \pi$ can be extracted from figure 11.7a. The rms load voltage is given by equation (12.4).

$$V_{rms} = V\left[\tfrac{1}{2\pi}\left\{(\pi-\alpha) - \tfrac{1}{2}(\sin 2\pi - \sin 2\alpha)\right\}\right]^{\frac{1}{2}}$$
$$= 240\times\left[\tfrac{1}{2\pi}\left\{(\pi - \tfrac{1}{3}\pi) - \tfrac{1}{2}(\sin 2\pi - \sin\tfrac{2}{3}\pi)\right\}\right]^{\frac{1}{2}}$$
$$= 240\times\sqrt{1\tfrac{1}{2}} = 229.8\text{V}$$

The rms output current is given by equation (12.10), that is

$$I_{Orms} = \frac{V}{Z}\left[\tfrac{1}{\pi}\left(\beta - \alpha - \frac{\sin(\beta-\alpha)}{\cos\phi}\cos(\beta+\alpha+\phi)\right)\right]^{\frac{1}{2}}$$
$$= \frac{240}{10}\left[\tfrac{1}{\pi}\left(\pi - \tfrac{1}{3}\pi - \frac{\sin(\pi - \frac{1}{3}\pi)}{\cos\frac{1}{4}\pi}\cos(\pi + \tfrac{1}{3}\pi + \tfrac{1}{4}\pi)\right)\right]^{\frac{1}{2}}$$
$$= 18.1\text{A}$$

The output power is given by

$$P_o = I_{rms}^2 R$$
$$= 18.1^2 \times 7.1\Omega = 2313\text{W}$$

The load power factor is

$$pf = \frac{P_o}{S} = \frac{2313\text{W}}{229.8\text{V} \times 18.1\text{A}} = 0.56$$

Example 12.1b: ***single-phase ac regulator - 2***

If the load of the 50 Hz 240V ac voltage regulator shown in figure 12.1 is Z = 7.1+j7.1 Ω, calculate the minimum controllable delay angle. Using this angle calculate

i. maximum rms output voltage and current, and hence
ii. maximum output power and power factor
iii. thyristor *I-V* and *di/dt* ratings

Solution

As in example 12.1a, from equation (12.3) the load natural power factor angle is

$$\phi = \tan^{-1} \omega L / R = \tan^{-1} 7.1/7.1 = \pi/4$$

The load impedance is Z=10Ω. The controllable delay angle range is $¼\pi \le \alpha \le \pi$.

i. The maximum controllable output occurs when $\alpha = ¼\pi$.

From equation (12.2) when $\alpha = \phi$ the output voltage is the supply voltage, V, and

$$i(\omega t) = \frac{\sqrt{2}V}{Z} \sin\ (\omega t - ¼\pi) \qquad \text{(A)}$$

The load hence supply rms maximum current, is therefore

$$I_{rms} = 240\text{V}/10\Omega = 24\text{A}$$

ii. Power $= I_{rms}^2 R = 24^2 \times 7.1\Omega = 4090\text{W}$

$$\text{power factor} = \frac{\text{power output}}{\text{apparent power output}}$$
$$= \frac{I_{rms}^2 R}{V I_{rms}} = \frac{24^2 \times 7.1\Omega}{240\text{V} \times 10\text{A}} = 0.71 \quad (= \cos\phi)$$

iii. Each thyristor conducts for π radians, between α and $\pi+\alpha$ for T1 and between $\pi+\alpha$ and $2\pi+\alpha$ for T2. The thyristor average current is

$$\bar{I}_T = \frac{1}{2\pi} \int_{\alpha=\phi}^{\alpha+\pi=\phi+\pi} \sqrt{2} V \sin(\omega t - \phi)\, d\omega t$$
$$= \frac{\sqrt{2}V}{\pi Z} = \frac{\sqrt{2} \times 240\text{V}}{\pi \times 10\Omega} = 10.8\text{A}$$

The thyristor rms current rating is

$$I_{Trms} = \left[\frac{1}{2\pi} \int_{\alpha=\phi}^{\alpha+\pi=\phi+\pi} \left\{ \sqrt{2} V \sin(\omega t - \phi) \right\}^2 d\omega t \right]^{½}$$
$$= \frac{\sqrt{2}V}{2Z} = \frac{\sqrt{2} \times 240\text{V}}{2 \times 10\Omega} = 17.0\text{A}$$

Maximum thyristor di/dt is derived from

$$d\,i(\omega t)/dt = d/dt \ \frac{\sqrt{2}V}{Z} \sin\ (\omega t - ¼\pi)$$
$$= \frac{\sqrt{2}V}{Z} \omega \cos\ (\omega t - ¼\pi) \qquad \text{(A/s)}$$

This has a maximum value when $\omega t - ¼\pi = 0$, that is at $\omega t = \alpha = \phi$, then

$$d\hat{i}(\omega t)/dt = \frac{\sqrt{2}V\omega}{Z}$$
$$= \frac{\sqrt{2} \times 240\text{V} \times 2\pi \times 50\text{Hz}}{10\Omega}$$
$$= 10.7\text{A/ms}$$

Thyristor forward and reverse blocking voltage requirements are $\sqrt{2}V = \sqrt{2} \times 240$.

12.2 Three-phase ac regulator

12.2.1 Fully-controlled three-phase ac regulator

The power to a three-phase star or delta-connected load may be controlled by the ac regulator shown in figure 12.2a with a star-connected load shown. If a neutral connection is made, load current can flow provided at least one thyristor is conducting. At high power levels, neutral connection is to be avoided, because of load triplen currents that may flow through the phase inputs and the neutral. With a balanced delta connected load, no triplen or even harmonic currents occur.

If the regulator devices in figure 12.2a, without the neutral connected, were diodes, each would conduct for ½π in the order T_1 to T_6 at ⅓π radians apart.

In the fully controlled ac regulator of figure 12.2a without a neutral connection, at least two devices must conduct for power to be delivered to the load. The thyristor trigger sequence is as follows. If thyristor T_1 is triggered at α, then for a symmetrical three-phase load voltage, the other trigger angles are T_3 at $\alpha+⅔\pi$ and T_5 at $\alpha+4\pi/3$. For the antiparallel devices, T_4 (which is in antiparallel with T_1) is triggered at $\alpha+\pi$, T_6 at $\alpha+5\pi/3$, and finally T_2 at $\alpha+7\pi/3$.

Figure 12.2b shows resistive load, line-to-neutral voltage waveforms for four different phase delay angles, α. Three distinctive conduction periods (plus a non-conduction period) exist.

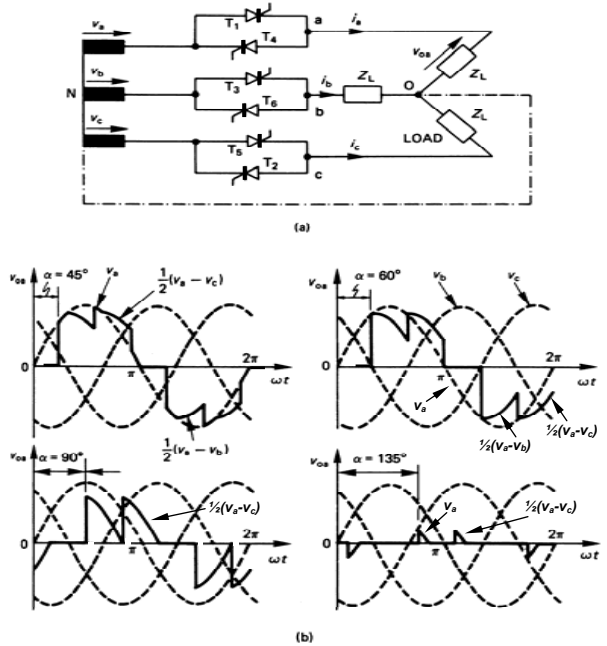

Figure 12.2. *Three-phase ac full-wave voltage controller: (a) circuit connection with a star load and (b) phase a, line-to-load neutral voltage waveforms for four firing delay angles.*

i. $0 \le \omega t \le \frac{1}{3}\pi$ [mode 2/3]

Full output occurs when $\alpha = 0$. For $\alpha \le \frac{1}{3}\pi$ three alternating devices conduct and one will be turned off by natural commutation. Only for $\omega t \le \frac{1}{3}\pi$ can three sequential devices be on simultaneously.

ii. $\frac{1}{3}\pi \le \omega t \le \frac{1}{2}\pi$ [mode 2/2]

The turning on of one device naturally commutates another conducting device and only two phases can be conducting, that is, only two thyristors conduct at any time. Line-to-neutral load voltage waveforms for $\alpha = \frac{1}{3}\pi$ and $\frac{1}{2}\pi$ are shown in figures 12.2b.

iii. $\frac{1}{2}\pi \le \omega t \le \frac{5}{6}\pi$ [mode 0/2]

Two devices must be triggered in order to establish load current and only two devices conduct at anytime. Line-to-neutral zero voltage periods occur and each device must be retriggered $\frac{1}{3}\pi$ after the initial trigger pulse. These zero output periods which develop for $\alpha \ge \frac{1}{2}\pi$ can be seen in figure 12.2b and are due to a previously on device commutating at $\omega t = \frac{5}{6}\pi$ then re-conducting at $\alpha + \frac{1}{3}\pi$. Except for regulator start up, the second firing pulse is not necessary if $\alpha \le \frac{1}{2}\pi$.

The interphase voltage falls to zero at $\alpha = \frac{5}{6}\pi$, hence for $\alpha \ge \frac{5}{6}\pi$ the output becomes zero.

Example 12.2: ***Three-phase ac regulator***

Evaluate expressions for the rms phase voltage ($V_{LL} = \sqrt{3}V_{phase} = \sqrt{3}\sqrt{2}\,V$) of the three-phase ac thyristor regulator shown in figure 12.2a, with a star-connected, balanced resistive load.

Solution

The waveforms in figure 12.2b are useful in determining the required bounds of integration. When three regulator thyristors conduct, the voltage (and the current) is of the form $\frac{\hat{V}}{\sqrt{2}}\sin\phi$, while when two devices conduct, the voltage (and the current) is of the form $\frac{\hat{V}}{2}\sin(\phi - \frac{1}{6}\pi)$. $\hat{V}$ is the maximum line voltage.

For phase delay angles $0 \le \alpha \le \frac{1}{3}\pi$

Examination of the $\alpha = \frac{1}{4}\pi$ waveform in figure 12.2b shows the voltage waveform is made from five sinusoidal segments. The rms load voltage per phase (line to neutral) is

$$V_{rms} = \hat{V}\left[\frac{1}{\pi}\left\{\int_{\alpha}^{\frac{2}{3}\pi}\tfrac{1}{3}\sin^2\phi\ d\phi + \int_{\frac{2}{3}\pi}^{\frac{1}{2}\pi+\alpha}\tfrac{1}{4}\sin^2(\phi-\tfrac{1}{6}\pi)\ d\phi + \int_{\frac{1}{2}\pi+\alpha}^{\frac{2}{3}\pi}\tfrac{1}{3}\sin^2\phi\ d\phi + \int_{\frac{2}{3}\pi}^{\frac{1}{2}\pi+\alpha}\tfrac{1}{4}\sin^2(\phi-\tfrac{1}{6}\pi)\ d\phi + \int_{\frac{1}{2}\pi+\alpha}^{\pi}\tfrac{1}{3}\sin^2\phi\ d\phi\right\}\right]^{\frac{1}{2}}$$

$$V_{rms} = I_{rms}R = V\left[1 - \tfrac{3}{2\pi}\alpha + \tfrac{3}{4\pi}\sin 2\alpha\right]^{\frac{1}{2}}$$

For phase delay angles $\frac{1}{3}\pi \le \alpha \le \frac{1}{2}\pi$

Examination of the $\alpha = \frac{1}{3}\pi$ or $\alpha = \frac{1}{2}\pi$ waveforms in figure 12.2b show the voltage waveform is comprised from two segments. The rms load voltage per phase is

$$V_{rms} = \hat{V}\left[\frac{1}{\pi}\left\{\int_{\alpha}^{\frac{1}{3}\pi+\alpha}\tfrac{1}{4}\sin^2(\phi-\tfrac{1}{6}\pi)\ d\phi + \int_{\frac{1}{3}\pi+\alpha}^{\frac{1}{2}\pi+\alpha}\tfrac{1}{4}\sin^2(\phi-\tfrac{1}{6}\pi)\ d\phi\right\}\right]^{\frac{1}{2}}$$

$$V_{rms} = I_{rms}R = V\left[\tfrac{1}{2} + \tfrac{9}{8\pi}\sin 2\alpha + \tfrac{3\sqrt{3}}{8\pi}\cos 2\alpha\right]^{\frac{1}{2}}$$

For phase delay angles $\frac{1}{2}\pi \le \alpha \le \frac{5}{6}\pi$

Examination of the $\alpha = \frac{3}{4}\pi$ waveform in figure 12.2b shows the voltage waveform is made from two segments. The rms load voltage per phase is

$$V_{rms} = \hat{V}\left[\frac{1}{\pi}\left\{\int_{\alpha}^{\frac{2}{3}\pi}\tfrac{1}{4}\sin^2(\phi - \tfrac{1}{6}\pi)\ d\theta + \int_{\frac{1}{3}\pi+\alpha}^{\frac{2}{3}\pi}\tfrac{1}{4}\sin^2(\phi - \tfrac{1}{6}\pi)\,d\phi\right\}\right]^{\frac{1}{2}}$$

$$V_{rms} = I_{rms}R = V\left[\tfrac{5}{4} - \tfrac{3}{2\pi}\alpha + \tfrac{3}{8\pi}\sin 2\alpha + \tfrac{3\sqrt{3}}{8\pi}\cos 2\alpha\right]^{\frac{1}{2}}$$

In each case the phase current and line to line voltage are related by $V_{Lrms} = \sqrt{3}I_{rms}R$ and $\hat{V} = \sqrt{2}\,V_L = \sqrt{6}\,V$.

♣

12.2.2 Half-controlled three-phase ac regulator

The half-controlled three-phase regulator shown in figure 12.3a requires only a single trigger pulse per thyristor and the return path is via a diode. Compared with the fully controlled regulator, the half-controlled regulator is simpler and does not give rise to dc components but does produce more line harmonics.

Figure 12.3b shows resistive symmetrical load, line-to-neutral voltage waveforms for four different phase delay angles, α. Three distinctive conduction periods exist.

i. $0 \le \alpha \le \frac{1}{3}\pi$

Before turn-on, one diode and one thyristor conduct in the other two phases. After turn-on two thyristors and one diode conduct, and the three-phase ac supply is impressed across the load. Examination of the $\alpha = \frac{1}{4}\pi$ waveform in figure 12.3b shows the voltage waveform is made from three segments. The rms load voltage per phase (line to neutral) is

$$V_{rms} = I_{rms}R = V\left[1 + \tfrac{3\alpha}{4\pi} - \tfrac{3}{8\pi}\sin 2\alpha\right]^{\frac{1}{2}} \qquad 0 \le \alpha \le \tfrac{1}{2}\pi \qquad (12.15)$$

ii. $\frac{1}{3}\pi \le \alpha \le \frac{2}{3}\pi$

Only one thyristor conducts at one instant and the return current is shared at different intervals by one ($\frac{1}{3}\pi \le \alpha \le \frac{1}{2}\pi$) or two ($\frac{1}{2}\pi \le \alpha \le \frac{2}{3}\pi$) diodes. Examination of the $\alpha = \frac{3}{8}\pi$ and $\alpha = \frac{5}{8}\pi$ waveforms in figure 12.3b show the voltage waveform is made from three segments, although different segments of the supply around $\omega t = \pi$. The rms load voltage per phase (line to neutral) in the first conducting case is given by equation (12.15) while after $\alpha = \frac{1}{2}\pi$ the rms voltage is

$$V_{rms} = I_{rms}R = V\left[\left\{\tfrac{11}{8} - \tfrac{3\alpha}{2\pi}\right\}\right]^{\frac{1}{2}} \qquad \tfrac{1}{2}\pi \le \alpha \le \tfrac{2}{3}\pi \qquad (12.16)$$

iii. $\frac{2}{3}\pi \le \alpha \le 7\pi/6$

Current flows in only one thyristor and one diode and at $7\pi/6$ zero power is delivered to the load. The output voltage waveform shown for $\alpha = \frac{3}{4}\pi$ in figure 12.3b has one component.

$$V_{rms} = I_{rms}R = V\left[\tfrac{7}{8} - \tfrac{3}{4\pi}\alpha + \tfrac{3}{16}\sin 2\alpha - \tfrac{3\sqrt{3}}{16}\cos 2\alpha\right]^{\frac{1}{2}} \qquad \tfrac{2}{3}\pi \le \alpha \le \tfrac{5}{6}\pi \qquad (12.17)$$

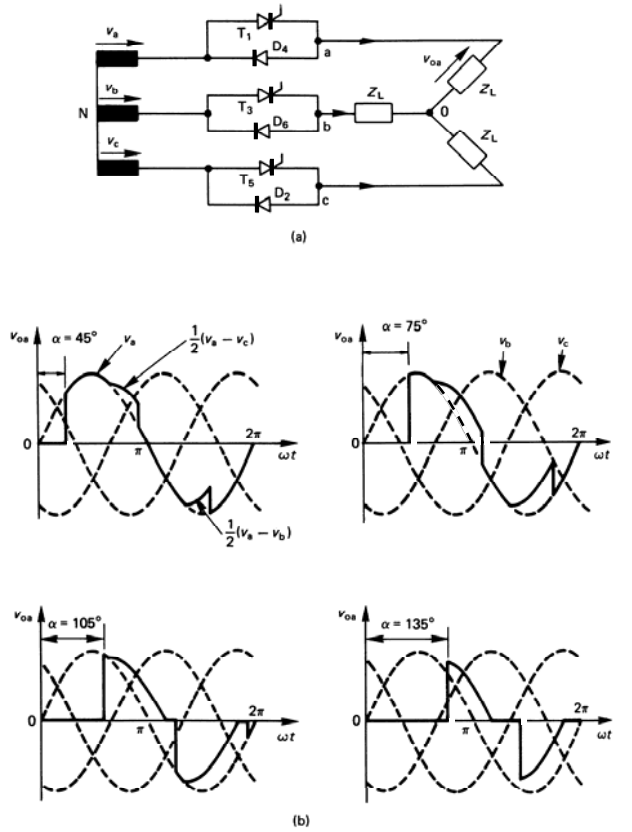

Figure 12.3. *Three-phase half-wave ac voltage regulator: (a) circuit connection with a star load and (b) phase a, line-to-load neutral voltage waveforms for four firing delay angles.*

For delta-connected loads where each phase end is accessible, the regulator shown in figure 12.4 can be employed in order to reduce thyristor current ratings. The phase rms voltage is given by

$$V_{rms}\ /\ phase = \sqrt{2}V\left[1 - \frac{\alpha}{\pi} + \frac{\sin 2\alpha}{2\pi}\right] \qquad 0 \le \alpha \le \pi \qquad (12.18)$$

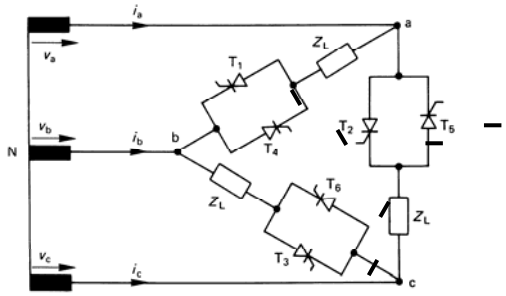

Figure 12.4. *A delta connected three-phase ac regulator.*

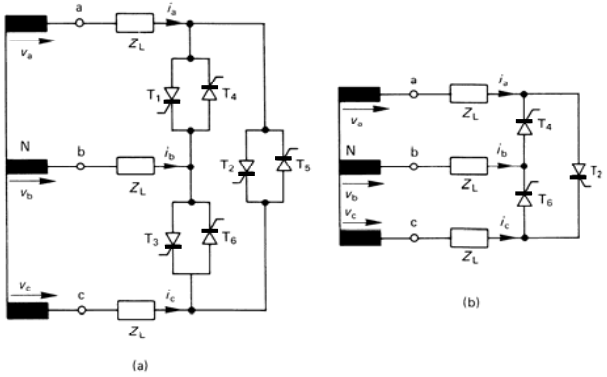

Figure 12.5. *Open-star three-phase ac regulators: (a) with six thyristors and (b) with three thyristors.*

For star-connected loads where access exists to a neutral that can be opened, the regulator in figure l2.5a can be used. This circuit produces identical load waveforms to those for the regulator in figure 12.2, except that the device current ratings are halved. Only one thyristor needs to be conducting for load current, compared with the circuit of figure 12.2 where two devices must be triggered.

The number of devices and control requirements for the regulator of figure 12.5a can be simplified by employing the regulator in figure 12.5b. Another simplification, at the expense of harmonics, is to connect one phase of the load in figure l2.2a directly to the supply, thereby eliminating a pair of line thyristors.

12.3 Integral cycle control

In thyristor heating applications, load harmonics are unimportant and integral cycle control, or burst firing, can be employed. Figure l2.6a shows the regulator when a triac is employed and figure 12.6b shows the output voltage indicating the regulator's operating principle.

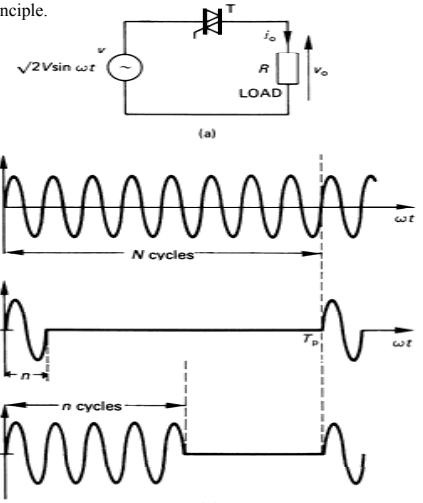

Figure 12.6. *Integral half-cycle single-phase ac control: (a) circuit connection using a triac; (b) output voltage waveforms for one-eighth maximum load power and nine-sixteenths maximum power.*

In many heating applications the load thermal time constant is long (relative to 20ms, that is 50Hz) and an acceptable control method involves a number of mains cycles on and then off. Because turn-on occurs at zero voltage cross-over and turn-off occurs at zero current, which is near a zero voltage cross-over, supply harmonics and radio frequency interference are low. The lowest order harmonic in the load is $1/T_p$.
The rms output voltage is

$$V_{rms} = \left(\frac{1}{2\pi} \int_0^{2\pi n/N} \left(\sqrt{2} V \sin N\omega t \right)^2 \, d\omega t \right)$$
$$V_{rms} = V\sqrt{n/N} \qquad (12.19)$$

The output power is

$$P = \frac{V^2}{R} \frac{n}{N} \qquad \text{(W)} \qquad (12.20)$$

where n is the number of on cycles and N is the number of cycles in the period T_p. Finer resolution output voltage control is achievable if integral half-cycles are used rather than full cycles. The average and rms thyristors currents are, respectively,

$$\bar{I}_{Th} = \frac{\sqrt{2}V}{\pi R} \frac{n}{N} \qquad I_{Th_{rms}} = \frac{\sqrt{2}V}{2R} \sqrt{\frac{n}{N}} \qquad (12.21)$$

From these two equations the distortion factor μ is $\sqrt{n/N}$ and the power transfer ratio is n/N. The supply displacement factor $\cos\psi$ is unity and supply power factor λ is $\sqrt{n/N}$, shown in figure 12.6b. The rms voltage at the supply frequency is $V\,n/N$. The equations remain valid if integral half cycle control is used. The introduction of sub-harmonics tends to restrict this control technique to resistive heating type application. Temperature effects on load resistance R have been neglected.

Example 12.3: ***Integral cycle control***

The power delivered to a 12Ω resistive heating element is derived from an ideal sinusoidal supply √2 240 sin 2π 50 t and is controlled by a series connected triac as shown in figure 12.6. The triac is controlled from its gate so as to deliver integral ac cycle pulses of three (n) consecutive ac cycles from four (N).
Calculate

i. The percentage power transferred compared to continuous ac operation
ii. The supply power factor, distortion factor, and displacement factor
iii. The supply frequency (50Hz) harmonic component voltage of the load voltage
iv. The triac maximum *di/dt* and *dv/dt* stresses
v. The phase angle α, to give the same load power when using phase angle control. Compare the maximum *di/dt* and *dv/dt* stresses with part iv.
vi. The output power steps when n, the number of conducted cycles is varied with respect to $N = 4$ cycles. Calculate the necessary phase control α equivalent for the same power output. Include the average and rms thyristor currents.
vii. What is the smallest power increment if half cycle control were to be used?

Solution
The key data is

$n = 3$
$N = 4$
$V = 240$ rms ac, 50Hz

i. The power transfer, given by equation (12.20), is

$$P = \frac{V^2}{R} \frac{n}{N} = \frac{240^2}{12\Omega} \times ¾ = 4800 \times ¾ = 3.6\text{kW}$$

That is 75% of the maximum power is transferred to the load as heating losses.

ii. The displacement factor, cosψ, is 1. The distortion factor is given by

$$\mu = \sqrt{\frac{n}{N}} = \sqrt{\frac{3}{4}} = 0.866$$

Thus the supply power factor, λ, is

$$\lambda = \mu \cos\psi = \sqrt{\frac{n}{N}} = 0.866 \times 1 = 0.866$$

iii. The 50Hz rms component of the load voltage is given by

$$V_{50\,Hz} = V \frac{n}{N} = 240 \times ¾ = 180\text{V rms}$$

iv. The maximum *di/dt* and *dv/dt* occur at zero cross over, when $t = 0$.

$$\frac{dV_s}{dt}\Big|_{\max} = \frac{d}{dt}\sqrt{2}\ 240 \sin 2\pi 50t \Big|_{t=0}$$
$$= \sqrt{2}\ 240\,(2\pi 50)\cos 2\pi 50t\Big|_{t=0}$$
$$= \sqrt{2}\ 240\,(2\pi 50) = 0.107\ \text{V/μs}$$

$$\frac{d}{dt}\frac{V_s}{R}\Big|_{\max} = \frac{d}{dt}\frac{\sqrt{2}\ 240}{12\Omega} \sin 2\pi 50t \Big|_{t=0}$$
$$= \sqrt{2}\ 20\,(2\pi 50)\cos 2\pi 50t\Big|_{t=0}$$
$$= \sqrt{2}\ 20\,(2\pi 50) = 8.89\ \text{A/ms}$$

v. To develop the same load power, 3600W, with phase angle control, with a purely resistive load, implies that both methods must develop the same rms current and voltage, that is, $V_{rms} = \sqrt{R\,P} = V\sqrt{n/N}$. From equation (12.4), when the extinction angle, $\beta = \pi$, since the load is resistive

$$V_{rms} = \sqrt{R \times P} = V\sqrt{n/N} = V\left[½\pi \left\{ (\pi - \alpha) + ½ \sin 2\alpha \right\} \right]^{½}$$

that is

$$\frac{n}{N} = \tfrac{1}{4\pi}\left\{(\pi-\alpha)+\tfrac{1}{2}\sin 2\alpha\right\}$$
$$= \tfrac{3}{4} = \tfrac{1}{4\pi}\left\{(\pi-\alpha)+\tfrac{1}{2}\sin 2\alpha\right\}$$

Solving $0 = \tfrac{1}{4}\pi - \alpha + \tfrac{1}{2}\sin 2\alpha$ iteratively gives $\alpha = 63.9°$.
When the triac turns on at α = 63.9°, the voltage across it drops virtually instantaneously from √2 240 sin 63.9 = 305V to zero. Since this is at triac turn-on, this very high *dv/dt* does not represent a turn-on *dv/dt* stress. The maximum triac *dv/dt* stress tending to turn it on is at zero voltage cross over, which is 107 V/ms, as with integral cycle control. Maximum *di/dt* occurs at triac turn on where the current rises from zero amperes to 305V/12Ω = 25.4A quickly. If the triac turns on in approximately 1μs, then this would represent a *di/dt* of 25.4A/μs. The triac initial *di/dt* rating would have to be in excess of 25.4A/μs.

cycles	period	power	$\bar{I}_{Th}$	$I_{Th_{rms}}$	Delay angle	Displacement factor	Distortion factor	Power factor
n	*N*	W	A	A	*α*	cos*ψ*	*μ*	*λ*
0	4	0	0	0	180°			
1	4	1200	2.25	7.07	114°	1	½	½
2	4	2400	4.50	10.0	90°	1	0.707	0.707
3	4	3600	6.75	12.2	63.9°	1	0.866	0.866
4	4	4800	9	14.1	1	1	1	1

vi. The output power can be varied using n = 0, 1, 2, 3, or 4 cycles of the mains. The output power in each case is calculated as in part 1 and the equivalent phase control angle, α, is calculated as in part v. The appropriate results are summarised in the table.

vii. Finer power step resolution can be attained if half cycle power pulses are used as in figure 12.6b. If one complete ac cycle corresponds to 1200W then by using half cycles, 600W power steps are possible. This results in nine different power levels if N = 4.

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12.4 Single-phase transformer tap-changer

Figure 12.7 shows a single-phase tap changer where the tapped ac voltage supply can be provided by a tapped transformer or autotransformer.
Thyristor T_3 (T_4) is triggered at zero voltage cross-over, then under phase control T_1 (T_2) is turned on. The output voltage for a resistive load is defined by

$$v_o = \sqrt{2}\,V_2 \sin\omega t \quad \text{(V)} \qquad \text{for } 0 \le \omega t \le \alpha \quad \text{(rad)} \tag{12.22}$$

$$v_o = \sqrt{2}\,V_1 \sin\omega t \quad \text{(V)} \qquad \text{for } \alpha \le \omega t \le \pi \quad \text{(rad)} \tag{12.23}$$

where α is the phase delay angle and $v_2 < v_1$.
For a resistive load the rms output voltage is

$$V_{rms} = \left[\frac{V_2^2}{\pi}(\alpha - \tfrac{1}{2}\sin 2\alpha) + \frac{V_1^2}{\pi}(\pi - \alpha + \tfrac{1}{2}\sin 2\alpha)\right]^{\frac{1}{2}} \tag{12.24}$$

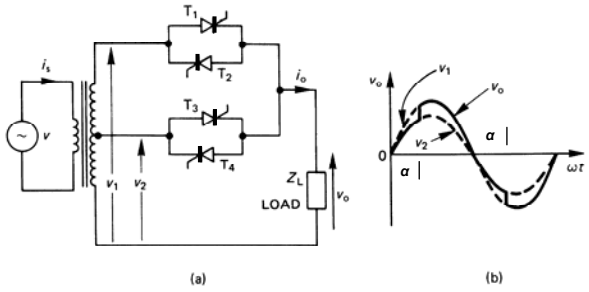

Figure 12.7. *An ac voltage regulator using a tapped transformer: (a) circuit connection and (b) output voltage waveform with a resistive load.*

Initially v_2 is impressed across the load. Turning on T_1 (T_2) reverse-biases T_3 (T_4), hence T_3 (T_4) turns off and the load voltage jumps to v_1. It is possible to vary the rms load voltage between v_2 and v_1. It is important that T_1 (T_2) and T_4 (T_3) do not conduct simultaneously, since such conduction short-circuits the transformer secondary.
With an inductive load circuit, when only T_1 and T_2 conduct, the output current is

$$i_o = \frac{\sqrt{2}V}{Z}\sin(\omega t - \phi) \quad \text{(A)} \tag{12.25}$$

where $Z = \sqrt{R^2 + (\omega L)^2}$ (ohms) $\phi = \tan^{-1}\omega L / R$ (rad)
It is important that T_3 and T_4 are not fired until $\alpha \ge \phi$, when the load current must have reached zero. Otherwise a transformer secondary short circuit occurs through T_1 (T_2) and T_4 (T_3).
For a resistive load, the thyristor rms currents for T_3, T_4 and T_1, T_2 respectively are

$$I_{Trms} = \frac{v_2}{2R}\sqrt{\frac{1}{\pi}(2\alpha - \sin 2\alpha)}$$
$$I_{Trms} = \frac{v_1}{2R}\sqrt{\frac{1}{\pi}(\sin 2\alpha - 2\alpha) + 2\pi} \qquad (12.26)$$

The thyristor voltages ratings are both v_1 - v_2, provided a thyristor is always conducting at any instant.

An extension of the basic operating principle is to use phase control on thyristors T_3 and T_4 as well as T_1 and T_2. It is also possible to use tap-changing in the primary circuit. The basic principle can also be extended from a single tap to a multi-tap transformer.

The basic operating principle of any multi-output tap changer, in order to avoid short circuits, independent of the load power factor is

- switch up in voltage when the load *V* and *I* have the same direction, delivering power
- switch down when *V* and *I* have the opposite direction, returning power.

12.5 Cycloconverter

The simplest cycloconverter is a single-phase ac input to single-phase ac output circuit as shown in figure 12.8a. It synthesises a low-frequency ac output from selected portions of a higher-frequency ac voltage source and consists of two converters connected back-to-back. Thyristors T_1 and T_2 form the positive converter group P, while T_3 and T_4 form the negative converter group N.

Figure 12.8b shows how an output frequency of one-fifth of the input supply frequency is generated. The P group conducts for five half-cycles (with T_1 and T_2 alternately conducting), then the N group conducts for five half-cycles (with T_3 and T_4 alternately conducting). The result is an output voltage waveform with a fundamental of one-fifth the supply with continuous load and supply current.

The harmonics in the load waveform can be reduced and rms voltage controlled by using phase control as shown in figure 12.8c. The phase control delay angle is greater towards the group changeover portions of the output waveform. The supply current is now distorted and contains a subharmonic at the cycloconverter output frequency, which for figure 12.8c is at one-fifth the supply frequency.

With inductive loads, one blocking group cannot be turned on until the load current through the other group has fallen to zero, otherwise the supply will be short-circuited. An intergroup reactor, L, as shown in figure 12.8a can be used to limit any intergroup circulating current, and to maintain a continuous load current.

A single-phase ac load fed from a three-phase ac supply, and three-phase ac load cycloconverters can also be realised as shown in figures 12.9a and 12.9b, respectively.

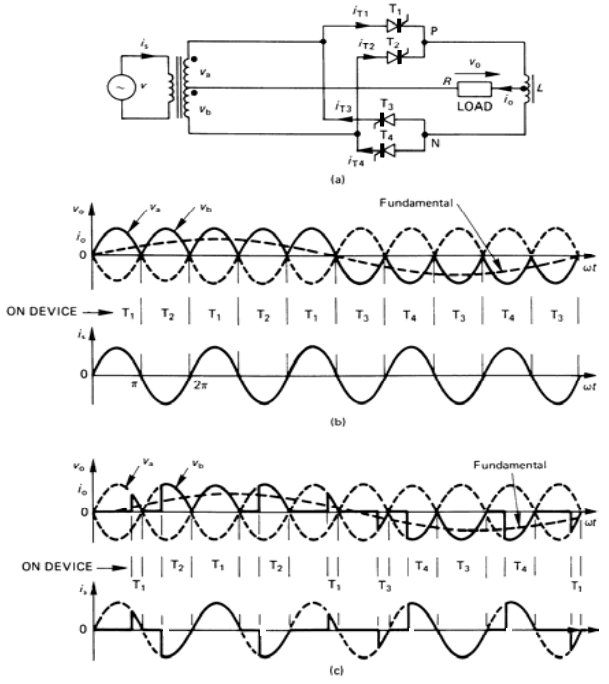

Figure 12.8. *Single-phase cycloconverter ac regulator: (a) circuit connection with a purely resistive load; (b) load voltage and supply current with 180° conduction of each thyristor; and (c) waveforms when phase control is used on each thyristor.*

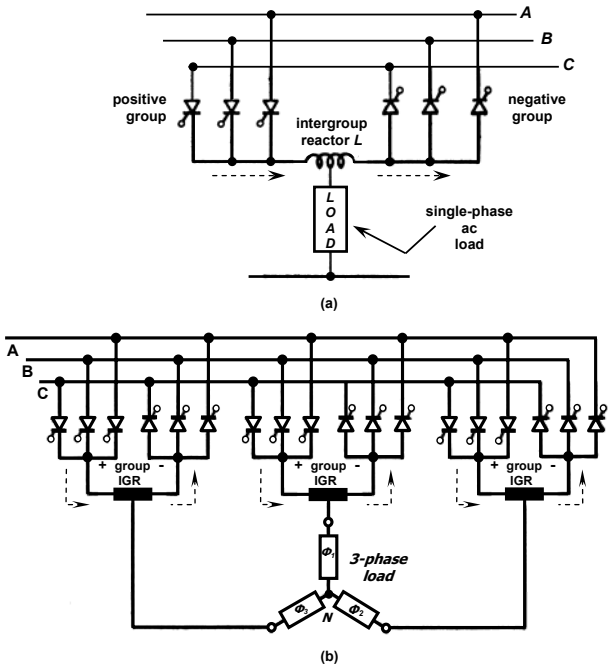

Figure 12.8. C*ycloconverter ac regulator circuits:*
(a) three-phase to single-phase and (b) three–phase supply to three-phase load.

12.6 The matrix converter

Commutation of the cycloconverter switches is restricted to natural commutation instances dictated by the supply voltages. This usually results in the output frequency being significantly less than the supply frequency if reasonable low harmonic output is required. In the matrix converter in figure 12.9b, the thyristors in figure 12.8b are replaced with fully controlled, bidirectional switches, like that shown in figure 12.9a.

Rather than eighteen switches and eighteen diodes, nine switches and thirty-six diodes can be used if a unidirectional voltage and current switch in a full-bridge configuration is used as shown in figure 6.11. These switch configurations allow converter current commutation as and when desired, provide certain condition are fulfilled. These switches allow any one input supply ac voltage and current to be directed to any one or more output lines. At any instant only one of the three input voltages can be connected to a given output. This flexibility implies a higher quality output voltage can be attained, with enough degrees of freedom to ensure the input currents are sinusoidal and with unity (or adjustable) power factor. The input *L-C* filter prevents matrix modulation frequency components from being injected into the input three-phase ac supply system.

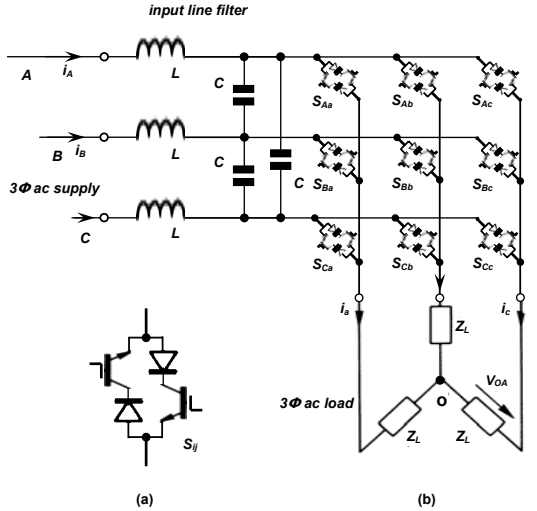

Figure 12.9. Three-phase input to three-phase output matrix *converter circuit:*
(a) bidirectional switch and (b) three–phase ac supply to three-phase ac load.

The relationship between the output voltages (v_a, v_b, v_c) and the input voltages (v_A, v_B, v_C) is determined by the states of the nine bidirectional switches (S_{ij}), according to

$$\begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} = \begin{pmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{pmatrix} \begin{pmatrix} v_A \\ v_B \\ v_C \end{pmatrix} \quad \text{(A)} \qquad (12.27)$$

With the balanced star load shown in figure 12.1c, the load neutral voltage v_o is given by

$$v_o = \tfrac{1}{3}\left(v_a + v_b + v_c\right) \qquad (12.28)$$

The line-to-neutral and line-to-line voltages are the same as those applicable to svm, namely

$$\begin{pmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{pmatrix} = \frac{1}{6}\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix} \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \quad \text{(V)} \qquad (12.29)$$

from which

$$\begin{pmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{pmatrix} = \tfrac{1}{2}\begin{pmatrix} 1 & -1 & -1 \\ 0 & 1 & 0 \\ -1 & 0 & 1 \end{pmatrix} \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \quad \text{(V)} \qquad (12.30)$$

Similarly the relationship between the input line currents (i_A, i_B, i_C) and the output currents (i_a, i_b, i_c) is determined by the states of the nine bidirectional switches (S_{ij}), according to

$$\begin{pmatrix} i_A \\ i_B \\ i_C \end{pmatrix} = \begin{pmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{pmatrix} \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} \quad \text{(A)} \qquad (12.31)$$

where the switches S_{ij} are constrained such that no two or three switches short the input lines or would cause discontinuous output current. Discontinuous output current cannot occur since no natural current freewheel paths exist. The input short circuit constraint is complied with by ensuring that only one switch in each column of the matrix in equation (12.31) is on at any time. Thus not all the 512 (2^9) states can be used, and only 27 states of the switch matrix can be utilised.

The maximum voltage gain, the ratio of the peak fundamental ac output voltage to the peak ac input voltage is $\frac{1}{2}\sqrt{3} = 0.866$. Above this level, called over-modulation, distortion of the input current occurs. Since the switches are bidirectional and fully controlled, power flow can be bidirectional. Control involves the use of a modulation index that varies sinusoidally. Since no intermediate energy storage stage is involved, such as a dc link, this total silicon solution to ac to ac conversion provides no ride-through, thus is not well suited to ups application.

12.7 Load efficiency and supply current power factor

One characteristic of ac regulators is non-sinusoidal load, hence supply current as illustrated in figure 12.lb. Difficulty therefore exists in defining the supply current power factor and the harmonics in the load current may detract from the load efficiency. For example, with a single-phase motor, current components other than the fundamental detract from the fundamental torque and increase motor heating, noise, and vibration. To illustrate the procedure for determining load efficiency and supply power factor, consider the circuit and waveforms in figure 12.1.

12.7.1 Load waveforms

The load voltage waveform is constituted from the sinusoidal supply voltage v and is defined by

$$v_o(\omega t) = \sqrt{2}V \sin \omega t \quad \text{(V)} \qquad \alpha \le \omega t \le \beta \qquad \pi + \alpha \le \omega t \le \pi + \beta \qquad (12.32)$$

and $v_o = 0$ elsewhere.

Fourier analysis of v_o yields the load voltage Fourier coefficients v_{an} and v_{bn} such that

$$v_o(\omega t) = \sum \{ v_{an} \cos n\omega t + v_{bn} \sin n\omega t \} \quad \text{(V)} \qquad (12.33)$$

for all values of n.

The load current can be evaluated by solving

$$Ri_o + L\frac{di_o}{dt} = \sqrt{2}\ V \sin \omega t \quad \text{(V)} \qquad (12.34)$$

over the appropriate bounds and initial conditions. From Fourier analysis of the load current i_o, the load current coefficients i_{an} and i_{bn} can be derived.

Derivation of the current waveform Fourier coefficients may prove complicated because of the difficulty of integrating an expression involving equation (12.2), the load current. An alternative and possibly simpler approach is to use the fact that each load Fourier voltage component produces a load current component at the associated frequency but displaced because of the load impedance at that frequency. That is

$$i_{an} = \tfrac{v_{an}}{R}\cos\phi_n \quad \text{(A)} \qquad i_{bn} = \tfrac{v_{bn}}{R}\cos\phi_n \quad \text{(A)} \qquad (12.35)$$

where $\phi_n = \tan^{-1} n\omega L / R$

The load current i_o is given by

$$i_o(\omega t) = \sum_{\forall n} \left\{ i_{an} \cos\left(n\omega t - \phi_n\right) + i_{bn} \sin\left(n\omega t - \phi_n\right) \right\} \quad \text{(A)} \qquad (12.36)$$

The load efficiency, η, which is related to the power dissipated in the resistive component R of the load, is defined by

$$\eta = \frac{\text{fundamental active power}}{\text{total active power}} = \frac{\tfrac{1}{2}\left(i_{a1}^2 R + i_{b1}^2 R\right)}{\tfrac{1}{2}\sum_{\forall n}\left(i_{an}^2 R + i_{bn}^2 R\right)} = \frac{i_{a1}^2 + i_{b1}^2}{\sum_{\forall n}\left(i_{an}^2 + i_{bn}^2\right)} \tag{12.37}$$

In general, the total load power is $\sum_{\forall n} v_{n\,rms} \times i_{n\,rms} \times \cos\phi_n$.

12.7.2 Supply waveforms

i. The supply distortion factor μ, displacement factor $\cos\psi$, and power factor λ give an indication of the adverse effects that a non-sinusoidal load current has on the supply as a result of thyristor phase control.
In the circuit of figure 12.la, the load and supply currents are the same and are given by equation (12.2). The supply current Fourier coefficients i_{san} and i_{sbn} are the same as for the load current Fourier coefficients i_{sa} and i_{sb} respectively, as previously defined.
The total supply power factor λ can be defined as

$$\lambda = \frac{\text{real power}}{\text{apparent power}} = \frac{\text{total mean input power}}{\text{total rms input VA}} = \frac{v_{1rms} i_{1rms} \cos\psi_1}{V_{rms} I_{rms}} = \frac{\frac{1}{\sqrt{2}}\sqrt{v_{sa1}^2 + v_{sb1}^2} \times \frac{1}{\sqrt{2}}\sqrt{i_{sa1}^2 + i_{sb1}^2} \times \cos\psi_1}{v \times \frac{1}{\sqrt{2}}\sqrt{i_{a1}^2 + i_{b1}^2}} \tag{12.38}$$

The supply voltage is sinusoidal hence supply power is not associated with the harmonic non-fundamental currents.

$$\lambda = \frac{v\sqrt{\tfrac{1}{2}\left(i_{sa1}^2 + i_{sb1}^2\right)}\ \cos\psi_1}{v\, i_{rms}} = \frac{\sqrt{\tfrac{1}{2}\left(i_{sa1}^2 + i_{sb1}^2\right)}\ \cos\psi_1}{i_{rms}} \tag{12.39}$$

where cos ψ, termed the displacement factor, is the fundamental power factor defined as

$$\cos\psi_1 = \cos\left(-\tan^{-1}\frac{i_{sa1}}{i_{sb1}}\right) \tag{12.40}$$

Equating with equation (12.39), the total supply power factor is defined as

$$\lambda = \mu \cos\psi_1 \tag{12.41}$$

The supply current distortion factor μ is the ratio of fundamental rms current to total rms current i_{srms}, that is

$$\mu = \frac{\sqrt{\tfrac{1}{2}\left(i_{sa1}^2 + i_{sb1}^2\right)}}{i_{rms}} \tag{12.42}$$

ii. The supply harmonic factor ρ is defined as

$$\rho = \frac{\text{total harmonic rms current (or voltage)}}{\text{fundamental rms current (or voltage)}} = \frac{I_h}{I_{1rms}} = \frac{I_h}{\sqrt{i_{sa1}^2 + i_{sb1}^2}} = \sqrt{\frac{i_{srms}^2}{i_{sa1}^2 + i_{sb1}^2} - 1} \tag{12.43}$$

where I_h is the total harmonic current,

$$I_h = \sqrt{I_{rms}^2 - I_{1rms}^2} = \sqrt{\sum_{n=2}^{\infty} I_{nrms}^2} = \frac{1}{\sqrt{2}}\sqrt{\sum_{n=2}^{\infty} i_{san}^2 + i_{sbn}^2} \tag{12.44}$$

iii. The supply crest factor δ is defined as the ratio of peak supply current $\hat{i}_s$ to the total rms current, that is

$$\delta = \hat{i}_s / I_{rms} \tag{12.45}$$

iv. The energy conversion factor υ is defined by

$$\upsilon = \frac{\text{fundamental output power}}{\text{fundamental input power}} = \frac{\frac{1}{\sqrt{2}}\sqrt{v_{a1}^2 + v_{b1}^2} \times \frac{1}{\sqrt{2}}\sqrt{i_{a1}^2 + i_{b1}^2} \times \cos\phi_1}{v \times \frac{1}{\sqrt{2}}\sqrt{i_{sa1}^2 + i_{sb1}^2} \times \cos\psi_1} \tag{12.46}$$

Example 12.4: ***Load efficiency***

If a purely resistive load R is fed with a voltage

$$v_o = \sqrt{2}\,V \sin\omega t + \frac{\sqrt{2}\,V}{3}\sin 3\omega t$$

what is the fundamental load efficiency?

Solution
The load current is given by

$$i_o = \frac{v_o}{R} = \frac{\sqrt{2}\,V}{R}\left(\sin\omega t + \frac{1}{3}\sin 3\omega t\right)$$

The load efficiency is given by equation (12.37), that is

$$\eta = \frac{\left(\frac{\sqrt{2}V}{R}\right)^2 R}{\left(\frac{\sqrt{2}V}{R}\right)^2 R + \left(\frac{\sqrt{2}V}{3R}\right)^2 R}$$

$$= \frac{1}{1 + 1/9} = 0.9$$

The introduced third harmonic component decreases the load efficiency by 10%.

♣

Reading list

Bird, B. M., et al., *An Introduction to Power Electronics*, John Wiley and Sons, 1993.

Dewan, S. B. and Straughen, A., *Power Semiconductor Circuits*, John Wiley and Sons, New York, 1975.

General Electric Company, *SCR Manual*, 6th Edition, 1979.

Shepherd, W., *Thyristor Control of AC Circuits*, Granada, 1975.

Problems

12.1. Determine the rms load current for the ac regulator in figure 12.3, with a resistive load R. Consider the delay angle intervals 0 to ½π, ½π to ⅔π and ⅔π to 7π /6.

12.2. The ac regulator in figure 12.3, with a resistive load R has one thyristor replaced by a diode. Show that the rms output voltage is

$$V_{rms} = \left[\frac{1}{2\pi}\left(2\pi - \alpha + \tfrac{1}{2}\sin 2\alpha\right)\right]^{\frac{1}{2}}$$

while the average output voltage is

$$\overline{V}_o = \frac{\sqrt{2}V}{2\pi}\left(\cos\alpha - 1\right)$$

12.3. Plot the load power for a resistive load for the fully controlled and half-controlled three-phase ac regulator, for varying phase delay angle, α. Normalise power with respect to $\hat{V}^2 / R$.

12.4. For the tap changer in figure 12.7, with a resistive load, calculate the rms output voltage for a phase delay angle α. If v_2 = 200 V ac and v_1 = 240 V ac, calculate the power delivered to a 10 ohm resistive load at delay angles of ¼π, ½π, and ¾π. What is the maximum power that can be delivered to the load?

12.5. A. 0.01 H inductance is added in series with the load in problem 12.4. Determine the load voltage and current waveforms at a firing delay angle of ½π. Assuming a 50 Hz supply, what is the minimum delay angle?

12.6. The thyristor T_2 in the single phase controller in figure 12.la is replaced by a diode. The supply is 240 V ac, 50 Hz and the load is 10 Ω resistive. For a delay angle of α = 90°, determine the

i. rms output voltage
ii. supply power factor
iii. mean output voltage
iv. mean input current.

[207.84 V; 0.866 lagging; 54 V; 5.4 A]

12.7. The single phase ac controller in figure 12.6 operating on the 240 V, 50 Hz mains is used to control a 10 Ω resistive heating load. If the load is supplied repeatedly for 75 cycles and disconnected for 25 cycles, determine the

i. rms load voltage,
ii. input power factor, λ, and
iii. the rms thyristor current.

12.8. The ac controller in problem 12.7 delivers 2.88 kW. Determine the duty cycle, n/N, and the input power factor, λ.

13

DC Choppers

A *dc chopper* is a dc-to-dc voltage converter. It is a static switching electrical appliance that in one conversion, changes an input fixed dc voltage to an adjustable dc output voltage with inductive intermediate energy storage. The name chopper is connected with the fact that the output voltage is a 'chopped up' quasi-rectangular version of the input dc voltage.

In chapters 11 and 12, thyristor devices were used in conjunction with an ac supply that causes thyristor turn-off at ac supply current reversal. This form of thyristor natural commutation, which is illustrated in figure 13.la, is termed line or source commutation.

When a dc source is used with a thyristor circuit, source facilitated commutation is clearly not possible. If the load is an *R-C* or *L-C* circuit as illustrated in figure 13.lb, the load current falls to zero and the thyristor in series with the dc supply turns off. Such a natural turn-off process is termed load commutation.

If the supply is dc and the load current has no natural zero current periods, such as with the *R-L* load, dc chopper circuit shown in figure 13.1c, the load current can only be commutated using a self-commutating switch, such as a GTO thyristor, CGT, IGBT or MOSFET. An SCR is not suitable since once the device is latched on in this dc supply application, it remains on.

The dc chopper in figure 13.1c is the simplest of the five dc choppers to be considered in this chapter. This dc chopper will be extensively analysed.

13.1 DC chopper variations

There are five types of dc choppers, of which four are a subset of the fifth that is a flexible but basic, four-quadrant H-bridge chopper shown in the centre of figure 13.2. Notice that the circuits in figure 13.2 are highlighted so that the derivation of each dc chopper from the fundamental H-bridge four-quadrant, dc chopper can be seen. Each chopper can be categorized depending on which output I_o-V_o quadrant or quadrants it can operate in, as shown in figure 13.2. The five different choppers in figure 13.2 are classified according to their output I_o-V_o capabilities as follows:

(a)	First quadrant -	I	$+V_o$ $+I_o$
(b)	Second quadrant -	II	$+V_o$ $-I_o$
(c)	Two quadrant -	I and II	$+V_o$ $\pm I_o$
(d)	Two quadrant -	I and IV	$\pm V_o$ $+I_o$
(e)	Four quadrant -	I, II, III, and IV	$\pm V_o$ $\pm I_o$

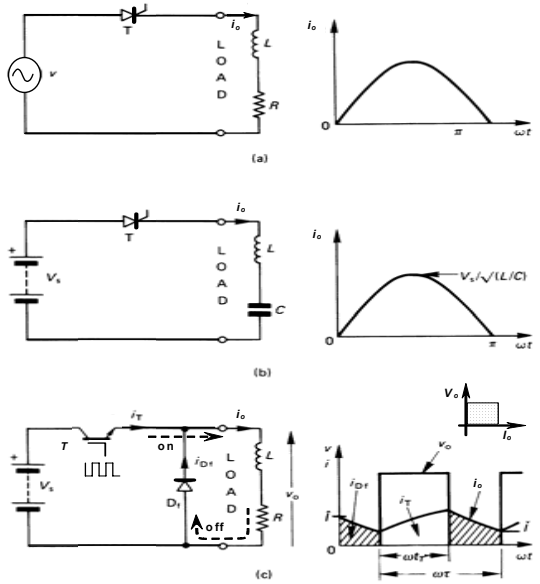

Figure 13.1. *Three basic types of switch commutation techniques: (a) source commutation; (b) load commutation; and (c) switch commutation.*

In the five choppers in the parts a to e of figure 31.2, the subscript of the active switch or switches specify in which quadrants operation is possible. For example, the chopper in figure 13.2d uses switches T_1 and T_3, so can only operate in the first ($+I_o$,$+V_o$) and third ($-I_o$,$-V_o$) quadrants.

The **first-quadrant chopper** in figure 13.2a (and figure 13.1c) can only produce a positive voltage across the load since the freewheel diode D_2 prevents a negative output voltage. Also, the chopper can only deliver current from the dc source to the load through the unidirectional switch T_1. It is therefore a single quadrant chopper and only operates in the first quadrant ($+I_o$,$+V_o$).

The **second-quadrant chopper,** ($-I_o$,$+V_o$), in figure 13.2b is a voltage boost circuit and current flows from the load to the supply, V_s. The switch T_2 is turned on to build-up the inductive load current. Then when the switch is turned off current is forced to flow through diode D_1 into the dc supply. The two current paths are shown in figure 13.1c.

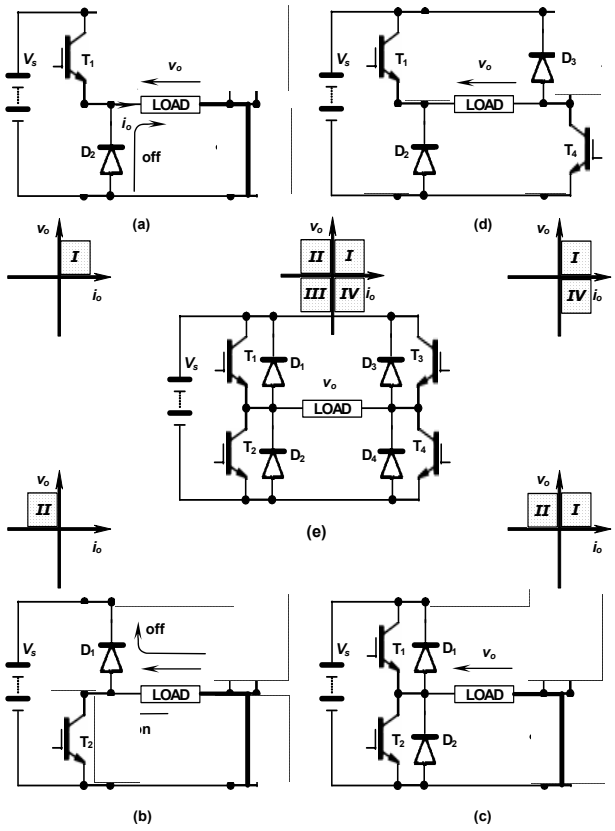

Figure 13.2. *Fundamental four-quadrant chopper (centre) showing derivation of four subclass dc choppers: (a) first-quadrant chopper - I; (b) second-quadrant chopper - II; (c) first and second quadrants chopper – I and II; (d) first and fourth quadrants chopper – I and IV; and (e) four-quadrant chopper.*

The two-quadrant chopper, **quadrants I and IV chopper,** ($+I_o, \pm V_o$), figure 13.2d, can produce a positive voltage, negative voltage or zero volts across the load, depending on the duty cycle of the switches and the switching sequence. When both switches are switched simultaneously, an on-state duty cycle of less than 50% ($\delta < ½$) results in a negative load voltage, while $\delta > ½$ produces a positive load voltage. Since V_o is reversible, the power flow direction is reversible. Zero voltage loops can be created by only turning off one of the two switches.

In the two-quadrant chopper, **quadrants I and II chopper,** ($\pm I_o, +V_o$), figure 13.2c, the load voltage is clamped to between 0V and V_s, because of the freewheel diodes D_1 and D_2. Because this chopper is a combination of the first-quadrant chopper in figure 13.2a and the second-quadrant chopper in figure 13.2b, it combines the characteristics of both. Bidirectional load current is possible but the average output voltage is always positive. Energy can be regenerated into the supply V_s due to the inductive stored energy which maintains current flow from the back emf source.

The **four-quadrant chopper** in the centre of figure 13.2 combines all the properties of the four subclass choppers. Its uses four switched and is capable of producing positive or negative voltages across the load, whilst delivering current to the load in either direction, ($\pm I_o, \pm V_o$).

The step-up chopper, or boost converter, considered in Chapter 15.4, may be considered a dc chopper variation, which has first quadrant characteristics.

13.2 First-Quadrant dc chopper

The basic circuit reproduced in figure 13.3a can be used to control a dc load such as a dc motor. As such, the dc load has a back-emf component, $E = k\phi\omega$, the polarity and magnitude of which are dependant on the flux ϕ, (field current i_f) and its direction, and the speed ω and its direction. If the *R-L* load (with time constant $\tau = L/R$) incorporates an opposing back emf, *E*, then when the switch is off and the diode D_2 is conducting, the load current can be forced to zero by the opposing back emf. Therefore two output load current modes can occur depending on the relative magnitude of the back emf, load time constant, and the switch on-state duty cycle. Continuous load current waveforms are shown in figure 13.3b, while waveforms for discontinuous load current, with period of zero current, are shown in figure 13.3c.

In both conduction cases, the average voltage across the load can be controlled by varying the on-to-off time duty cycle of the switch, T_1. The on-state duty cycle, δ, is normally controlled by using pulse-width modulation, frequency modulation, or a combination of both. When the switch is turned off the inductive load current continues and flows through the load freewheel diode, D_2, shown in figure 13.2a

The analysis to follow assumes

- No source impedance
- Constant switch duty cycle
- Steady state conditions have been reached
- Ideal semiconductors and
- No load impedance temperature effects.

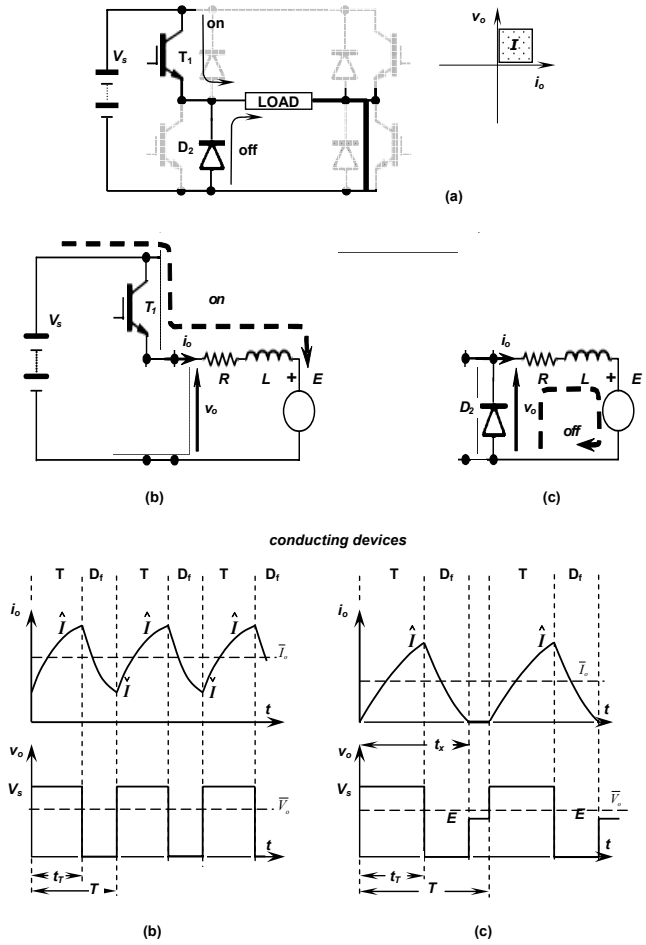

Figure 13.3. *First-quadrant dc chopper and two basic modes of chopper output current operation: (a) basic circuit and current paths; (b) continuous load current; and (c) discontinuous load current after t = t_x.*

13.2.1 Continuous load current

Load waveforms for continuous load current conduction are shown in figure 13.3b. The output voltage v_o, or load voltage is defined by

$$v_o(t) = \begin{cases} V_s & \text{for } 0 \le t \le t_T \\ 0 & \text{for } t_T \le t \le T \end{cases} \tag{13.1}$$

The mean load voltage is

$$\begin{aligned} \bar{V}_o &= \frac{1}{T}\int_0^{t_T} v_o(t)\,dt = \frac{1}{T}\int_0^{t_T} V_s\,dt \\ &= \frac{t_T}{T}V_s = \delta V_s \end{aligned} \tag{13.2}$$

where the switch on-state duty cycle $\delta = t_T/T$ is defined in figure 13.3b.
The rms load voltage is

$$\begin{aligned} V_{rms} &= \left[\frac{1}{T}\int_0^{t_T} v_o^2(t)\,dt\right]^{1/2} = \left[\frac{1}{T}\int_0^{t_T} V_s^2\,dt\right]^{1/2} \\ &= \sqrt{\frac{t_T}{T}}\,V_s = \sqrt{\delta}\,V_s \end{aligned} \tag{13.3}$$

The output ac ripple voltage is

$$\begin{aligned} V_r &= \sqrt{V_{rms}^2 - V_o^2} \\ &= \sqrt{\left(\sqrt{\delta}\,V_s\right)^2 - \left(\delta V_s\right)^2} = V_s\sqrt{\delta(1-\delta)} \end{aligned} \tag{13.4}$$

The maximum rms ripple voltage in the output occurs when δ=½ giving an rms ripple voltage of ½V_s.
The output voltage ripple factor is

$$\begin{aligned} RF &= \frac{V_r}{\bar{V}_o} = \sqrt{\left(\frac{V_{rms}}{\bar{V}_o}\right)^2 - 1} \\ &= \sqrt{\left(\frac{\sqrt{\delta}\,V_s}{\delta V_s}\right)^2 - 1} = \sqrt{\frac{1}{\delta} - 1} \end{aligned} \tag{13.5}$$

Thus as the duty cycle $\delta \to 1$, the ripple factor tends to zero, consistent with the output being dc, that is $V_r = 0$.

Steady-state time domain analysis of first-quadrant chopper
- with load back emf and continuous output current

The time domain load current can be derived in a number of ways.

- First, from the Fourier coefficients of the output voltage, the current can be found by dividing by the load impedance at each harmonic frequency.
- Alternatively, the various circuit currents can be found from the time domain load current equations.

i. Fourier coefficients: The Fourier coefficients of the load voltage are independent of the circuit and load parameters and are given by

$$a_n = \frac{V_s}{n\pi}\sin 2\pi n\delta$$
$$b_n = \frac{V_s}{n\pi}\left(1-\cos 2\pi n\delta\right) \qquad (13.6)$$

Thus the peak magnitude and phase of the n^{th} harmonic are given by

$$c_n = \sqrt{a_n^2 + b_n^2}$$
$$\phi_n = \tan^{-1} a_n \big/ b_n$$

Substituting expressions from equation (13.6) yields

$$c_n = \frac{2V_s}{n\pi}\sin \pi n\delta$$
$$\phi_n = \tan^{-1}\frac{\sin 2\pi n\delta}{1-\cos 2\pi n\delta} = ½\pi - \pi n\delta \qquad (13.7)$$

where

$$v_n = c_n \sin\left(n\,\omega t + \phi_n\right) \qquad (13.8)$$

such that

$$v_o(t) = V_o + \sum_{n=1}^{\infty} c_n \sin\left(n\,\omega t + \phi_n\right) \qquad (13.9)$$

The load current is given by

$$i_o(t) = \sum_{n=0}^{\infty} i_n = \frac{\overline{V}_o}{R} + \sum_{n=1}^{\infty}\frac{v_n}{Z_{o_n}} = \frac{\overline{V}_o}{R} + \sum_{n=1}^{\infty}\frac{c_n \sin\left(n\,\omega t - \phi_n\right)}{Z_{o_n}} \qquad (13.10)$$

where the load impedance at each frequency is given by

$$Z_{o_n} = \sqrt{R^2 + \left(n\,\omega L\right)^2}$$

ii. Time domain differential equations: By solving the appropriate time domain differential equations, the continuous load current shown in figure 13.3b is defined by

During the **switch on-period**, when $v_o(t)=V_s$

$$L\frac{di_o}{dt} + R\,i_o + E = V_s$$

which yields

$$i_o(t) = \frac{V_s - E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \check{I}\,e^{\frac{-t}{\tau}} \qquad \text{for} \quad 0 \le t \le t_T \qquad (13.11)$$

During the **switch off-period**, when $v_o(t)= 0$

$$L\frac{di_o}{dt} + R\,i_o + E = 0$$

which, after shifting the zero time reference to t_T, in figure 13.3a, gives

$$i_o(t) = -\frac{E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}\,e^{\frac{-t}{\tau}} \qquad \text{for} \quad 0 \le t \le T - t_T \qquad (13.12)$$

where $\hat{I} = \frac{V_s}{R}\frac{1-e^{\frac{-t_T}{\tau}}}{1-e^{\frac{-T}{\tau}}} - \frac{E}{R}$ (A)

and $\check{I} = \frac{V_s}{R}\frac{e^{\frac{t_T}{\tau}}-1}{e^{\frac{T}{\tau}}-1} - \frac{E}{R}$ (A) (13.13)

The output ripple current, for continuous conduction, is independent of the back emf E and is given by

$$I_{p-p} = \Delta i_o = \hat{I} - \check{I} = \frac{V_s}{R}\,\frac{(1-e^{\frac{-t_T}{\tau}})(1-e^{\frac{-T+t_T}{\tau}})}{1-e^{\frac{-T}{\tau}}} \qquad (13.14)$$

which in terms of the on-state duty cycle, $\delta=t_T/T$, becomes

$$I_{p-p} = \frac{V_s}{R}\,\frac{(1-e^{\frac{-\delta T}{\tau}})(1-e^{\frac{-(1-\delta)T}{\tau}})}{1-e^{\frac{-T}{\tau}}} \qquad (13.15)$$

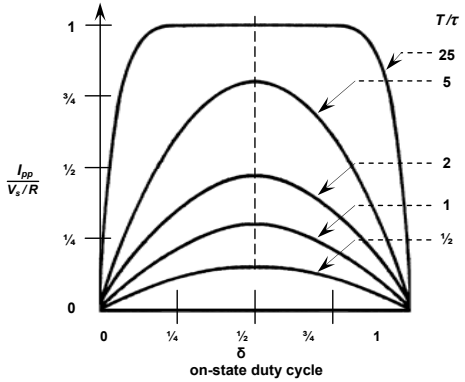

Figure 13.4. *Ripple current as a function of duty cycle δ=t_T/T and ratio of cycle period T (switching frequency, f_s=1/T) to load time constant τ=L/R. Valid only for continuous load current conduction.*

The peak-to-peak ripple current can be extracted from figure 13.4, which is a family of curves for equation (13.15), normalised with respect to V_s/R. For a given load time constant $\tau=L/R$, switching frequency $f_s=1/T$, and switch on-state duty cycle δ, the ripple current can be extracted. This figure shows a number of important features of the ripple current.

- The ripple current reduces to zero as $\delta\to 0$ and $\delta\to 1$.
- Differentiation of equation (13.15) reveals that the maximum ripple current $\hat{I}_{p-p}$ occurs at $\delta = ½$.

- The longer the load L/R time constant, τ, the lower the output ripple current $I_{p\text{-}p}$.
- The higher the switching frequency, $1/T$, the lower the output ripple.

If the switch conducts continuously (δ=1), then substitution of t_T=T into equations (13.11) to (13.13) gives

$$i_o = \hat{I} = \check{I} = \frac{V_s - E}{R} \qquad \text{(A)} \tag{13.16}$$

The mean output current with continuous load current is found by integrating the load current over two periods, the switch conduction given by equation (13.11) and diode conduction given by equation (13.12), which yields

$$\begin{aligned} \bar{I}_o &= \frac{1}{T}\int_0^T i_o(t)\,dt = \left(\bar{V}_o - E\right)\Big/R \\ &= \left(\delta V_s - E\right)\Big/R \qquad \text{(A)} \end{aligned} \tag{13.17}$$

The input and output powers are related such that

$$\begin{aligned} P_{in} &= P_{out} \\ P_{in} &= V_s \bar{I}_i = V_S\left(\frac{\delta(V_s - E)}{R} - \frac{\tau}{T}\left(\hat{I} - \check{I}\right)\right) \\ P_{out} &= \frac{1}{T}\int_0^T v_o(t) i_o(t)\,dt \\ &= I_{o\,rms}^2 R + E\bar{I}_o = I_{o\,rms}^2 R + E\left(\frac{\delta V_s - E}{R}\right) \end{aligned} \tag{13.18}$$

from which the average input current can be evaluated.

Alternatively, the average input current, which is the average switch current, $\bar{I}_{switch}$, can be derived by integrating the switch current which is given by equation (13.11) that is

$$\begin{aligned} \bar{I}_i &= \bar{I}_{switch} = \frac{1}{T}\int_0^{t_T} i_o(t)\,dt \\ &= \frac{1}{T}\int_0^{t_T}\left(\frac{V_s - E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \check{I}\,e^{\frac{-t}{\tau}}\right)dt \\ &= \frac{\delta(V_s - E)}{R} - \frac{\tau}{T}\left(\hat{I} - \check{I}\right) \end{aligned} \tag{13.19}$$

The term $\hat{I} - \check{I} = I_{p\text{-}p}$ is the peak-to-peak ripple current, which is given by equation (13.15). By Kirchhoff's current law, the average diode current $\bar{I}_{diode}$ is the difference between the average output current $\bar{I}_o$ and the average input current, $\bar{I}_i$, that is

$$\begin{aligned} \bar{I}_{diode} &= \bar{I}_o - \bar{I}_i \\ &= \left(\delta V_s - E\right)\Big/R - \frac{\delta(V_s - E)}{R} + \frac{\tau}{T}\left(\hat{I} - \check{I}\right) \\ &= \frac{\tau}{T}\left(\hat{I} - \check{I}\right) - \frac{E(1-\delta)}{R} \end{aligned} \tag{13.20}$$

Alternatively, the average diode current can be found by integrating the diode current given in equation (13.12), as follows

$$\begin{aligned} \bar{I}_{diode} &= \frac{1}{T}\int_0^{T-t_T}\left(-\frac{E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}\,e^{\frac{-t}{\tau}}\right)dt \\ &= \frac{\tau}{T}\left(\hat{I} - \check{I}\right) - \frac{E(1-\delta)}{R} \end{aligned} \tag{13.21}$$

If E represents motor back emf, then the electromagnetic energy conversion efficiency is given by

$$\eta = \frac{E\bar{I}_o}{P_{in}} = \frac{E\bar{I}_o}{V_s \bar{I}_i} \tag{13.22}$$

The chopper effective input impedance at the dc source is given by

$$Z_{in} = \frac{V_s}{\bar{I}_i} \tag{13.23}$$

For an R-L load without a back emf, set E = 0 in the foregoing equations. The discontinuous load current analysis to follow is not valid for an R-L, with E=0 load, since the load current never reaches zero, but at best asymptotes towards zero.

13.2.2 Discontinuous load current

With an opposing emf E in the load, the load current can reach zero during the off-time, at a time t_x shown in figure 13.3c. The time t_x can be found by

- deriving an expression for $\hat{I}$ from equation (13.11), setting t=t_T,
- this equation is substituted into equation (13.12) which is equated to zero, having substituted for t=t_x.

yielding

$$t_x = t_T + \tau \ln\left(1 + \frac{V_s - E}{E}\left(1 - e^{\frac{-t_T}{\tau}}\right)\right) \qquad \text{(s)} \tag{13.24}$$

This equation shows that $t_x > t_T$. Figure 13.5 can be used to determine if a particular set of operating conditions involves discontinuous load current.

The load voltage waveform for discontinuous load current conduction shown in figure 13.3c is defined by

$$v_o(t) = \begin{Bmatrix} V_s & \text{for } 0 \le t \le t_T \\ 0 & \text{for } t_T \le t \le t_x \\ E & \text{for } t_x \le t \le T \end{Bmatrix} \tag{13.25}$$

If discontinuous load current exists for a period T - t_x, from t_x until T, then the mean output voltage is

$$\begin{aligned} \bar{V}_o &= \frac{1}{T}\left(\int_0^{t_T} V_s\,dt + \int_{t_T}^{t_x} 0\,dt + \int_{t_x}^{T} E\,dt\right) \\ \bar{V}_o &= \delta V_s + \frac{T - t_x}{T}E \qquad \text{(V)} \quad \text{for } t_x \ge t_T \end{aligned} \tag{13.26}$$

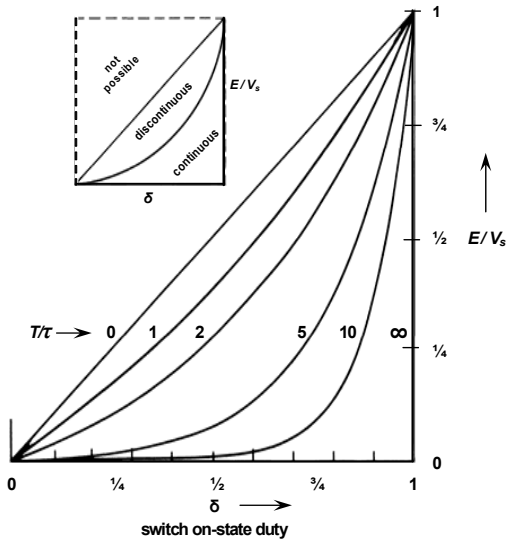

Figure 13.5. *Bounds of discontinuous load current with E>0.*

The rms output voltage with discontinuous load current conduction is given by

$$V_{rms} = \left[\frac{1}{T}\left(\int_0^{t_T} V_s^2 dt + \int_{t_T}^{t_x} 0^2 d + \int_{t_x}^{T} E^2 dt\right)\right]^{1/2} = \sqrt{\delta V_s^2 + \frac{T - t_x}{T} E^2} \quad \text{(V)} \tag{13.27}$$

The ac ripple current and ripple factor can be found by substituting equations (13.26) and (13.27) into

$$V_r = \sqrt{V_{rms}^2 - V_o^2} \tag{13.28}$$

and

$$RF = \frac{V_r}{\overline{V}_o} = \sqrt{\left(\frac{V_{rms}}{\overline{V}_o}\right)^2 - 1} \tag{13.29}$$

Steady-state time domain analysis of first-quadrant chopper
- with load back emf and discontinuous output current

i. Fourier coefficients: The load current can be derived indirectly by using the output voltage Fourier series. The Fourier coefficients of the load voltage are

$$a_n = \frac{V_s}{n\pi}\sin 2\pi n\delta - \frac{E}{n\pi}\sin 2\pi n\, t_x/T$$
$$b_n = \frac{V_s}{n\pi}\left(1-\cos 2\pi n\delta\right) - \frac{E}{n\pi}\left(1-\cos 2\pi n\, t_x/T\right) \tag{13.30}$$

which using

$$c_n = \sqrt{a_n^2 + b_n^2}$$
$$\phi_n = \tan^{-1} a_n/b_n$$

give

$$v_o(t) = \overline{V}_o + \sum_{n=1}^{\infty} c_n \sin\left(n\omega t + \phi_n\right) \tag{13.31}$$

The appropriate division by $Z_n = \sqrt{R^2 + (n\omega L)^2}$ yields the output current.

ii. Time domain differential equations: For discontinuous load current, $\breve{I} = 0$. Substituting this condition into the time domain equations (13.11) to (13.14) yields equations for discontinuous load current, specifically:

During the **switch on-period**, when $v_o(t)=V_s$,

$$i_o(t) = \frac{V_s - E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) \qquad \text{for} \quad 0 \le t \le t_T \tag{13.32}$$

During the **switch off-period**, when $v_o(t)=0$, after shifting the zero time reference to t_T,

$$i_o(t) = -\frac{E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}\, e^{\frac{-t}{\tau}} \qquad \text{for} \quad 0 \le t \le t_x - t_T \tag{13.33}$$

where from equation (13.32), with $t=t_T$,

$$\hat{I} = \frac{V_s - E}{R}\left(1 - e^{\frac{-t_T}{\tau}}\right) \quad \text{(A)} \tag{13.34}$$

After t_x, $v_o(t)=E$ and the load current is zero, that is

$$i_o(t) = 0 \qquad \text{for} \quad t_x \le t \le T \tag{13.35}$$

The output ripple current, for discontinuous conduction, is dependent of the back emf E and is given by equation (13.34), that is

$$I_{p-p} = \hat{I} = \frac{V_s - E}{R}\left(1 - e^{\frac{-t_T}{\tau}}\right) \tag{13.36}$$

Since $\breve{I} = 0$, the mean output current for discontinuous conduction, is

$$\overline{I}_o = \frac{1}{T}\int_0^{t_x} i_o(t)\,dt = \frac{1}{T}\left[\int_0^{t_T} \frac{V_s - E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) dt + \int_0^{t_x - t_T} \frac{-E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}\, e^{\frac{-t}{\tau}}\, dt\right]$$
$$= \left(\overline{V}_o - E\right)/R$$

$$\bar{I}_o = \frac{\delta V_s + \left(1 - \frac{t_x}{T}\right)E}{R} - \frac{E}{R} = \left(\delta V_s - \frac{t_x}{T}E\right)\Big/R \qquad \text{(A)} \qquad (13.37)$$

The input and output powers are related such that

$$P_{in} = V_s \bar{I}_i \qquad P_{out} = I_{o\,rms}^2 R + E\bar{I}_o \qquad P_{in} = P_{out} \qquad (13.38)$$

from which the average input current can be evaluated.
Alternatively the average input current, which is the switch average current, is given by

$$\begin{aligned}\bar{I}_i = \bar{I}_{switch} &= \frac{1}{T}\int_0^{t_T} i_o(t)\,dt \\ &= \frac{1}{T}\int_0^{t_T} \frac{V_s - E}{R}\left(1 - e^{\frac{-t}{\tau}}\right)dt \\ &= \frac{V_s - E}{R}\left(\delta - \frac{\tau}{T}\left(1 - e^{\frac{-t_T}{\tau}}\right)\right) = \frac{V_s - E}{R}\delta - \frac{\tau}{T}\hat{I}\end{aligned} \qquad (13.39)$$

The average diode current $\bar{I}_{diode}$ is the difference between the average output current $\bar{I}_o$ and the average input current, $\bar{I}_i$, that is

$$\begin{aligned}\bar{I}_{diode} &= \bar{I}_o - \bar{I}_i \\ &= \frac{\tau}{T}\hat{I} - \frac{E\left(\frac{t_x}{T} - \delta\right)}{R}\end{aligned} \qquad (13.40)$$

Alternatively, the average diode current can be found by integrating the diode current given in equation (13.33), as follows

$$\begin{aligned}\bar{I}_{diode} &= \frac{1}{T}\int_0^{t_x - t_T}\left(-\frac{E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}e^{\frac{-t}{\tau}}\right)dt \\ &= \frac{\tau}{T}\hat{I} - \frac{E\left(\frac{t_x}{T} - \delta\right)}{R}\end{aligned} \qquad (13.41)$$

If E represents motor back emf, then electromagnetic energy conversion efficiency is given by

$$\eta = \frac{E\bar{I}_o}{P_{in}} = \frac{E\bar{I}_o}{V_s\bar{I}_i} \qquad (13.42)$$

The chopper effective input impedance is given by

$$Z_{in} = \frac{V_s}{\bar{I}_i} \qquad (13.43)$$

Example 13.1: ***DC chopper with load back emf (first quadrant)***

A first-quadrant dc-to-dc chopper feeds an inductive load of 10 ohms resistance, 50mH inductance, and back emf of 55V dc, from a 340V dc source. If the chopper is operated at 200Hz with a 25% on-state duty cycle, determine, with and without (rotor standstill) the back emf:

i. the load average and rms voltages;
ii. the rms ripple voltage, hence ripple factor;
iii. the maximum and minimum output current, hence the peak-to-peak output ripple in the current;
iv. the current in the time domain;
v. the average load output current, average switch current, and average diode current;
vi. the input power, hence output power and rms output current;
vii. effective input impedance, (and electromagnetic efficiency for $E > 0$);
viii. sketch the output current and voltage waveforms.

Solution
The main circuit and operating parameters are

- on-state duty cycle δ = ¼
- period $T = 1/f_s$ = 1/200Hz = 5ms
- on-period of the switch t_T = 1.25ms
- load time constant $\tau = L/R$ = 0.05H/10Ω = 5ms

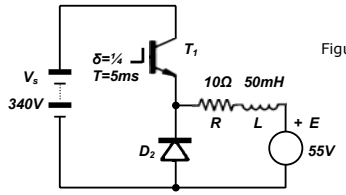

Figure Example 13.1. *Circuit diagram.*

i. From equations (13.2) and (13.3) the average and rms output voltages are both independent of the back emf, namely

$$\begin{aligned}\bar{V}_o &= \frac{t_T}{T}V_s = \delta V_s \\ &= ¼ \times 340\text{V} = 85\text{V} \\ V_r &= \sqrt{\frac{t_T}{T}}V_s = \sqrt{\delta}\,V_s \\ &= \sqrt{¼} \times 240\text{V} = 120\text{V rms}\end{aligned}$$

ii. The rms ripple voltage hence ripple factor are given by equations (13.4) and (13.5), that is

$$\begin{aligned}V_r &= \sqrt{V_{rms}^2 - V_o^2} = V_s\sqrt{\delta(1-\delta)} \\ &= 340\text{V}\sqrt{¼ \times (1 - ¼)} = 147.2\text{V ac}\end{aligned}$$

and

$$RF = \frac{V_r}{V_o} = \sqrt{\frac{1}{\delta} - 1}$$

$$= \sqrt{\frac{1}{¼} - 1} = \sqrt{3} = 1.732$$

No back emf, E = 0

iii. From equation (13.13), with E=0, the maximum and minimum currents are

$$\hat{I} = \frac{V_s}{R}\frac{1 - e^{\frac{-t_T}{\tau}}}{1 - e^{\frac{-T}{\tau}}} = \frac{340\text{V}}{10\Omega} \times \frac{1 - e^{\frac{\text{-1.25ms}}{5\text{ms}}}}{1 - e^{\frac{\text{-5ms}}{5\text{ms}}}} = 11.90\text{A}$$

$$\check{I} = \frac{V_s}{R}\frac{e^{\frac{t_T}{\tau}} - 1}{e^{\frac{T}{\tau}} - 1} = \frac{340\text{V}}{10\Omega} \times \frac{e^{¼} - 1}{e^{1} - 1} = 5.62\text{A}$$

The peak-to-peak ripple in the output current is therefore

$$I_{p-p} = \hat{I} - \check{I}$$

$$= 11.90\text{A} - 5.62\text{A} = 6.28\text{A}$$

Alternatively the ripple can be extracted from figure 13.4 using T/τ =1 and δ = ¼.

iv. From equations (13.11) and (13.12), with E = 0, the time domain load current equations are

$$i_o = \frac{V_s}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \check{I}\, e^{\frac{-t}{\tau}}$$

$$i_o(t) = 34 \times \left(1 - e^{\frac{-t}{5ms}}\right) + 5.62 \times e^{\frac{-t}{5\text{ms}}}$$

$$= 34 - 28.38 \times e^{\frac{-t}{5\text{ms}}} \quad \text{(A)} \qquad \text{for} \quad 0 \le t \le 1.25\text{ms}$$

$$i_o = \hat{I}\, e^{\frac{-t}{\tau}}$$

$$i_o(t) = 11.90 \times e^{\frac{-t}{5\text{ms}}} \quad \text{(A)} \qquad \text{for} \quad 0 \le t \le 3.75\text{ms}$$

v. The average load current from equation (13.17), with E = 0, is

$$\bar{I}_o = \bar{V}_o / R = 85\text{V} / 10\Omega = 8.5\text{A}$$

The average switch current, which is the average supply current, is

$$\bar{I}_i = \bar{I}_{switch} = \frac{\delta(V_s - E)}{R} - \frac{\tau}{T}\left(\hat{I} - \check{I}\right)$$

$$= ¼ \times (340\text{V} - 0) / 10\Omega - \frac{5\text{ms}}{5\text{ms}} \times (11.90\text{A} - 5.62\text{A}) = 2.22\text{A}$$

The average diode current is the difference between the average load current and the average input current, that is

$$\bar{I}_{diode} = \bar{I}_o - \bar{I}_i$$

$$= 8.50\text{A} - 2.22\text{A} = 6.28\text{A}$$

vi. The input power is the dc supply multiplied by the average input current, that is

$$P_{in} = V_s \bar{I}_i = 340\text{V} \times 2.22\text{A} = 754.8\text{W}$$

$$P_{out} = P_{in} = 754.8\text{W}$$

From equation (13.18) the rms load current is given by

$$\bar{I}_{o_{rms}} = \sqrt{\frac{P_{out}}{R}}$$

$$= \sqrt{\frac{754.8\text{W}}{10\Omega}} = 8.7\text{A rms}$$

vii. The chopper effective input impedance is

$$Z_{in} = \frac{V_s}{\bar{I}_i}$$

$$= \frac{340\text{V}}{2.22\text{A}} = 153.2\ \Omega$$

Load back emf, E = 55V

i. and ii. The average output voltage, rms output voltage, ac ripple voltage, and ripple factor are independent of back emf, provided the load current is continuous. The earlier answers for E = 0 are applicable.

iii. From equation (13.13), the maximum and minimum load currents are

$$\hat{I} = \frac{V_s}{R}\frac{1 - e^{\frac{-t_T}{\tau}}}{1 - e^{\frac{-T}{\tau}}} - \frac{E}{R} = \frac{340\text{V}}{10\Omega} \times \frac{1 - e^{\frac{\text{-1.25ms}}{5\text{ms}}}}{1 - e^{\frac{\text{-5ms}}{5\text{ms}}}} - \frac{55\text{V}}{10\Omega} = 6.40\text{A}$$

$$\check{I} = \frac{V_s}{R}\frac{e^{\frac{t_T}{\tau}} - 1}{e^{\frac{T}{\tau}} - 1} - \frac{E}{R} = \frac{340\text{V}}{10\Omega} \times \frac{e^{¼} - 1}{e^{1} - 1} - \frac{55\text{V}}{10\Omega} = 0.12\text{A}$$

The peak-to-peak ripple in the output current is therefore

$$I_{pp} = \hat{I} - \check{I}$$

$$= 6.4\text{A} - 0.12\text{A} = 6.28\text{A}$$

The ripple value is the same as the E = 0 case, which is as expected since ripple current is independent of back emf with continuous output current.
Alternatively the ripple can be extracted from figure 13.4 using T/τ =1 and δ=¼.

iv. The time domain load current is defined by

$$i_o = \frac{V_s - E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \check{I}\, e^{\frac{-t}{\tau}}$$

$$i_o(t) = 28.5 \times \left(1 - e^{\frac{-t}{5ms}}\right) + 0.12 e^{\frac{-t}{5ms}}$$

$$= 28.5 - 28.38 e^{\frac{-t}{5ms}} \quad \text{(A)} \qquad \text{for} \quad 0 \le t \le 1.25\text{ms}$$

$$i_o = -\frac{E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}\, e^{\frac{-t}{\tau}}$$

$$i_o(t) = -5.5 \times \left(1 - e^{\frac{-t}{5ms}}\right) + 6.4 e^{\frac{-t}{5ms}}$$

$$= -5.5 + 11.9 e^{\frac{-t}{5ms}} \quad \text{(A)} \qquad \text{for} \quad 0 \le t \le 3.75\text{ms}$$

v. The average load current from equation (13.37) is

$$\bar{I}_o = {}^{V_o - E}\!/_{R}$$

$$= 85\text{V-}55\text{V}/10\Omega = 3\text{A}$$

The average switch current is the average supply current,

$$\bar{I}_i = \bar{I}_{switch} = \frac{\delta(V_s - E)}{R} - \frac{\tau}{T}\left(\hat{I} - \check{I}\right)$$

$$= \tfrac{1}{4} \times \frac{(340\text{V} - 55\text{V})}{10\Omega} - \frac{5\text{ms}}{5\text{ms}} \times (6.40\text{A} - 0.12\text{A}) = 0.845\text{A}$$

The average diode current is the difference between the average load current and the average input current, that is

$$\bar{I}_{diode} = \bar{I}_o - \bar{I}_i$$

$$= 3\text{A} - 0.845\text{A} = 2.155\text{A}$$

vi. The input power is the dc supply multiplied by the average input current, that is

$$P_{in} = V_s \bar{I}_i = 340\text{V} \times 0.845\text{A} = 287.3\text{W}$$

$$P_{out} = P_{in} = 287.3\text{W}$$

From equation (13.18) the rms load current is given by

$$\bar{I}_{o_{rms}} = \sqrt{\frac{P_{out} - E\bar{I}_o}{R}}$$

$$= \sqrt{\frac{287.3\text{W} - 55\text{V} \times 3\text{A}}{10\Omega}} = 3.5\text{A rms}$$

vii. The chopper effective input impedance is

$$Z_{in} = \frac{V_s}{\bar{I}_i}$$

$$= \frac{340\text{V}}{0.845\text{A}} = 402.4\ \Omega$$

The electromagnetic efficiency is given by equation (13.22), that is

$$\eta = \frac{E\bar{I}_o}{P_{in}}$$

$$= \frac{55\text{V} \times 3\text{A}}{287.3\text{W}} = 57.4\%$$

viii. The output voltage and current waveforms for the first-quadrant chopper, with and without back emf, are shown in the figure to follow.

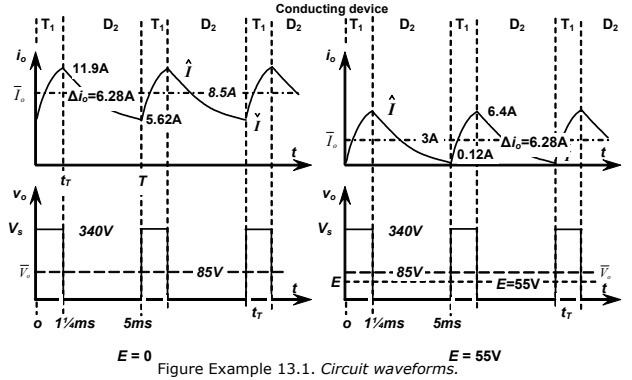

Figure Example 13.1. *Circuit waveforms.*

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Example 13.2: ***DC chopper with load back emf***
- verge of discontinuous conduction

A first-quadrant dc-to-dc chopper feeds an inductive load of 10 ohms resistance, 50mH inductance, and back emf of 55V dc, from a 340V dc source. If the chopper is operated at 200Hz with a 25% on-state duty cycle, determine:

i. the maximum back emf before discontinuous load current conduction commences with δ=¼;
ii. with 55V back emf, what is the minimum duty cycle before discontinuous load current conduction; and
iii. minimum switching frequency at E=55V and t_T = 1.25ms before discontinuous conduction.

Solution
The main circuit and operating parameters are

- on-state duty cycle $\delta = ¼$
- period $T = 1/f_s = 1/200\text{Hz} = 5\text{ms}$
- on-period of the switch $t_T = 1.25\text{ms}$
- load time constant $\tau = L/R = 0.05\text{H}/10\Omega = 5\text{ms}$

First it is necessary to establish whether the given conditions represent continuous or discontinuous load current. The current extinction time t_x for discontinuous conduction is given by equation (13.24), and yields

$$t_x = t_T + \tau\,\ell n\left(1+\frac{V_s - E}{E}\left(1-e^{\frac{-t_T}{\tau}}\right)\right)$$

$$= 1.25\text{ms} + 5\text{ms}\times\ell n\left(1+\frac{340\text{V} - 55\text{V}}{55\text{V}}\times\left(1 - \text{e}^{\frac{-1.25\text{ms}}{5\text{ms}}}\right)\right) = 5.07\text{ms}$$

Since the cycle period is 5ms, which is less than the necessary time for the current to fall to zero (5.07ms), the load current is continuous. From example 13.1 part iv, with E=55V the load current falls from 6.4A to near zero (0.12A) at the end of the off-time, thus the chopper is operating near the verge of discontinuous conduction. A small increase in E, decrease in the duty cycle δ, or increase in switching period T, would be expected to result in discontinuous load current.

i. $\hat{E}$
The necessary back emf can be determined graphically or analytically.
Graphically:
The bounds of continuous and discontinuous load current for a given duty cycle, switching period, and load time constant can be determined from figure 13.5.
Using δ=¼, $T/\tau = 1$ with τ=5ms, and T = 5ms, figure 13.5 gives E/V_s=0.165. That is, $E = 0.165\times V_s = 0.165\times340\text{V} = 56.2\text{V}$
Analytically:
The chopper is operating too close to the boundary between continuous and discontinuous load current conduction for accurate readings to be obtained from the graphical approach, using figure 13.5. Examination of the expression for minimum current, equation (13.13), gives

$$\check{I} = \frac{V_s}{R}\frac{e^{\frac{t_T}{\tau}}-1}{e^{\frac{T}{\tau}}-1} - \frac{E}{R} = 0$$

Rearranging to give the back emf, E, produces

$$E = V_s\frac{e^{\frac{t_T}{\tau}}-1}{e^{\frac{T}{\tau}}-1}$$

$$= 340\text{V}\times\frac{\text{e}^{\frac{1.25\text{ms}}{5\text{ms}}}\text{-1}}{\text{e}^{\frac{5\text{ms}}{5\text{ms}}}\text{-1}} = 56.2\text{V}$$

That is, if the back emf increases from 55V to 56.2V then at that voltage, discontinuous load current commences.

ii. $\check{\delta}$
If equation (13.13) is solved for $\check{I} = 0$ then

$$\check{I} = \frac{V_s}{R}\frac{e^{\frac{t_T}{\tau}}-1}{e^{\frac{T}{\tau}}-1} - \frac{E}{R} = 0$$

Rearranging to isolate t_T gives

$$t_T = \tau\,\ell n\left(1+\frac{E}{V_s}\left(e^{\frac{T}{\tau}}-1\right)\right)$$

$$= 5\text{ms}\times\ell n\left(1+\frac{55\text{V}}{340\text{V}}\left(\text{e}^{\frac{5\text{ms}}{5\text{ms}}}\text{ - 1}\right)\right)$$

$$= 1.226\text{ms}$$

If the switch on-state period is reduced by 0.024ms, from 1.250ms to 1.226ms (24.52%), operation is then on the verge of discontinuous conduction.

iii. $\hat{T}$
If the switching frequency is decreased such that T=t_x, then the minimum period for discontinuous load current is given by equation (13.24). That is,

$$t_x = T = t_T + \tau\,\ell n\left(1+\frac{V_s - E}{E}\left(1-e^{\frac{-t_T}{\tau}}\right)\right)$$

$$T = 1.25\text{ms} + 5\text{ms}\times\ell n\left(1+\frac{340\text{V} - 55\text{V}}{55\text{V}}\times\left(1 - \text{e}^{\frac{-1.25\text{ms}}{5\text{ms}}}\right)\right) = 5.07\text{ms}$$

Discontinuous conduction operation occurs if the period is increased by 0.07ms.

In conclusion, for the given load, for continuous conduction to cease, the following operating conditions can be changed

- increase the back emf E from 55V to 56.2V
- decrease the duty cycle δ from 25% to 24.52% (t_T decreased from 1.25ms to 1.226ms)
- increase the switching period T by 0.07ms, from 5ms to 5.07ms (from 200Hz to 197.2Hz), with the switch on-time, t_T, unchanged from 1.25ms.

Appropriate simultaneous smaller changes in more than one parameter would suffice.

♣

Example 13.3: ***DC chopper with load back emf – discontinuous conduction***

A first-quadrant dc-to-dc chopper feeds an inductive load of 10 ohms resistance, 50mH inductance, and back emf of 100V dc, from a 340V dc source. If the chopper is operated at 200Hz with a 25% on-state duty cycle, determine:

i. the load average and rms voltages;
ii. the rms ripple voltage, hence ripple factor;
iii. the maximum and minimum output current, hence the peak-to-peak output ripple in the current;

iv. the current in the time domain;
v. the load average current, average switch current and average diode current;
vi. the input power, hence output power and rms output current;
vii. effective input impedance, and electromagnetic efficiency; and
viii. Sketch the circuit, load, and output voltage and current waveforms.

Solution

The main circuit and operating parameters are

- on-state duty cycle $\delta = ¼$
- period $T = 1/f_s = 1/200\text{Hz} = 5\text{ms}$
- on-period of the switch $t_T = 1.25\text{ms}$
- load time constant $\tau = L/R = 0.05\text{H}/10\Omega = 5\text{ms}$

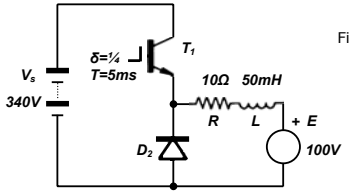


Figure Example 13.3.
Circuit diagram.

Confirmation of discontinuous load current can be obtained by evaluating the minimum current given by equation (13.13), that is

$$\check{I} = \frac{V_s}{R}\frac{e^{\frac{t_T}{\tau}}-1}{e^{\frac{T}{\tau}}-1} - \frac{E}{R}$$

$$\check{I} = \frac{340\text{V}}{10\Omega}\times\frac{e^{\frac{1.25\text{ms}}{5\text{ms}}}\text{-}1}{e^{\frac{5\text{ms}}{5\text{ms}}}\text{-}1} - \frac{100\text{V}}{10\Omega} = 5.62\text{A} - 10\text{A} = -4.38\text{A}$$

The minimum practical current is zero, so clearly discontinuous current periods exist in the load current. The equations applicable to discontinuous load current need to be employed.

The current extinction time is given by equation (13.24), that is

$$t_x = t_T + \tau\,\ell n\left(1+\frac{V_s-E}{E}\left(1-e^{\frac{-t_T}{\tau}}\right)\right)$$

$$= 1.25\text{ms} + 5\text{ms}\times\ell n\left(1+\frac{340\text{V} - 100\text{V}}{100\text{V}}\times\left(1 - e^{\frac{1.25\text{ms}}{5\text{ms}}}\right)\right)$$

$$= 1.25\text{ms} + 2.13\text{ms} = 3.38\text{ms}$$

i. From equations (13.26) and (13.27) the load average and rms voltages are

$$\overline{V}_o = \delta V_s + \frac{T-t_x}{T}E$$

$$= ¼\times 340\text{ V} + \frac{5\text{ms} - 3.38\text{ms}}{5\text{ms}}\times 100\text{V} = 117.4\text{V}$$

$$V_{rms} = \sqrt{\delta V_s^2 + \frac{T-t_x}{T}E^2}$$

$$= \sqrt{¼\times 340^2 + \frac{5\text{ms} - 3.38\text{ms}}{5\text{ms}}\times 100^2} = 179.3\text{V rms}$$

ii. From equations (13.28) and (13.29) the rms ripple voltage, hence ripple factor, are

$$V_r = \sqrt{V_{rms}^2 - V_o^2}$$

$$= \sqrt{179.3^2 - 117.4^2} = 135.5\text{V ac}$$

$$RF = \frac{V_r}{\overline{V}_o} = \frac{135.5\text{V}}{117.4\text{V}} = 1.15$$

iii. From equation (13.36), the maximum and minimum output current, hence the peak-to-peak output ripple in the current, are

$$\hat{I} = \frac{V_s - E}{R}\left(1-e^{\frac{-t_T}{\tau}}\right)$$

$$= \frac{340\text{V-}100\text{V}}{10\Omega}\times\left(1 - e^{\frac{-1.25\text{ms}}{5\text{ms}}}\right) = 5.31\text{A}$$

The minimum current is zero so the peak-to-peak ripple current is $\Delta i_o = 5.31\text{A}$.

iv. From equations (13.32) and (13.33), the current in the time domain is

$$i_o(t) = \frac{V_s - E}{R}\left(1-e^{\frac{-t}{\tau}}\right)$$

$$= \frac{340\text{V} - 100\text{V}}{10\Omega}\times\left(1-e^{\frac{-t}{5\text{ms}}}\right)$$

$$= 24\times\left(1-e^{\frac{-t}{5\text{ms}}}\right) \quad \text{(A)} \qquad \text{for} \quad 0 \le t \le 1.25\text{ms}$$

$$i_o(t) = -\frac{E}{R}\left(1-e^{\frac{-t}{\tau}}\right) + \hat{I}\,e^{\frac{-t}{\tau}}$$

$$= -\frac{100\text{V}}{10\Omega}\times\left(1-e^{\frac{-t}{5\text{ms}}}\right) + 5.31e^{\frac{-t}{5\text{ms}}}$$

$$= 15.31\times e^{\frac{-t}{5\text{ms}}} - 10 \quad \text{(A)} \qquad \text{for} \quad 0 \le t \le 2.13\text{ms}$$

$$i_o(t) = 0 \qquad \text{for} \quad 3.38\text{ms} \le t \le 5\text{ms}$$

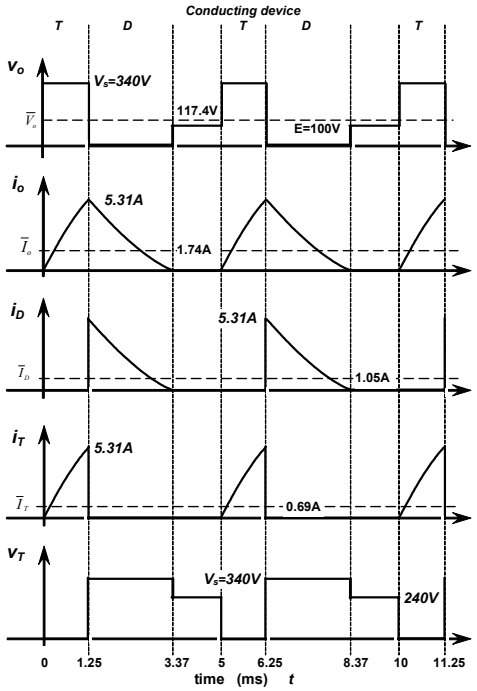


Figure Example 13.3. *Circuit waveforms.*

v. From equations (13.37) to (13.40), the load average current, average switch current, and average diode current are

$$\overline{I}_o = \overline{V}_o - E \Big/ R$$
$$= 117.4\text{V} - 100\text{V} \Big/ 10\Omega = 1.74\text{A}$$
$$\overline{I}_{diode} = \frac{\tau}{T}\hat{I} - \frac{E\left(\frac{t_x}{T} - \delta\right)}{R}$$
$$= \frac{5\text{ms}}{5\text{ms}} \times 5.31\text{A} - \frac{100\text{V} \times \left(\frac{3.38\text{ms}}{5\text{ms}} - 0.25\right)}{10\Omega} = 1.05\text{A}$$

$$\overline{I}_i = \overline{I}_o - \overline{I}_{diode}$$
$$= 1.74\text{A} - 1.05\text{A} = 0.69\text{A}$$

vi. From equation (13.38), the input power, hence output power and rms output current are

$$P_{in} = V_s \overline{I}_i = 340\text{V} \times 0.69\text{A} = 234.6\text{W}$$
$$P_{in} = P_{out} = I^2_{o\,rms} R + E\overline{I}_o$$

Rearranging gives

$$I_{o_{rms}} = \sqrt{P_{in} - E\overline{I}_o} \,/\, R$$
$$= \sqrt{234.6\text{W} - 100\text{V} \times 0.69\text{A}} \,/\, 10\Omega = 1.29\text{A}$$

vii. From equations (13.42) and (13.43), the effective input impedance, and electromagnetic efficiency for $E > 0$

$$Z_{in} = \frac{V_s}{\overline{I}_i} = \frac{340\text{V}}{0.69\text{A}} = 493\Omega$$
$$\eta = \frac{E\overline{I}_o}{P_{in}} = \frac{E\overline{I}_o}{V_s\overline{I}_i} = \frac{100\text{V} \times 1.74\text{A}}{340\text{V} \times 0.69\text{A}} = 74.2\%$$

viii. The circuit, load, and output voltage and current waveforms are plotted in figure example 13.3.

♣

13.3 Second-Quadrant dc chopper

The second-quadrant dc-to-dc chopper shown in figure 13.2b transfers energy from the load, back to the dc energy source, called *regeneration*. Its operating principles are the same as those for the boost switch mode power supply analysed in chapter 15.4. The two energy transfer modes are shown in figure 13.6. Energy is transferred from the back emf E to the supply V_s, by varying the switch T_2 on-state duty cycle. Two modes of transfer can occur, as with the first-quadrant chopper already considered. The current in the load inductor can be either continuous or discontinuous, depending on the specific circuit parameters and operating conditions.

In this analysis it is assumed that:

- No source impedance;
- Constant switch duty cycle;
- Steady-state conditions have been reached;
- Ideal semiconductors; and
- No load impedance temperature effects.

13.3.1 Continuous inductor current

Load waveforms for continuous load current conduction are shown in figure 13.7a. The output voltage v_o, load voltage, or switch voltage, is defined by

$$v_o(t) = \begin{cases} 0 & \text{for } 0 \le t \le t_T \\ V_s & \text{for } t_T \le t \le T \end{cases} \qquad (13.44)$$

The mean load voltage is

$$\begin{aligned} \overline{V}_o &= \frac{1}{T}\int_0^T v_o(t)\,dt = \frac{1}{T}\int_{t_T}^T V_s\,dt \\ &= \frac{T-t_T}{T}V_s = (1-\delta)V_s \end{aligned} \qquad (13.45)$$

where the switch on-state duty cycle $\delta = t_T/T$ is defined in figure 13.7a.

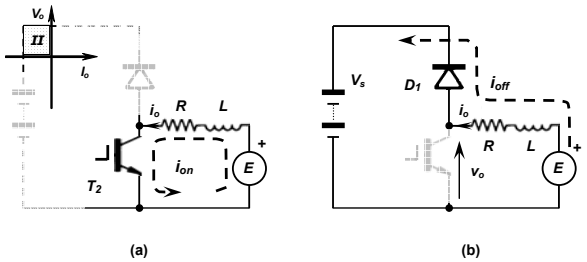


Figure 13.6. *Stages of operation for the second-quadrant chopper: (a) switch-on, boosting current and (b) switch-off, energy into V_s.*

Alternatively the voltage across the dc source V_s is

$$V_s = \frac{1}{1-\delta}\overline{V}_o \qquad (13.46)$$

Since $0 \le \delta \le 1$, the step-up voltage ratio, to regenerate into V_s, is continuously adjustable from unity to infinity.
The average output current is

$$\overline{I}_o = \frac{E-\overline{V}_o}{R} = \frac{E-V_s(1-\delta)}{R} \qquad (13.47)$$

The average output current can also be found by integration of the time domain output current i_o. By solving the appropriate time domain differential equations, the continuous load current i_o shown in figure 13.7a is defined by
During the **switch on-period**, when v_o=0

$$L\frac{di_o}{dt} + Ri_o = E$$

which yields

$$i_o(t) = \frac{E}{R}\left(1-e^{\frac{-t}{\tau}}\right) + \check{I}e^{\frac{-t}{\tau}} \qquad \text{for} \quad 0 \le t \le t_T \qquad (13.48)$$

During the **switch off-period**, when v_o=V_s

$$L\frac{di_o}{dt} + Ri_o + V_s = E$$

which, after shifting the zero time reference to t_T, gives

$$i_o(t) = \frac{E-V_s}{R}\left(1-e^{\frac{-t}{\tau}}\right) + \hat{I}e^{\frac{-t}{\tau}} \qquad \text{for} \quad 0 \le t \le T-t_T \qquad (13.49)$$

$$\text{where} \quad \hat{I} = \frac{E}{R} - \frac{V_s}{R}\frac{e^{\frac{-t_T}{\tau}} - e^{\frac{-T}{\tau}}}{1-e^{\frac{-T}{\tau}}} \quad \text{(A)}$$

$$\text{and} \quad \check{I} = \frac{E}{R} - \frac{V_s}{R}\frac{1-e^{\frac{-T+t_T}{\tau}}}{1-e^{\frac{-T}{\tau}}} \quad \text{(A)} \qquad (13.50)$$

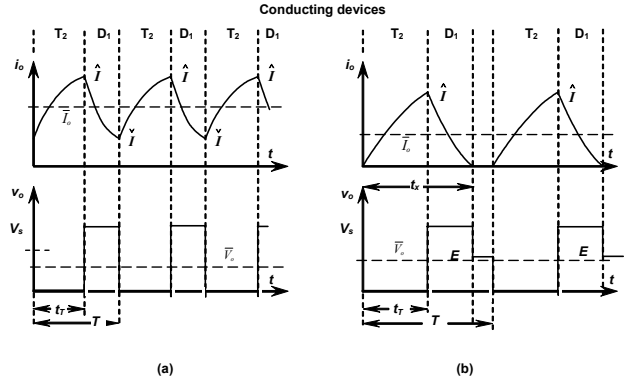


Figure 13.7. *Second-quadrant chopper output modes of current operation: (a) continuous inductor current and (b) discontinuous inductor current.*

The output ripple current, for continuous conduction, is independent of the back emf E and is given by

$$I_{p-p} = \hat{I} - \check{I} = \frac{V_s}{R}\,\frac{(1+e^{\frac{-T}{\tau}}) - (e^{\frac{-t_T}{\tau}} + e^{\frac{-T+t_T}{\tau}})}{1-e^{\frac{-T}{\tau}}} \qquad (13.51)$$

which in terms of the on-state duty cycle, δ=t_T/T, becomes

$$I_{p-p} = \frac{V_s}{R}\,\frac{(1-e^{\frac{-\delta T}{\tau}})(1+e^{\frac{-T}{\tau}})}{1-e^{\frac{-T}{\tau}}} \tag{13.52}$$

This is the same expression derived in 13.2.1 for the first-quadrant chopper. The normalised ripple current design curves in figure 13.3 are valid for the second-quadrant chopper.

The average switch current, $\overline{I}_{switch}$, can be derived by integrating the switch current given by equation (13.48), that is

$$\begin{aligned}\overline{I}_{switch} &= \frac{1}{T}\int_0^{t_T} i_o(t)\,dt \\ &= \frac{1}{T}\int_0^{t_T}\left(\frac{E}{R}\left(1-e^{\frac{-t}{\tau}}\right)+\check{I}\,e^{\frac{-t}{\tau}}\right)dt \\ &= \frac{\delta E}{R}-\frac{\tau}{T}\left(\hat{I}-\check{I}\right)\end{aligned} \tag{13.53}$$

The term $\hat{I}-\check{I} = I_{p-p}$ is the peak-to-peak ripple current, which is given by equation (13.51). By Kirchhoff's current law, the average diode current $\overline{I}_{diode}$ is the difference between the average output current $\overline{I}_o$ and the average switch current, $\overline{I}_{switch}$, that is

$$\begin{aligned}\overline{I}_{diode} &= \overline{I}_o - \overline{I}_{switch} \\ &= \frac{E-V_s(1-\delta)}{R}-\frac{\delta E}{R}+\frac{\tau}{T}\left(\hat{I}-\check{I}\right) \\ &= \frac{\tau}{T}\left(\hat{I}-\check{I}\right)-\frac{(V_s-E)(1-\delta)}{R}\end{aligned} \tag{13.54}$$

The average diode current can also be found by integrating the diode current given in equation (13.49), as follows

$$\begin{aligned}\overline{I}_{diode} &= \frac{1}{T}\int_0^{T-t_T}\left(\frac{E-V_s}{R}\left(1-e^{\frac{-t}{\tau}}\right)+\hat{I}\,e^{\frac{-t}{\tau}}\right)dt \\ &= \frac{\tau}{T}\left(\hat{I}-\check{I}\right)-\frac{(V_s-E)(1-\delta)}{R}\end{aligned} \tag{13.55}$$

The power produced by the back emf source E is

$$P_E = E\overline{I}_o = E\left(\frac{E-V_s(1-\delta)}{R}\right) \tag{13.56}$$

The power delivered to the dc source V_s is

$$P_{V_s} = V_s\overline{I}_{diode} = V_s\left(\frac{\tau}{T}\left(\hat{I}-\check{I}\right)-\frac{(V_s-E)(1-\delta)}{R}\right) \tag{13.57}$$

The difference between the two powers is the power lost in the load resistor, R, that is

$$\begin{aligned}P_E &= P_{V_s} + I_{o_{rms}}^2 R \\ I_{o_{rms}} &= \sqrt{\frac{E\overline{I}_o - V_s\overline{I}_{diode}}{R}}\end{aligned} \tag{13.58}$$

The efficiency of energy transfer between the back emf E and the dc source V_s is

$$\eta = \frac{P_{V_s}}{P_E} = \frac{V_s\overline{I}_{diode}}{E\overline{I}_o} \tag{13.59}$$

13.3.2 Discontinuous inductor current

With low duty cycles, δ, low inductance, L, or a relatively high dc source voltage, V_s, the minimum output current may reach zero at t_x, before the period T is complete, as shown in figure 13.7b. Equation (13.50) gives a boundary identity that must be satisfied for zero current,

$$\check{I} = \frac{E}{R}-\frac{V_s}{R}\,\frac{1-e^{\frac{T-t_T}{\tau}}}{1-e^{\frac{-T}{\tau}}} \;=\; 0 \tag{13.60}$$

That is

$$\frac{E}{V_s} = \frac{1-e^{\frac{-T+t_T}{\tau}}}{1-e^{\frac{-T}{\tau}}} \tag{13.61}$$

Alternatively, the time domain equations (13.48) and (13.49) can be used, such that $\check{I}=0$. An expression for the extinction time t_x can be found by substituting $t=t_T$ into equation (13.48). The resulting expression for $\hat{I}$ is then substituted into equation (13.49) which is set to zero. Isolating the time variable, which becomes t_x, yields

$$\begin{aligned}\hat{I} &= \frac{E}{R}\left(1-e^{\frac{-t_T}{\tau}}\right) \\ 0 &= \frac{E-V_s}{R}\left(1-e^{\frac{-t_x}{\tau}}\right)+\frac{E}{R}\left(1-e^{\frac{-t_T}{\tau}}\right)e^{\frac{-t_x}{\tau}}\end{aligned}$$

which yields

$$t_x = t_T + \tau\,\ell n\left(1+\frac{E}{V_s-E}\left(1-e^{\frac{-t_T}{\tau}}\right)\right) \tag{13.62}$$

This equation shows that $t_x \geq t_T$. Load waveforms for discontinuous load current conduction are shown in figure 13.7b.

The output voltage v_o, load voltage, or switch voltage, is defined by

$$v_o(t) = \begin{cases} 0 & \text{for } 0 \leq t \leq t_T \\ V_s & \text{for } t_T \leq t \leq t_x \\ E & \text{for } t_x \leq t \leq T \end{cases} \tag{13.63}$$

The mean load voltage is

$$\overline{V}_o = \frac{1}{T}\int_0^T v_o(t)\,dt = \frac{1}{T}\left(\int_{t_T}^{t_x} V_s\,dt + \int_{t_x}^{T} E\,dt\right)$$

$$= \frac{t_x - t_T}{T} V_s + \frac{T - t_x}{T} E = \left(\frac{t_x}{T} - \delta\right) V_s + \left(1 - \frac{t_x}{T}\right) E$$
$$\overline{V}_o = E - \delta V_s + \frac{t_x}{T}\left(V_s - E\right) \tag{13.64}$$

where the switch on-state duty cycle $\delta = t_T/T$ is defined in figure 13.7b.
The average output current is

$$\overline{I}_o = \frac{E - \overline{V}_o}{R} = \frac{\delta V_s - \frac{t_x}{T}\left(V_s - E\right)}{R} \tag{13.65}$$

The average output current can also be found by integration of the time domain output current i_o. By solving the appropriate time domain differential equations, the continuous load current i_o shown in figure 13.7a is defined by
During the **switch on-period**, when $v_o = 0$

$$L\frac{di_o}{dt} + R i_o = E$$

which yields

$$i_o(t) = \frac{E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) \qquad \text{for} \quad 0 \le t \le t_T \tag{13.66}$$

During the **switch off-period**, when $v_o = V_s$

$$L\frac{di_o}{dt} + R i_o + V_s = E$$

which, after shifting the zero time reference to t_T, gives

$$i_o(t) = \frac{E - V_s}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I} e^{\frac{-t}{\tau}} \qquad \text{for} \quad 0 \le t \le t_x - t_T \tag{13.67}$$

$$\text{where} \quad \hat{I} = \frac{E}{R}\left(1 - e^{\frac{-t_T}{\tau}}\right) \quad \text{(A)}$$
$$\text{and} \quad \check{I} = 0 \quad \text{(A)} \tag{13.68}$$

After t_x, $v_o(t) = E$ and the load current is zero, that is

$$i_o(t) = 0 \qquad \text{for} \quad t_x \le t \le T \tag{13.69}$$

The output ripple current, for discontinuous conduction, is dependent of the back emf E and is given by equation (13.68),

$$I_{p-p} = \hat{I} = \frac{E}{R}\left(1 - e^{\frac{-t_T}{\tau}}\right) \tag{13.70}$$

The average switch current, $\overline{I}_{switch}$, can be derived by integrating the switch current given by equation (13.66), that is

$$\overline{I}_{switch} = \frac{1}{T}\int_0^{t_T} i_o(t)\,dt$$
$$= \frac{1}{T}\int_0^{t_T}\left(\frac{E}{R}\left(1 - e^{\frac{-t}{\tau}}\right)\right)dt \tag{13.71}$$
$$= \frac{\delta E}{R} - \frac{\tau}{T}\hat{I}$$

The term $\hat{I} = I_{p-p}$ is the peak-to-peak ripple current, which is given by equation (13.70). By Kirchhoff's current law, the average diode current $\overline{I}_{diode}$ is the difference between the average output current $\overline{I}_o$ and the average switch current, $\overline{I}_{switch}$, that is

$$\overline{I}_{diode} = \overline{I}_o - \overline{I}_{switch}$$
$$= \frac{\delta V_s - \frac{t_x}{T}\left(V_s - E\right)}{R} - \frac{\delta E}{R} + \frac{\tau}{T}\hat{I} \tag{13.72}$$
$$= \frac{\tau}{T}\hat{I} - \frac{\left(\frac{t_x}{T} - \delta\right)\left(V_s - E\right)}{R}$$

The average diode current can also be found by integrating the diode current given in equation (13.67), as follows

$$\overline{I}_{diode} = \frac{1}{T}\int_0^{t_x - t_T}\left(\frac{E - V_s}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I} e^{\frac{-t}{\tau}}\right)dt$$
$$= \frac{\tau}{T}\hat{I} - \frac{\left(\frac{t_x}{T} - \delta\right)\left(V_s - E\right)}{R} \tag{13.73}$$

The power produced by the back emf source E is

$$P_E = E\overline{I}_o \tag{13.74}$$

The power delivered to the dc source V_s is

$$P_{V_s} = V_s \overline{I}_{diode} \tag{13.75}$$

Alternatively, the difference between the two powers is the power lost in the load resistor, R, that is

$$P_E = P_{V_s} + I_{o_{rms}}^2 R$$
$$I_{o_{rms}} = \sqrt{\frac{E\overline{I}_o - V_s\overline{I}_{diode}}{R}} \tag{13.76}$$

The efficiency of energy transfer between the back emf and the dc source is

$$\eta = \frac{P_{V_s}}{P_E} = \frac{V_s\overline{I}_{diode}}{E\overline{I}_o} \tag{13.77}$$

Example 13.4: ***Second-quadrant DC chopper – continuous conduction***

A dc-to-dc chopper capable of second-quadrant operation is used in a 200V dc battery electric vehicle. The machine armature has 1 ohm resistance and 1mH inductance.

i. The machine is used for regenerative braking. At a constant speed downhill, the back emf is 150V, which results in a 10A braking current. What is the switch on-state duty cycle if the machine is delivering continuous output current? What is the minimum chopping frequency for these conditions?

ii. At this speed, (that is, E=150V), determine the minimum duty cycle for continuous inductor current, if the switching frequency is 1kHz. What is the average braking current at the critical duty cycle? What is the regenerating efficiency and the rms machine output current?

iii. If the chopping frequency is increased to 5kHz, at the same speed, (that is, E=150V), what is the critical duty cycle and the corresponding average machine current?

Solution

The main circuit operating parameters are

- V_s=200V
- E=150V
- load time constant $\tau = L/R$ = 1H/1Ω = 1ms

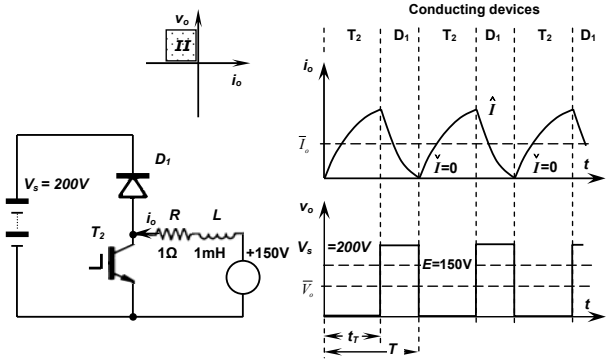


Figure Example 13.4. *Circuit diagram and waveforms.*

i. The relationship between the dc supply V_s and the machine back emf E is given by equation (13.47), that is

$$\bar{I}_o = \frac{E - \bar{V}_o}{R} = \frac{E - V_s(1-\delta)}{R}$$

$$10\text{A} = \frac{150\text{V} - 200\text{V}\times(1 - \delta)}{1\Omega}$$

that is

$$\delta = 0.3 \equiv 30\% \quad \text{and} \quad \bar{V}_o = 140\text{V}$$

The expression for the average machine output current is based on continuous armature inductance current. Therefore the switching period must be shorter than the time t_x predicted by equation (13.62) for the current to reach zero, before the next switch on-period. That is, for t_x=T and δ=0.3

$$t_x = t_T + \tau\,\ell n\left(1 + \frac{E}{V_s - E}\left(1 - e^{\frac{-t_T}{\tau}}\right)\right)$$

This simplifies to

$$1 = 0.3 + \frac{1\text{ms}}{T}\ell n\left(1 + \frac{150\text{V}}{200\text{V - }150\text{V}}\left(1 - e^{\frac{-0.3T}{1\text{ms}}}\right)\right)$$

$$e^{0.7T} = 4 - 3e^{-0.3T}$$

Iteratively solving this transcendental equation gives T= 0.4945ms. That is the switching frequency must be greater than $f_s = 1/T$ = 2.022kHz, else machine output current discontinuities occur, and equation (13.47) is invalid. The switching frequency can be reduced if the on-state duty cycle is increased as in the next part of this example.

ii. The operational boundary condition giving by equation (13.61), using T=$1/f_s$ =1/1kHz = 1ms, yields

$$\frac{E}{V_s} = \frac{1 - e^{\frac{-T + t_T}{\tau}}}{1 - e^{\frac{-T}{\tau}}}$$

$$\frac{150\text{V}}{200\text{V}} = \frac{1 - \text{e}^{\frac{(\delta - 1)\times 1\text{ms}}{1\text{ms}}}}{1 - \text{e}^{\frac{-1\text{ms}}{1\text{ms}}}}$$

Solving gives δ=0.357. That is, the on-state duty cycle must be at least 35.7% for continuous machine output current at a switching frequency of 1kHz.

For continuous inductor current, the average output current is given by equation (13.47), that is

$$\bar{I}_o = \frac{E - \bar{V}_o}{R} = \frac{E - V_s(1-\delta)}{R}$$

$$= \frac{150\text{V - }\bar{V}_o}{1\Omega} = \frac{150\text{V - }200\text{V}\times(1 - 0.357)}{1\Omega} = 21.4\text{A}$$

$$\bar{V}_o = 150\text{V - }21.4\text{A}\times 1\Omega = 128.6\text{V}$$

The average machine output current of 21.4A is split between the switch and the diode (which is in series with V_s).

The diode current is given by equation (13.54)

$$\bar{I}_{diode} = \bar{I}_o - \bar{I}_{switch}$$

$$= \frac{\tau}{T}\left(\hat{I} - \check{I}\right) - \frac{(V_s - E)(1-\delta)}{R}$$

The minimum output current is zero while the maximum is given by equation (13.68).

$$\hat{I} = \frac{E}{R}\left(1 - e^{\frac{-t_T}{\tau}}\right) = \frac{150\text{V}}{1\Omega}\times\left(1 - \text{e}^{\frac{-0.357\times 1\text{ms}}{1\text{ms}}}\right) = 45.0\text{A}$$

Substituting into the equation for the average diode current gives

$$\bar{I}_{diode} = \frac{1\text{ms}}{1\text{ms}}\times(45.0\text{A - }0\text{A}) - \frac{(200\text{V - }150\text{V})\times(1 - 0.357)}{1\Omega} = 12.85\text{A}$$

The power delivered by the back emf E is

$$P_E = E\overline{I}_o = 150\text{V}\times 21.4\text{A} = 3210\text{W}$$

While the power delivered to the 200V battery source V_s is

$$P_{V_s} = V_s \overline{I}_{diode} = 200\text{V}\times 12.85\text{A} = 2570\text{W}$$

The regeneration transfer efficiency is

$$\eta = \frac{P_{V_s}}{P_E} = \frac{2570\text{W}}{3210\text{W}} = 80.1\%$$

The energy generated deficit, 640W (3210W - 2570W)), is lost in the armature resistance, as I^2R heat dissipated. The output rms current is

$$I_{o_{rms}} = \sqrt{\frac{P}{R}} = \sqrt{\frac{640\text{W}}{1\Omega}} = 25.3\text{A rms}$$

iii. At an increased switching frequency of 5kHz, the duty cycle would be expected to be much lower than the 35.7% as at 1kHz. The operational boundary between continuous and discontinuous armature inductor current is given by equation (13.61), that is

$$\frac{E}{V_s} = \frac{1-e^{\frac{-T+t_T}{\tau}}}{1-e^{\frac{-T}{\tau}}}$$

$$\frac{150\text{V}}{200\text{V}} = \frac{1 - \text{e}^{\frac{(-1+\delta)\times 0.2\text{ms}}{1\text{ms}}}}{1 - \text{e}^{\frac{-0.2\text{ms}}{1\text{ms}}}}$$

which yields $\delta = 26.9\%$.

The machine average output current is given by equation (13.47)

$$\overline{I}_o = \frac{E-\overline{V}_o}{R} = \frac{E-V_s(1-\delta)}{R}$$

$$= \frac{150\text{V}-\overline{V}_o}{1\Omega} = \frac{150\text{V} - 200\text{V}\times(1 - 0.269)}{1\Omega} = 3.8\text{A}$$

such that the average output voltage $\overline{V}_o$ is 146.2V.

♣

13.4 Two-quadrant dc chopper - Q I and Q II

Figure 13.8 shows the basic two-quadrant dc chopper, which is basically a reproduction of the circuit in figure 13.2c. Depending on the load and operating conditions the chopper can seamlessly change between and act in two modes

- Devices T_1 and D_2 form the first-quadrant chopper shown in figure 13.2a, and analysed in section 13.2. Energy is delivered from the dc source V_s to the *R-L-E* load.
- Devices T_2 and D_1 form the second-quadrant chopper shown in figure 13.2c, which is analysed in section 13.3. Energy is delivered from the generating load dc source E, to the dc source V_s.

The two independent choppers can be readily combined as shown in figure 13.8a.

The average output voltage $\overline{V}_o$ and the instantaneous output voltage v_o are never

negative, whilst the average source current of V_s can be positive (Quadrant I) or negative (Quadrant II). If the two choppers are controlled to operate independently, with the constraint that T_1 and T_2 do not conduct simultaneously, then the analysis in sections 13.2 and 13.3 are valid. Alternately, it is not uncommon the unify the operation of the two choppers, as follows.

If the chopper is operated such that the switches T_1 and T_2 act in a complementary manner, that is either T_1 or T_2 is on, then some of the independent flexibility offered by each chopper is lost. Essentially the consequence of complementary switch operation is that no extended zero current periods exist in the output, as shown in figures 13.8a and b. Thus the equations describing the features of the first-quadrant chopper in section 13.2.1, for continuous load current, are applicable to this chopper, with slight modification to account for the fact that both the minimum and maximum currents can be negative.

The analysis for continuous inductor current in section 13.2 is valid, but the minimum current is not restricted to zero. Consequently four possible output modes can occur, depending on the relative polarity of the maximum and minimum currents shown in figure 18.8b and c.

i. $\check{I} > 0$, $\hat{I} > 0$ and $\overline{I}_o > 0$
   When the minimum current (hence average output current) is greater than zero, the chopper is active in the first-quadrant. Typical output voltage and current waveforms are shown in figure 13.3a. The switch T_2 and diode D_1 do not conduct during any portion of the operating period.
ii. $\check{I} < 0$, $\hat{I} > 0$ and $\overline{I}_o > 0$
   When the minimum current is negative but the maximum positive current is larger in magnitude, then for a highly inductive load, the average output current is greater than zero, and the chopper operates in the first-quadrant. If the load is not highly inductive the boundary is determined by the average output current $\overline{I}_o > 0$. The various circuit waveforms are shown in figure 13.8b.
iii. $\check{I} < 0$, $\hat{I} > 0$ and $\overline{I}_o < 0$
   For a highly inductive load, if the magnitude of the negative peak is greater than the positive maximum, the average is less than zero and the chopper is operating in the regenerative mode, quadrant II. If the load is not highly inductive the boundary is determined by the average output current $\overline{I}_o < 0$.
iv. $\check{I} < 0$, $\hat{I} < 0$ and $\overline{I}_o < 0$
   When the maximum current and the average current are both negative, the chopper is operational in the second-quadrant. Since the load current never goes positive, switch T_1 and diode D_2 never conduct, as shown in figure 13.8c.

In all cases the average output voltage is solely determined by the switch T_1 on-time duty cycle, since when this switch is turned on the supply V_s is impressed across the load, independent of the direction of the load current. When $i_o > 0$, switch T_1 conducts while if $i_o < 0$, the diode in parallel to switch T_1, namely D_2 conducts, clamping the load to V_s.

The output voltage, which is independent of the load, is described by

$$v_o(t) = \begin{cases} V_s & \text{for } 0 \le t \le t_T \\ 0 & \text{for } t_T \le t \le T \end{cases} \qquad (13.78)$$

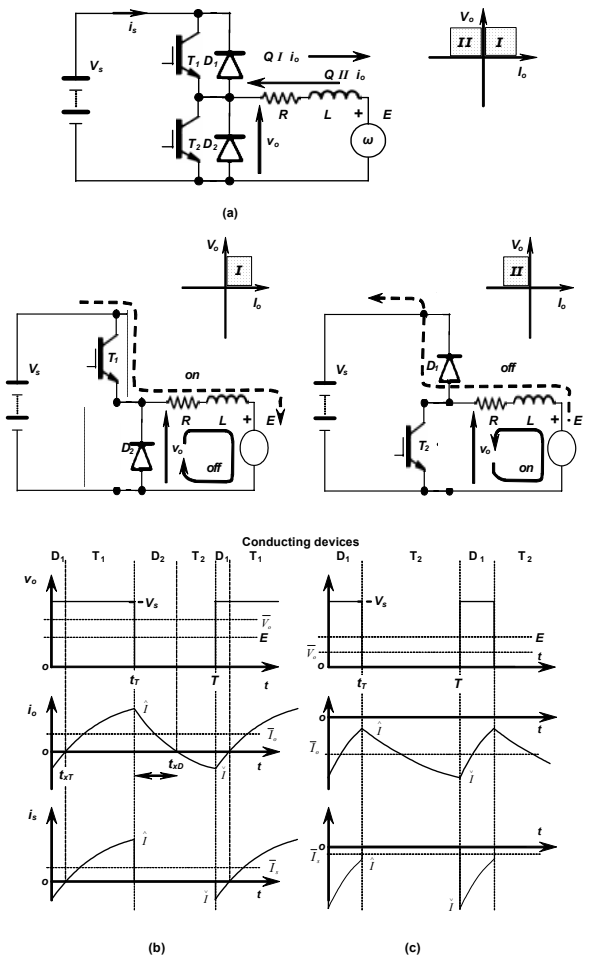


Figure 13.8. *Two-quadrant (I and II) dc chopper circuit where v_o>0: (a) basic two-quadrant dc chopper; (b) operation and waveforms for quadrant I; and (c) operation and waveforms for quadrant II, regeneration into V_s.*

Thus

$$\overline{V}_o = \frac{1}{T}\int_0^{t_T} V_s dt = \frac{t_T}{T} V_s = \delta V_s \tag{13.79}$$

The rms output voltage is also determined solely by the duty cycle,

$$V_{rms} = \left[\frac{1}{T}\int_0^{t_T} V_s^2 \, dt\right]^{1/2} = \sqrt{\delta}\, V_s \tag{13.80}$$

The output ac ripple voltage, hence ripple factor are given by equations (13.3) and (13.5), and are independent of the load:

$$V_r = \sqrt{V_{rms}^2 - V_o^2} = V_s\sqrt{\delta(1-\delta)} \tag{13.81}$$

and

$$RF = \frac{V_r}{\overline{V}_o} = \sqrt{\frac{1}{\delta} - 1} \tag{13.82}$$

The Fourier series for the load voltage can be used to determine the load current at each harmonic frequency as described by equations (13.6) to (13.10).
The time domain differential equations from section 13.2.1 are also valid, where there is no zero restriction on the minimum load current value.
In a **positive voltage loop**, when $v_o(t)=V_s$ and V_s is impressed across the load, the load circuit condition is described by

$$i_o(t) = \frac{V_s - E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \check{I}\, e^{\frac{-t}{\tau}} \qquad \text{for} \quad 0 \le t \le t_T \tag{13.83}$$

During the **switch off-period**, when v_o=0, forming a zero voltage loop

$$i_o(t) = -\frac{E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}\, e^{\frac{-t}{\tau}} \qquad \text{for} \quad 0 \le t \le T - t_T \tag{13.84}$$

where

$$\text{where} \quad \hat{I} = \frac{V_s}{R}\frac{1 - e^{\frac{-t_T}{\tau}}}{1 - e^{\frac{-T}{\tau}}} - \frac{E}{R} \quad \text{(A)}$$

$$\text{and} \quad \check{I} = \frac{V_s}{R}\frac{e^{\frac{t_T}{\tau}} - 1}{e^{\frac{T}{\tau}} - 1} - \frac{E}{R} \quad \text{(A)} \tag{13.85}$$

The peak-to-peak ripple current is independent of E,

$$I_{p-p} = \frac{V_s}{R}\frac{(1 - e^{\frac{-\delta T}{\tau}})(1 - e^{\frac{-(1-\delta)T}{\tau}})}{1 - e^{\frac{-T}{\tau}}} \tag{13.86}$$

The average output current, $\overline{I}_o$, may be positive or negative and is given by

$$\overline{I}_o = \frac{1}{T}\int_0^T i_o(t)\, dt = \left(\overline{V}_o - E\right)\Big/R = \left(\delta V_s - E\right)\Big/R \quad \text{(A)} \tag{13.87}$$

The direction of the net power flow between E and V_s determines the chopper

operating quadrant. If $\overline{V}_o > E$ then average power flow is to the load, as shown in figure 13.8b, while if $\overline{V}_o < E$, the average power flow is back into the source V_s, as shown in figure 13.8c.

$$V_s \overline{I}_s = \pm I_{o_{rms}}^2 R + E\overline{I}_o \tag{13.88}$$

Thus the sign of $\overline{I}_o$ determines the direction of net power flow, hence quadrant of operation.

Calculation of individual device average currents in the time domain is complicated by the fact that the energy may flow between the dc source V_s and the load via the switch T_1 (energy to the load) or diode D_1 (energy from the load). It is therefore necessary to ascertain the zero current crossover time, when $\hat{I}$ and $\check{I}$ have opposite signs, which will then specify the necessary bounds of integration. Equations (13.83) and (13.84) are equated to zero and solved for the time at zero crossover, t_{xT} and t_{xD}, respectively, shown in figure 13.8b.

$$\begin{aligned} t_{xT} &= \tau\, \ell n\left(1 - \frac{\check{I}R}{V_s - E}\right) \quad \text{with respect to } t = 0 \\ t_{xD} &= \tau\, \ell n\left(1 + \frac{\hat{I}R}{E}\right) \quad \text{with respect to } t = t_T \end{aligned} \tag{13.89}$$

The necessary integration for each device can then be determined with the aid of the device conduction information in the parts of figure 13.8 and Table 13.1.

Table 13.1 Device average current ratings

Device and integration bounds, a to b	$\hat{I} > 0, \check{I} > 0$	$\hat{I} > 0, \check{I} < 0$	$\hat{I} < 0, \check{I} < 0$
$\overline{I}_{T1} = \frac{1}{T}\int_a^b \frac{V_s - E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \check{I}e^{\frac{-t}{\tau}}dt$	0 to t_T	t_{xT} to t_T	0 to 0
$\overline{I}_{D1} = \frac{1}{T}\int_0^b \frac{V_s - E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \check{I}e^{\frac{-t}{\tau}}dt$	0 to 0	0 to t_{xT}	0 to t_T
$\overline{I}_{T2} = \frac{1}{T}\int_a^b -\frac{E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}e^{\frac{-t}{\tau}}dt$	0 to 0	t_{xD} to $T - t_T$	0 to $T - t_T$
$\overline{I}_{D2} = \frac{1}{T}\int_0^b -\frac{E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}e^{\frac{-t}{\tau}}dt$	0 to $T - t_T$	0 to t_{xD}	0 to 0

The electromagnetic energy transfer efficiency is determined from

$$\begin{aligned} \eta &= \frac{E\overline{I}_o}{V_s\overline{I}_i} \quad \text{for } \overline{I}_o > 0 \\ \eta &= \frac{V_s\overline{I}_i}{E\overline{I}_o} \quad \text{for } \overline{I}_o < 0 \end{aligned} \tag{13.90}$$

Example 13.5: ***Two-quadrant DC chopper with load back emf***

The two-quadrant dc-to-dc chopper in figure 13.8a feeds an inductive load of 10 ohms resistance, 50mH inductance, and back emf of 100V dc, from a 340V dc source. If the chopper is operated at 200Hz with a 25% on-state duty cycle, determine:

i. the load average and rms voltages;
ii. the rms ripple voltage, hence ripple factor;
iii. the maximum and minimum output current, hence the peak-to-peak output ripple in the current;
iv. the current in the time domain;
v. the current crossover times, if applicable;
vi. the load average current, average switch current and average diode current for all devices;
vii. the input power, hence output power and rms output current;
viii. effective input impedance and electromagnetic efficiency; and
ix. Sketch the circuit, load, and output voltage and current waveforms.

Subsequently determine the necessary change in

x. Duty cycle δ to result in zero average output current and
xi. Back emf E to result in zero average load current

Solution

The main circuit and operating parameters are

- on-state duty cycle $\delta = ¼$
- period $T = 1/f_s = 1/200\text{Hz} = 5\text{ms}$
- on-period of the switch $t_T = 1.25\text{ms}$
- load time constant $\tau = L/R = 0.05\text{H}/10\Omega = 5\text{ms}$

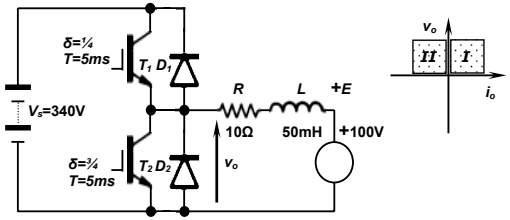


Figure Example 13.5. *Circuit diagram.*

i. From equations (13.79) and (13.80) the load average and rms voltages are

$$v_o = \frac{t_T}{T}V_s = \frac{1.25\text{ms}}{5\text{ms}} \times 340\text{V} = ¼ \times 340\text{V} = 85\text{V}$$

$$V_{rms} = \sqrt{\delta}\, V_s = \sqrt{¼} \times 340\text{V} = 170\text{V} \quad \text{rms}$$

ii. The rms ripple voltage, hence ripple factor, from equations (13.81) and (13.82) are

$$V_r = \sqrt{V_{rms}^2 - V_o^2} = V_s\sqrt{\delta(1-\delta)}$$
$$= \sqrt{170^2 - 85^2} = 340\text{V}\sqrt{¼ \times (1 - ¼)} = 147.2\text{V}$$
$$RF = \frac{V_r}{\overline{V}_o} = \sqrt{\frac{1}{\delta} - 1} = \sqrt{\frac{1}{¼} - 1} = 1.732$$

iii. From equations (13.85) and (13.86), the maximum and minimum output current, hence the peak-to-peak output ripple in the current are given by

$$\hat{I} = \frac{V_s}{R}\frac{1-e^{\frac{-t_T}{\tau}}}{1-e^{\frac{-T}{\tau}}} - \frac{E}{R} = \frac{340\text{V}}{10\Omega} \times \frac{1 - \text{e}^{\frac{-1.25\text{ms}}{5\text{ms}}}}{1 - \text{e}^{\frac{-5\text{ms}}{5\text{ms}}}} - \frac{100\text{V}}{10\Omega} = 1.90\text{A}$$

$$\check{I} = \frac{V_s}{R}\frac{e^{\frac{t_T}{\tau}}-1}{e^{\frac{T}{\tau}}-1} - \frac{E}{R} = \frac{340\text{V}}{10\Omega} \times \frac{\text{e}^{\frac{1.25\text{ms}}{5\text{ms}}} - 1}{\text{e}^{\frac{5\text{ms}}{5\text{ms}}} - 1} - \frac{100\text{V}}{10\Omega} = -4.38\text{A}$$

The peak-to-peak ripple current is therefore $\Delta i_o = 1.90\text{A} - -4.38\text{A} = 6.28\text{A}$ p-p.

iv. The current in the time domain is given by equations (13.83) and (13.84)

$$i_o(t) = \frac{V_s - E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \check{I}e^{\frac{-t}{\tau}}$$
$$= \frac{340\text{V-}100\text{V}}{10\Omega} \times \left(1 - e^{\frac{-t}{5\text{ms}}}\right) - 4.38 \times e^{\frac{-t}{5\text{ms}}}$$
$$= 24 \times \left(1 - e^{\frac{-t}{5\text{ms}}}\right) - 4.38 \times e^{\frac{-t}{5\text{ms}}}$$
$$= 24 - 28.38 \times e^{\frac{-t}{5\text{ms}}} \qquad \text{for} \quad 0 \le t \le 1.25\text{ms}$$

$$i_o(t) = -\frac{E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}e^{\frac{-t}{\tau}}$$
$$= -\frac{100V}{10\Omega} \times \left(1 - e^{\frac{-t}{5\text{ms}}}\right) + 1.90 \times e^{\frac{-t}{5\text{ms}}}$$
$$= -10 \times \left(1 - e^{\frac{-t}{5\text{ms}}}\right) + 1.90 \times e^{\frac{-t}{5\text{ms}}}$$
$$= -10 + 11.90 \times e^{\frac{-t}{5\text{ms}}} \qquad \text{for} \quad 0 \le t \le 3.75\text{ms}$$

v. Since the maximum current is greater than zero (1.9A) and the minimum is less that zero (- 4.38A), the current crosses zero during the switch on-time and off-time. The time domain equations for the load current are solved for zero to give the cross over times t_{xT} and t_{xD}, as given by equation (13.89), or solved from the time domain output current equations as follows.
During the switch on-time

$$i_o(t) = 24 - 28.38 \times e^{\frac{-t}{5\text{ms}}} = 0 \qquad \text{where} \quad 0 \le t = t_{xT} \le 1.25\text{ms}$$
$$t_{xT} = 5\text{ms} \times \ell n\frac{28.38}{24} = 0.838\text{ms}$$

During the switch off-time

$$i_o(t) = -10 + 11.90 \times e^{\frac{-t}{5\text{ms}}} = 0 \qquad \text{where} \quad 0 \le t = t_{xD} \le 3.75\text{ms}$$
$$t_{xD} = 5\text{ms} \times \ell n\frac{11.90}{10} = 0.870\text{ms}$$

(1.250ms + 0.870ms = 2.12ms with respect to switch turn-on)

vi. The load average current, average switch current, and average diode current for all devices;

$$\overline{I}_o = \left(\overline{V}_o - E\right)\Big/R = \left(\delta V_s - E\right)\Big/R$$
$$\left(85\text{V} - 100\text{V}\right)\Big/10\Omega = -1.5\text{A}$$

When the output current crosses zero current, the conducting device changes. Table 13.1 gives the necessary current equations and integration bounds for the condition $\hat{I} > 0$, $\check{I} < 0$. Table 13.1 shows that all four semiconductors are involved in the output current cycle.

$$\overline{I}_{T1} = \frac{1}{T}\int_{t_{xT}}^{t_T} \frac{V_s - E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \check{I}e^{\frac{-t}{\tau}}dt$$
$$= \frac{1}{5\text{ms}}\int_{0.838\text{ms}}^{1.25\text{ms}} 24 - 28.38 \times e^{\frac{-t}{5\text{ms}}}dt = 0.081\text{A}$$

$$\overline{I}_{D1} = \frac{1}{T}\int_{0}^{t_{xT}} \frac{V_s - E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \check{I}e^{\frac{-t}{\tau}}dt$$
$$= \frac{1}{5\text{ms}}\int_{0}^{0.84\text{ms}} 24 - 28.38 \times e^{\frac{-t}{5\text{ms}}}dt = -0.357\text{A}$$

$$\overline{I}_{T2} = \frac{1}{T}\int_{t_{xD}}^{T-t_T} -\frac{E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}e^{\frac{-t}{\tau}}dt$$
$$= \frac{1}{5\text{ms}}\int_{0870\text{ms}}^{3.75\text{ms}} -10 + 11.90 \times e^{\frac{-t}{5\text{ms}}}dt = -1.382\text{A}$$

$$\overline{I}_{D2} = \frac{1}{T}\int_{0}^{t_{xD}} -\frac{E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}e^{\frac{-t}{\tau}}dt$$
$$= \frac{1}{5\text{ms}}\int_{0}^{0.870ms} -10 + 11.90 \times e^{\frac{-t}{5\text{ms}}}dt = 0.160\text{A}$$

Check $\overline{I}_o + \overline{I}_{T1} + \overline{I}_{D1} + \overline{I}_{T2} + \overline{I}_{D2} = -1.5\text{A} + 0.080\text{A} - 0.357\text{A} - 1.382\text{A} + 0.160\text{A} = 0$

vii. The input power, hence output power and rms output current;

$$P_{in} = P_{V_s} = V_s \overline{I}_i = V_s\left(\overline{I}_{T1} + \overline{I}_{D1}\right)$$

$$= 340\text{V}\times\left(0.080\text{A} - 0.357\text{A}\right) = -95.2\text{W}, \text{ (charging } V_s\text{)}$$

$$P_{out} = P_E = E\overline{I}_o = 100\text{V}\times\left(-1.5\text{A}\right) = -150\text{W}, \text{ that is generating } 150\text{W}$$

From

$$V_s I_s = I_{o_{rms}}^2 R + E\overline{I}_o$$

$$I_{o_{rms}} = \sqrt{\frac{P_{out} - P_{in}}{R}} = \sqrt{\frac{150\text{W} - 92.5\text{W}}{10\Omega}} = 2.34\text{A rms}$$

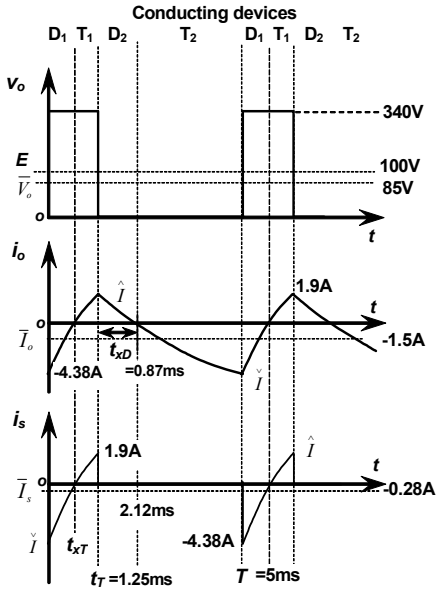


Figure Example 13.5. *Circuit waveforms*

viii. Since the average output current is negative, energy is being transferred from the back emf E to the dc source V_s, the electromagnetic efficiency of conversion is given by

$$\eta = \frac{V_s \overline{I}_i}{E\overline{I}_o} \text{ for } \overline{I}_o < 0$$

$$= \frac{95.2\text{W}}{150\text{W}} = 63.5\%$$

The effective input impedance is

$$Z_{in} = \frac{V_s}{\overline{I}_i} = \frac{V_s}{\overline{I}_{T1} + \overline{I}_{D1}} = \frac{340\text{V}}{0.080\text{A} - 0.357\text{A}} = -1214\Omega$$

ix. The circuit, load, and output voltage and current waveforms are sketched in the figure for example 13.5.

x. Duty cycle δ to result in zero average output current can be determined from the expression for the average output current, equation (13.87), that is

$$\overline{I}_o = \frac{\delta V_s - E}{R} = 0$$

that is

$$\delta = \frac{E}{V_s} = \frac{100\text{V}}{340\text{V}} = 29.4\%$$

xi. As in part x, the average load current equation can be rearranged, this time to give the back emf E that results in zero average load current

$$\overline{I}_o = \frac{\delta V_s - E}{R} = 0$$

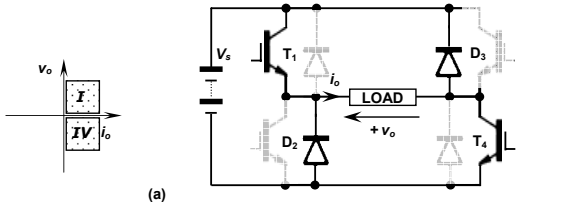
that is

$$E = \delta V_s = ¼\times 340\text{V} = 85\text{V}$$

♣

13.5 Two-quadrant dc chopper - Q 1 and Q IV

The unidirectional current, two-quadrant dc chopper, or asymmetrical half H-bridge shown in figure 13.9a incorporates two switches T_1 and T_4 and two diodes D_2 and D_3. In using switches T_1 and T_4 the chopper operates in the first and fourth quadrants, that is, bi-directional voltage output v_o but unidirectional current, i_o.
The chopper can operate in two quadrants (I and IV), depending on the load and switching sequence. Power can be delivered to the load, or received from the load provided the polarity of the back emf E is reversed. Because of this need to reverse the back emf for regeneration, this chopper is not commonly used in dc machine control. On the other hand, the chopper circuit configuration is commonly used to meet the converter requirements of the switched reluctance machine, which only needs unipolar current to operate. Also see chapter 15.5 for an smps variation.
The asymmetrical half H-bridge chopper has three different output voltage states, where one state has redundancy. Both the output voltage v_o and output current i_o are with reference to the first quadrant arrows in figure 13.9.



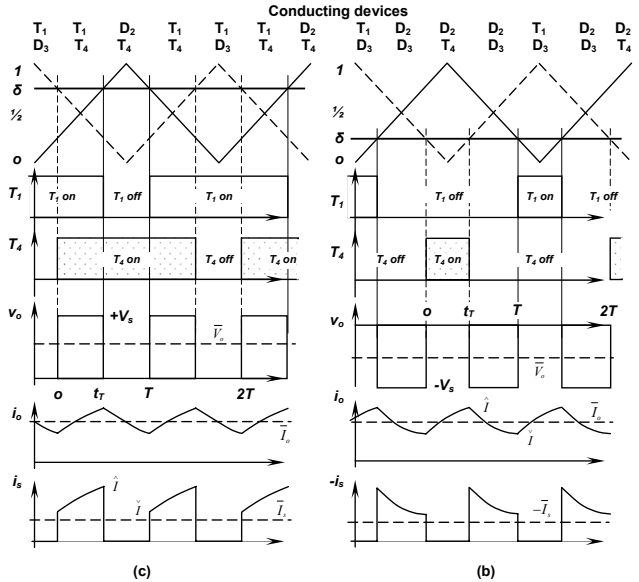


Figure 13.9. *Two-quadrant (I and IV) dc chopper (a) circuit where i_o>0: (b) operation in quadrant IV, regeneration into V_s; and (c) operation in quadrant I.*

State #1

When both switches T_1 and T_4 conduct, the supply V_s is impressed across the load, as shown in figure 13.10a. Energy is drawn from the dc source V_s.

T_1 and T_4 conducting: $v_o = V_s$

State #2

If only one switch is conducting, and therefore also one diode, the output voltage is zero, as shown in figure 13.10b. Either switch (but only one on at any time) can be the on-switch, hence providing redundancy, that is

T_1 and D_3 conducting: $v_o = 0$

T_4 and D_2 conducting: $v_o = 0$

State #3

When both switches are off, the diodes D_2 and D_3 conduct load energy back into the dc source V_s, as in figure 13.10c. The output voltage is $-V_s$, that is

T_1 and T_4 are not conducting: $v_o = -V_s$

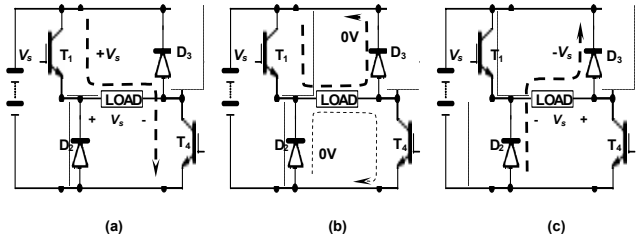


Figure 13.10. *Two-quadrant (I and IV) dc chopper operational current paths: (a) T_1 and T_4 forming a $+V_s$ path; (b) T_1 and D_3 (or T_4 and D_2) forming a zero voltage loop; and (c) D_2 and D_3 creating a $-V_s$ path.*

The two zero output voltage states can most effectively be used if alternated during any switching sequence. In this way, the load switching frequency (load ripple current frequency) is twice the switching frequency of the switches. This reduces the output current ripple for a given switch operating frequency (which minimises the load inductance necessary for continuous load current conduction). Also, by alternating the zero voltage loop, the semiconductor losses are evenly distributed. Specifically, a typical sequence to achieve this feature would be

T_1 and T_4	V_s	
T_1 and D_3	0	
T_1 and T_4	V_s	
T_4 and D_2	0	(not T_1 and D_3 again)
T_1 and T_4	V_s	
T_1 and D_3	0, etc.	

The sequence can also be interleaved in the regeneration mode, when only one switch is on at any instant, as follows

D_2 and D_3	$-V_s$	(that is T_1 and T_4 off)
T_1 and D_3	0	
D_2 and D_3	$-V_s$	
T_4 and D_2	0	(not T_1 and D_3 again)
D_2 and D_3	$-V_s$	
T_1 and D_3	0, etc.	

In switched reluctance motor drive application there may be no alternative to using only $\pm V_s$ control loops without the intermediate zero voltage state.
There are two basic modes of chopper switching operation.

- *Multilevel switching* is when both switches are controlled independently to give all three output voltage states, namely $\pm V_s$ and 0V.
- *Bipolar switching (*or *two level switching)* is when both switches operate in unison, where they turn on together and off together. Only two voltage output states (hence the term bipolar), are possible, $+V_s$ and $-V_s$.

13.5.1 dc chopper:– Q I and Q IV – multilevel output voltage switching

The interleaved zero voltage states can be readily achieved if the control carrier waveforms for the two switches are displaced by 180°, as shown in figure 13.9b and c, for continuous load current. This requirement can be realised if two up-down counters are displaced by 180°, when generating the necessary triangular carriers. As shown in figures 13.9b and c, the switching frequency $1/T_s$ is determine by the triangular wave frequency $1/2T$, whilst advantageously the load experiences twice that frequency, $1/T$, hence the output current has reduced ripple, for a given switch operating frequency.

i. $0 \le \delta \le ½$

It can be seen in figure 13.9b that when $\delta \le ½$ both switches never conduct simultaneously hence the output voltage is either 0 or $-V_s$. Operation is in the fourth quadrant. The average output voltage is load independent and for $0 \le \delta \le ½$, using the waveforms in figure 13.9b, is given by

$$\overline{V}_o = \frac{1}{T}\int_{t_T}^{T} -V_s \, dt = \frac{-V_s}{T}\left(T - t_T\right) = -V_s\left(1 - \frac{t_T}{T}\right) \tag{13.91}$$

Examination of figure 13.9b reveals that the relationship between t_T and δ must produce

$$\text{when } \delta = 0, t_T = T \text{ and } v_o = -V_s$$
$$\text{when } \delta = ½, t_T = 0 \text{ and } v_o = 0$$

that is

$$\delta = ½\frac{t_T}{T}$$

(the period of the carrier, $2T$, is twice the switching period, T) which after substituting for t_T/T in equation (13.91) gives

$$\begin{aligned} \overline{V}_o &= -V_s\left(1 - \frac{t_T}{T}\right) \\ &= -V_s\left(1 - 2\delta\right) = V_s\left(2\delta - 1\right) \quad \text{for} \quad 0 \le \delta \le ½ \end{aligned} \tag{13.92}$$

Operational analysis in the fourth quadrant, $\delta \le ½$, is similar to the analysis for the second-quadrant chopper in figure 13.2b and analysed in section 13.3. Operation is characterised by first shorting the output circuit to boost the current, which on removing the output short, forces current back into the supply V_s, via a freewheel diode. The characteristics of this mode of operation are described by the equations (13.48) to (13.77) for the second-quadrant chopper analysed in 13.3, where the

output current may again be continuous or discontinuous. The current and voltage references are both reversed in translating equations applicable in Q II to Q IV.

ii. $½ \le \delta \le 1$

As shown in figure 13.9c, when $\delta \ge ½$ and operation is in the first quadrant, at least one switch is conducting hence the output voltage is either $+V_s$ or 0. For continuous load current, the average output voltage is load independent and for $½ \le \delta \le 1$ is given by

$$\overline{V}_o = \frac{1}{T}\int_0^{t_T} V_s dt = \frac{V_s}{T} t_T \tag{13.93}$$

Examination of figure 13.9c reveals that the relationship between t_T and δ must produce

$$\text{when } \delta = ½, t_T = 0 \text{ and } v_o = 0$$
$$\text{when } \delta = 1, t_T = T \text{ and } v_o = V_s$$

that is

$$\delta = ½\left(\frac{t_T}{T} + 1\right)$$

which on substituting for t_T/T in equation (13.93) gives

$$\overline{V}_o = V_s\frac{t_T}{T} = V_s\left(2\delta - 1\right) \quad \text{for} \quad ½ \le \delta \le 1 \tag{13.94}$$

Since the average output voltage is the same in each case ($0 \le \delta \le 1$), the output current mean is given by the same expression, namely

$$\overline{I}_o = \frac{\overline{V}_o - E}{R} == \frac{V_s(2\delta - 1) - E}{R} \tag{13.95}$$

Operation in the first quadrant, $\delta \ge ½$, is characterised by the first-quadrant chopper shown in figure 13.2a and considered in section 13.2 along with the equations within that section. The load current can be either continuous, in which case equations (13.6) to (13.23) are valid; or discontinuous in which case equations (13.24) to (13.43) are applicable. Aspects of this mode of switching are extended in section 13.5.3.

In applying the equations for the chopper in section 13.2 for the first-quadrant chopper, and the equations in section 13.3 for the second-quadrant chopper, the duty cycle in each case is replaced by

- 2δ -1 in the case of $\delta \ge ½$ for the first-quadrant chopper and
- 2δ in the case of $\delta \le ½$ for the fourth-quadrant chopper.

This will account for the scaling and offset produced by the triangular carrier signal decoding.

13.5.2 dc chopper: – Q I and Q IV – bipolar voltage switching

When both switches operate in the same state, that is, both switches are on simultaneously or both are off together, operation is termed bipolar or two level switching.

From figure 13.11 the chopper output states are

- T_1 and T_4 on $\quad v_o = V_s$
- T_1 and T_4 off $\quad v_o = -V_s$

From figure 13.11, the average output voltage is

$$\begin{aligned}\overline{V}_o &= \frac{1}{T}\left(\int_0^{t_T} V_s\,dt + \int_{t_T}^{T} -V_s\,dt\right) \\ &= \frac{V_s}{T}\left(t_T - T + t_T\right) = \left(2\delta - 1\right)V_s\end{aligned} \tag{13.96}$$

The rms output voltage is independent of the duty cycle and is V_s.
The output ac ripple voltage is

$$\begin{aligned}V_r &= \sqrt{V_{rms}^2 - V_o^2} \\ &= \sqrt{V_s^2 - \left(2\delta - 1\right)^2 V_s^2} = 2V_s\sqrt{\delta\left(1-\delta\right)}\end{aligned} \tag{13.97}$$

which is a maxima at δ = ½ and a minima for δ = 0 and δ = 1.

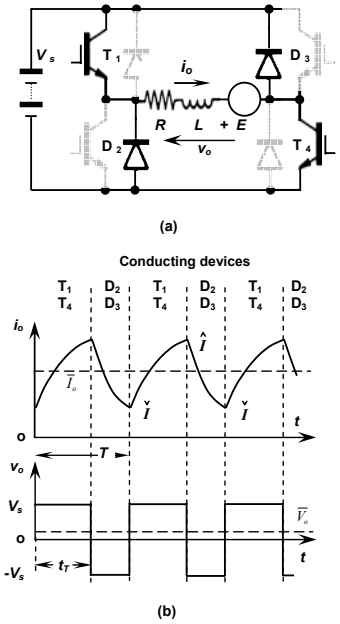


Figure 13.11. *Two-quadrant (I and IV) dc chopper operation in the bipolar output mode: (a) circuit showing load components and (b) chopper output waveforms.*

The output ripple factor is

$$\begin{aligned}RF &= \frac{V_r}{V_o} = \frac{2V_s\sqrt{\delta\left(1-\delta\right)}}{\left(2\delta-1\right)V_s} \\ &= \frac{2\sqrt{\delta\left(1-\delta\right)}}{\left(2\delta-1\right)}\end{aligned} \tag{13.98}$$

Although the average output voltage may reverse, the load current is always positive but can be discontinuous or continuous. Equations describing bipolar output are presented in the next section, 13.5.3, which considers multilevel output voltage switching states.

13.5.3 Multilevel output voltage states, dc chopper

In switched reluctance machine drives it is not uncommon to operate the asymmetrical half H-bridge shown in figure 13.9 such that

- both switches operate in the on-state together to form $+V$ voltage loops;
- switches operate independently the give zero voltage loops; and
- both switches are simultaneously off, forming $-V$ voltage output loops.

The control objective is to generate a current output pulse that tracks a reference shape which starts from zero, rises to maintain a fixed current level, with hysteresis, then the current falls back to zero. The waveform shown in figure 13.12 fulfils this specification.
The switching strategy to produce the current waveform in figure 13.12 aims at:

- For rising current:- use $+V$ loops (and zero volt loops only if necessary)
- For near constant current:- use zero voltage loops (and $\pm V$ loops only if necessary to increase or decrease the current)
- For falling current:- use $-V$ loops (and zero volts loops only if necessary)

Operation is further characterised by continuous load current during the pulse.
Energy is supplied to the load from the source during $+V$ loops, and returned to the supply during $-V$ loop periods.
The chopper output current during each period is described by equations previously derived in this chapter, but reproduced as follows.
In a **positive voltage loop**, (T_1 and T_4 are both on), when $v_o(t)=V_s$ and V_s is impressed across the load, the load circuit condition is described by

$$L\frac{di_o}{dt} + Ri_o + E = V_s$$

which yields

$$i_o\left(t\right) = \frac{V_s - E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \check{I}\,e^{\frac{-t}{\tau}} \qquad \text{for} \quad 0 \le t \le t^+ \tag{13.99}$$

During the first switching cycle the current starts from zero, so $\check{I}$ =0. Otherwise $\check{I}$ is the lower reference, I^-, from the previous cycle.
The current at the end of the period is the reference level I^+, whilst the time to rise to I^+ is derived by equating equation (13.99) to I^+ and solving for time t^+ at the end of the period. Solving $i_o(t^+)= I^+$ for t^+ , gives

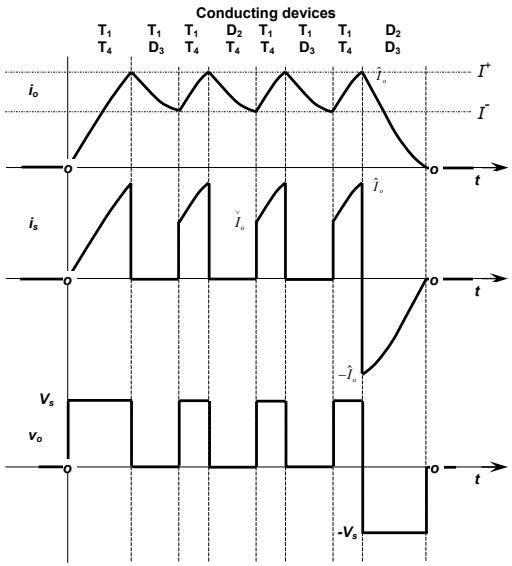


Figure 13.12. *Two-quadrant (I and IV) dc chopper operation in a multilevel output voltage mode.*

$$t^{+} = \tau \ln\left(\frac{V_s - E - \check{I}R}{V_s - E - I^{+}R}\right) \qquad (13.100)$$

In a **zero voltage loop**, when $v_o(t)$=0, such as circuit loops involving T_1 and D_3 (or T_4 and D_2), the circuit equation is given by

$$L\frac{di_o}{dt} + Ri_o + E = 0$$

which gives

$$i_o(t) = -\frac{E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}e^{\frac{-t}{\tau}} \qquad \text{for} \quad 0 \le t \le t^{o} \qquad (13.101)$$

where $\hat{I}$ equals the reference current level, I^{+} from the previous switching period. The current at the end of the period is the reference level I^{-}, whilst the time to fall to I^{-} is given by equating equation (13.101) to I^{-} and solving for time, t^{o} at the end of the period.

$$t^{o} = \tau\, \ell n\left(\frac{E + \hat{I}R}{E + I^{-}R}\right) \qquad (13.102)$$

In a **negative voltage loop**, when both switches T_1 and T_4 are off, the current falls rapidly and the circuit equation, when $v_o(t) = -V_s$, is

$$L\frac{di_o}{dt} + Ri_o + E = -V_s$$

which gives

$$i_o(t) = \frac{-E - V_s}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}e^{\frac{-t}{\tau}} \qquad \text{for} \quad 0 \le t \le t^{-} \qquad (13.103)$$

where $\hat{I}$ equals the reference current level, I^{+} from the previous switching period. The current at the end of the period is I^{-}, whilst the time to reach I^{-} is given by equating equation (13.101) to I^{-} and solving for time t^{-} at the end of the period.

$$t^{-} = \tau\, \ell n\left(\frac{V_s + E + \hat{I}R}{V_s + E + I^{-}R}\right) \qquad (13.104)$$

The same equation is used to determine the time for the final current period when the current decays to zero, whence $I^{-} = 0$.
The characteristics and features of the three output voltage states are illustrated in the following example, 13.6.

Example 13.6: ***Asymmetrical, half H-bridge, dc chopper***

The asymmetrical half H-bridge, dc-to-dc chopper in figure 13.9 feeds an inductive load of 10 ohms resistance, 50mH inductance, and back emf of 55V dc, from a 340V dc source. The chopper output current is controlled in a hysteresis mode within a current band between limits 5A and 10A. Determine the period of the current shape shown in the figure example 13.6,

i. when only $\pm V_s$ loops are used and
ii. when a zero volt loop is used to maintain tracking within the 5A band.

In each case calculate the switching frequency if the current were to be maintained within the hysteresis band for a prolonged period.
How do the on-state losses compare between the two control approaches?

Solution
The main circuit and operating parameters are

- E = 55V and V_s = 340V
- load time constant $\tau = L/R$ = 0.05H/10Ω = 5ms
- I^{+} = 10A and I^{-} = 5A

Examination of the figure shows that only one period of the cycle differs, namely the second period, t_2, where the current is required to fall to the lower hysteresis band level, -5A. The period of the other three regions (t_1, t_3, and t_4) are common and independent of the period of the second region, t_2.
t_1: The first period, the initial rise time, $t^{+} = t_1$ is given by equation (13.100), where I^{+}=10A and $\check{I}$ = 0A.

$$t^{+} = \tau\, \ell n\left(\frac{V_s - E - \check{I}R}{V_s - E - I^{+}R}\right)$$

$$\text{that is} \quad t_1 = 5\text{ms} \times \ell n\left(\frac{340\text{V} - 55\text{V} - 0\text{A}\times 10\Omega}{340\text{V} - 55\text{V} - 10\text{A}\times 10\Omega}\right) = 2.16\text{ms}$$

***t*₃:** In the third period, the current rises from the lower hysteresis band limit of 5A to the upper band limit 10A. The duration of the current increase is given by equation (13.100) again, but with $\check{I} = I^- = 5\text{A}$.

$$t^+ = \tau \ell n\left(\frac{V_s - E - \check{I}R}{V_s - E - I^+R}\right)$$

$$\text{that is} \quad t_3 = 5\text{ms} \times \ell n\left(\frac{340\text{V} - 55\text{V} - 5\text{A}\times 10\Omega}{340\text{V} - 55\text{V} - 10\text{A}\times 10\Omega}\right) = 1.20\text{ms}$$

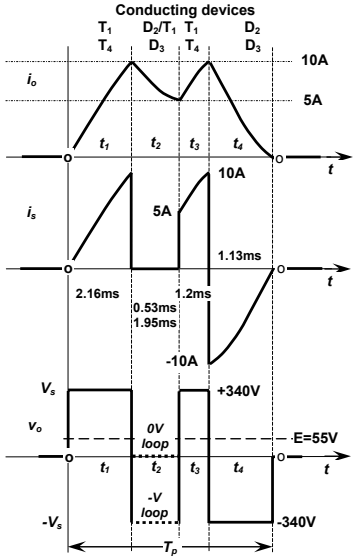


Figure Example 13.6. *Circuit waveforms.*

***t*₄:** The fourth and final period is a negative voltage loop where the current falls from the upper band limit of 10A to I^- which equals zero. From equation (13.104) with $\hat{I} = I^+ = 10\text{A}$ and $I^- = 0\text{A}$

$$t^- = \tau \ell n\left(\frac{V_s + E + \hat{I}R}{V_s + E + I^-R}\right)$$

$$\text{that is} \quad t_4 = 5\text{ms} \times \ell n\left(\frac{340\text{V} + 55\text{V} + 10\text{A}\times 10\Omega}{340\text{V} + 55\text{V} + 0\text{A}\times 10\Omega}\right) = 1.13\text{ms}$$

The current pulse period is given by

$$\begin{aligned} T_p &= t_1 + t_2 + t_3 + t_4 \\ &= 2.16\text{ms} + t_2 + 1.20\text{ms} + 1.13\text{ms} \\ &= 4.49\text{ms} + t_2 \end{aligned}$$

i. ***t*₂:** When only $-V_s$ paths are used to decrease the current, the time t_2 is given by equation (13.104), with $I^- = 5\text{A}$ and $\hat{I} = 10\text{A}$,

$$t^- = \tau \ell n\left(\frac{V_s + E + \hat{I}R}{V_s + E + I^-R}\right)$$

$$\text{that is} \quad t_2 = 5\text{ms} \times \ell n\left(\frac{340\text{V} + 55\text{V} + 10\text{A}\times 10\Omega}{340\text{V} + 55\text{V} + 5\text{A}\times 10\Omega}\right) = 0.53\text{ms}$$

The total period, T_p, of the chopped current pulse when a 0V loop is not used, is

$$\begin{aligned} T_p &= t_1 + t_2 + t_3 + t_4 \\ &= 2.16\text{ms} + 0.53\text{ms} + 1.20\text{ms} + 1.13\text{ms} = 5.02\text{ms} \end{aligned}$$

ii. ***t*₂:** When a zero voltage loop is used to maintain the current within the hysteresis band, the period time t_2 is given by equation (13.102), with $I^- = 5\text{A}$ and $\hat{I} = 10\text{A}$,

$$t^o = \tau \ell n\left(\frac{E + \hat{I}R}{E + I^-R}\right)$$

$$\text{that is} \quad t_2 = 5\text{ms} \times \ell n\left(\frac{55\text{V} + 10\text{A}\times 10\Omega}{55\text{V} + 5\text{A}\times 10\Omega}\right) = 1.95\text{ms}$$

The total period, T_p, of the chopped current pulse when a 0V loop is used, is

$$\begin{aligned} T_p &= t_1 + t_2 + t_3 + t_4 \\ &= 2.16\text{ms} + 1.95\text{ms} + 1.20\text{ms} + 1.13\text{ms} = 6.44\text{ms} \end{aligned}$$

The current falls significantly faster within the hysteresis band if negative voltage loops are employed rather that zero voltage loops, 0.53ms versus 1.95ms.

The switching frequency within the current bounds has a period $t_2 + t_3$, and each case is summarized in the following table.

Using zero voltage current loops reduces the switching frequency of the H-bridge switches by a factor of almost four, for a given peak-to-peak ripple current.

If the on-state voltage drop of the switches and the diodes are similar for the same current level, then the on-state losses are similar, and evenly distributed for both control methods. The on-state losses are similar because each of the three states always involves the same current variation flowing through two semiconductors. The principal difference is in the significant increase in switching losses when only $\pm V$ loops are used (1:3.42).

Table Example 13.6. Switching losses.

Voltage loops	$t_2 + t_3$	Current ripple frequency	Switch frequency	Switch loss ratio
±V	0.53ms+1.20ms = 1.73ms	578Hz	578Hz	$\frac{578}{169} = 3.42$
+V and zero	1.95ms+1.20ms = 3.15ms	317Hz	169Hz	1

♣

13.6 Four-quadrant dc chopper

The four-quadrant H-bridge dc chopper is shown in figure 13.13 where the load current and voltage are referenced with respect to T_1, so that the quadrant of operation with respect to the switch number is persevered.

The H-bridge is a flexible basic configuration where its use to produce single-phase ac is considered in chapter 14.1.1, while its use in smps applications is considered in chapter 15.8.2. It can also be used as a dc chopper for the four-quadrant control of a dc machine.

With the flexibility of four switches, a number of different control methods can be used to produce four-quadrant output voltage and current (bidirectional voltage and current). All practical methods should employ complementary device switching in each leg (either T_1 or T_4 on but not both and either T_2 or T_3 on, but not both) so as to minimise distortion by ensuring current continuity around zero current output.

One control method involves controlling the H-bridge as two virtually independent two-quadrant choppers, with the over-riding restriction that no two switches in the same leg conduct simultaneously. One chopper is formed with T_1 and T_4 grouped with D_2 and D_3, which gives positive current i_o but bidirectional voltage $\pm v_o$ (QI and QIV operation). The second chopper is formed by grouping T_2 and T_3 with D_1 and D_4, which gives negative output current $-i_o$, but bi-direction voltage $\pm v_o$ (QII and QIII operation).

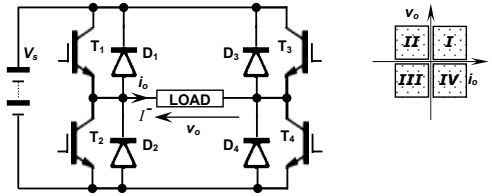


Figure 13.13. *Four-quadrant dc chopper circuit, showing first quadrant i_o and v_o references.*

The second control method is to unify the operation of all four switches within a generalised control algorithm.

With both control methods, the chopper output voltage can be either multilevel or bipolar, depending on whether zero output voltage loops are employed or not. Bipolar output states increase the ripple current magnitude, but do facilitate faster current reversal, without crossover distortion. Operation is independent of the direction of the output current i_o.

Since the output voltage is reversible for each control method, a triangular based modulation control method, as used with the asymmetrical H-bridge dc chopper in figure 13.9, is applicable in each case. Two generalised unified H-bridge control approaches are considered.

13.6.1 Unified four-quadrant dc chopper - bipolar voltage output switching

The simpler output to generate is bipolar output voltages, which use one reference carrier triangle as shown in figure 13.14 parts (c) and (d). The output voltage switches between $+V_s$ and $-V_s$ and the relative duration of each state depends on the magnitude of the modulation index δ.

If $\delta = 0$ then T_1 and T_4 never turn-on since T_2 and T_3 conduct continuously which impresses $-V_s$ across the load.

At the other extreme, **if $\delta = 1$** then T_1 and T_4 are on continuously and V_s is impressed across the load.

If $\delta = ½$ then T_1 and T_4 are turned on for half of the period T, while T_2 and T_3 are on for the remaining half of the period. The output voltage is $-V_s$ for half of the time and $+V_s$ for the remaining half of any period. The average output voltage is therefore zero, but disadvantageously, the output current needlessly ripples about zero (with an average value of zero).

The chopper output voltage is defined in terms of the triangle voltage reference level v_Δ by

- $v_\Delta > \delta$, $v_o = -V_s$
- $v_\Delta < \delta$, $v_o = +V_s$

From figure 13.14c and d, the average output voltage varies linearly with δ such that

$$\begin{aligned}\overline{V}_o &= \frac{1}{T}\left(\int_0^{t_T} +V_s\,dt + \int_{t_T}^{T} -V_s\,dt\right)\\ &= \frac{1}{T}(2t_T - T)V_s = \left(2\frac{t_T}{T} - 1\right)V_s\end{aligned} \qquad (13.105)$$

Examination of figures 13.14c and d reveals that the relationship between t_T and δ must produce

when $\delta = 0, t_T = 0$ and $v_o = -V_s$

when $\delta = ½, t_T = ½T$ and $v_o = 0$

when $\delta = 1, t_T = T$ and $v_o = +V_s$

that is

$$\delta = \frac{t_T}{T}$$

which on substituting for t_T/T in equation (13.105) gives

$$\overline{V}_o = \left(2\frac{t_T}{T} - 1\right) V_s = (2\delta - 1)\, V_s \quad \text{for} \quad 0 \le \delta \le 1 \tag{13.106}$$

The average output voltage can be positive or negative, depending solely on δ. No current discontinuity occurs since the output voltage is never zero. Even when the average is zero, ripple current flows though the load.
The rms output voltage is independent of the duty cycle and is V_s.
The output ac ripple voltage is

$$V_r = \sqrt{V_{rms}^2 - V_o^2} = \sqrt{V_s^2 - (2\delta - 1)V_s^2} = 2V_s\sqrt{\delta(1-\delta)} \tag{13.107}$$

The ac ripple voltage is zero at $\delta = 0$ and $\delta = 1$, when the output voltage is pure dc, namely - V_s or V_s, respectively. The maximum ripple voltage occurs at $\delta = ½$, when $V_r = V_s$.
The output ripple factor is

$$RF = \frac{V_r}{V_o} = \frac{2V_s\sqrt{\delta(1-\delta)}}{(2\delta - 1)V_s} = \frac{2\sqrt{\delta(1-\delta)}}{(2\delta - 1)} \tag{13.108}$$

Circuit operation is characterized by two time domain equations

During the **on-period for T1 and T4**, when $v_o(t)=V_s$

$$L\frac{di_o}{dt} + Ri_o + E = V_s$$

which yields

$$i_o(t) = \frac{V_s - E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \check{I}\, e^{\frac{-t}{\tau}} \qquad \text{for} \quad 0 \le t \le t_T \tag{13.109}$$

During the **on-period for T2 and T3**, when $v_o(t)= - V_s$

$$L\frac{di_o}{dt} + Ri_o + E = -V_s$$

which, after shifting the zero time reference to t_T, gives

$$i_o(t) = -\frac{V_s + E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}\, e^{\frac{-t}{\tau}} \qquad \text{for} \quad 0 \le t \le T - t_T \tag{13.110}$$

The initial conditions $\hat{I}$ and $\check{I}$ are determined by using the usual steady-state boundary condition method.

$$\text{where} \quad \hat{I} = \frac{V_s}{R}\frac{1 - 2e^{\frac{-t_T}{\tau}} + e^{\frac{-T}{\tau}}}{1 - e^{\frac{-T}{\tau}}} - \frac{E}{R} \quad \text{(A)}$$

$$\text{and} \quad \check{I} = \frac{V_s}{R}\frac{2e^{\frac{t_T}{\tau}} - 1 + e^{\frac{-T}{\tau}}}{1 - e^{\frac{-T}{\tau}}} - \frac{E}{R} \quad \text{(A)} \tag{13.111}$$

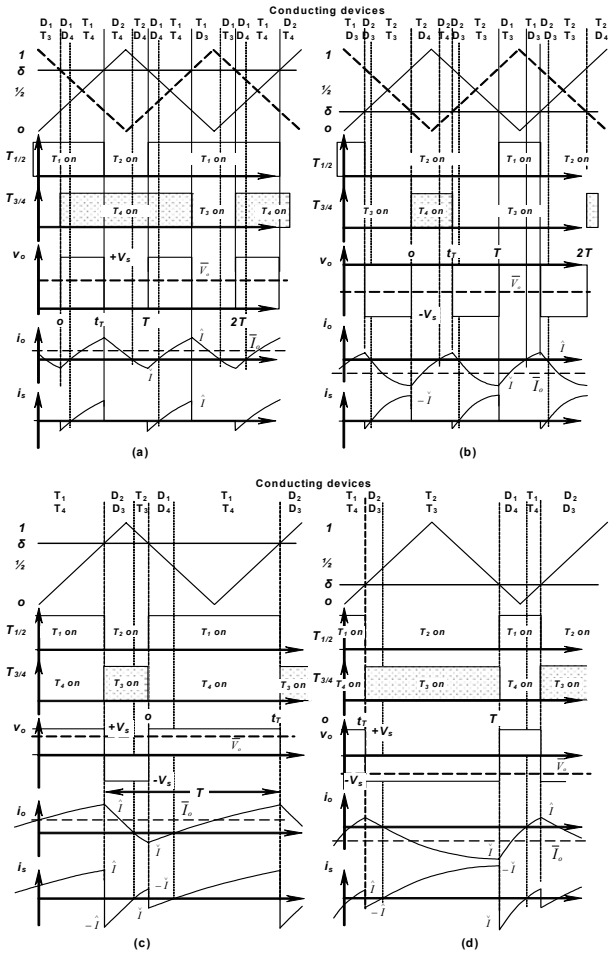


Figure 13.14. *Four-quadrant dc chopper circuit waveforms: multilevel output voltage (a) with $\overline{V}_o > 0$ and $\overline{I}_o > 0$; (b) with $\overline{V}_o < 0$ and $\overline{I}_o < 0$; bipolar output voltage (c) with $\overline{V}_o > 0$ and $\overline{I}_o > 0$; (d) with $\overline{V}_o < 0$ and $\overline{I}_o < 0$.*

The peak-to-peak ripple current is independent of load emf, *E*.
The mean output current is given by

$$\bar{I}_o = \left(\bar{V}_o - E\right)\Big/R = \left((1-2\delta)V_s - E\right)\Big/R \qquad \text{(A)} \qquad (13.112)$$

which can be positive or negative, as seen in figure 13.14c and d.
Figures 13.14c and d show chopper output voltage and current waveforms for conditions of positive average voltage and current in part (c) and negative average voltage and current in part (d). Each part is shown with the current having a positive maximum value and a negative minimum value. Such a load current condition involves activation of all possible chopper conducting paths (sequences) as shown at the top of each part in figure 13.14 and transposed to table 13.3A. The table shows how the conducting device possibilities decrease if the minimum value is positive or the maximum value is negative.

Table 13.3A. Four-quadrant chopper bipolar output voltage states

Conducting devices sequences								
$\bar{V}<0$					$\bar{V}>0$			
T_1	D_2			$\check{I}>0$	T_1	D_2		
T_4	D_3				T_4	D_3		
$\bar{V}<0$					$\bar{V}>0$			
T_1	D_2	T_2	D_1	$\hat{I} > 0$	T_1	D_2	T_2	D_1
T_4	D_3	T_3	D_4	$\hat{I} < 0$	T_4	D_3	T_3	D_4
$\bar{V}<0$					$\bar{V}>0$			
		T_2	D_1	$\hat{I}<0$			T_2	D_1
		T_3	D_4				T_3	D_4

If the minimum output current is positive, that is, $\check{I}$ is positive, then only components for a first and fourth quadrant chopper conduct. Specifically T_2, T_3, D_1, and D_4 do not conduct. Examination of figure 12.14c shows that the output current conduction states are as shown in table 13.3A for $\check{I}>0$.
If the output current never goes positive, that is $\hat{I}$ is negative, then T_1, T_4, D_2, and D_3 do not conduct. The conducting sequence becomes as shown in table 13.3A for $\hat{I}<0$. Because the output is bipolar ($\pm V_s$), the average chopper output voltage, $\bar{V}_o$ does not affect the three possible steady state sequences. Table 13.3A shows that the conducting devices are independent of the average output voltage polarity. That is, the switching states are the same on the left and right sides of table 13.3A.
The transition between these three possible sequences, due to a current level polarity change, is seamless. The only restriction is that devices in any leg do not conduct simultaneously. This is ensured by inserting a brief dead-time between a switch turning off and its leg complement being turned on. That is, dead-time between the switching of the complementary pair (T_1-T_2), and in the other leg the complementary pair is (T_3-T_4).

13.6.2 Unified four-quadrant dc chopper - multilevel voltage output switching

In order to generate three output states, specifically $\pm V_s$ and 0V, two triangular references are used which are displaced by 180° from one another as shown in figure 13.14a and b. One carrier triangle is used to specify the state of T_1 and T_2 (the complement of T_1), while the other carrier triangle specifies the state of switches T_3 and T_4, (the complement of T_3). The output voltage switches between $+V_s$, 0V, and $-V_s$ depending on the modulation index δ, such that $0 \le \delta \le 1$. A characteristic of the output voltage is that, depending on δ, only a maximum of two of the three states appear in the output, in steady-state.
If $\boldsymbol{\delta = 0}$ then T_1 and T_4 never turn-on since T_2 and T_3 conduct continuously which impresses $-V_s$ across the load. As δ increases from zero, the 0V state appears as well as the $-V_s$ state, the later of which decreases in duration as δ increases.
At $\boldsymbol{\delta = ½}$ the output is zero since T_2 and T_3 (or T_1 and T_4) are never on simultaneously to provide a path involving the dc source. The output voltage is formed by alternating 0V loops (T_1 and T_3 on, alternating to T_2 and T_4 on, etc.). The average output voltage is therefore zero. The ripple current for zero voltage output is therefore minimised and independent of any load emf.
At the extreme $\boldsymbol{\delta = 1}$, T_1 and T_4 are on continuously and V_s is impressed across the load. As δ is reduced from one, the 0V state is introduced, progressively lengthening to all of the period as δ reaches ½.
The voltage output in terms of the triangular level v_Δ reference is defined by

For $0 \le \delta < ½$
- $v_\Delta > \delta$, $v_o = -V_s$
- $v_\Delta < \delta$, $v_o = 0$

For $\delta = ½$
- $v_\Delta > \delta$, $v_o = 0$
- $v_\Delta < \delta$, $v_o = 0$

For $½ > \delta \ge 1$
- $v_\Delta > \delta$, $v_o = 0$
- $v_\Delta < \delta$, $v_o = V_s$

From figure 13.14b **for $\boldsymbol{\delta < ½}$**, the average output voltage varies linearly with δ such that

$$\begin{aligned}\bar{V}_o &= \frac{1}{T}\left(\int_0^{t_T} 0\,dt + \int_{t_T}^{T} -V_s\,dt\right) \\ &= \frac{1}{T}\left(t_T - T\right)V_s = \left(\frac{t_T}{T} - 1\right)V_s\end{aligned} \qquad (13.113)$$

Examination of figure 13.14b reveals that the relationship between t_T and δ must produce

$$\text{when } \delta = 0,\ t_T = 0 \text{ and } v_o = -V_s$$
$$\text{when } \delta = ½,\ t_T = T \text{ and } v_o = 0$$

that is

$$\delta = ½\frac{t_T}{T}$$

which on substituting for t_T/T in equation (13.113) gives

$$\begin{aligned}\overline{V}_o &= \left(\frac{t_T}{T}-1\right)V_s \\ &= (2\delta-1)\,V_s\end{aligned} \qquad (13.114)$$

From figure 13.14a **for $\delta > ½$**, the average output voltage varies linearly with δ such that

$$\begin{aligned}\overline{V}_o &= \frac{1}{T}\left(\int_0^{t_T} V_s\,dt + \int_{t_T}^{T} 0\,dt\right) \\ &= V_s\frac{t_T}{T}\end{aligned} \qquad (13.115)$$

Examination of figure 13.14a reveals that the relationship between t_T and δ must produce

$$\text{when } \delta = ½, t_T = 0 \text{ and } v_o = 0$$
$$\text{when } \delta = 1, t_T = T \text{ and } v_o = V_s$$

that is

$$\delta = ½\left(\frac{t_T}{T}+1\right)$$

which on substituting for t_T/T in equation (13.115) gives

$$\overline{V}_o = (2\delta-1)V_s \qquad (13.116)$$

Since the same expression results for $\delta \le ½$ with bipolar switching, the average output current is the same for the range $0 \le \delta \le 1$, that is

$$\overline{I}_o = \left(\overline{V}_o - E\right)\Big/R = \left((2\delta-1)V_s - E\right)\Big/R \qquad \text{(A)} \qquad (13.117)$$

which can be positive or negative, depending on δ and the load emf, E.
Although the average voltage equations of the multilevel and bipolar controlled dc choppers are the same, the rms voltage and ripple voltage differ, as does the peak-to-peak output ripple current. Unlike the bipolar controlled chopper, the rms voltage for the multilevel controlled chopper is not a single continuous function.
For $\delta \le ½$ the rms load voltage is

$$\begin{aligned}V_{rms} &= \left[\frac{1}{T}\int_{t_T}^{T}(V_s)^2\,dt\right]^{½} \\ &= \sqrt{1-2\delta}\;\;V_s\end{aligned} \qquad (13.118)$$

The output ac ripple voltage is

$$\begin{aligned}V_r &= \sqrt{V_{rms}^2 - V_o^2} \\ &= \sqrt{\left(\sqrt{1-2\delta}\;V_s\right)^2 - \left((2\delta-1)V_s\right)^2} \\ &= \sqrt{2}\;V_s\sqrt{\delta(1-2\delta)}\end{aligned} \qquad (13.119)$$

The minimum rms ripple voltage in the output occurs when δ=½ or 0 giving an rms ripple voltage of zero, since the average is a dc value at the extremes (0V and -V_s respectively). The maximum ripple occurs at δ = ¼, when V_r = ½V_s, which is the same as when δ = ¾, (but half that obtained with the bipolar output control method, V_s).

For $\delta \ge ½$ the rms load voltage is

$$\begin{aligned}V_{rms} &= \left[\frac{1}{T}\int_{t_T}^{T}(-V_s)^2\,dt\right]^{½} \\ &= \sqrt{2\delta-1}\;\;V_s\end{aligned} \qquad (13.120)$$

The output ac ripple voltage is

$$\begin{aligned}V_r &= \sqrt{V_{rms}^2 - V_o^2} \\ &= \sqrt{\left(\sqrt{2\delta-1}\;V_s\right)^2 - \left((2\delta-1)V_s\right)^2} \\ &= \sqrt{2}\;V_s\sqrt{(2\delta-1)(1-\delta)}\end{aligned} \qquad (13.121)$$

The minimum rms ripple voltage in the output occurs when δ=½ or 1 giving an rms ripple voltage of zero, since the average is a dc value at the extremes (0V and V_s respectively). The maximum ripple occurs at δ=¾, when V_r =½V_s, which is half that obtained with the bipolar output control method.
The output voltage ripple factor is

$$\begin{aligned}RF &= \frac{V_r}{\overline{V}_o} = \sqrt{\left(\frac{V_{rms}}{\overline{V}_o}\right)^2 - 1} \\ &= \sqrt{2\times\frac{1-\delta}{2\delta-1}}\end{aligned} \qquad (13.122)$$

Thus as the duty cycle $\delta \to 1$, the ripple factor tends to zero, consistent with the output being dc, that is V_r=0. The ripple factor is undefined when the average output voltage is zero, at δ = ½.
Circuit operation is characterized by three time domain equations.
During the **on-period for T1 and T4**, when $v_o(t)=V_s$

$$L\frac{di_o}{dt} + R\,i_o + E = V_s$$

which yields

$$i_o(t) = \frac{V_s - E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \check{I}\,e^{\frac{-t}{\tau}} \qquad \text{for} \quad 0 \le t \le t_T \text{ and } \delta \ge ½ \qquad (13.123)$$

During the **on-period for T2 and T3**, when $v_o(t)$=- V_s

$$L\frac{di_o}{dt} + R\,i_o + E = -V_s$$

which, after shifting the zero time reference to t_T, gives

$$i_o(t) = -\frac{V_s + E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}\,e^{\frac{-t}{\tau}} \qquad \text{for} \quad 0 \le t \le T - t_T \text{ and } \delta \le ½ \qquad (13.124)$$

The third equation is for a zero voltage loop.
During the **switch off-period**, when $v_o(t)$=0

$$L\frac{di_o}{dt} + R\,i_o + E = 0$$

which, after shifting the zero time reference, in figure 13.14a or b, gives

$$i_o(t) = -\frac{E}{R}\left(1 - e^{\frac{-t}{\tau}}\right) + \hat{I}\, e^{\frac{-t}{\tau}}$$

$$0 \le t \le t_T \text{ and } \delta \le ½ \qquad (13.125)$$

$$0 \le t \le T - t_T \text{ and } \delta \ge ½$$

The initial conditions $\hat{I}$ and $\check{I}$ are determined by using the usual steady-state boundary condition method and are dependent on the transition states. For example, for continuous steady-state transitions between $+V_s$ loops and 0V loops, the boundary conditions are given by

$$\text{where} \quad \hat{I} = \frac{V_s}{R}\frac{1 - e^{\frac{-t_T}{\tau}}}{1 - e^{\frac{-T}{\tau}}} - \frac{E}{R} \quad \text{(A)} \qquad (13.126)$$

$$\text{and} \quad \check{I} = \frac{V_s}{R}\frac{e^{\frac{t_T}{\tau}} - 1}{e^{\frac{T}{\tau}} - 1} - \frac{E}{R} \quad \text{(A)}$$

Figures 13.14a and b show output voltage and current waveforms for conditions of positive average voltage and current in part (a) and negative average voltage and current in part (b). Each part is shown with the current having a positive maximum value and a negative minimum value. Such a load current condition involves the activation of all possible chopper conducting paths, which are shown at the top of each part in figure 13.14 and transposed to table 13.3B. The conducting device possibilities decrease if the minimum value is positive or the maximum value is negative.

Table 13.3B. A Four-quadrant chopper multilevel output voltage states

Conducting devices sequences																
$\overline{V}>0$									$\overline{V}<0$							
		T_1	D_2			T_1	T_1	$\check{I}>0$	T_1	D_2			D_2	D_2		
		T_4	T_4			T_4	D_3		D_3	D_3			T_4	D_3		
$\overline{V}>0$									$\overline{V}<0$							
D_1	D_1	T_1	D_2	T_2	D_1	T_1	T_1	$\check{I}<0$	T_1	D_2	T_2	T_2	D_2	D_2	T_2	D_1
T_3	D_4	T_4	T_4	D_4	D_4	T_4	D_3	$\hat{I}>0$	D_3	D_3	T_3	D_4	T_4	D_3	T_3	T_3
$\overline{V}>0$									$\overline{V}<0$							
D_1	D_1			T_2	D_1			$\hat{I}<0$			T_2	T_2			T_2	D_1
T_3	D_4			D_4	D_4						T_3	D_4			T_3	T_3

If the minimum output current is positive, that is, $\check{I}$ is positive, then only components for a first and fourth quadrant chopper conduct. Specifically T_2, T_3, D_1, and D_4 do not conduct, thus do not appear in the output sequence. Examination of figure 12.14c shows that the output current conduction states are as shown in table 13.3B for $\check{I} > 0$.

If the output current never goes positive, that is $\hat{I}$ is negative, then T_1, T_4, D_2, and D_3 do not conduct, thus do not appear in the output device sequence. The conducting sequence is as shown in table 13.3B for $\hat{I} < 0$.
Unlike the bipolar control method, the output sequence is affected by the average output voltage level, as well as the polarity of the output current swing. The transition between the six possible sequences due to load voltage and current polarity changes, is seamless. The only restriction is that devices in any leg do not conduct simultaneously. This is ensured by inserting a brief dead-time between a switch turning off and its leg complement being turned on.

Example 13.7: ***Four-quadrant dc chopper***

The H-bridge, dc-to-dc chopper in figure 13.13 feeds an inductive load of 10 ohms resistance, 50mH inductance, and back emf of 55V dc, from a 340V dc source. If the chopper is operated with a 200Hz multilevel carrier as in figure 13.14 a and b, with a modulation depth of $\delta = ¼$, determine:

i. the average output voltage and switch T_1 on-time
ii. the rms output voltage and ac ripple voltage
iii. the average output current, hence quadrant of operation
iv. the electromagnetic power being extracted from the back emf *E*.

If the mean load current is to be halved, what is

v. the modulation depth, *δ*, requirement
vi. the average output voltage and the corresponding switch T_1 on-time
vii. the electromagnetic power being extracted from the back emf *E*?

Solution

The main circuit and operating parameters are

- modulation depth $\delta = ¼$
- period $T_{carrier} = 1/f_{carrier} = 1/200\text{Hz} = 5\text{ms}$
- E=55V and V_s=340V dc
- load time constant $\tau = L/R = 0.05\text{H}/10\Omega = 5\text{ms}$

i. The average output voltage is given by equation (13.114), and for $\delta < ½$,

$$\overline{V}_o = \left(\frac{t_T}{T} - 1\right)V_s = (2\delta - 1)V_s$$

$$= 340\text{V} \times (2 \times ¼ - 1) = -170\text{V}$$

where

$$t_T = 2\delta T = 2 \times ¼ \times (½ \times 5\text{ms}) = 1.25\text{ms}$$

Figure 13.14 reveals that the carrier frequency is half the switching frequency, thus the 5ms in the above equation has been halved. The switches T_1 and T_4 are turned on for 1.25ms, while T_2 and T_3 are subsequently turned on for 3.75ms.

ii. The rms load voltage, from equation (13.118), is

$$V_{rms} = \sqrt{1-2\delta}\ V_s$$
$$= 340\text{V}\times\sqrt{1 - 2\times¼} = 240\text{V rms}$$

From equation (13.119), the output ac ripple voltage is

$$V_r = \sqrt{2}\,V_s\sqrt{\delta(1-2\delta)}$$
$$=\sqrt{2}\times 340\text{V}\times\sqrt{¼\times(1 - 2\times¼)} = 170\text{V ac}$$

iii. The average output current is given by equation (13.117)

$$\bar{I}_o = \frac{\bar{V}_o - E}{R} = \frac{(2\delta-1)V_s - E}{R}$$
$$= \frac{340\text{V}\times(2\times¼ - 1) - 55\text{V}}{10\Omega} = -22.5\text{A}$$

Since both the average output current and voltage are negative (-170V and -22.5A) the chopper with a modulation depth of $\delta = ¼$, is operating in the third quadrant.

iv. The electromagnetic power developed by the back emf E is given by

$$P_E = E\bar{I}_o = 55\text{V}\times(-22.5\text{A}) = -1237.5\text{W}$$

v. The average output current is given by

$$\bar{I}_o = \left.(\bar{V}_o - E)\right/R = \left.((2\delta-1)V_s - E)\right/R$$

when the mean current is -11.25A, $\delta = 0.415$, as derived in part vi.

vi. Then, if the average current is halved to -11.25A

$$\bar{V}_o = E + \bar{I}_o R$$
$$=55\text{V} - 11.25\text{A}\times 10\Omega = -57.5\text{V}$$

The average output voltage rearranged in terms of the modulation depth δ gives

$$\delta = ½\left(1+\frac{\bar{V}_o}{V_s}\right)$$
$$= ½\times\left(1 + \frac{-57.5\text{V}}{340\text{V}}\right) = 0.415$$

The switch on-time when $\delta < ½$ is given by

$$t_T = 2\delta T = 2\times 0.415\times(½\times 5\text{ms}) = 2.07\text{ms}$$

From figure 13.14b both T_1 and T_4 are turned on for 2.07ms, although, from table 13.3B, for negative load current, $\bar{I}_o = -11.25\text{A}$, the parallel connected freewheel diodes D_1 and D_4 conduct alternately, rather than the switches (assuming $\hat{I}_o < 0$). The switches T_1 and T_4 are turned on for 1.25ms, while T_2 and T_3 are subsequently turned on for 2.93ms.

vii. The electromagnetic power developed by the back emf E is halved and is given by

$$P_E = E\bar{I}_o = 55\text{V}\times(-11.25\text{A}) = -618.75\text{W}$$

♣

Reading list

Dewan, S. B. and Straughen, A., *Power Semiconductor Circuits,*
John Wiley and Sons, New York, 1975.

Dubey, G.K., *Power Semiconductor Controlled Drives,*
Prentice-Hall International, 1989.

Mohan, N., Undeland, T. M., and Robbins, W.P., *Power Electronics: Converters, Applications and Design,*
John Wiley and Sons, New York, 2003.

Problems

13.1. The dc GTO thyristor chopper shown in figure 13.lc operates at 1 kHz and supplies a series 5 Ω and 10 mH load from an 84 V dc battery source. Derive general expressions for the mean load voltage and current, and the load rms voltage at an on-time duty cycle of δ. Evaluate these parameters for $\delta = 0.25$.
[21 V, 4.2 A; 42 V]

13.2. The dc chopper in figure 13.lc controls a load of $R = 10\ \Omega$, $L = 10$ mH and 40 V battery. The supply is 340 V dc and the chopping frequency is 5 kHz. Calculate (a) the peak-to-peak load ripple current, (b) the average load current, (c) the rms load current, (d) the effective input resistance, and (e) the rms switch current.

14

Power Inverters

Inversion is the conversion of dc power to ac power at a desired output voltage or current and frequency. A static inverter circuit performs this transformation.
The terms voltage-fed and current-fed are used in connection with inverter circuits.
A *voltage-fed inverter* is one in which the dc input voltage is essentially constant and independent of the load current drawn. The inverter specifies the load voltage while the drawn current shape is dictated by the load.
A *current-fed inverter* (or current source inverter) is one in which the source, hence the load current is predetermined and the load impedance determines the output voltage. The supply current cannot change quickly. This is achieved by series dc supply inductance which prevents sudden changes in current. The load current magnitude is controlled by varying the input dc voltage to the large inductance, hence inverter response to load changes is slow. Being a current source, the inverter can survive an output short circuit thereby offering fault ride-through properties.
Voltage control may be required to maintain a fixed output voltage when the dc input voltage regulation is poor, or to control power to a load. The inverter and its output can be single-phase, three-phase or multi-phase. Variable output frequency may be required for ac motor speed control where, in conjunction with voltage or current control, constant motor flux can be maintained.
Inverter output waveforms are usually rectilinear in nature and as such contain harmonics which may lead to reduced load efficiency and performance. Load harmonic reduction can be achieved by either filtering, selected harmonic-reduction chopping or pulse-width modulation.
The quality of an inverter output is normally evaluated in terms of its harmonic factor, ρ, distortion factor, μ, and total harmonic distortion, *thd*. In section 12.6.2 these first two factors were defined in terms of the supply current. For inverters the factors are redefined in terms of the output voltage harmonics as follows

$$\rho_n = \left|\frac{V_n}{V_1}\right| = n\mu_n \qquad n > 1 \tag{14.1}$$

The distortion factor for an individual harmonic is

$$\mu_n = \left|\frac{V_n}{nV_1}\right| = \frac{\rho_n}{n} \tag{14.2}$$

$$thd = \sqrt{\left[\sum_{n\geq 2}^{\infty}\left(\frac{V_n}{n}\right)^2\right]} \Big/ V_1 = \sqrt{\sum_{n\geq 2}^{\infty}\mu_n^2} = \sqrt{\sum_{n\geq 2}^{\infty}\left(\frac{\rho_n}{n}\right)^2} \tag{14.3}$$

The factor V_n/n is used since the harmonic currents produced in an inductive load attenuate with frequency. The harmonic currents produce unwanted heating and torque oscillations in ac motors, although such harmonic currents are not a drawback to the power delivered to a resistive heating load.

14.1 dc-to-ac voltage-fed inverter bridge topologies

14.1.1 Single-phase voltage-fed inverter bridge

Figure 14.la shows an H-bridge inverter for producing an ac voltage and employing switches which may be transistors (MOSFET or IGBT), or at high powers, thyristors (GTO or CGT). Device conduction patterns are also shown in figures 14.lb and c. With inductive loads (not purely resistive), stored energy at turn-off is fed through the bridge reactive feedback or freewheel diodes D_1 to D_4. These four diodes clamp the load voltage to within the dc supply rails (0 to V_s).

14.1.1i - *Square-wave output*
Figure 14.lb shows waveforms for a square-wave output ($2t_1=t_2$) where each device is turned on as appropriate for 180°, (that is π) of the output voltage cycle (state sequence 10, 01, 10, ..). The load current i_L grows exponentially through T_1 and T_2 (state 10) according to

$$V_s = L\frac{di_L}{dt} + i_L R \qquad \text{(V)} \tag{14.4}$$

When T_1 and T_2 are turned off, T_3 and T_4 are turned on (state 01), thereby reversing the load voltage. Because of the inductive nature of the load, the load current cannot reverse and load reactive energy flows back into the supply via diodes D_3 and D_4 (which are in parallel with T_3 and T_4 respectively) according to

$$-V_s = L\frac{di_L}{dt} + i_L R \qquad \text{(V)} \tag{14.5}$$

The load current falls exponentially and at zero, T_3 and T_4 become forward-biased and conduct load current, thereby feeding power to the load.
The output voltage is a square wave of magnitude $\pm V_s$ and has an rms value of V_s.
For a simple *R-L* load, with time constant $\tau = L/R$, during the first cycle with no initial load current, solving equation (14.4) yields a load current

$$i_L(t) = \frac{V_s}{R}\left(1 - e^{\frac{-t}{\tau}}\right) \qquad \text{(A)} \tag{14.6}$$

Under steady-state load conditions, the initial current is $\breve{I}$ as shown in figure 14.lb, and equation (14.4) yields

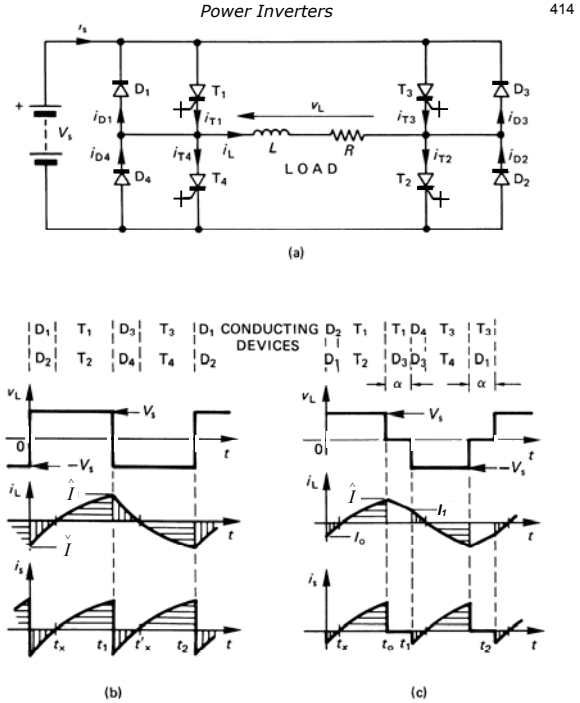


Figure 14.1. *GCT thyristor single-phase bridge inverter: (a) circuit diagram; (b) square-wave output voltage; and (c) quasi-square-wave output voltage.*

$$i_L(t) = \frac{V_s}{R} - \left(\frac{V_s}{R} - \check{I}\right)e^{\frac{-t}{\tau}} \quad \text{(A)} \qquad 0 \le t \le t_1 \quad \text{(s)} \tag{14.7}$$

for $v_L = V_s$ (V)

$\check{I} \le 0$ (A)

During the second half-cycle ($t_1 \le t \le t_2$) when the supply is effectively reversed across the load, equation (14.5) yields

$$i_L(t) = -\frac{V_s}{R} + \left(\frac{V_s}{R} + \hat{I}\right)e^{\frac{-t}{\tau}} \quad \text{(A)} \qquad 0 \le t \le t_2 - t_1 \quad \text{(s)} \tag{14.8}$$

for $v_L = -V_s$ (V)

$\hat{I} \ge 0$ (A)

A new time axis has been used in equation (14.8) starting at $t = t_1$ in figure 14.lb. Since $\hat{I} = -\check{I}$, the initial steady-state current $\hat{I}$ can be found from equation (14.7) when, at $t = t_1$, $i_L = \hat{I}$ yielding

$$\hat{I} = \frac{V_s}{R}\frac{1 - e^{\frac{-t_1}{\tau}}}{1 + e^{\frac{-t_1}{\tau}}} = \frac{V_s}{R}\tanh\left(\frac{t_1}{2\tau}\right) \quad \text{(A)} \tag{14.9}$$

The zero current cross-over point t_x, shown on figure 14.1b, can be found by solving equation (14.7) for t when $i_L = 0$, which yields

$$t_x = \tau\,\ell n\left(1 - \frac{\check{I}R}{V_s}\right) = \tau\,\ell n\left(1 + \frac{\hat{I}R}{V_s}\right) \quad \text{(s)} \tag{14.10}$$

The average thyristor current, $\bar{I}_{TH}$, average diode current, $\bar{I}_D$, and mean source current, $\bar{I}_s$ can be found by integration of the load current over the appropriated bounds.

$$\bar{I}_T = \frac{1}{t_2}\int_{t_x}^{t_1} i_L(t)\,dt = \frac{1}{t_2}\left[\frac{V_s}{R}(t_1 - t_o) + \tau\left(\frac{V_s}{R} + \hat{I}\right)\left(e^{\frac{-t_1}{\tau}} - e^{\frac{-t_o}{\tau}}\right)\right] \tag{14.11}$$

where i_L is given by equation (14.7) and

$$\bar{I}_D = \frac{1}{t_2}\int_0^{t_x} -i_L(t)\,dt = \frac{1}{t_2}\left[-\frac{V_s}{R}t_x - \tau\left(\frac{V_s}{R} + \hat{I}\right)\left(e^{\frac{-t_x}{\tau}} - 1\right)\right] \tag{14.12}$$

where i_L is given by equation (14.8)

Inspection of the source current waveform in figure 14.1b shows that the average source current is related to the average semiconductor device currents by

$$\bar{I}_s = 2\left(\bar{I}_{TH} - \bar{I}_D\right) = \frac{1}{t_2}\left[\frac{V_s}{R}t_1 + \tau\left(\frac{V_s}{R} + \hat{I}\right)\left(e^{\frac{-t_1}{\tau}} - 1\right)\right] \tag{14.13}$$

The steady-state mean power delivered by the dc supply and absorbed by the resistive load component is given by

$$P_L = \frac{1}{t_1}\int_0^{t_1} V_s\, i_L(t)\ dt \ = \ V_s \bar{I}_s \qquad \text{(W)} \qquad (14.14)$$

where $i_L(t)$ is given by equation (14.7).
The rms output voltage is V_s and the output fundamental frequency f_o is $f_o = 1/t_1 = 1/t_2$.
The instantaneous output voltage expressed as a Fourier series is given by

$$V_L = \frac{4}{\pi} V_s \sum_{n\ odd}^{\infty} \frac{1}{n} \sin n\omega t \qquad \text{(V)} \qquad (14.15)$$

and for $n = 1$ the output rms fundamental voltage v_{o1} is

$$v_{o1} = \frac{2\sqrt{2}}{\pi} V_s = 0.90 V_s \qquad \text{(V)} \qquad (14.16)$$

The load current can be expressed in terms of the Fourier voltage waveform series, that is

$$i_L(\omega t) = \frac{4}{\pi} V_s \sum_{n=1,3,5}^{\infty} \frac{1}{nZ_n} \sin\left(n\omega t - \phi_n\right) \qquad (14.17)$$

where $Z_n = \sqrt{R^2 + (n\omega L)^2}$

$\phi_n = \tan^{-1} n\omega L / R$

14.1.1ii - *Quasi-square-wave output*
The rms output voltage can be varied by producing a quasi-square output voltage ($2t_1=t_2$, $t_0<t_1$) as shown in figure 14.1c. After T_1 and T_2 have been turned on (state 10), at the angle π-α one device is turned off. If T_1 is turned off, the load current slowly freewheels through T_2 and D_4 (state 00) in a zero voltage loop according to

$$0 = L\frac{di_L}{dt} + i_L R \qquad \text{(V)} \qquad (14.18)$$

When T_2 is turned off and T_4 and T_3 turned on (state 01), the remaining load current rapidly reduces to zero through diodes D_3 and D_4. When the load current reaches zero, T_3 and T_4 become forward biased and the output current reverses through T_3 and T_4.
The output voltage shown in figure 14.lc consists of a sequence of non-zero voltages $\pm V_s$, alternated with zero output voltage periods. During the zero output period a diode and switch conduct, firstly T_1 and D_3 in the first period, and T_3 and D_1 in the second zero output period. In each case, a *zero voltage loop* is formed by a switch, diode, and the load. The next two zero output sequences would be T_2 and D_4 then T_4 and D_2, forming *alternating zero voltage loops* (sequence 10, 00, 01, 11, 10, ..) rather than repeating a continuous T_1 and D_3 then T_3 and D_1 sequence of zero voltage loops (sequence 10, 11, 01, 11, 10, .. or sequence 10, 00, 01, 00, 10, ..). By alternating the zero voltage loops (between states 00 and 11), losses are uniformly distributed between the semiconductors, device switching frequency is half that experienced by the load, and a finer output voltage resolution is achievable.
With reference to figure 14.lc, the load current i_L for an applied quasi square-wave voltage is defined as follows.

(i) $v_L > 0$

$$i_{L_I}(t) = \frac{V_s}{R} - \left(\frac{V_s}{R} - I_o\right) e^{\frac{-t}{\tau}} \qquad 0 \le t \le t_o \qquad (14.19)$$

for $I_o \le 0$ (A)

(ii) $v_L = 0$

$$i_{L_{II}}(t) = \hat{I}\, e^{\frac{-t}{\tau}} \qquad 0 \le t \le t_1 - t_o \qquad (14.20)$$

for $\hat{I} \ge 0$ (A)

(iii) $v_L < 0$

$$i_L(t) = -\frac{V_s}{R} + \left(\frac{V_s}{R} + I_1\right) e^{\frac{-t}{\tau}} = -i_{L_I}(t) \qquad 0 \le t \le t_o \qquad (14.21)$$

for $I_1 \ge 0$ (A)

The currents I_o , $\hat{I}$, and I_1 are given by

$$I_o = -\frac{V_s}{R}\ \frac{e^{\frac{-t_1+t_o}{\tau}} - e^{\frac{-t_1}{\tau}}}{1+e^{\frac{-t_1}{\tau}}} \qquad \text{(A)} \qquad (14.22)$$

$$\hat{I} = \frac{V_s}{R}\ \frac{1-e^{\frac{t_o}{\tau}}}{1+e^{\frac{-t_1}{\tau}}} \qquad \text{(A)} \qquad (14.23)$$

$$I_1 = -I_o \qquad \text{(A)} \qquad (14.24)$$

The zero current cross-over instant, t_x, shown in figure 14.1c, is found by solving equation (14.19) for t when i_L equals zero current.

$$t_x = \tau\, \ell n\left(1 - \frac{I_o R}{V_s}\right) \qquad (14.25)$$

The average thyristor current, $\bar{I}_{TH}$, average diode current, $\bar{I}_D$, and mean source current, $\bar{I}_s$ can be found by integration of the load current over the appropriated bounds (assuming alternating zero volt loops).

$$\bar{I}_T = \frac{1}{t_2}\int_{t_x}^{t_1} i_{L_I}(t)\,dt + \frac{1}{2t_2}\int_0^{t_1-t_o} i_{L_{II}}(t)\,dt \qquad (14.26)$$

where i_L is given by equations (14.19) and (14.20) for the respective integrals, and

$$\bar{I}_D = \frac{1}{t_2}\int_0^{t_x} -i_{L_I}(t)\,dt + \frac{1}{2t_2}\int_0^{t_1-t_o} i_{L_{II}}(t)\,dt \qquad (14.27)$$

where i_L is given by equations (14.19) and (14.20) for the respective integrals.
Inspection of the source current waveform in figure 14.1b shows that the average source current is related to the average semiconductor device currents by

$$\bar{I}_s = \frac{1}{t_1}\int_0^{to} i_{L_I}(t)dt = 2\left(\bar{I}_{TH} - \bar{I}_D\right) \qquad (14.28)$$

The steady-state mean load and source powers are

$$P_L = \frac{1}{t_1}\int_0^{t_o} V_s\, i_L(t)\ dt \ = \ V_s \bar{I}_s \qquad \text{(W)} \qquad (14.29)$$

where $i_L(t)$ is given by equation (14.19).
The variable rms output voltage is

$$v_{rms} = \sqrt{\frac{1}{t_1}\int_0^{t_1} V_s^2\,dt} = \sqrt{1-\alpha/\pi}\;V_s \qquad (14.30)$$

and the output fundamental frequency f_o is $f_o = 1/t_2$.

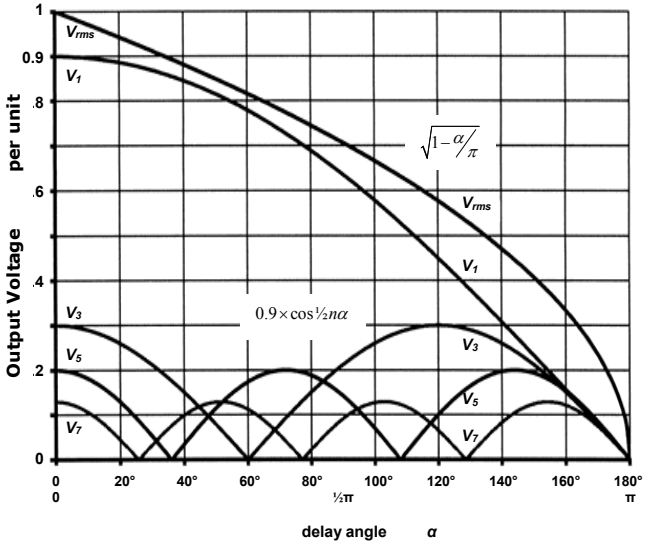


Figure 14.2a. *Full bridge inverter output voltage harmonics normalised with respect to square wave rms output voltage, V_{rms}=V_s.*

The output voltage V_L in its Fourier coefficient series form is given by

$$V_L = \frac{4}{\pi} V_s \sum_{n\,odd}^{\infty} \frac{\cos ½n\alpha}{n} \sin n\omega t \qquad \text{(V)} \qquad (14.31)$$

and for n = 1, the rms fundamental of the output voltage v_{o1} is given by

$$v_{o1} = \frac{2\sqrt{2}}{\pi} V_s \cos ½\alpha = 0.90 \times V_s \times \cos ½\alpha \qquad \text{(V)} \qquad (14.32)$$

The characteristics of these load voltage harmonics are shown in figure 14.2a.
The load current can be expressed in terms of the Fourier voltage waveform series, that is

$$i_L(\omega t) = \frac{4}{\pi} V_s \sum_{n=1,3,..}^{\infty} \frac{\cos ½n\alpha}{nZ_n} \sin\left(n\omega t - \phi_n\right) \qquad (14.33)$$

where $Z_n = \sqrt{R^2 + (n\omega L)^2}$

$\phi_n = \tan^{-1} n\omega L/R$

A variation of the basic four-switch dc to ac single-phase H-bridge is the half-bridge version where two series switches (one pole or leg) and diodes are replaced by a split two-capacitor source, as shown in figure 14.2a. This reduces the number of semiconductors and gate circuit requirements, but at the expense of halving the maximum output voltage. Example 14.3 illustrates the half-bridge and its essential features. Behaviour characteristics are as for the full-bridge, square-wave, single-phase inverter but V_s is replaced by ½V_s in the appropriate equations. Only a square-wave output voltage can be obtained. Since zero volt loops cannot be created, no rms voltage control is possible. The rms output voltage is ½V_s.

Example 14.1a: ***Single-phase H-bridge with an L-R load***

A single-phase H-bridge inverter, as shown in figure 14.la, supplies a 10 ohm resistance with inductance 50 mH from a 340 V dc source. If the bridge is operating at 50 Hz, determine the load rms voltage and current and steady-state current waveforms with

i. a square-wave output
ii. a quasi-square-wave output with a 50 per cent on-time.

Solution

The time constant of the load, τ = 0.05mH/10Ω = 5 ms and t_2 = 20ms.
i. The output voltage rms value is 340 V ac.
Equation (14.9) gives the load current at the time when the supply polarity is reversed across the load, as shown in figure 14.lb, that is

$$\hat{I} = -\check{I} = \frac{V_s}{R} \frac{1 - e^{\frac{-t_2}{\tau}}}{1 + e^{\frac{-t_1}{\tau}}} \qquad \text{(A)}$$

where t_1 = 10 ms. Therefore

$$\hat{I} = -\check{I} = \frac{340\text{V}}{10\Omega} \times \frac{1 - e^{-2}}{1 + e^{-2}} \qquad \text{(A)}$$

$$= 25.9\text{A}$$

When v_L = +340 V, from equation (14.7) the load current is given by

$$i_L = 34 - (34 + 25.9)\, e^{-200t} = 34 - 59.9e^{-200t} \qquad 0 \le t \le 10 \text{ ms}$$

From equation (14.10) the zero current cross-over time, t_x, occurs at
$5\text{ms} \times \ell n\left(1 + 25.9\text{A} \times 10\Omega/340\text{V}\right) = 2.83$ ms after load voltage reversal.
When v_L = -340 V, from equation (14.8) the load current is given by

$$i_L = -34 + (34 + 25.9)\, e^{-200t} = -34 + 59.9e^{-200t} \qquad 0 \le t \le 10 \text{ ms}$$

The mean power delivered to the load is given by equation (14.14), that is

$$P_L = \frac{1}{10\text{ms}}\int_0^{10ms} 340\text{V} \times \{34 - 59.9 \times e^{-200t}\}\ dt$$
$$= 2755\text{ W}$$

From $P = i^2 R$, the load rms current is

$$i_{Lrms} = \sqrt{P_L / R} = \sqrt{2755\text{W} / 10\Omega} = 16.60\text{A}$$

ii. The quasi-square output voltage has a 5 ms on-time, t_o, and a 5 ms period of zero volts.
From equation (14.30) the rms output voltage is

$$V_s\sqrt{1 - 5\text{ms}/10\text{ms}} = V_S/\sqrt{2} = 240\text{V rms}.$$

The current during the different intervals is specified by equations (14.19) to (14.24). Alternately, the steady-state load current equations can be specified by determining the load current equations for the first few cycles at start-up until steady-state conditions are attained.

First 5 ms on-period when v_L = 340 V and initially i_L = 0 A

$$i_L = 34 - 34\ e^{-200t}$$

and at 5ms, i_L = 21.5A
First 5 ms zero-period when v_L = 0 V

$$i_L = 21.5\ e^{-200t}$$

and at 5ms, i_L =7.9A
Second 5 ms on-period when v_L = -340 V

$$i_L = -34 + (34+7.9)\ e^{-200t}$$

with i_L = 0 at 1 ms and ending with i_L = -18.6 A
Second 5 ms zero-period when v_L = 0 V

$$i_L = -18.6\ e^{-200t}$$

ending with i_L = -6.8A
Third 5 ms on-period when v_L = 340 V

$$i_L = 34 - (34+6.8)\ e^{-200t}$$

with i_L = 0 at 0.9 ms and ending with i_L = 19.0 A
Third 5 ms zero-period when v_L = 0 V

$$i_L = 19.0\ e^{-200t}$$

ending with i_L = 7.0A
Fourth 5 ms on-period when v_L = -340 V

$$i_L = -34 + (34+7.0)\ e^{-200t}$$

with i_L = 0 at 0.93 ms and ending with i_L = -18.9 A
Fourth 5 ms zero-period when v_L = 0 V

$$i_L = -18.9\ e^{-200t}$$

ending with i_L = -7.0A
Steady-state load current conditions have been reached and the load current

waveform is as shown in figure 14.1c. Convergence of an iterative solution is more rapid if the periods considered are much longer than the load time constant.
The mean load power for the quasi-square wave is given by

$$P_L = \frac{1}{10\text{ms}}\int_0^{5ms} 340\text{V} \times \{34 - 41 \times e^{-200t}\}\ dt$$
$$= 1378\text{ W}$$

The load rms current is

$$i_{Lrms} = \sqrt{P_L / R} = \sqrt{1378\text{W} / 10\Omega} = 11.74\text{A}$$

Example 14.1b: ***H-bridge inverter ac output factors***

In each waveform case of example 14.1a calculate

i. the average and peak current in the switches
ii. the average and peak current in the diodes
iii. the peak blocking voltage of each semiconductor type
iv. the average source current
v. the harmonic factor and distortion factor of the lowest order harmonic
vi. the total harmonic distortion

Solution

Square-wave
i. The peak current in the switch is $\hat{I}$ = 25.9 A and the current zero cross-over occurs at t_x=2.83ms. The average switch current, from equation (14.11) is

$$\bar{I}_T = \frac{1}{20\text{ms}}\int_{2.83\text{ms}}^{10\text{ms}} (34 - 59.9\ e^{-200t})\ dt$$
$$= 5.71\text{ A}$$

ii. The peak diode current is 25.9 A. The average diode current from equation (14.12) is

$$\bar{I}_D = \frac{1}{20\text{ms}}\int_0^{2.83\text{ms}} (34 - 59.9\ e^{-200t})\ dt$$
$$= 1.66\text{ A}$$

iii. The maximum blocking voltage of each device is 340 V dc.

iv. The average supply current is

$$\bar{I}_s = 2\left(\bar{I}_{TH} - \bar{I}_D\right)$$
$$= 2 \times \left(5.71\text{A} - 1.66\text{A}\right) = 8.10\text{A}$$

This results in the supply delivery power of 340Vdc × 8.10A = 2754W

v. From equation (14.15), with the third as the lowest harmonic, the distortion factors are

$$hf = \rho_3 = \left|\frac{V_3}{V_1}\right| = \tfrac{1}{3}, \text{ that is, } 33\tfrac{1}{3} \text{ per cent}$$

$$df = \mu_3 = \left|\frac{V_3}{3V_1}\right| = \tfrac{1}{9}, \text{ that is, } 11.11 \text{ per cent}$$

vi. From equation (14.15)

$$thd = \sqrt{\sum\left(\frac{V_n}{n}\right)^2}\ /V_1$$
$$= \sqrt{\left(\tfrac{1}{3}\right)^2 + \left(\tfrac{1}{5}\right)^2 + \left(\tfrac{1}{7}\right)^2 + ...}$$
$$= 46.2 \text{ per cent}$$

Quasi-square-wave, $\alpha = \tfrac{1}{2}\pi$ (5 ms) and from equation (14.25) t_x= 0.93ms
i. The peak switch current is 18.9 A.
From equation (14.26) the average switch current, using alternating zero volt loops, is

$$\bar{I}_T = \frac{1}{20\text{ms}}\int_{0.93\text{ms}}^{5\text{ms}} (34 - 41e^{-200t})\,dt + \frac{1}{40\text{ms}}\int_0^{5\text{ms}} 19e^{-200t}dt$$
$$= 2.18 + 1.50 = 3.68 \text{ A}$$

ii. The peak diode current (and peak switch current) is 18.9 A. The average diode current, from equation (14.27), when using alternating zero volt loops, is given by

$$\bar{I}_D = \frac{1}{20\text{ms}}\int_0^{0.93\text{ms}} \left(-34 + 41e^{-200t}\right)dt + \frac{1}{40\text{ms}}\int_0^{5\text{ms}} 19e^{-200t}dt$$
$$= 0.16 + 1.50 = 1.66 \text{ A}$$

iii. The maximum blocking voltage of each device type is 340 V.

iv. The average supply current is

$$\bar{I}_s = 2\left(\bar{I}_{TH} - \bar{I}_D\right)$$
$$= 2\times\left(3.68\text{A} - 1.66\text{A}\right) = 4.04\text{A}$$

This results in the supply delivery power of 340Vdc × 4.04A = 1374W

v. The harmonics are given by equations (14.1) to (14.3)

$$hf = \rho_3 = \left|\frac{V_3}{V_1}\right| = \tfrac{1}{3\sqrt{2}} / \tfrac{1}{\sqrt{2}} = \tfrac{1}{3}, \text{ that is, } 33\tfrac{1}{3} \text{ per cent}$$

$$df = \mu_3 = \left|\frac{V_3}{nV_1}\right| = \rho_3/n = \tfrac{1}{9}, \text{ that is, } 11.11 \text{ per cent}$$

vi.

$$thd = \sqrt{\left[\sum_{n\geq 2}^{\infty}\left(\frac{V_n}{n}\right)^2\right]}\ /V_1$$
$$= \sqrt{\left(\frac{1}{3}\right)^2 + \left(\frac{-1}{5}\right)^2 + \left(\frac{1}{7}\right)^2 + \left(\frac{1}{9}\right)^2 + ...}$$
$$= 46.2 \text{ per cent}$$

♣

Example 14.2: ***Harmonic analysis of H-bridge with an L-R load***

For each delay case (α = 0° and α = 90°) in example 14.1, using Fourier voltage analysis, determine (ignore harmonics above the 10th):

i. the magnitude of the fundamental and first four harmonics
ii. the load rms voltage and current
iii. load power
iv. load power factor

Solution

The appropriate harmonic analysis is outline in the following table, for α = 0° and α = 90°.

n	Z_n	V_n	I_n	V_n (α=90°)	I_n
harmonic	$\sqrt{R^2 + (2\pi 50nL)^2}$	$\frac{0.9V_s}{n}$	V_n/Z_n	$\frac{0.9V_s}{n}\cos(\frac{1}{2}n\alpha)$	V_n/Z_n
	Ω	V	A	V	A
1	18.62	306	16.43	216.37	11.62
3	48.17	102	2.12	-72.12	-1.50
5	79.17	61.2	0.77	-43.28	-0.55
7	110.41	43.71	0.40	30.91	0.28
9	141.72	34	0.24	24.04	0.17
		332.95V	16.59A	235.43V	11.73A

i The magnitude of the fundamental voltage is 306V for the square wave and is reduced to 216V when a phase delay angle of 90° is introduced. The table shows that the harmonics magnitudes reduce as the harmonic order increases.

ii The rms load current and voltage can be derived by the square root of the sum of the squares of the fundamental and harmonic components, that is, for the current

$$i_{rms} = \sqrt{I_1^2 + I_3^2 + I_5^2 + ...}$$

The load rms currents, from the table, are 16.59A and 11.73A, which agree with the values obtained in example 14.1a. Notice that the predicted rms voltages of 333V and 235V differ significantly from the values in example 14.1a, given by $V_s\sqrt{1-\gamma_\pi}$, namely 340V and 240.4V respectively. This is because the magnitude of the harmonics higher in order than 10 are not insignificant. The error introduced into the rms current value by ignoring these higher order voltages is insignificant because the impedance increases approximately proportionally with harmonic number, hence the resultant current is becomes smaller the order increases.

iii The load power is the load i^2R loss, that is

$$P_L = i_{rms}^2 R = 16.59^2 \times 10\Omega = 2752\text{W} \quad \text{for} \quad \alpha = 0$$
$$P_L = i_{rms}^2 R = 11.73^2 \times 10\Omega = 1376\text{W} \quad \text{for} \quad \alpha = 90°$$

iv The load power factor is the ratio of real power dissipated to apparent power, that is

$$pf = \frac{P}{S} = \frac{i_{rms}^2 R}{i_{rms} v_{rms}} = \frac{2752\text{W}}{16.59\text{A} \times 340\text{V}} = 0.488 \text{ for } \alpha = 0$$
$$pf = \frac{P}{S} = \frac{i_{rms}^2 R}{i_{rms} v_{rms}} = \frac{1376\text{W}}{11.79\text{A} \times 240.4\text{V}} = 0.486 \text{ for } \alpha = 90°$$

♣

Example 14.3: ***Single-phase half-bridge with an L-R load***

A single-phase half-bridge inverter as shown in the figure 14.2, supplies a 10 ohm resistance with inductance 50 mH from a 340 V dc source. If the bridge is operating at 50 Hz, determine for the square-wave output

v. steady-state current waveforms
vi. the load rms voltage
vii. the peak load current and its time domain solution, $i_L(t)$
viii. the average and peak current in the switches
ix. the average and peak current in the diodes
x. the peak blocking voltage of each semiconductor type
xi. the power delivered to the load and rms load current

Solution

From examples 14.1 and 14.2, τ = 5ms.

i. Figure 14.2 shows the output voltage and current waveforms, with various circuit component current waveforms superimposed. Note that no zero voltage loops can be created with the half-bridge. Only load voltages $\pm\frac{1}{2}V_s$, that is ±170V, are possible.

ii. The output voltage swing is $\pm\frac{1}{2}V_s$, ±170V, thus the rms output voltage is $\frac{1}{2}V_s$, 170V. This is, half that of the full-bridge inverter using the same magnitude source voltage V_s, 340V.

iii. The peak load current is half that given by equation (14.9), that is

$$\hat{I} = \frac{\frac{1}{2}V_s}{R}\frac{1-e^{\frac{-t_1}{\tau}}}{1+e^{\frac{-t_1}{\tau}}} = \frac{\frac{1}{2}V_s}{R}\tanh\left(\frac{t_1}{2\tau}\right)$$
$$= \frac{\frac{1}{2}\times 340\text{V}}{10\Omega} \times \tanh\left(\frac{10\text{ms}}{2\times 5\text{ms}}\right) = 12.95\text{A}$$

The load current waveform is defined by equations (14.7) and (14.8), specifically

$$i_{L_I}(t) = \frac{\frac{1}{2}V_s}{R} - \left(\frac{\frac{1}{2}V_s}{R} - \check{I}\right)e^{\frac{-t}{\tau}}$$
$$= \frac{\frac{1}{2}\times 340\text{V}}{10\Omega} - \left(\frac{\frac{1}{2}\times 340\text{V}}{10\Omega} + 12.95\text{A}\right)e^{\frac{-t}{5\text{ms}}}$$
$$= 17 - 29.95\, e^{\frac{-t}{5\text{ms}}} \qquad \text{for} \qquad 0 \le t \le 10\text{ms}$$

and

$$i_{L_{II}}(t) = -\frac{\frac{1}{2}V_s}{R} + \left(\frac{\frac{1}{2}V_s}{R} + \hat{I}\right)e^{\frac{-t}{\tau}}$$
$$= -\frac{\frac{1}{2}\times 340\text{V}}{10\Omega} + \left(\frac{\frac{1}{2}\times 340\text{V}}{10\Omega} + 12.95\right)e^{\frac{-t}{5\text{ms}}}$$
$$= -17 + 29.95\, e^{\frac{-t}{5\text{ms}}} \qquad \text{for} \qquad 0 \le t \le 10\text{ms}$$

By halving the effective supply voltage, the current swing is also halved.

iv. The peak switch current is $\hat{I} = 12.95\mathbf{A}$.

The average switch current is given by

$$\bar{I}_T = \frac{1}{20\text{ms}}\int_{2.83\text{ms}}^{10\text{ms}} (17 - 29.95e^{\frac{-t}{5\text{ms}}})\, dt$$
$$= 2.86 \text{ A}$$

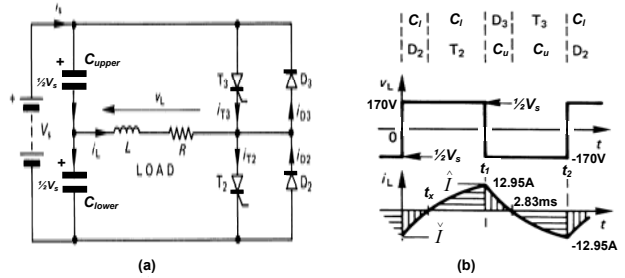


Figure 14.2. *GCT thyristor single-phase half-bridge inverter: (a) circuit diagram and (b) square-wave output voltage.*

v. The peak diode current is $\hat{I} = 12.95\text{A}$.
The average diode current is given by

$$\bar{I}_D = \frac{1}{20\text{ms}} \int_0^{2.83\text{ms}} \left(17 - 29.95 e^{\frac{-t}{5\text{ms}}}\right) dt$$
$$= 0.83 \text{ A}$$

vi. When a switch or diode of a parallel pair conduct, the complementary pair of devices experience a voltage V_s, 340V. Thus although the load experiences half the supply voltage, the semiconductors experience twice that voltage, the same as with the full bridge inverter.

vii. The load power is found by averaging the instantaneous load power, that is

$$P_L = \frac{1}{10\text{ms}} \int_0^{10\text{ms}} 170\text{V} \times \left(17 - 29.95 \times \text{e}^{-200t}\right) dt$$
$$= 638.5 \text{ W}$$

♣

14.1.2 Three-phase voltage-fed inverter bridge

The basic dc to three-phase voltage-fed inverter bridge is shown in figure 14.3. It comprises six power switches together with six associated reactive feedback diodes. Each of the three inverter legs operates at a relative time displacement (phase) of ⅔π, 120°.

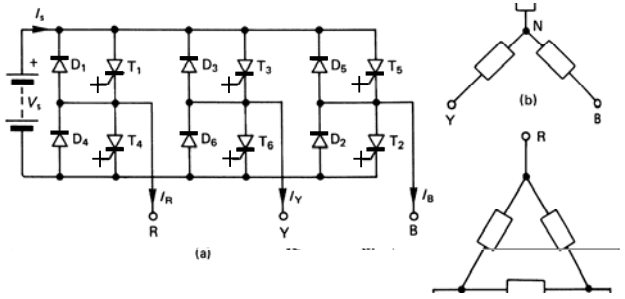


Figure 14.3. *Three-phase inverter circuit:*
(a) GCT thyristor bridge inverter; (b) star-type load; and (c) delta-type load.

14.1.2i - 180° (π) conduction

Figure 14.4 shows inverter bridge quasi-square output voltage waveforms for a 180° switch conduction pattern. Each switch conducts for 180°, such that no two semiconductor switches across the voltage rail conduct simultaneously. Six patterns exist for one output cycle and the rate of sequencing these patterns specifies the bridge output frequency. The conducting switches during the six distinct intervals are shown and can be summarised as in Table 14.1.

Table 14.1. Quasi-square-wave six conduction states - *180° conduction*.

Interval	***Three** conducting switches*								*leg state*	*voltage vector*
1	T_1	T_2	T_3						101	v_5
2		T_2	T_3	T_4					001	v_1
3			T_3	T_4	T_5				011	v_3
4				T_4	T_5	T_6			010	v_2
5					T_5	T_6	T_1		110	v_6
6						T_6	T_1	T_2	100	v_4

The three output voltage waveforms can be derived by analysing a resistive star load and considering each of the six connection patterns, as shown in figure 14.5. Effectively the resistors representing the three-phase load are sequentially cycled anticlockwise one at a time, being alternately connected to each supply rail.
Alternatively, the generation of the three-phase voltages can be analysed analytically by using the rotating *voltage space vector* technique. With this approach, the output voltage state from each of the three inverter legs (or poles) is encoded as summarised in the table 14.1, where a '1′ signifies the upper switch in the leg is on, while a '0′ means the lower switch is on in that leg. The resultant binary number (one bit for each of the three inverter legs), represents the output voltage vector number (when converted to decimal). The six voltage vectors are shown in figure 14.6 forming sextant boundaries, where the quasi-square output waveform in figure 14.4b is generated by stepping instantaneously from one vector position to another in an anticlockwise direction. Note that the rotational stepping sequence is arranged such that when rotating in either direction, only one leg changes state, that is, one device turns off and then the complementary switch of that leg turns on, at each step. This minimises the inverter switching losses. The dwell time of the created rotating vector at each of the six vector positions, is ⅓π ($\frac{1}{6}T$) of the cycle period (T). Note that the line-to-line zero voltage states 000 and 111 are not used. These represent the condition when ***either*** all the upper switches (T_1, T_3, T_5) are on ***or*** all the lower switches (T_2, T_4, T_5) are switched on. Phase reversal can be obtained by interchanging two phase outputs, or as is the preferred method, the direction of the rotating vector sequence is reversed. Reversing is therefore effectively achieved by back-tracking along each output waveform.

With reference to figure 14.4b, the line-to-load neutral voltage is defined by

$$v_{RN} = \frac{2}{\pi} V_s \left[\sin\omega t + \tfrac{1}{5}\sin 5\omega t + \tfrac{1}{7}\sin 7\omega t + \tfrac{1}{11}\sin 11\omega t + \ldots\right] \quad \text{(V)} \qquad (14.34)$$

similarly for v_{YN} and v_{BN}, where ωt is substituted by $\omega t+⅔\pi$ and $\omega t-⅔\pi$ respectively.

The line-to-line voltage, from equation (14.31) with $\alpha = ⅓\pi$, is defined by

$$v_{RB} = \frac{2\sqrt{3}}{\pi} V_s \left[\sin\omega t - \tfrac{1}{5}\sin 5\omega t - \tfrac{1}{7}\sin 7\omega t + \tfrac{1}{11}\sin 11\omega t + \ldots\right] \quad \text{(V)} \qquad (14.35)$$

and similarly for v_{BY} and v_{YR}. Figure 14.4b shows that v_{RB} is shifted $\frac{1}{6}\pi$ with respect to v_{RN}, hence to obtain the three line voltages while maintaining a v_{RN} reference, ωt should be substituted with $\omega t + \frac{1}{6}\pi$, $\omega t - ½\pi$ and $\omega t - \frac{5}{6}\pi$, respectively.

Since the interphase voltages consist of two square waves displaced by ⅔π, no triplen harmonics (3, 6, 9, . . .) exist. The outputs comprise harmonics given by the series $n = 6r \pm 1$ where $r \geq 0$ and is an integer. The nth harmonic has a magnitude of $1/n$ relative to the fundamental.

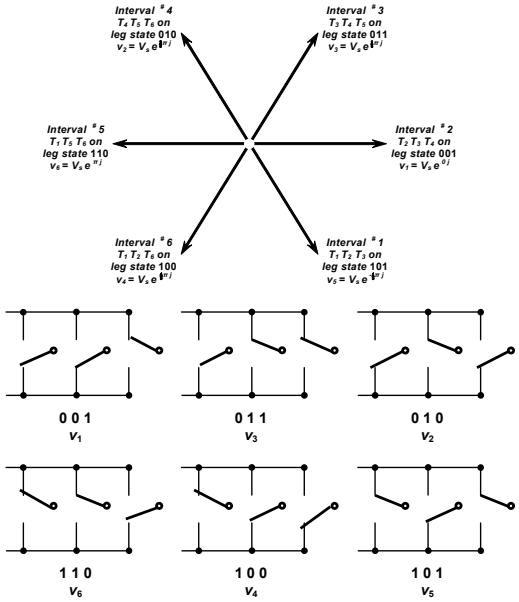


Figure 14.6. *Generation and arrangement of the six quasi-square inverter output voltage states.*

By examination of the interphase output voltages in figure 14.4 it can be established that the mean half-cycle voltage is ⅔V_s and the rms value is $\sqrt{⅔}\ V_s$, namely 0.816 V_s. From equation (14.35) the rms value of the fundamental is $\sqrt{6}\ V_s/\pi$, namely 0.78 V_s, that is $3/\pi$ times the total rms voltage value.

The three-phase inverter output voltage properties are summarised in Table 14.2.

Table 14.2. Quasi-squarewave voltage properties

Conduction period	Fundamental voltage		Characteristic		
	peak	rms	Total rms	Distortion Factor	THD
	$\hat{V}_1$	V_1	V_{rms}	μ	thd
180°	**(V)**	**(V)**	**(V)**		
Phase Voltage $V_{L\text{-}N}$	$\frac{2}{\pi}V_s$ $= 0.637V_s$	$\frac{\sqrt{2}}{\pi}V_s$ $= 0.450\,V_s$	$\frac{\sqrt{2}}{3}V_s$ $= 0.471V_s$	$\frac{3}{\pi}$ $= 0.955$	$\sqrt{\frac{\pi^2}{9}-1}$ $= 0.311$
Line Voltage $V_{L\text{-}L}$	$\frac{2\sqrt{3}}{\pi}V_s$ $= 1.10\,V_s$	$\frac{\sqrt{6}}{\pi}V_s$ $= 0.78\,V_s$	$\sqrt{\frac{2}{3}}V_s$ $= 0.816V_s$	$\frac{3}{\pi}$ $= 0.955$	$\sqrt{\frac{\pi^2}{9}-1}$ $= 0.311$
120°	**(V)**	**(V)**	**(V)**		
Phase Voltage $V_{L\text{-}N}$	$\frac{\sqrt{3}}{\pi}V_s$ $= 0.551\,V_s$	$\frac{\sqrt{6}}{2\pi}V_s$ $= 0.390\,V_s$	$\frac{1}{\sqrt{6}}V_s$ $= 0.408V_s$	$\frac{3}{\pi}$ $= 0.955$	$\sqrt{\frac{\pi^2}{9}-1}$ $= 0.311$
Line Voltage $V_{L\text{-}L}$	$\frac{3}{\pi}V_s$ $= 0.955V_s$	$\frac{3}{\sqrt{2}\,\pi}V_s$ $= 0.673\,V_s$	$\frac{1}{\sqrt{2}}V_s$ $= 0.707V_s$	$\frac{3}{\pi}$ $= 0.955$	$\sqrt{\frac{\pi^2}{9}-1}$ $= 0.311$

14.1.2ii - 120° (⅔π) conduction

The basic three-phase inverter bridge in figure 14.3 can be controlled with each switch conducting for 120°. As a result, at any instant only two switches (one upper and one non-complementary lower) conduct and the resultant quasi-square output voltage waveforms are shown in figure 14.7. A 60° (⅓π), dead time exists between two series switches conducting, thereby providing a safety margin against *simultaneous conduction* of the two series devices (for example T_1 and T_4) across the dc supply rail. This safety margin is obtained at the expense of a lower semi-conductor device utilisation and rms output voltage than with 180° device conduction. The device conduction pattern is summarised as in Table 14.3.

Figure 14.4b for 180° conduction and 14.7b for 120° conduction show that the line to neutral voltage of one conduction pattern is proportional to the line-to-line voltage of the other. That is from equation (14.31) with $\alpha = ⅓\pi$

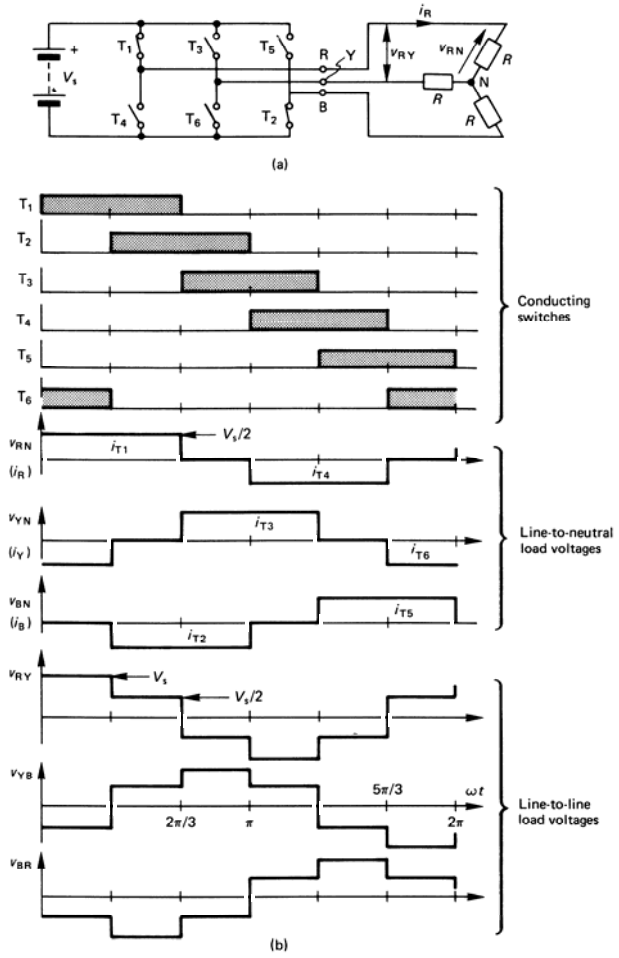


Figure 14.7. *A three-phase bridge inverter employing 120° switch conduction with a resistive star load: (a) the bridge circuit showing T_1 and T_2 conducting and (b circuit voltage and current waveforms.*

$$v_{RN}\left(\tfrac{2}{3}\pi\right) = \tfrac{1}{2}v_{RY}\left(\pi\right)$$
$$= \frac{\sqrt{3}}{\pi}V_s\left[\sin\omega t - \tfrac{1}{5}\sin 5\omega t - \tfrac{1}{7}\sin 7\omega t + \tfrac{1}{11}\sin 11\omega t + \ldots\right] \quad \text{(V)} \qquad (14.36)$$

and

$$v_{RY}\left(\tfrac{1}{3}\pi\right) = \tfrac{3}{2}v_{RN}\left(\pi\right)$$
$$= \frac{3}{\pi}V_s\left[\sin\omega t + \tfrac{1}{5}\sin 5\omega t + \tfrac{1}{7}\sin 7\omega t + \tfrac{1}{11}\sin 11\omega t + \ldots\right] \quad \text{(V)} \qquad (14.37)$$

Also $v_{RY} = \sqrt{3}\, v_{RN}$ and the phase relationship between these line and phase voltages, of $\frac{1}{6}\pi$, has not been retained. That is, with respect to figure 14.7b, substitute ωt with $\omega t + \frac{1}{6}\pi$ in equation (14.36) and $\omega t + \frac{1}{3}\pi$ in equation (14.37).
The output voltage properties for both 120° and 180° switch conduction are summarised in the Table 14.2.

Table 14.3. Quasi-squarewave conduction states - *120° conduction*.

Interval	***Two** conducting devices*						
1	T_1	T_2					
2		T_2	T_3				
3			T_3	T_4			
4				T_4	T_5		
5					T_5	T_6	
6						T_6	T_1

14.1.3 Inverter output voltage and frequency control techniques

It is a common requirement that the output voltage and/or frequency of an inverter be varied in order to control the load power or, in the case of an induction motor, to control the shaft speed and torque. The six modulation control techniques to be considered are:

- Variable voltage dc link
- Single-pulse width modulation
- Multi-pulse width modulation
- Multi-pulse, selected notching modulation
- Sinusoidal pulse width modulation
- Triplen injection
    - Triplens injected into the modulation waveform
    - Voltage space vector modulation

14.1.3i - Variable voltage dc link

The rms voltage of a square-wave can be changed and controlled by varying the dc link source voltage. A *variable dc link* voltage can be achieved with a dc chopper as considered in chapter 13 or an ac phase-controlled thyristor bridge as considered in sections 11.2 and 11.5. A dc link *L-C* smoothing filter may be necessary.

14.1.3ii - Single-pulse width modulation

Simple pulse-width control can be employed as considered in section 14.1.1b, where a single-phase bridge is used to produce a quasi-square-wave output voltage as shown in figure 14.1c.
An alternative method of producing a quasi-square wave of controllable pulse width is to transformer-add the square-wave outputs from two push-pull bridge inverters as shown in figure 14.8a. By phase-shifting the output by α, a quasi-square sum results as shown in figure 14.8b.

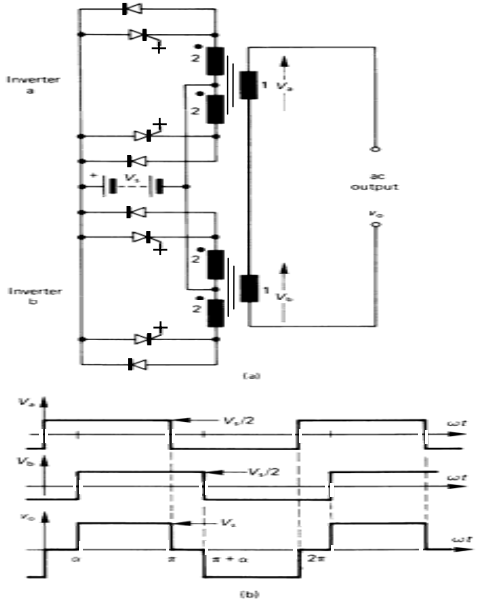


Figure 14.8. *Voltage control by combining phase-shifted push-pull inverters: (a) two inverters with two transformers for summing and (b) circuit voltage waveforms for a phase displacement of α.*

The output voltage can be described by

$$V_o = \sum_{n\ odd}^{\infty} v_{an} \sin n\omega t \qquad \text{(V)} \qquad (14.38)$$

where

$$v_{an} = \frac{2}{\pi}\int_{-½\pi}^{½\pi} V_s \cos n\alpha\, d\alpha = \frac{4}{n\pi} V_s \cos(½n\alpha) \qquad \text{(V)} \qquad (14.39)$$

The rms output voltage is

$$V_r = V_s\sqrt{1 - \alpha/\pi} \qquad \text{(V)} \qquad (14.40)$$

and the rms value of the fundamental is

$$V_1 = \frac{2\sqrt{2}}{\pi} V_s \cos ½\alpha \qquad \text{(V)} \qquad (14.41)$$

As α increases, the magnitude of the harmonics, particularly the third, becomes significant compared with the fundamental magnitude. This type of control may be used in high power applications.

14.1.3iii - Multi-pulse width modulation

An extension of the single-pulse modulation technique is multiple-notching as shown in figure 14.9. The bridge switches are controlled so as to vary the on to off time of each notch, δ, thereby varying the output rms voltage which is given by $V_{rms} = \sqrt{\delta}\, V_s$. Alternatively, the number of notches can be varied.

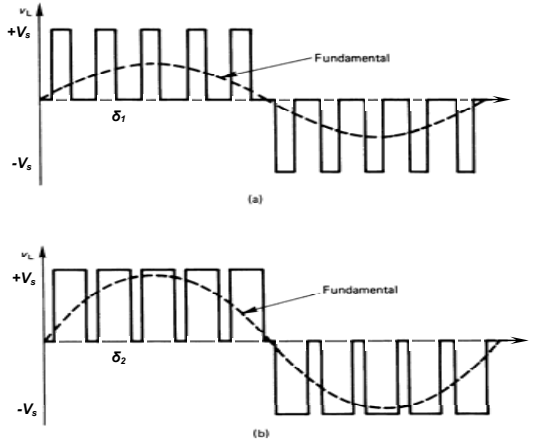


Figure 14.9. *Inverter control giving variable duty cycle of five notches per half cycle: (a) low duty cycle, δ_1, hence low fundamental magnitude and (b) higher duty cycle, δ_2, for a high fundamental voltage output.*

The harmonic content at lower output voltages is significantly lower than that obtained with single-pulse modulation. The increased switching frequency does increase the magnitude of higher harmonics and the switching losses.

14.1.3iv - Multi-pulse, selected notching modulation

Selected elimination of lower-order harmonics can be achieved by producing an output waveform as shown in figure 14.10. The exact switching points are calculated off-line so as to eliminate the required harmonics. For *n* switchings per half cycle, *n* selected harmonics can be eliminated.
In figure 14.10 two notches per half cycle are introduced; hence any two selected harmonics can be eliminated. The more notches, the lower is the output fundamental. For example, with two notches, the third and fifth harmonics are eliminated. From

$$b_n = \frac{4}{\pi}\int_0^{\frac{1}{2}\pi} f(\theta)\sin n\theta\, d\theta \quad \text{for} \quad n = 1, 2, 3, ... \tag{14.42}$$

$$b_3 = \frac{4}{3\pi}V_s\left(1 - 2\cos 3\alpha + 2\cos 3\beta\right) = 0$$

and

$$b_5 = \frac{4}{5\pi}V_s\left(1 - 2\cos 5\alpha + 2\cos 5\beta\right) = 0$$

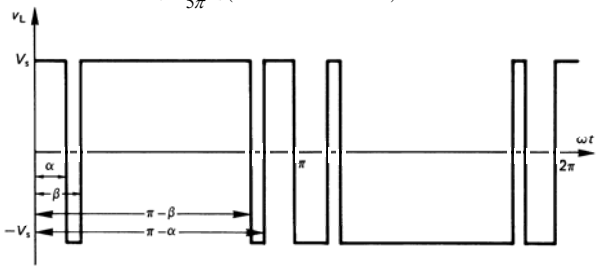


Figure 14.10. *Output voltage harmonic reduction for a single-phase bridge using selected notching.*

Solving yields $\alpha = 23.6°$ and $\beta = 33.3°$. The fundamental rms component of the output voltage waveform is 0.84 of a square wave, which is $(2\sqrt{2}/\pi)V_s$. Ten switching intervals exist compared with two per cycle for a square wave, hence switching losses and control circuit complexity are increased.
In the case of a three-phase inverter bridge, the third harmonic does not exist, hence the fifth and seventh (b_5 and b_7) can be eliminated with $\alpha = 16.3°$ and $\beta = 22.1$. The 5th, 7th, 11th, and 13th can be eliminated with the angles 10.55°, 16.09°, 30.91°, and 32.87° respectively. Because the waveforms have quarter wave symmetry, only angles for 90° need be stored.

The output rms voltage magnitude can be varied by controlling the dc link voltage or by transformer-adding two phase-displaced bridge outputs as demonstrated in figure 14.8. The rms magnitude can be changed by introducing an extra constraint to be satisfied, along with the harmonic eliminating constraints.
The multi pulse selected notching modulation technique can be extended to the *optimal pulse-width modulation method,* where harmonics may not be eliminated, but minimised according to a specific criterion. In this method, the quarter wave output is considered to have a number of switching angles. These angles are selected so as, for example, to eliminate certain harmonics, minimise the rms of the ripple current, or any other desired performance index. The resultant non-linear equations are solved using numerical methods off-line. The computed angles are then stored in a ROM look-up table for use. A set of angles must be computed and stored for each desired level of the voltage fundamental and output frequency.
The optimal pwm approach is particularly useful for high-power, high-voltage GCT thyristor inverters, which tend to be limited in switching frequency by device switching losses.

14.1.3v - Sinusoidal pulse-width modulation (pwm)

1 - Natural sampling

(a) Synchronous carrier
The output voltage waveform and method of generation for synchronous carrier, natural sampling sinusoidal pwm, suitable for the single-phase bridge of figure 14.1, are illustrated in figure 14.11. The switching points are determined by the intersection of the triangular carrier wave f_c and the reference modulation sine wave, f_o. The output frequency is at the sine-wave frequency f_o and the output voltage is proportional to the magnitude of the sine wave. The amplitude M ($0 \le M \le 1$) is called the modulation index. For example, figure 14.11a shows maximum voltage output *(*$M = 1$), while in figure 14.11b where the sine-wave magnitude is halved *(*$M = 0.5$*),* the output voltage is halved.
If the frequency of the modulation sinewave, f_o, is an integer multiple of the triangular wave carrier-frequency, f_c that is, $f_c = nf_o$ where n is integer, then the modulation is *synchronous,* as shown in figure 14.11. If n is odd then the positive and negative output half cycles are symmetrical and the output voltage contains no even harmonics. In a three-phase system if n is a multiple of 3 (and odd), the carrier is a triplen of the modulating frequency and the spectrum does not contain the carrier or its harmonics.

$$f_c = (6q + 3)f_o = nf_o \tag{14.43}$$

for $q = 1, 2, 3$.
Sinusoidal pwm requires a carrier of much higher frequency than the modulation frequency. The generated rectilinear output voltage pulses are modulated such that their duration is proportional to the instantaneous value of the sinusoidal waveform at the centre of the pulse; that is, the pulse area is proportional to the corresponding value of the modulating sine wave.

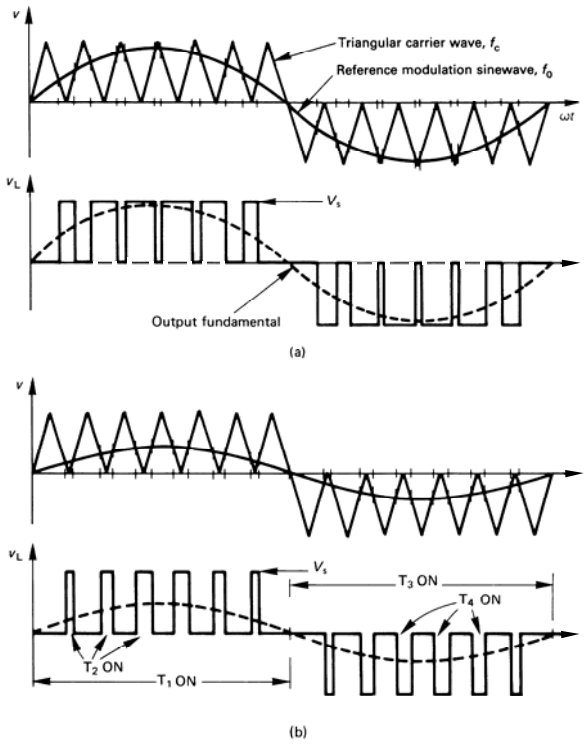


Figure 14.11. *Derivation of trigger signals for naturally sampled pulse-width modulation waveforms: (a) for a high fundamental output voltage (M = 1) and (b) for a lower output voltage (M = 0.5), with conducting devices shown.*

If the carrier frequency is very high, an averaging effect occurs, resulting in a sinusoidal fundamental output with high-frequency harmonics, but minimal low-frequency harmonics.

Rather than using a triangular carrier, which has an alternating offset as shown in figure 14.11, a triangular carrier without an offset can be used. Now the output only approximates the ideal. Figure 14.12 shows this pwm generation technique

and voltage output waveform applied to the three-phase inverter in figure 14.3. The offset carrier is not applicable to three-phase pwm generation since complementary switch action is required. That is, one switch in the inverter leg must always be on. It will be noticed that, unlike the output in figure 14.11, no zero voltage output periods exist. This has the effect that, in the case of GCT thyristor bridges, a large number of commutation cycles is required. When zero output periods exist, as in figure 14.11, one GCT thyristor is commutated and the complementary device in that leg is not turned on. The previously commutated device can be turned back on without the need to commutate the complementary device, as would be required with the pwm technique illustrated in figure 14.12. Commutation losses are reduced, control circuitry simplified and the likelihood of simultaneous conduction of two series devices is reduced.

The alternating zero voltage loop concept can be used, where in figure 14.11b, rather than T_1 being on continuously during the first half of the output cycle, T_2 is turned off leaving T_1 on, then when either T_1 or T_2 must be turned off, T_1 is turned off leaving T_2 on.

(b) Asynchronous carrier

When the carrier is not an interger multiple of the modulation waveform, asynchronous modulation results. Because the output frequency, f_o, is usually variable over a wide range, it is difficult to ensure $f_c = nf_o$. To achieve synchronism, the carrier frequency must vary with frequency f_o. Simpler generating systems result if a fixed carrier frequency is used, resulting in asynchronism between f_o and f_c at most output frequencies. Left over, incomplete carrier cycles create slowly varying output voltages, called subharmonics, which may be troublesome with low carrier frequencies, as found in high-power drives. Natural sampling, asynchronous sinusoidal pwm is usually restricted to analogue or ASIC implementation. The harmonic consequences of asynchronous-carrier natural-sampling are similar to asynchronous-carrier regular-sampling in 2 to follow.

2 - Regular sampling

Asynchronous carrier

When a fixed carrier frequency is used, usually no attempt is made to synchronise the modulation frequency. The output waveforms do not have quarter-wave symmetry which produces subharmonics. These subharmonics are insignificant if $f_c >> f_o$, usually, $f_c > 20 f_o$.

The implementation of sinusoidal pwm with microprocessors or digital signal processors is common because of flexibility and the elimination of analogue circuitry associated problems. The digital pwm generation process involves scaling, by multiplication, of the per unit sine-wave samples stored in ROM. The multiplication process is time-consuming, hence natural sampling is not possible. In order to minimise the multiplication rate, the sinusoidal sine-wave reference is replaced by a quantised stepped representation of the sine-wave. Figure 14.13 shows two methods used. Sampling is synchronised to the carrier frequency and the multiplication process is performed at three times the sampling rate for three-phase pwm generation (once for each phase).

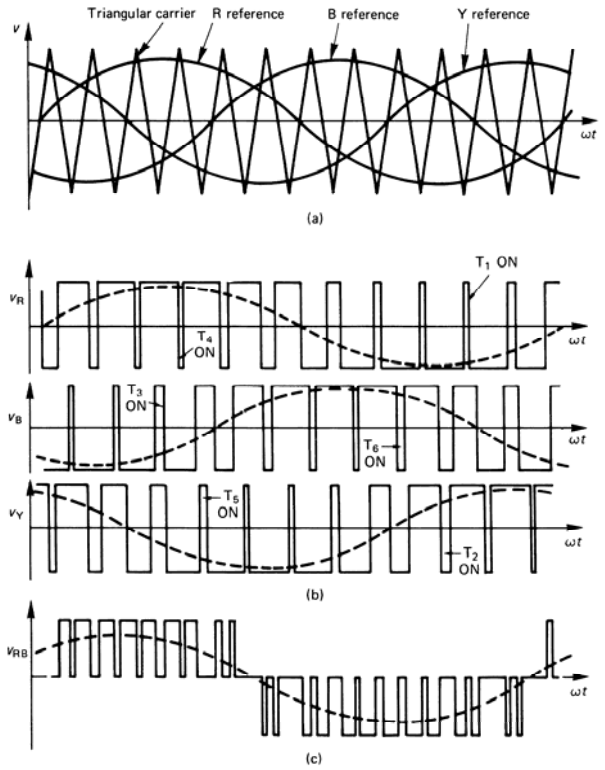


Figure 14.12. *Naturally sampled pulse-width modulation waveforms suitable for a three-phase bridge inverter: (a) reference signals; (b) conducting devices and fundamental sine waves; and (c) one output line-to-line voltage waveform.*

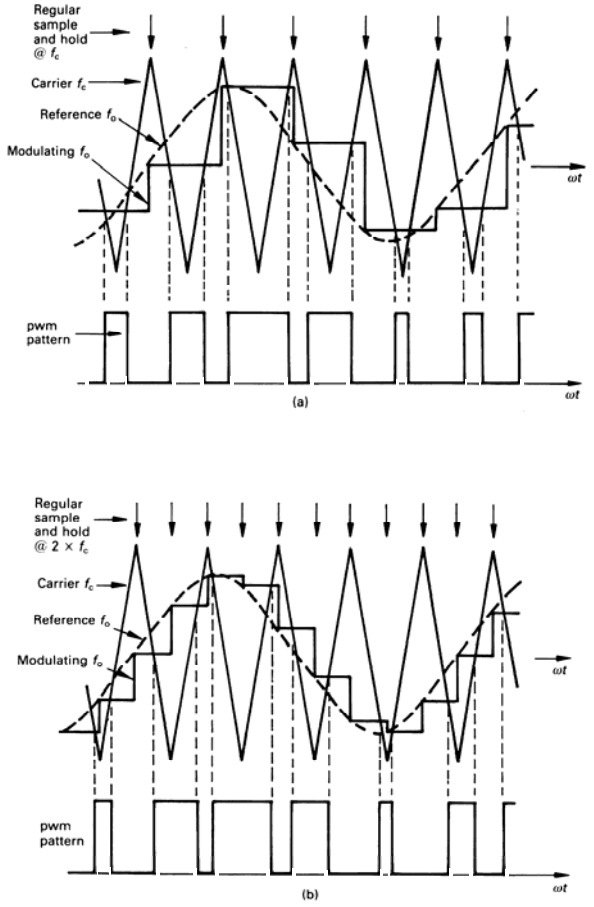


Figure 14.13. *Regular sampling, asynchronous, sinusoidal pulse-width-modulation: (a) symmetrical modulation and (b) asymmetrical modulation.*

Symmetrical modulation

Figure 14.13a illustrates the process of symmetrical modulation, where sampling is at the carrier frequency. The quantised sine-wave is stepped and held at each sample point. The triangular carrier is then compared with the step sine-wave sample. The modulation process is termed symmetrical modulation because the intersection of adjacent sides of the triangular carrier with the stepped sine-wave, about the non-sampled carrier peak, are equidistant about the carrier peak. The pulse width, independent of the modulation index *M,* is symmetrical about the triangular carrier peak not associated with sampling, as illustrated by the upper pulse in figure 14.14. The pulse width is given by

$$t_{ps} = \frac{1}{2f_c}\left(1 - M \sin 2\pi f_o t_1\right) \qquad (14.44)$$

where t_1 is the time of sampling.

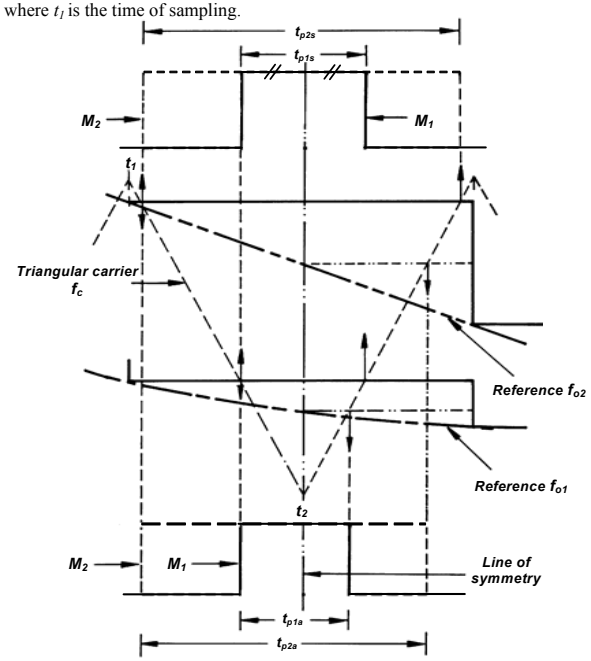


Figure 14.14. *Regular sampling, asynchronous, sinusoidal pulse-width-modulation, showing double edge: (upper) asymmetrical modulation and (lower) symmetrical modulation.*

Asymmetrical modulation

Asymmetrical modulation is produced when the carrier is compared with a stepped sine wave produced by sampling and holding at twice the carrier frequency, as shown in figure 14.13b. Each side of the triangular carrier about a sampling point intersects the stepped waveform at different step levels. The resultant pulse width is asymmetrical about the sampling point, as illustrated by the lower pulse in figure 14.14 for two modulation waveform magnitudes. The pulse width is given by

$$t_{pa} = \frac{1}{2f_c}\left(1 - \tfrac{1}{2}M\left(\sin 2\pi f_o t_1 + \sin 2\pi f_o t_2\right)\right) \qquad (14.45)$$

where t_1 and t_2 are the times at sampling such that $t_2 = t_1 + 1/2f_c$.

Figure 14.14 shows that a change in the modulation index M varies the pulse width on each edge, termed *double edge modulation.* A triangular carrier produces double edge modulation, while a sawtooth carrier produces *single edge modulation,* independent of the sampling technique.

3 - Frequency spectra of pwm waveforms

The most common form of sinusoidal modulation for three-phase inverters is regular sampling, asynchronous, fixed frequency carrier, pwm. If $f_c > 20f_o$, low frequency subharmonics can be ignored. The output spectra consists of the modulation frequency f_o with magnitude M. Also present are the spectra components associated with the triangular carrier, f_c. For any sampling, these are f_c and the odd harmonics of f_c. (The triangular carrier f_c contains only odd harmonics). These decrease in magnitude with increasing frequency. About the frequency nf_c are components of f_o spaced at $\pm 2f_o$, which generally decrease in magnitude when further away from nf_c. That is, at f_c the harmonics present are f_c, $f_c \pm 2f_o$, $f_c \pm 4f_o$, ... while about $2f_c$, the harmonics present are $2f_c \pm f_o$, $2f_c \pm 3f_o$,..., but $2f_c$ is not present. The typical output spectrum is shown in figure 14.15. The relative magnitudes of the sidebands vary with modulation depth and the carrier related frequencies present, f_h, are given by

$$f_h = \left(\tfrac{1}{2} + \frac{-1^{n+1}}{2}\right) n f_c \pm \left(2k - \left(\tfrac{1}{2} + \frac{-1^{n}}{2}\right)\right) f_o \qquad (14.46)$$

where $k = 1, 2, 3,....$ (sidebands) and $n = 1, 2, 3,....$ (carrier)

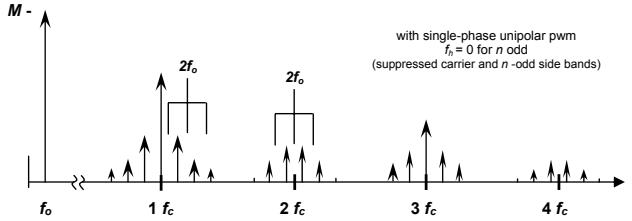


Figure 14.15. *Location of carrier harmonics and modulation frequency sidebands, showing all sideband separated by $2f_m$.*

Although the various pwm techniques produce other less predominate spectra components the main difference is seen in the magnitude of the carrier harmonics and sidebands. The magnitudes increase as the pwm type changes from naturally sampling to regular sampling, then from asymmetrical to symmetrical modulation, and finally from double edge to single edge. With a three-phase inverter, the carrier and its harmonics do not appear in the line-to-line voltages since the carrier is co-phase to the three modulation waveforms.

14.1.3vi - Phase dead-banding

Dead banding is when one phase (leg) is in a fixed on state, and the remaining phases are appropriately modulated so that the phase currents remain sinusoidal. The dead banding occurs for 60° periods of each cycle with the phase with the largest magnitude voltage being permanently turned on. Sequentially each switch is clamped to the appropriate link rail. The leg output is in a high state if it is associated with the largest positive phase voltage magnitude, while the phase output is zero if it is associated with the largest negative phase magnitude. Thus the phase outputs are cycled, being alternately clamped high and low for 60° every 180° as shown in figure 14.16. A consequence of dead banding is reduced switching losses since each leg is not switched at the carrier frequency for 120° (two 60° periods 180° apart). A consequence of dead banding is increased ripple current. Dead banding is achieved with discontinuous modulating reference signals. Dead banding for a continuous 120° per phase leg is also possible but the switching loss savings are not uniformly distributed amongst the six inverter switches.

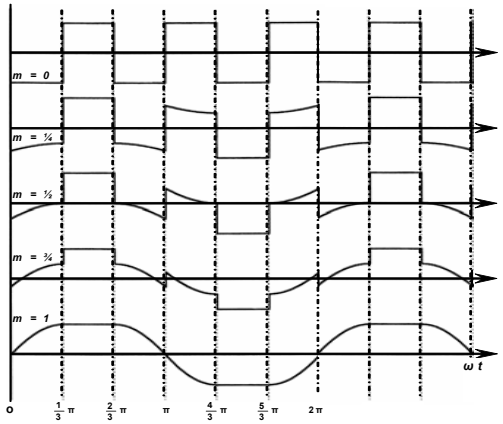


Figure 14.16. *Modulation reference waveform for phase dead banding.*

14.1.3vii - Triplen Injection modulation

The magnitude of the fundamental can be increased from 0.827pu to 0.955pu without introducing output voltage distortion, by the injection of triplen components, which are co-phasal in a three-phase system, and therefore do not appear in the line currents. Two basic approaches can be used to affect this undistorted output voltage magnitude increase.

- Triplen injection into the modulation waveform or
- Voltage space vector modulation

- Triplens injected into the modulation waveform

An inverter reconstitutes three-phase voltages with a maximum magnitude of 0.827 ($3\sqrt{3}/2\pi$) of the fixed three-phase input ac supply. A motor designed for the fixed mains supply is therefore under-fluxed at rated frequency and not fully utilised on an inverter. As will be shown, by adding third harmonic voltage injection, the flux level can be increased to 0.955 ($3/\pi$) of that produced on the three-phase ac mains supply.
If overmodulation ($M > 1$) is not allowed, then the modulation wave $M \sin \omega t$ is restricted in magnitude to $M = 1$, as shown in figure 14.17a.

If $V_{RN} = M \sin\omega t \le 1$pu
and $V_{YN} = M \sin(\omega t + \frac{2}{3}\pi) \le 1$ pu
then $V_{RY} = \sqrt{3}\, M \sin(\omega t - \frac{1}{6}\pi)$
where $0 \le M \le 1$

In a three-phase pwm generator, the fact that harmonics at $3f_o$ (and multiples of $3f_o$) vectorally cancel can be utilised effectively to increase M beyond 1, yet still ensure modulation occurs for every carrier frequency cycle.

Let $V_{RN} = M' \sin\omega t + \frac{1}{6} \sin 3\omega t) \le 1$ pu
and $V_{YN} = M' (\sin(\omega t + \frac{2}{3}\pi) + \frac{1}{6} \sin 3(\omega t + \frac{2}{3}\pi)) \le 1$ pu
then $V_{RY} = \sqrt{3}\, M' \sin(\omega t - \frac{1}{6}\pi)$

V_{RN} has a maximum instantaneous value of 1 pu at $\omega t = \pm\frac{1}{3}\pi$, as shown in figure 14.17b. Therefore

$$V_{RN}\left(\omega t = \tfrac{1}{3}\pi\right) = \frac{\sqrt{3}}{2} M' = 1$$

that is

$$\widehat{M}' = \frac{2}{\sqrt{3}} \widehat{M} = 1.155 \widehat{M} \qquad (14.47)$$

Thus the fundamental of the phase voltage is $M' \sin \omega t = 1.155\, M \sin \omega t$. That is, if the modulation reference $\sin \omega t + \frac{1}{6} \sin 3\omega t$ is used, the fundamental output voltage is 15.5 per cent larger than when $\sin \omega t$ is used as a reference. The increased fundamental is shown in figure 14.17b.

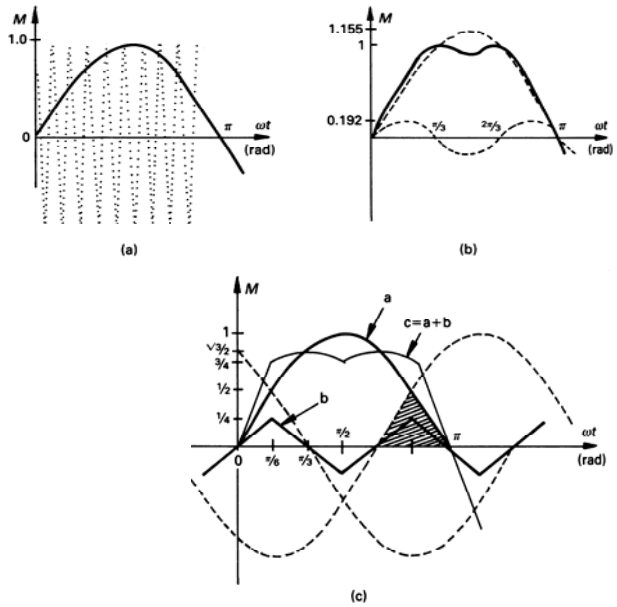


Figure 14.17. *Modulation reference waveforms: (a) sinusoidal reference, sin ωt; (b) third harmonic injection reference, sin ωt + ⅙sin 3ωt; and (c) triplen injection reference, sin ωt + (1/√3π){9/8sin3ωt - 80/81sin9ωt + . . .} where the near triangular waveform b is half the magnitude of the shaded area.*

The spatial voltage vector technique injects the triplens according to

$$V_{RN} = M'\left\{\sin\omega t + \frac{1}{\sqrt{3}\pi}\sum_{r=0}^{\infty}\frac{(-1)^r}{\left[(2r+1)-\frac{1}{3}\right]\left[(2r+1)+\frac{1}{3}\right]}\right\}\sin\left[(2r+1)3\omega t\right] \qquad (14.48)$$

The Fourier triplen series represents half the magnitude of the shaded area in figure 14.17c (the waveform marked 'b'), which is formed by the three-phase voltage waveforms. The spatial voltage vector waveform is defined by

$$\begin{aligned} &\frac{3}{2}\sin(\omega t) && 0 \le \omega t \le \tfrac{1}{6}\pi \\ &\frac{\sqrt{3}}{2}\sin(\omega t + \tfrac{1}{6}\pi) && \tfrac{1}{6}\pi \le \omega t \le \tfrac{1}{2}\pi \end{aligned} \qquad (14.49)$$

The use of this reference increases the duration of the zero volt loops, thereby decreasing inverter output ripple. The maximum modulation index is 1.155. Third harmonic injection, yielding M = 1.155, is a satisfactory approximation to spatial voltage vector.

- *Voltage space vector pwm*

When generating three-phase quasi-square output voltages, the inverter switches step progressively to each of the six switch output possibilities (states). In figure 14.6, when producing the quasi-square output, each of these six states is represented by an output voltage space vector. Each vector has a ⅓π displacement from its two adjacent states, and each has a length V_s which is the pole output voltage relative to the inverter 0V rail. Effectively, the quasi-square three-phase output is generated by a rotating vector of length V_s, jumping successively from one output state to the next in the sequence, and in so doing creating six sectors. The speed of rotation, in particular the time for one rotation, determines the inverter output frequency. The sequence of voltage vectors $\{v_1, v_3, v_2, v_6, v_4, v_5\}$ is arranged such that stepping from one state to the next involves only one of the three poles changing state. Thus the number of inverter devices needing to change states (switch) at each transition, is minimised.
[If the inverter switches are relabelled, upper switches T_1, T_2, T_3 - right to left; and lower switches T_4, T_5, T_6 - right to left: then the rotating voltage sequence becomes $\{v_1, v_2, v_3, v_4, v_5, v_6\}$]
Rather than stepping ⅓π radians per step, from one voltage space vector position to the next, thereby producing a six-step quasi-square fixed magnitude voltage output, the rotating vector is rotated in smaller steps based on the position being updated at a constant rate (carrier frequency). Furthermore, the vector length can be varied, to a magnitude less than V_s.
To incorporate a variable rotating **vector length** (modulation depth), it is necessary to vary the average voltage in each carrier period. Hence pulse width modulation is used in the period between each finite step of the rotating vector. Pulse width modulation requires the introduction of zero voltage output states, namely all the top switches on (state 111, v_7) or all the lower switches on (state 000, v_0). These two extra states are shown in figure 14.18, at the centre of the hexagon. Now the pole-to-pole output voltage can be zero, which allows duty cycle variation to achieve variable average output voltage for each phase, within each carrier period, proportional to the magnitude of the position vector.
To facilitate **vector positions** (angles) that do not lie on one of the six quasi-square output vectors, an intermediate vector $V_{o/p}e^{j\theta}$ is resolved into the vector sum of the two quasi-square vectors adjacent to the rotating vector. This process is shown in figure 14.19 for a voltage vector $V_{o/p}$ that lies in sector I, between output states v_1 (001) and v_3 (011). The voltage vector has been resolved into the two components V_a and V_b as shown.
The time represented by quasi-square vectors v_1 and v_3 is the carrier period T_c, in each case. Therefore the portion of T_c associated with v_a and v_b is scaled proportionally to v_1 and v_3, giving t_a and t_b.

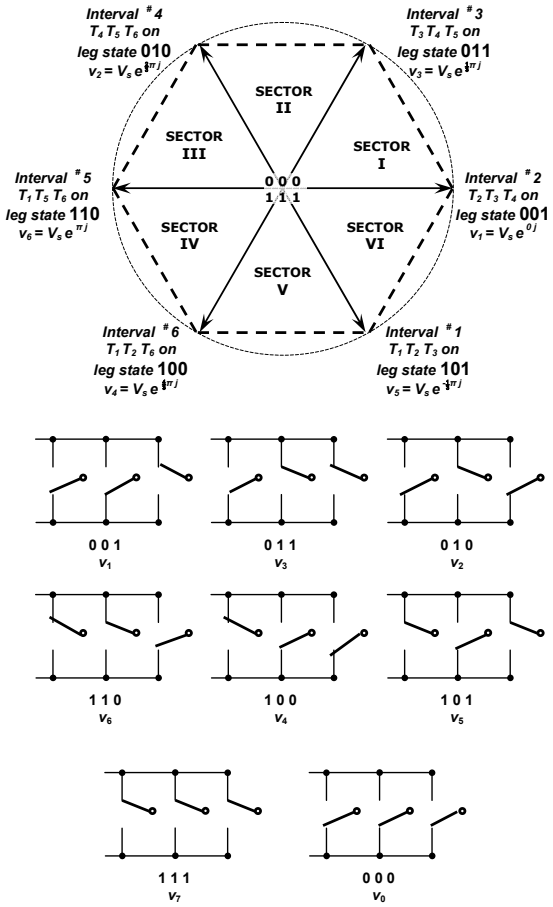


Figure 14.18. *Instantaneous output voltage states for the three legs of an inverter.*

$$\frac{t_a}{T_c} = \frac{|V_a|}{|v_1|} = \frac{\frac{2}{\sqrt{3}} V_{o/p} \sin\left(\frac{1}{3}\pi - \theta\right)}{V_s}$$

$$\frac{t_b}{T_c} = \frac{|V_b|}{|v_3|} = \frac{\frac{2}{\sqrt{3}} V_{o/p} \sin\theta}{V_s} \qquad (14.50)$$

where $|v_1| = |v_3|$

The two sine terms in equation (14.50) generate two sine waves displaced by 120°, identical to that generated with standard carrier based sinusoidal pwm.

The sum of t_a and t_b cannot be greater than the carrier period T_c, thus

$$t_a + t_b \le T_c$$
$$t_a + t_b + t_o = T_c \qquad (14.51)$$

where the slack variable t_o has been included to form an equality. The equality dictates that vector v_1 is used for a period t_a, v_3 is used for a period t_b, and during period t_o, the null vector, v_0 or v_7, at the centre of the hexagon is used, which do not affect the average voltage during the carrier interval T_c.

A further constraint is imposed in the time domain. The rotating voltage vector is a fixed length for all rotating angles, for a given inverter output voltage. Its length is restricted in both time and space. Obviously the resolved component lengths cannot exceed the pole vector length, V_s. Additionally, the two vector magnitudes are each a portion of the carrier period, where t_a and t_b could be both equal to T_c, that is, they both have a maximum length V_s. The anomaly is that voltages v_a and v_b are added vectorially but their durations (times t_a and t_b) are added linearly. The longest time $t_a + t_b$ possible is when t_o is zero, as shown in figures 14.19a and 14.18a, by the hexagon boundary. The shortest vector to the boundary is where both resolving vectors have a length $\frac{1}{2}V_s$, as shown in figure 14.19b. For such a condition, $t_a = t_b = \frac{1}{2}T_c$, that is $t_a + t_b = T_c$. Thus for a constant inverter output voltage, when the rotating voltage vector has a constant length, $\hat{V}_{o/p}$, the locus of allowable rotating reference voltage vectors must be within the circle scribed by the maximum length vector shown in figure 14.19b. As shown, this vector has a length $v_1 \cos 30°$, specifically $0.866V_s$. Thus the full quasi-square vectors v_1, v_2, etc., which have a magnitude of $1 \times V_s$, cannot be used for generating a sinusoidal output voltage. The excess length of each quasi-square voltage (which represents time) is accounted for by using zero state voltage vectors for a period corresponding to that extra length (1- cos 30° at maximum output voltage).

Having calculated the necessary periods for the inverter poles (t_a, t_b, and t_o), the carrier period switching pattern can be assigned in two ways.

- Minimised current ripple
- Minimised switching losses, using dead banding

Each approach is shown in figure 14.20, using single edged modulation. The waveforms are based on the equivalent of symmetrical modulation where the pulses are symmetrical about the carrier trough. By minimising the current ripple, seven switching states are used per carrier cycle, while for loss minimisation (dead banding) only five switching states occur, but at the expense of increased ripple

current in the output current. When dead banding, the zero voltage state v_0 is used in even numbered sextants and v_7 is used in odd numbered sextants.
Sideband and harmonic component magnitudes can be decreased if double-edged modulation placement of the states is used, which requires recalculation of t_a, t_b, and t_o at the carrier crest, as well as at the trough.

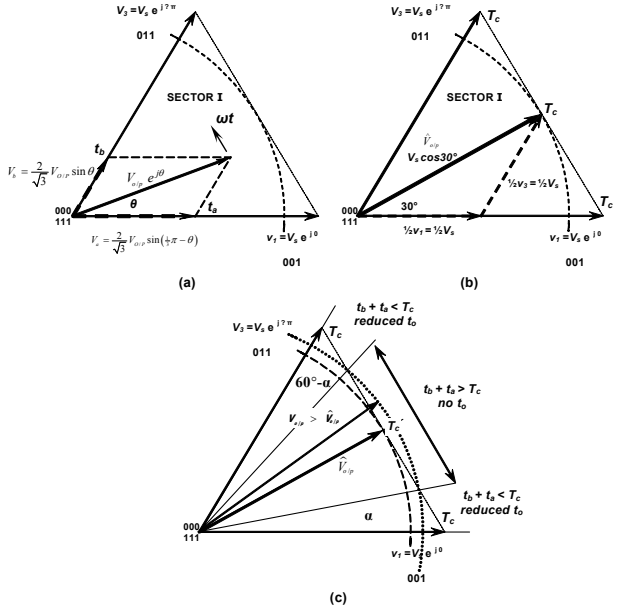


Figure 14.19. *First sector of inverter operational area involving pole outputs 001 and 011: (a) general rotating voltage vector; (b) maximum allowable voltage vector length for undistorted output voltages; and (c) over modulation.*

Over-modulation is when the magnitude of the demanded rotating vector is greater than $\hat{V}_{o/p}$ such that the zero voltage time reduces to zero, $t_o = 0$, during a portion of the time of one rotation of the output vector. Initially this occurs at 30° $\left(\frac{1}{6}\pi\left(2N_{\text{sector}}-1\right)\right)$ when the output vector length reaches $\hat{V}_{o/p}$, as shown in figure 14.19b. As the demand voltage magnitude increases further, the region around the 30° vector position where t_o ceases to occur, increases as shown in figure 14.19c. When the output rotational vector magnitude increases to V_s, the maximum possible, angle α reduces to zero, and t_o ceases to occur at any rotational angle.

The values of t_a, t_b, and t_o (if greater than zero), are calculated as usual, but pulse times are assigned pro rata to fit within the carrier period T_c.

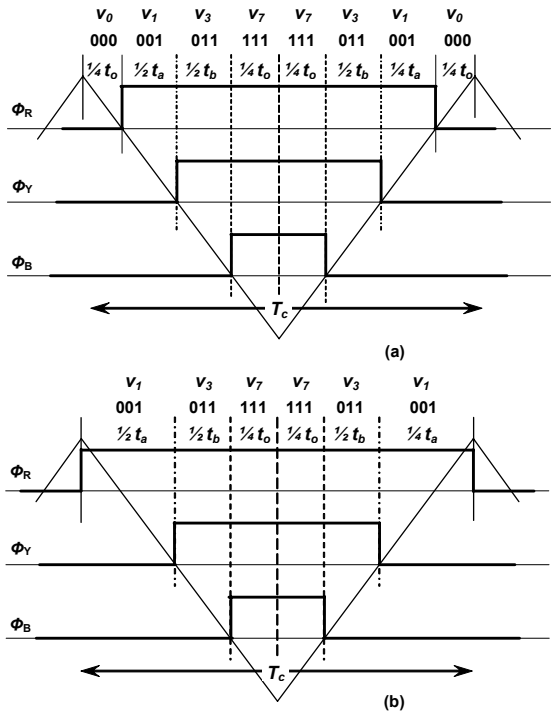


Figure 14.20. *Assignment of pole periods t_a and t_b based on: (a) minimum current ripple and (b) minimum switching transitions per carrier cycle, T_c.*

14.2 dc-to-ac controlled current-sourced inverters

In current-fed inverters (or alternatively current sourced inverter, *CSI*) the dc supply is of high reactance, being inductive so as to maintain the required inverter output bidirectional current independent of the inverter load.

14.2.1 Single-phase current fed inverter

A single-phase, controlled current-sourced bridge is shown in figure 14.21a and its near square-wave output current is shown in figure 14.21b. No freewheel diodes are required and the thyristors required forced commutation and have to withstand reverse voltages. An inverter path must be maintained at all times for the source controlled current.

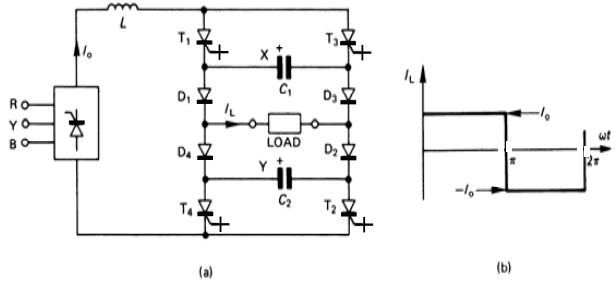


Figure 14.21. *Single-phase controlled-current sourced bridge inverter: (a) bridge circuit with a current source input and (b) load current waveform.*

Consider thyristors T_1 and T_2 on and conducting the constant load current. The capacitors are charged with plates X and Y positive as a result of the previous commutation cycle.

- ***Phase I***

  Thyristors T_1 and T_2 are commutated by triggering thyristors T_3 and T_4. The capacitors impress negative voltages across the respective thyristors to be commutated off, as shown in figure 14.22a. The load current is displaced from T_1 and T_2 via the path T_3-C_1-D_1, the load and D_2-C_2-T_4. The two capacitors discharge in series with the load, each capacitor reverse biasing the thyristor to be commutated, T_1 and T_2 as well as diodes D_3 to D_4. The capacitors discharge linearly (due to the constant current source).

- ***Phase II***

  When both capacitors are discharged, the load current transfers from D_1 to D_2 and from D_3 to D_4, which connects the capacitors in parallel with the load via diodes D_1 to D_2. The plates X and Y now charge negative, ready for the next commutation cycle, as shown in figure 14.22b. Thyristors T_1 and T_2 are now forward biased and must have attained forward blocking ability before the start of phase 2.

The on-going thyristor automatically commutates the outgoing thyristor. This repeated commutation sequencing is a processed termed *auto-sequential thyristor commutation*. The load voltage is load dependent and usually has controlled voltage spikes during commutation.

Since the GTO and CGT both can be commutated from the gate, the two commutation capacitors C_1 and C_2 are not necessary. Commutation overlap is still essential. Also, if the thyristors have reverse blocking capability, the four diodes D_1 to D_4 are not necessary. IGBTs require series blocking diodes, which increases on-state losses. In practice, the current source inverter is only used in very high-power applications (>1MVA), and the ratings of the self-commutating thyristor devices can be greatly extended if the simple external capacitive commutation circuits shown in figure 14.21 are used to reduce thyristor turn-off stresses.

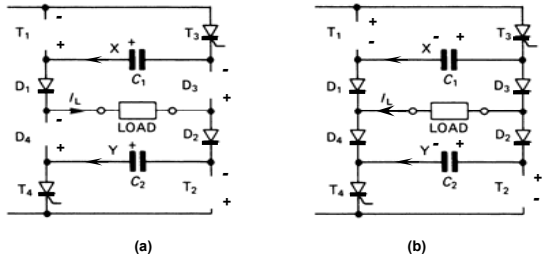


Figure 14.22. *Controlled-current sourced bridge inverter showing commutation of T_1 and T_2 by T_3 and T_4: (a) capacitors C_1 and C_2 discharging and T_1, T_2, D_3, and D_4 reversed biased and (b) C_1, C_2, and the load in parallel with C_1 and C_2 charging.*

14.2.2 Three-phase current fed inverter

A three-phase controlled current-sourced inverter is shown in figure 14.23a. Only two thyristors can be on at any instant, that is, the 120° thyristor conduction principle shown in figure 14.7 is used. A quasi-square line current results, as illustrated in figure 14.23b. There is a 60° phase displacement between commutation of an upper device followed by commutation of a lower device. An upper device (T_1, T_3, T_5) is turned on to commutate another upper device, and a lower device (T_2, T_4, T_6) commutate another lower device. The three upper capacitors are all involved with each upper device commutation, whilst the same constraint applies to the lower capacitors. Thyristor commutation occurs in two distinct phases.

- ***Phase I***

  In figure 14.24a the capacitors C_{13}, C_{35}, C_{51} are charged with the shown polarities as a result of the earlier commutation of T_5. T_1 is commutated by turning on T_3. During commutation, the capacitor between the two commutating switches is in parallel with the two remaining capacitors which

are effectively connected in series. Capacitor C_{13} provides displacement current whilst in parallel, C_{35} and C_{151} in series also provide thyristor T_1 displacement current, thereby reverse biasing T_1.

- ***Phase II***

When the capacitors have discharged, T_1 becomes forward biased, as shown in figure 14.24b, and must have regained forward blocking capability before the applied positive *dv/dt*. The capacitor voltages reverse as shown in figure 14.24b and when fully charged, diode D_1 ceases to conduct. Independent of this commutation, lower thyristor T_2 is commutated by turning on T_4, 60° later.

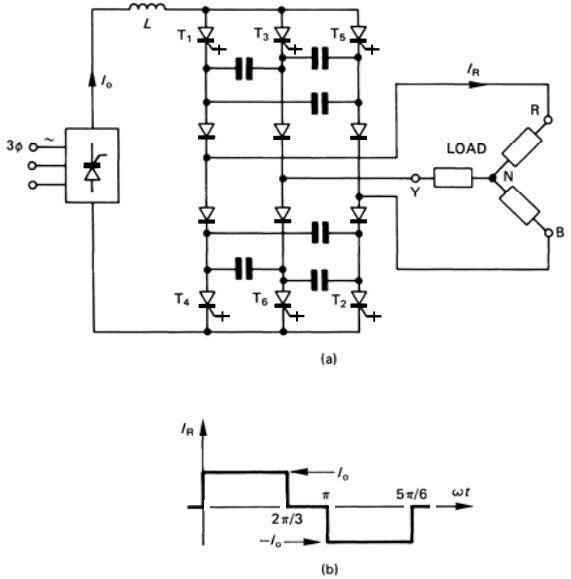


Figure 14.23. *Three-phase controlled-current sourced bridge inverter: (a) bridge circuit with a current source input and (b) load current waveform for one phase showing 120° conduction.*

As with the single-phase current sourced inverter, assisted capacitor commutation can greatly improve the capabilities of self-commutating thyristors, such as the GTO thyristor and GCT. The output capacitors stiffen the output ac voltage.

A typical application for a three-phase current-sourced inverter would be to feed and control a three-phase induction motor. Varying load requirements are met by changing the source current level over a number of cycles by varying the link inductor input voltage.

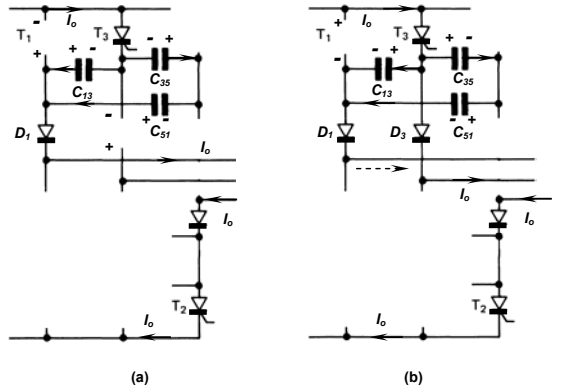


Figure 14.24. *Controlled-current sourced bridge three-phase inverter showing commutation of T_1 and T_3: (a) capacitors C_{13} discharging in parallel with C_{35} and C_{51} discharging in series, with T_1 and D_3 reversed biased (b) C_{13}, C_{35}, and C_{51} charging in series with the load , with T_1 forward biased.*

An important advantage of the controlled current source concept, as opposed to the constant voltage link, is good fault tolerance and protection. An output short circuit or simultaneous conduction in an inverter leg is controlled by the current source. Its time constant is usually longer than that of the input converter, hence converter shut-down can be initiated before the link current can rise to a catastrophic level.

PWM techniques are applicable to current fed inverters in order to reduce current harmonics, thereby reducing load losses and pulsating motor shaft torques. Since current fed inverters are most attractive in very high-power applications, inverter switching is minimised by using optimal pwm. The central 60° portion about the maximums of each phase cannot be modulated, since link current must flow and during such periods both the other phases require the opposite current direction. Attempts to over come such pwm restrictions include using a current sourced inverter with additional parallel current displacement paths as shown in figure 14.25. The auxiliary thyristors, T_{upper} and T_{lower}, and capacitors, C_R, C_Y, and C_B, provide alternative current paths (extra control states) and temporary energy storage. The auxiliary thyristor can be commutated by the extra capacitors.

Characteristics and features of current fed inverters

- The inverter is simple and can utilise rectifier grade thyristors. The switching devices must have reverse blocking capability and experience high voltages (both forward and reverse) during commutation.
- Commutation capability is load current dependent and a minimum load is required. This limits the operating frequency and precludes use in UPS systems. The limited operating frequency can result in torque pulsations.

- The inverter can recover from an output short circuit hence the system is rugged and reliable – fault tolerant.
- The converter-inverter configuration has inherent four quadrant capability without extra power components. Power inversion is achieved by reversing the converter average voltage output with a delay angle of $\alpha > \frac{1}{2}\pi$, as in the three-phase fully controlled converter shown in figure 11.18 (or 14.5.3). In the event of a power supply failure, mechanical braking is necessary. Dynamic braking is possible with voltage fed systems.
- Current fed inverter systems have sluggish performance and stability problems on light loads and at high frequency. On the other hand, voltage fed systems have minimal stability problems and can operate open loop.
- Each machine must have its own controlled rectifier and inverter. The dc link of the voltage fed scheme can be used by many inverters or many machines can utilise one inverter. A dc link offers limited ride-through.
- Current feed inverters tend to be larger in size and weight, because of the link inductor and filtering requirements.

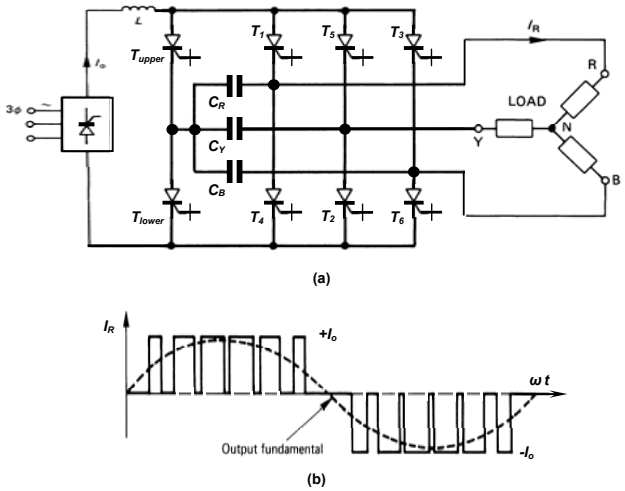


Figure 14.25. *Three-phase controlled-current sourced bridge inverter with alternative commutation current paths: (a) bridge circuit with a current source input and two extra thyristors and (b) load current waveform for one phase showing 180° conduction involving pwm switching.*

14.3 Resonant inverters

The voltage source inverters considered in 14.1 involve inductive loads and the use of switches that are hard switched. That is, the switches experience simultaneous maximum voltage and current during turn-on and turn-off with an inductive load. The current fed inverters considered in 14.2 required capacitive circuits to commutate the bridge switches. When self-commutatable devices are used in current fed inverters, hard switching occurs. In resonant inverters, the load enables commutation of the bridge switches with near zero voltage or current switch conditions, resulting in low switching losses. A characteristic of resonant circuits is that at regular, definable instants

- for a step load voltage, the series *L*-*C*-*R* load current sinusoidally reverses or
- for a step load current, the parallel *L*-*C*-*R* load voltage sinusoidally reverses.

If the load can be resonated, as considered in chapter 6.2.3, then switching stresses can be significantly reduced for a given power through put, provided switching is synchronised to the *V* or *I* zero crossing.

Three types of resonant converters utilise zero voltage or zero current switching.

- load-resonant converters
- resonant-switch dc-to-dc converters
- resonant dc link and forced commutated converters

The single-phase load-resonant converter, which is extensively used in induction heating applications, is presented and analysed in this chapter. Such resonant load converters use an *L*-*C* load which oscillates, thereby providing load zero current or voltage intervals at which the converter switches can be commutated with minimal electrical stress. Resonant switch dc-to-dc converters are presented in chapter 15.9.

Two basic resonant-load single-phase inverters are used, depending on the *L*-*C* load arrangement:

- current fed inverter with a parallel *L*-*C* resonant (tank) load circuit:
  switch turn-off at zero load voltage instants and turn-on with zero voltage
  switch overlap is essential (a continuous source current path is required)
- voltage fed inverter with a series connected *L*-*C* resonant load:
  switch turn-off at zero load current instants and turn-on with zero current
  switch under lap is essential (to avoid dc voltage source short circuiting)

Each load circuit type can be fed from a single ended circuit or H-bridge circuit depending on the load *Q* factor. This classification is divided according to

- symmetrical full bridge for low *Q* load circuits (class D)
- asymmetrical singled ended circuit for a high *Q* load circuit (class E)

High *Q* circuits can also use a full bridge inverter configuration, if desired, for higher through-put power.

In induction heating applications, the resistive part of the resonant load, called the work-piece, is the active load to be heated - melted, where the heating load is usually transformer coupled. Energy transfer control complication is usually associated with the fact that the resistance of the load work-piece changes as it heats up and melts, since resistivity is temperature dependant. However, control is essentially independent of the voltage and current levels and is related to the resonant frequency which is *L* and *C* dependant. Inverter bridge operation is near

the load resonant frequency so that the output waveform is essentially sinusoidal. By ensuring operation is below the resonant frequency, such that the load is capacitive, the resultant leading current can be used to self commutate thyristor converters which may be used in high power series resonant circuits. This same capacitive load commutation effect is obtained for parallel resonant circuits with thyristor current fed inverters operating just above resonance. The output power is controlled by controlling the converter output frequency.

14.3.1 L-C resonant circuits

L-C-R resonant circuits, whether parallel or series connected are characterised by the load impedance being capacitive at low frequency and inductive at high frequency for the series circuit, and visa versa for the parallel case. The transition frequency between being capacitive and inductive is the resonant frequency, ω_o, at which frequency the *L-C-R* load circuit appears purely resistive and maximum power is transferred to the load, *R*. *L-C-R* circuits are classified according to circuit quality factor Q_s resonant frequency, ω_o, and bandwidth, *BW*, for both parallel and series circuits. The characteristics for the parallel and series resonant circuits are related since every practical series *L-C-R* circuit has a parallel equivalent, and visa versa.

As shown in figure 14.26 each resonant half cycle is characterised by

- the series resonant circuit current is zero at maximum capacitor stored energy
- the parallel resonant circuit voltage is zero at maximum inductor stored energy

The capacitor in a series resonant circuit must have an external path through which to release its stored energy. The parallel resonant circuit can release its stored inductive energy within its parallel circuit, without an external circuit. The stored energy can transfer back and forth between the *L* and *C*, gradually dissipating in the circuit *R*.

14.3.1i - Series resonant *L-C-R* circuit

The series *L-C-R* circuit current for a step input voltage V_s, with initial capacitor voltage v_o and series inductor current i_o is given by

$$i(\omega t) = \frac{V_s - v_o}{\omega L} \times e^{-\alpha t} \times \sin \omega t + i_o \times e^{-\alpha t} \times \frac{\omega_o}{\omega} \times \cos(\omega t + \phi) \qquad (14.52)$$

where

$$\omega^2 = \omega_o^2 (1 - \xi^2) \qquad \omega_o = \frac{1}{\sqrt{LC}} \qquad \alpha = \frac{R}{2L} \qquad \frac{1}{2Q_s} = \xi = \frac{R}{2\omega_o L}$$

ξ is the damping factor. The capacitor voltage is important because it specifies the energy retained in the *L-C-R* circuit at the end of each half cycle.

$$v_c(\omega t) = V_s - (V_s - v_o)\frac{\omega_o}{\omega} e^{-\alpha t} \cos(\omega t - \phi) + \frac{i_o}{\omega C} e^{-\alpha t} \sin \omega t \qquad (14.53)$$

where

$$\tan \phi = \frac{\alpha}{\omega} \quad \text{and} \quad \omega_o^2 = \omega^2 + \alpha^2$$

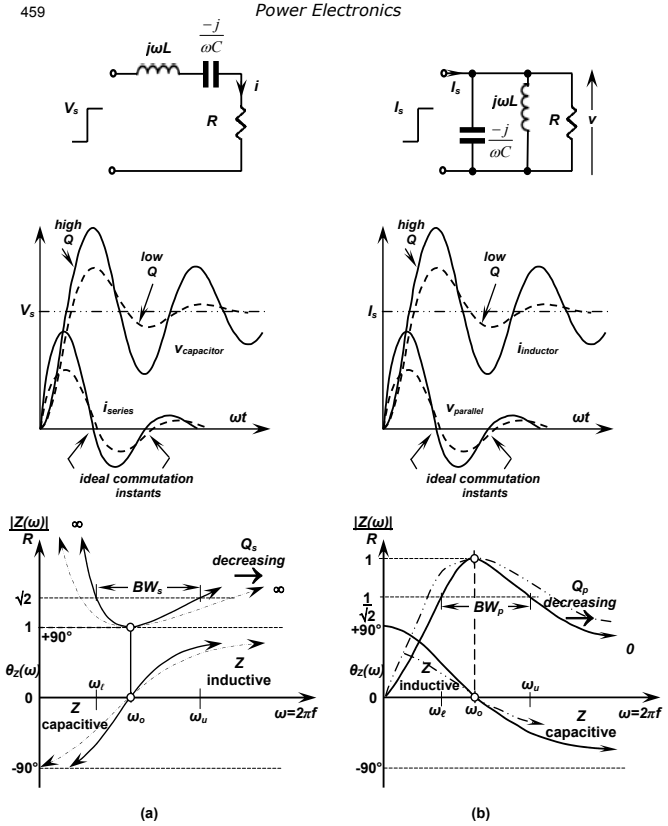


Figure 14.26. *Resonant circuits, step response, and frequency characteristics: (a) series L-C-R circuit and (b) parallel L-C-R circuit.*

At the series circuit resonance frequency ω_o, the lowest possible circuit impedance results, $Z=R$, hence it can be termed, low-impedance resonance. The series circuit quality factor or figure of merit, Q_s is defined by

$$Q_s = \frac{\text{reactive power}}{\text{average power}} = \frac{2\pi \times \text{maximum stored energy}}{\text{energy dissipated per cycle}} = \frac{2\pi \tfrac{1}{2} L i^2}{\tfrac{1}{2} R i^2 / f_o} = \frac{\omega_o L}{R} = \frac{1}{2\xi} = \frac{Z_o}{R} \quad (14.54)$$

where

$$Z_o = \sqrt{\frac{L}{C}} \qquad (\Omega)$$

The half-power bandwidth BW_s is given by

$$BW_s = \frac{\omega_o}{Q_s} = \frac{2\pi f_o}{Q_s} \quad (14.55)$$

and upper and lower half-power frequencies are related by $\omega = \sqrt{\omega_l \omega_u}$.

$$\omega_\ell^u = \omega_o \pm \alpha$$
$$f_\ell^u = f_o \pm \frac{R}{4\pi L} \quad (14.56)$$

Figure 14.26a shows the time-domain step-response of the series *L-C-R* circuit for a high *Q* load and a low *Q* case. In the low *Q* case, to maintain and transfer sufficient energy to the load *R*, the circuit requires re-enforcement every half sine cycle, while with a high circuit *Q*, re-enforcement is only necessary once per sinusoidal cycle. Thus for a high circuit *Q*, full bridge excitation is not necessary, yielding a simpler power circuit as shown in figure 14.27a and b.
The energy transferred to the load resistance *R*, per half cycle $1/2f_r$, is

$$W_{\frac{1}{2}} = \int_0^\pi i(\omega t)^2 R \, d\omega t \quad (14.57)$$

The active power transferred to the load depends on the repetition rate of the excitation, f_r.

$$P = W_{\frac{1}{2}} \times f_r \qquad (W) \quad (14.58)$$

14.3.1ii - Parallel resonant *L-C-R* circuit

The load for the parallel case is a parallel *L-C* circuit, where the active load is represented by resistance in the inductive path. For analysis, the series *L-R* circuit is converted into its parallel *R-L* equivalent circuit, thus forming the equivalent parallel *L-C-R* circuit shown in figure 14.26b. A parallel resonant circuit is used in conjunction with a current source inverter, thus the parallel circuit is excited with a step input current. The voltage across a parallel *L-C-R* circuit for a step input current I_s, with initial capacitor voltage v_o and initial inductor current i_o is given by

$$v(\omega t) = v_c(\omega t) = \frac{I_s - i_o}{\omega C} \times e^{-\alpha t} \times \sin \omega t + v_{co} \times e^{-\alpha t} \times \frac{\omega_o}{\omega} \times \cos(\omega t + \phi) \quad (14.59)$$

The inductor current is important since it specifies the tank circuit stored energy at the end of each half cycle.

$$i_L(\omega t) = I_s - (I_s - i_o) \times \frac{\omega_o}{\omega} \times e^{-\alpha t} \times \cos(\omega t - \phi) + \frac{v_o}{\omega L} \times e^{-\alpha t} \times \sin \omega t \quad (14.60)$$

where

$$\alpha = \frac{1}{2CR}$$

The circuit *Q* for a parallel resonant circuit is

$$Q_p = \omega_o RC = \frac{R}{\omega_o L} = \frac{R}{Z_o} = \frac{1}{Q_s} \quad (14.61)$$

where Z_o and ω_o are defined as in equations (14.52) and (14.54), except *L, C,* and *R* refer to the parallel circuit values.

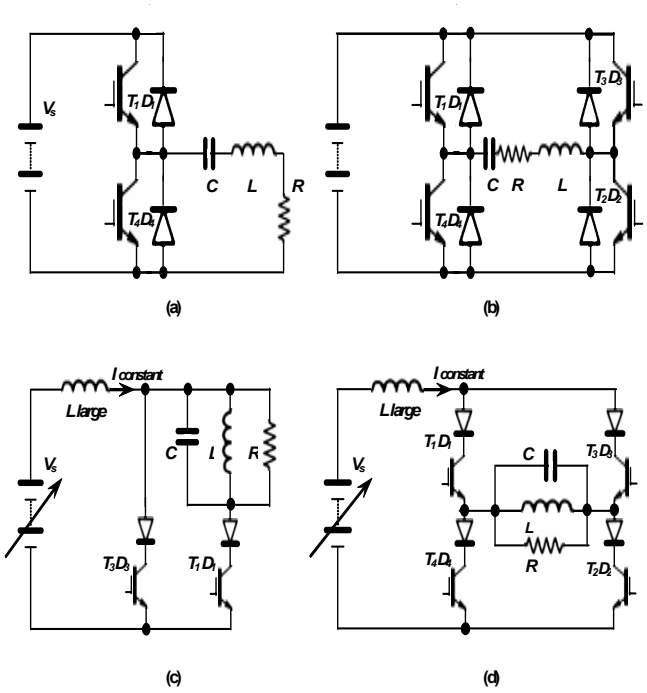


Figure 14.27. *Resonant converter circuits:*
(a) series L-C-R with a high Q; (b) low Q series L-C-R; (c) parallel L-C-R and high Q; and (b) low Q parallel L-C-R circuit.

The half-power bandwidth BW_p is given by

$$BW_p = \frac{\omega_o}{Q_p} = \frac{2\pi f_o}{Q_p} \qquad (14.62)$$

and upper and lower half power frequencies are related by $\omega = \sqrt{\omega_l \omega_u}$.
At the parallel circuit resonance frequency ω_o, the highest possible circuit impedance results, $Z=R$, hence it can be termed, high-impedance resonance.
The energy transferred to the load resistance R, per half cycle $1/2f_r$, is

$$W_{½} = \int_0^{\pi} v(\omega t)^2 / R \, d\omega t \qquad (14.63)$$

The active power to the load depends on the repetition rate of the excitation, f_r.

$$P = W_{½} \times f_r \qquad \text{(W)} \qquad (14.64)$$

14.3.2 Series resonant inverters

Series resonant circuits use a voltage source inverter as considered in 14.1.1 and shown in figure 14.27a and b. If the load Q is high, then the resonance of energy from the energy source, V_s, need only be re-enforced every second half-cycle, thereby simplifying converter and control requirements. A high Q circuit is characterised by successive half-cycle capacitor voltage peak magnitudes being of similar magnitude, that is the decay rate is

$$\frac{v_{c_n}}{v_{c_{n+1}}} = e^{\frac{\pi}{2Q}} \approx 1 \quad \text{for } Q \gg 1 \qquad (14.65)$$

Thus there is sufficient energy stored in C to be transferred to the load R, without need to involve the supply V_s. The circuit is simpler and control is easier.
Also, for any Q, each converter can be used with or without the shown freewheel diodes. Without freewheel diodes, the switches have to block high reverse voltages due to the energy stored by the capacitor. MOSFET and IGBTs require series diodes to achieve the reverse voltage blocking requirements. In high power resonant applications, the reverse blocking abilities of the GTO and GCT make it an ideal converter switch. Better load resonant control is obtained if freewheel diodes are not used.

14.3.2i - Series resonant inverter – single inverter leg

Operation of the series load asymmetrical circuit in figure 14.27a depends on the timing of the switches.

1 - Lagging operation (advancing the switch turn-off angle)

If the converter is operated at a frequency above resonance (effected by commutating the switches before the end of an oscillation cycle), the inductor reactance dominates and the load appears inductive. The load current lags the voltage as shown in figure 14.28. This figure shows the conducting devices and that a switch is turned on when its parallel diode is conducting. Turn-on therefore occurs at a low voltage, while turn-off is as with a hard switched inductive load.
Operation and switch timing is as follows:

Switch T1 is turned on while its anti-parallel diode is conducting and the current in the diode reaches zero and the current transfers to, and begins to oscillate through the switch T1. The capacitor charges to a maximum voltage and before

the current reverses, the switch T1 is turned off. The current is diverted through diode D4. T4 is turned on which allows the oscillation to reverse. Before the current in T4 reaches zero, it is turned off and current is diverted to diode D1, which returns energy to the supply. The resonant cycle is repeated when T1 is turned on before the current in diode D1 reaches zero and the process continues.

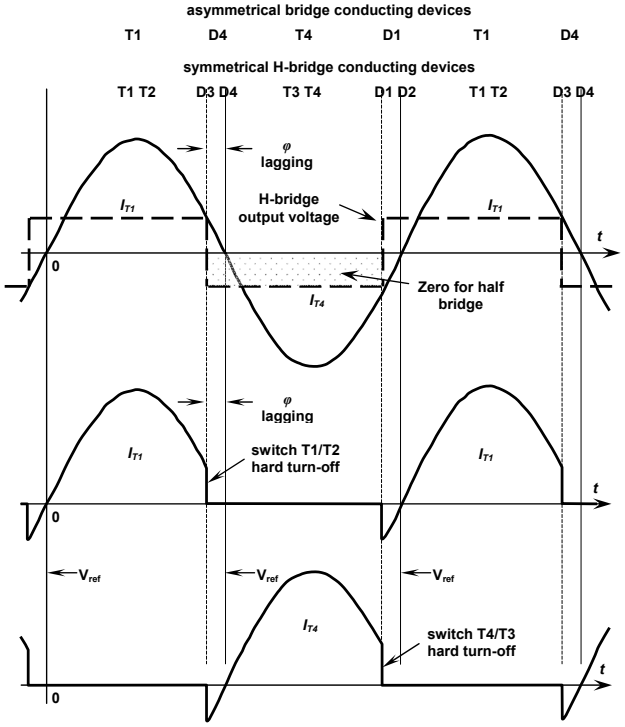


Figure 14.28. *Series L-C-R high Q resonance using the converter circuit in figure 14.27a and b, with a lagging power factor φ.*

2 - Leading operation (delaying the switch turn-on angle)

By operating the converter at a frequency below resonance (effectively by delaying switch turn-on until after the end of an oscillation cycle), the capacitor reactance

dominates and the load appears capacitive. The load current leads the voltage as shown in figure 14.29. This figure shows the conducting devices and that a switch is turned off when its parallel diode is conducting. Turn-off therefore occurs at a low current, while turn-on is as with a hard switched inductive load. Fast recovery diodes are therefore essential.

Operation and switch timing is as follows:

Diode D4 is conducting when switch T1 is turned on, which provides a step input voltage V_s to the series *L-C-R* load circuit, and the current continues to oscillate. The capacitor charges to a maximum voltage and the current reverses through D1, feeding energy back into the supply. T1 is then turned off with zero current.

The switch T4 is turned on, commutating D1, and the current oscillates through the zero volt loop created through T4 and the load. The oscillation current reverses through diode D4, when T4 is turned off with zero current.

T1 is turned on and the process continues.

Without the freewheel diodes the half oscillation cycles are controlled completely by the switches. On the other hand, with freewheel diodes, the timing of switch turn-on and turn-off is determined by the load current zeros, if maximum energy transfer to the load is to be gained.

The series circuit steady-state current at resonance for the asymmetrical bridge can be approximated by assuming $\omega_o \approx \omega$, such that in equation (14.52) $i_o = 0$:

$$i(\omega t) = \frac{1}{1 - e^{\frac{-\alpha\pi}{\omega}}} \times \frac{V_s}{\omega L} \times e^{-\alpha t} \times \sin \omega t \qquad 0 \le \omega t \le \pi \tag{14.66}$$

which is valid for the + V_s loop (through T1) and zero voltage loop (through T4) modes of cycle operation at resonance, provided the time reference is moved to the beginning of each half-cycle.

In steady-state the successive capacitor voltage maxima are

$$\hat{V}_c = V_s \frac{1}{1 - e^{-\alpha\pi/\omega}} \quad \text{and} \quad \check{V}_c = -V_s \frac{e^{-\alpha\pi/\omega}}{1 - e^{-\alpha\pi/\omega}} \tag{14.67}$$

The peak-to-peak capacitor voltage is therefore

$$V_{c_{p-p}} = \frac{1 + e^{-\alpha\pi/\omega}}{1 - e^{-\alpha\pi/\omega}} \times V_s = V_s \times \coth(\alpha\pi/2\omega) \approx \frac{2\omega}{\alpha\pi} \times V_s \tag{14.68}$$

The energy transferred to the load *R*, per half sine cycle (per current pulse) is

$$W = \int_0^{\pi/\omega} i^2 R dt = \int_0^{\pi/\omega} \left(\frac{1}{1 - e^{\frac{-\alpha\pi}{\omega}}} \times \frac{V_s}{\omega L} \times e^{-\alpha t} \times \sin \omega t \right)^2 R \, dt$$
$$= \tfrac{1}{2} C V_s^2 \coth\left(\alpha\pi / 2\omega\right) \tag{14.69}$$

14.3.2ii - Series resonant inverter – H-bridge inverter

When the load *Q* is not high, the capacitor voltage between successive absolute peaks decays significantly, leaving insufficient energy to maintain high efficiency energy transfer to the load *R*. In such cases the resonant circuit is re-enforced with energy from the dc source V_s every half-resonant cycle, by using a full H-bridge as shown in figure 14.27b.

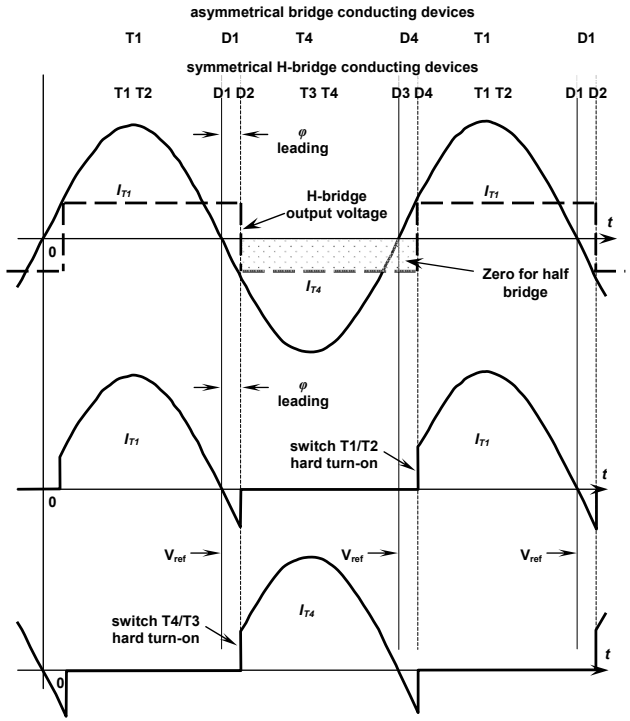


Figure 14.29. *Series L-C-R high Q resonance using the converter circuit in figure 14.27a and b, with a leading power factor φ.*

Operation is characterised by turning on switches T1 and T2 to provide energy from the source during one half of the cycle, then having turned T1 and T2 off, T3 and T4 are turned on for the second resonant half cycle. Energy is again drawn from the supply V_s, and when the current reaches zero, T3 and T4 are turned off.

Without bridge freewheel diodes, the switches support high reverse bias voltages, but the switches control the start of each oscillation half cycle. With freewheel diodes the oscillations can continue independent of the switch states. The diodes return energy to the supply, hence reducing the energy transferred to the load. Correct timing of the switches minimises currents in the freewheel diodes, hence minimises the energy needlessly being returned to the supply. Energy to the load

is maximised. As with the asymmetrical bridge, the switches can be used to control the effective load power factor. By advancing turn-off to before the switch current reaches zero, the load can be made to appear inductive, while delaying switch turn-on produces a capacitive load effect. The timing sequencing of the conducting devices, for load power factor control, are shown in figures 14.28 and 14.29.

The series circuit steady-state current at resonance for the symmetrical H-bridge can be approximated by assuming $\omega_o \approx \omega$, such that in equation (14.52) $i_o = 0$:

$$i(\omega t) = \frac{2}{1 - e^{\frac{-\alpha\pi}{\omega}}} \times \frac{V_s}{\omega L} \times e^{-\alpha t} \times \sin \omega t \qquad 0 \le \omega t \le \pi \qquad (14.70)$$

which is valid for the $\pm V_s$ voltage loops of cycle operation at resonance, provided the time reference is moved to the beginning of each half-cycle.

In steady-state the capacitor voltage maxima are

$$\hat{V}_c = V_s \frac{1 + e^{-\alpha\pi/\omega}}{1 - e^{-\alpha\pi/\omega}} = V_s \times \coth(\alpha\pi / 2\omega) = -\check{V}_c \qquad (14.71)$$

The peak-to-peak capacitor voltage is therefore

$$V_{c_{p-p}} = 2 \times \frac{1 + e^{-\alpha\pi/\omega}}{1 - e^{-\alpha\pi/\omega}} V_s = 2V_s \coth(\alpha\pi / 2\omega) \approx \frac{4\omega}{\alpha\pi} \times V_s \qquad (14.72)$$

The energy transferred to the load R, per half sine cycle (per current pulse) is

$$W = \int_0^{\pi/\omega} i^2 R \, dt = \int_0^{\pi/\omega} \left(\frac{2}{1 - e^{\frac{-\alpha\pi}{\omega}}} \times \frac{V_s}{\omega L} \times e^{-\alpha t} \times \sin \omega t \right)^2 R \, dt$$
$$= 2CV_s^2 \coth\left(\alpha\pi \big/ 2\omega\right) \qquad (14.73)$$

Notice the voltage swing is twice that with the asymmetrical bridge, hence importantly, the power delivered to the load is increased by a factor of four.

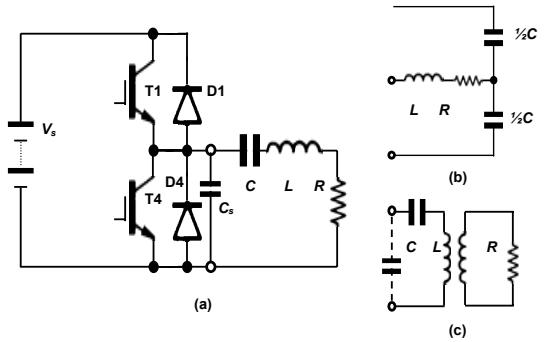


Figure 14.30. *Different resonant load arrangements: (a) switch turn-off snubber capacitor C_s; (b) split capacitor; and (c) series coupled circuit for induction heating.*

14.3.2iii - Circuit variations

Figure 14.30a shows an asymmetrical bridge with a turn-off snubber C_s, where $C_s << C$, hence resonant circuit properties are not affected. The capacitive turn-off snubber is only effective if switch turn-off is advanced such that switch hard turn-off would normally result, that is, the resonant circuit appears capacitive. The snubber acts on both switches since small signal wise (short dc sources), switches T1 and T4 are in parallel.

Figure 14.30b shows a series resonant load used with split resonant capacitance. Resonance re-enforcement occurs every half cycle as with the full H-bridge topology, but only two switches are used.

Figure 14.31c shows a transformer-coupled series circuit which equally could be a parallel circuit with C in parallel with the coupled circuit, as shown. Under light loads, the transformer magnetising current influences operation.

14.3.3 Parallel resonant inverters

Parallel resonant circuits use a current source inverter as considered in 14.2.1 and shown in figure 14.27c and d. If the load Q is high, then resonance need only be re-enforced every second half-cycle, thereby simplifying converter and control requirements. A common feature of parallel resonant circuits fed from a current source, is that commutation of the switches involves overlap where the output of the current source is briefly shorted.

14.3.3i - Parallel resonant inverter – single inverter leg

Figure 14.27c shows an asymmetrical converter for high Q parallel load circuits. Energy is provided from the constant current source every second half cycle by turning on switch T1. When T1 is turned on (and T3 is then turned off) the voltage across the L-C-R circuit resonates from zero to a maximum and back to zero volts. The energy in the inductor reaches a maximum at each zero voltage instant. T3 is turned on (at zero volts) to divert current from T1, which is then turned off with zero terminal voltage. The energy in the load inductor resonates within the load circuit, with the load in an open circuit state, since T1 is off. The sequence continues when the load voltage resonates back to zero as shown in figure 14.26b.

The parallel circuit steady-state voltage at resonance for the asymmetrical bridge can be approximated by assuming $\omega_o \approx \omega$, such that in equation (14.59) $v_o = 0$:

$$v(\omega t) = \frac{1}{1 - e^{\frac{-\alpha\pi}{\omega}}} \times \frac{I_s}{\omega C} \times e^{-\alpha t} \times \sin \omega t \qquad 0 \le \omega t \le \pi \qquad (14.74)$$

which is valid for both the $+I_s$ loop and open circuit load modes of cycle operation, provided the time reference is moved to the beginning of each half-cycle.

In steady-state the successive inductor current maxima are

$$\hat{I}_L = I_s \frac{1}{1 - e^{-\alpha\pi/\omega}} \quad \text{and} \quad \check{I}_L = I_s \frac{-e^{-\alpha\pi/\omega}}{1 - e^{-\alpha\pi/\omega}} \qquad (14.75)$$

The energy transferred to the load R, per half sine cycle (per voltage pulse) is

$$W = \int_0^{\pi/\omega} v^2/R \; dt = \int_0^{\pi/\omega} \left(\frac{1}{1-e^{\frac{-\alpha\pi}{\omega}}} \times \frac{I_s}{\omega C} \times e^{-\alpha t} \times \sin \omega t \right)^2 / R \, dt \qquad (14.76)$$
$$= \tfrac{1}{2} L I_s^2 \coth\left(\frac{\alpha\pi}{2\omega}\right)$$

14.3.3ii - Parallel resonant inverter – H-bridge inverter

If the load Q is low, or maximum energy transfer to the load is required, the full bridge converter shown in figure 14.26d is used.
Operation involves T1 and T2 directing the constant source current to the load and when the load voltage falls to zero, T3 and T4 are turned on (and T1 and T2 then turned off). Overlapping the switching sequence ensures a path always exists for the current source. At the next half sinusoidal cycle voltage zero, T1 and T2 are turned on and then T3 and T4 are turned off.
The parallel circuit steady-state voltage for the symmetrical H-bridge can be approximated by assuming $\omega_o \approx \omega$, such that in equation (14.59) $v_o = 0$:

$$v(\omega t) = \frac{2}{1-e^{\frac{-\alpha\pi}{\omega}}} \times \frac{I_s}{\omega C} \times e^{-\alpha t} \times \sin \omega t \qquad 0 \le \omega t \le \pi \qquad (14.77)$$

which is valid for both the + I_s loops of cycle operation, provided the time reference is moved to the beginning of each half-cycle.
In steady-state the successive inductor current maxima are

$$\hat{I}_L = I_s \frac{1+e^{-\alpha\pi/\omega}}{1-e^{-\alpha\pi/\omega}} = I_s \times \coth(\alpha\pi/2\omega) = -\check{I}_L \qquad (14.78)$$

The energy transferred to the load R, per half sine cycle (per voltage pulse) is

$$W = \int_0^{\pi/\omega} v^2/R \; dt = \int_0^{\pi/\omega} \left(\frac{2}{1-e^{\frac{-\alpha\pi}{\omega}}} \times \frac{I_s}{\omega C} \times e^{-\alpha t} \times \sin \omega t \right)^2 / R \, dt$$
$$= 2 L I_s^2 \coth\left(\frac{\alpha\pi}{2\omega}\right)$$

As with a series resonant circuit, the full bridge delivers four times more power to the load than the asymmetrical bridge circuit. Similarly, the load power and power factor can be controlled by operating above or below the resonant frequency, by delaying or advancing the appropriate switching instances.

Example 14.4: ***Half-bridge with a series L-C-R load***

An asymmetrical half-bridge inverter as shown in the figure 14.27a, with the dc rail *L-C* decoupling shown in figure 14.32, supplies a 1 ohm resistance load with series inductance 100 μH from a 340 V dc source. If the bridge is to operating at 10kHz, determine:

i. the necessary series C for resonance at 10kHz and the resultant Q
ii. the peak load current, its steady-state time domain solution, and peak capacitor voltages

iii. the bridge rms voltage and fundamental voltage across the *L-C-R* load
iv. the power delivered to the load and the frequency when half power is delivered to the load. What is the switching advance/delay time?
v. the peak blocking voltage of each semiconductor type (and for the case when the freewheel diodes are not employed)
vi. the average, rms, and peak current in the switches and diodes
vii. the resonant capacitor specification
viii. the dc supply current and the dc link capacitor rms current
ix. summarise conditions if the load is supplied from an H-bridge

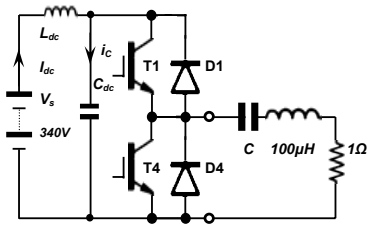


Figure 14.32. *Asymmetrical-bridge series-resonance circuit.*

Solution

i. From $\omega_o = 2\pi f_o = 1/\sqrt{LC}$ the necessary capacitance for resonance at 10kHz and 100μH is

$$C = \frac{1}{(2 \times \pi \times 10kHz)^2 \times 100\mu H} = 2.5\mu F$$

The circuit quality factor Q is given by

$$Q = \frac{Z_o}{R} = \sqrt{\frac{L}{C}} / R = \sqrt{\frac{100\mu H}{2.5\mu F}} / 1\Omega = 6.3$$

Therefore

$\alpha = 5 \times 10^3$ Ω/H $\omega = 62.6$ krad/s (9.968 kHz)
$\xi = 0.079$ $BW_s = 9.97$ krad/s (1.587kHz)
$Z_o = 6.3$ Ω

ii. The steady-state current is given by equation (14.66)

$$i(\omega t) = \frac{1}{1-e^{\frac{-\alpha\pi}{\omega}}} \times \frac{V_s}{\omega L} \times e^{-\alpha t} \times \sin \omega t$$
$$= 245.5 \times e^{-5000t} \times \sin(2\pi 10\text{kHz} \times t)$$

Since the Q is high, a reasonably accurate estimate of the peak current results if the current expression is evaluated at sin(½π), that is t =25μs, which yields $\hat{i}$ = 216.7A. The rms load current is 216.7A/√2 = 153.2A rms
From equation (14.67) the maximum capacitor voltages are

$$\hat{V}_c = V_s \frac{1}{1-e^{-\alpha\pi/\omega}} \quad \text{and} \quad \check{V}_c = V_s \frac{-e^{-\alpha\pi/\omega}}{1-e^{-\alpha\pi/\omega}}$$
$$= \frac{340\text{V}}{1-e^{-0.25}} \qquad = -\frac{340\text{V}e^{-0.25}}{1-e^{-0.25}}$$
$$= 1537\text{V} \qquad = -1197\text{V}$$

iii. The bridge output voltage is a square wave of magnitude 340V and 0V, with a 50% duty cycle. The rms output voltage is therefore 340/√2=240.4V.
Since the load is at resonance, the current is in phase with the fundamental of the bridge output voltage. The fundament voltage magnitude is given by

$$b_1 = \frac{1}{\pi}\int_0^{\pi} V_s \sin 1\omega t = \frac{2V_s}{\pi} = 216.5\text{V peak}$$
$$\equiv \frac{\sqrt{2}V_s}{\pi} = 153\text{V rms}$$

The rms load current results because of the fundamental voltage, that is, the peak sine current is 216.5V/1Ω = 216.5A peak or 153V/1Ω = 153A rms. This agrees with the current values calculated in part b.

iv. The power delivered to the load is given by

$$P = i_{rms}^2 R = i_{b1}^2 R$$
$$= 153\text{A}^2 \times 1\Omega = 23.41\text{kW}$$

Substitution into equation (14.69) gives 23.15kW at a pulse rate of 2×10kHz. Alternately

$$P = V_s \times \bar{I} = V_s \times 0.45 \times I_{rms}$$
$$= 340\text{V} \times 0.45 \times 153\text{A} = 23.42\text{kW}$$

The half-power frequencies are when the reactive voltage equals the resistive voltage.

$$f_t^u = f_o \pm \frac{R}{4\pi L}$$
$$= 10\text{kHz} \pm 796\text{Hz}$$

Thus at 9204 Hz and 10796 Hz the voltage across the resistive part of the load is reduced to 1/√2 of the inverter output voltage. The power (proportional to voltage squared) is therefore halved at the half-power frequencies.
Operating above resonance, $f > f_o$ produces an inductive load and this is achieved by turning T1 and T4 off prematurely. Zero current turn-on occurs, but hard switching results at turn-off. To operate at the 10796Hz (92.6μs) upper half-power frequency the period has to be reduced from 100μs (10kHz) to 92.6μs. The period of each half cycle has to be reduced by ½×(100μs - 92.6μs) = 3.7μs
Operating below resonance, $f < f_o$ produces a capacitive load and this is achieved by turning T1 and T4 on late. Zero current turn-off occurs, but hard switching

results at turn-on. By delaying turn-on of each switch by ½×(109μs - 100μs), 4.5μs, the effective oscillation frequency will be decreased to the lower half-power frequency, 9204Hz.

v. The bridge diodes, which do not conduct at resonance, clamp switch and diode maximum supporting voltages to the rail voltage, 340V dc.
Note that if clamping diodes were not employed the device maximum off-state voltages would occur during switch change over, when one switch has just been turned off, and just before the on-going switch is turned on. The load current is zero, so the load terminal voltage is the capacitor voltage.
Switch T1 would need to support
a forward voltage of V_s - $\check{v}$ = 340V + 1197V =1537V = $\hat{v}$ and
a reverse voltage of $\hat{v}$ - V_s = 1537V - 340V = 1197V = - $\check{v}$, while
Switch T4 supports
a forward voltage of $\hat{v}$ = 1537V and
a reverse voltage of - $\check{v}$ = 1197V.
Thyristor family devices must be used, or devices with a series connected diode, which will increase the converter on-state losses.

vi. At resonance the two freewheel diodes do not conduct.
The rms load current is 153.2 A at 10 kHz, where switch T1 conducts half the cycle and T4 conducts the other half which is the opposite polarity of the cycle. Each switch therefore has an rms current rating of 153.2/√2 = 108.3A rms.
Since both switches conduct the same current shape, each has an average current rating of a half-wave rectified sine of magnitude 216.5A, that is

$$\bar{I}_{T1} = \frac{1}{2\pi}\int_0^{\pi} 216.5 \sin\omega t\, dt = \frac{1}{\pi} \times 216.5\text{A}$$
$$= 0.45 \times 216.5/\sqrt{2} = 97.4\text{A}$$

By Kirchhoff's current law, this current value for T1 is also equal to the average dc input current from the supply V_s.

vii. The capacitor has a bipolar voltage and current requirement of ±1537V and ±216.7 A. The rms ratings are therefore ≈1087V rms and 153A rms. A metallised polypropylene capacitor capable of 10kHz ac operation, with a maximum dv/dt rating of approximately ½×(1537+1197)×ω, that is 85.6V/μs, is required.

viii. The dc supply current is the average value of the half-wave rectified sinusoidal load current, which is the average current in T1. That is

$$I_{dc} = 0.45 \times 153.1\text{A rms}$$
$$= 68.9\text{A dc}$$

The rms current in the dc link capacitor is related to the dc input current and switch T1 rms current (as found in part f), by

$$I_c = \sqrt{I_{T1}^2 - I_{dc}^2}$$
$$= \sqrt{108.3^2 - 68.9^2} = 83.6\text{A rms}$$

ix. The load dependant parameters C, ω_o, ω, α, Q, BW, ξ, and half power points remain unchanged.

From equation (14.70) the steady-state current is double that for the asymmetrical bridge,

$$i(\omega t) = \frac{2}{1-e^{\frac{-\alpha\pi}{\omega}}} \times \frac{V_s}{\omega L} \times e^{-\alpha t} \times \sin \omega t$$

$$= 491 \times e^{-5000t} \times \sin(2\pi 10\text{kHz} \times t)$$

The peak current is $\hat{i} = 433.4\text{A}$.

The rms load current is 433.4A/√2 = 306.4A rms

From equation (14.71) both the maximum capacitor voltages are

$$\hat{V}_c = V_s \frac{1+e^{-\alpha\pi/\omega}}{1-e^{-\alpha\pi/\omega}} = -\check{V}_c$$

$$= 340\text{V} \frac{1+e^{-0.25}}{1-e^{-0.25}} = 2734\text{V}$$

The power delivered to the load is four times the asymmetrical case and is

$$P = i_{rms}^2 R = 306.4\text{A}^2 \times 1\Omega = 93.88\text{kW}$$

The average switch current is 194.8A, but the average supply current is four times the asymmetrical case and is 275.5.6A.

♣

14.3.4 *Single-switch current source series resonant inverter*

The inverter in figure 14.31 is applicable to high Q load circuits such that the output is essentially sinusoidal, with zero average current. Based on the operating mechanisms, a sinusoidal current implies the switch has a 50% duty cycle. The switch turns on and off at zero volts so switch losses are low and the operating frequency can be high. The input inductor L_{large} in conjunction with the input voltage source, during steady state operation, act as a current source input, I_s, for the resonant circuit, such that $V_s I_s$ is equal to the power delivered to the load R.

When the switch T1 is turned on, with zero terminal voltage, it conducts both the constant current I_s and the current i_o resonating in the output circuit, as shown in the circuit waveforms in figure 14.31. The resonating load current builds up. The switch T1, which is in parallel with C_s, is turned off. Current from the switch is diverted to C_s, which charges from an initial voltage of zero. C_s thus forms a turn-off snubber in parallel with T1. The charge on C_s eventually resonates back to zero at which instant the switch is turned on, again, with zero turn-on loss.

The resonant frequency is $\omega_o = 1/\sqrt{L_o C_o}$ and because of the high Q, a small change in the switching frequency significantly decreases the output current, hence output voltage.

As with any current source inverter, the peak switch voltage is in excess of V_s. Since the current is sinusoidal, the average load voltage and inductor voltage are zero. Therefore the average voltage across C_o and C_s is the supply voltage V_s. The peak switch voltage can be estimated to be in excess of V_s /0.45 which is based on a half-wave rectified average sinusoidal voltage.

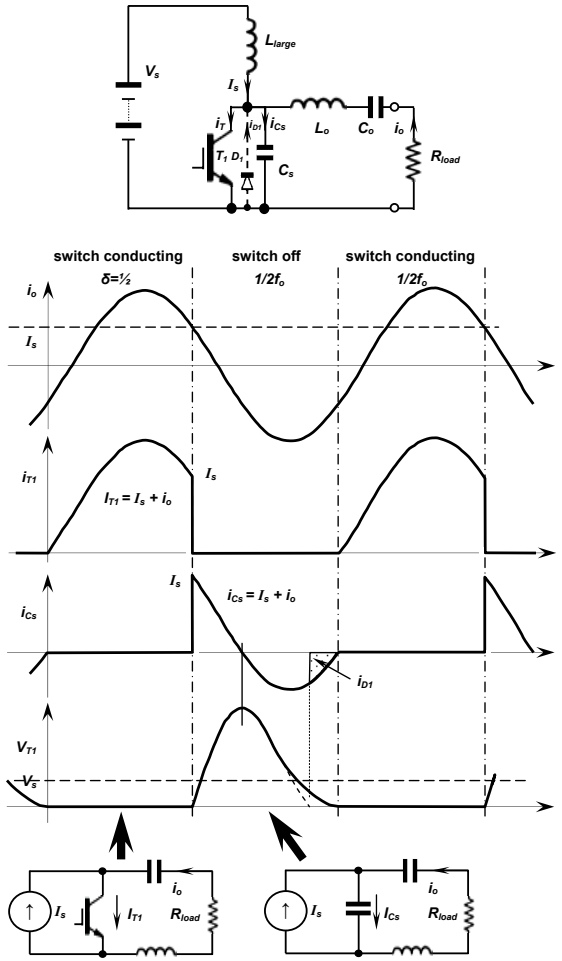


Figure 14.31. *Single-switch, current-source resonant converter circuit and waveforms.*

If the load conditions change and the switch duty cycle is varied from δ = ½, circuit voltages increase and capacitor C_s voltage discharges before the circuit current reaches zero. The capacitor and switch are bypassed with current flowing through the diode D1. This diode prevents the switch from experiencing a negative voltage and the capacitor from charging negatively.
Although such resonant converters offer features such as low switching losses and low radiated EMI, optimal control and performance are difficult to maintain and extremely high circuit voltages occur at low duty cycles.

14.4 Multi-level voltage-source inverters

The conventional three-phase, six-switch dc to ac voltage-source inverter is shown in figure 14.3. Each of the three inverter legs has an output which can provide one of two voltage levels, V_s, when the upper switch (or diode) is on, and 0 when the lower switch (or diode) conducts. The quality of the output waveform is determined by the resolution and switching frequency of the pwm technique used.

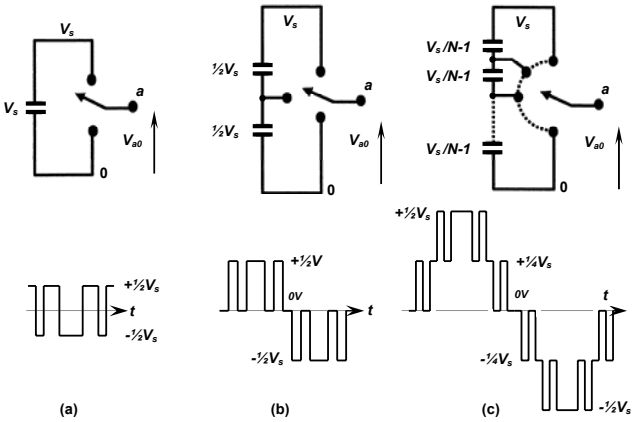


Figure 14.33. *One phase leg of a voltage-source bridge inverter with: (a) two levels; (b) three levels; and (c) N-levels, with N-1 capacitors and waveform for five levels.*

A multilevel inverter (directly or indirectly) divides the dc rail, so that the output of the leg can be more than two levels, as shown in figure 14.33 for a diode clamped multilevel inverter model. In this way, the output quality is improved because both pulse width modulation and amplitude modulation can be used. The output pole is made from more than two series connected switches, so the total dc rail can be the sum of the voltage rating of the individual switches. Very high output voltages can

be achieved, where each device does not experience a voltage in excess of its individual rating.
A multilevel inverter allows higher output voltages with low distortion (due to the use of both pulse width and amplitude modulation) and reduced output *dv/dt*.
There are three main types of multilevel converters

- Diode clamped
- Flying capacitor, and
- Cascaded H-bridge

14.4.1 Diode clamped multilevel inverter

Figure 14.33 shows the basic principle of the diode clamped (or neutral point clamped) multilevel inverter, where only one dc supply, V_s, is used and N is the number levels present in the output voltage between the leg output and the inverter negative terminal, $V_{a\text{-}neg}$. The capacitors split the dc rail voltage into a number of lower voltage levels, each of which can be tapped and connected to the leg output through switches. Only one string of series connected capacitors is used for any number of output phase legs.
The number of levels in the line-to-line voltage waveform will be

$$k = 2N - 1 \tag{14.79}$$

while the number of levels in the line to load neutral of a star (wye) load will be

$$p = 2k - 1 \tag{14.80}$$

The number of capacitors required, independent of the number of phase, is

$$N_{cap} = N - 1 \tag{14.81}$$

while the number of clamping diodes per phase is

$$D_{clamp} = 2(N - 1) \tag{14.82}$$

The number of possible switch states is

$$n_{states} = N^{phases} \tag{14.83}$$

and the number of switches in each leg is

$$S_n = 2(N - 1) \tag{14.84}$$

The basic three-level inverter is shown in figure 14.34, along with the basic three-level voltage from the leg output to centre tap of the capacitor string, R (neutral point). When switch T_1 is on, its complement T_1' is off, and visa versa. Similarly for the pair of switches T_2 and T_2'. Specifically T_1 and T_2 on give the output $+½V_s$, T_1' and T_2' on give the output $-½V_s$, and T_2 and T_1' on give the output 0. Essential to attaining these output levels, are the clamping diodes D_u and D_l. These two diodes clamp the outer switches to the capacitor string mid-point, which is half the dc rail voltage. In this way, no switch experiences a voltage in excess of half the dc rail voltage. Inner switches must be turned on (or off) before outer switches are turned on (or off).
The five-level inverter uses four capacitors and eight switches in each inverter leg. A set of clamping diodes (three in total for each leg) clamp the complementary switches in each leg. The output is characterised by having five levels, $\pm½V_s$, $\pm¼V_s$, and zero. Some of the clamping diodes experience voltages in excess of that experienced by the main switches. Series connection of some of the clamping

diodes avoids this limitation, but at the expense of increasing the number of clamping diodes from 2× (*N*-1) to (*N*-1)×(*N*-2) per phase. Thus, depending on the diode position in the structure, two diodes have blocking requirements of

$$V_{RB} = \frac{N-1-k}{N-1} V_s \qquad (14.85)$$

where $1 \le k \le N\text{-}2$. These diodes require series connection of diodes, if all devices in the structure are to support $V_s/(N\text{-}1)$. For $N > 2$, capacitor imbalance occurs. The general output voltage, to the centre of the capacitor string is given by

$$V_{an} = \frac{V_s}{N-1}(T_1 + T_2 + .. \quad .. + T_{N-1} - \tfrac{1}{2}(N-1)) \qquad (14.86)$$

Table 14.4. Conduction paths in the diode clamped three-level inverter

V_{out}	On switches	Current path		Active clamping diodes
		$+ i_L$	$- i_L$	
½ V_s	T_1 T_2	T_1 T_2	D_1 D_2	none
0	T_1' T_2	D_{cu} T_2	T_1' D_{cl}	D_{cu} D_{cl}
-½ V_s	T_1' T_2'	T_1' T_2'	D_1' D_2'	none

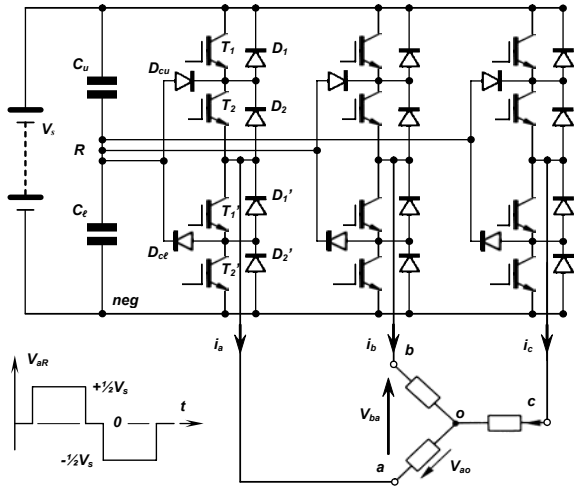


Figure 14.34. *Three-phase, voltage-source, three-level, diode-clamped (NPC) bridge inverter.*

14.4.2 Flying capacitor multilevel inverter

One leg of a fly-capacitor clamped five-level voltage source inverter is shown in figure 14.35, where capacitors are used to clamp the switch voltages to ¼V_s. The available output voltages are ±½V_s, ±¼V_s, and 0, where the output is connected to the dc link (V_s and 0) indirectly via capacitors. Figure 14.35 shows that in general, switches T_n and T_{n+1} connect to capacitor C_n. The configuration offers more available switch states than the clamped diode inverter, and this redundancy allows better, flexible control of capacitor voltages. For example, Table 14.5 shows that there are six states for obtaining 0V output, and four states for each of ±¼V_s. The output states ±½V_s do not involve the capacitors, hence they offer no redundant states. The basic switch restriction is that only one complementary switch (e.g., T_4 or T_4') is on at any time, so as to prevent shorting of a flying capacitor.
The number of levels in the line-to-line voltage waveform will be

$$k = 2N - 1 \qquad (14.87)$$

while the number of levels in the line to load neutral of a star (wye) load will be

$$p = 2k - 1 \qquad (14.88)$$

The number of capacitors required, which is dependent of the number of phase, is for each phase,

$$N_{cap} = \tfrac{1}{2}(N-1)(N-2) \qquad (14.89)$$

Table 14.5. Five-level flying-capacitor inverter output states (phase A to R)

mode	V_{AR}	switching states				capacitors			paths
		T_1	T_2	T_3	T_4	C_1	C_2	C_3	
1	½V_s	1	1	1	1	=	=	=	½V_s
2	¼V_s	1	1	1	0	=	=	+	½V_s -V_{C3}
N-1 states		1	1	0	1	=	+	-	½V_s -V_{C2}+V_{C3}
		1	0	1	1	+	-	=	½V_s-V_{C1}+V_{C2}
		0	1	1	1	-	=	=	-½V_s+V_{C1}
3	0	1	1	0	0	=	+	=	½V_s -V_{C2}
N^2-4N+1 states		1	0	1	0	+	-	+	½V_s-V_{C1}+V_{C2} -V_{C3}
		0	1	1	0	-	=	+	-½V_s+V_{C1}-V_{C3}
		1	0	0	1	+	=	-	½V_s-V_{C1+}-V_{C3}
		0	1	0	1	-	+	-	-½V_s+V_{C1}-V_{C2}+V_{C3}
		0	0	1	1	=	-	=	-½V_s +V_{C2}
4	-¼V_s	1	0	0	0	+	=	=	½V_s-V_{C1}
N-1 states		0	1	0	0	-	+	=	-½V_s+V_{C1}-V_{C2}
		0	0	1	0	=	-	+	-½V_s -V_{C2} -V_{C3}
		0	0	0	1	=	=	-	-½V_s +V_{C3}
5	-½V_s	0	0	0	0	=	=	=	-½V_s

The number of possible switch states is

$$n_{states} = N^{phases} \tag{14.90}$$

and the number of switches in each leg is

$$S_n = 2(N-1) \tag{14.91}$$

The current output paths in Table 14.5 are made up by the series (and parallel) connection of the flying capacitors through the turn-on of the appropriate switches. Capacitors shown as negative are discharging in the formed path, while those shown as positive are charging. Use of the shown redundant states allows control of the voltage level on all the flying capacitors, while providing the desired output voltages.

A feature of the flying capacitor multilevel inverter is its ride through capability due to the large capacitance used. On the other hand, the capacitors have a high voltage rating and suffer from high current ripple, since they conduct the full load current when connected into an active output voltage state. Capacitor initial charging is also problematic' especially given the capacitors for each leg are independent.

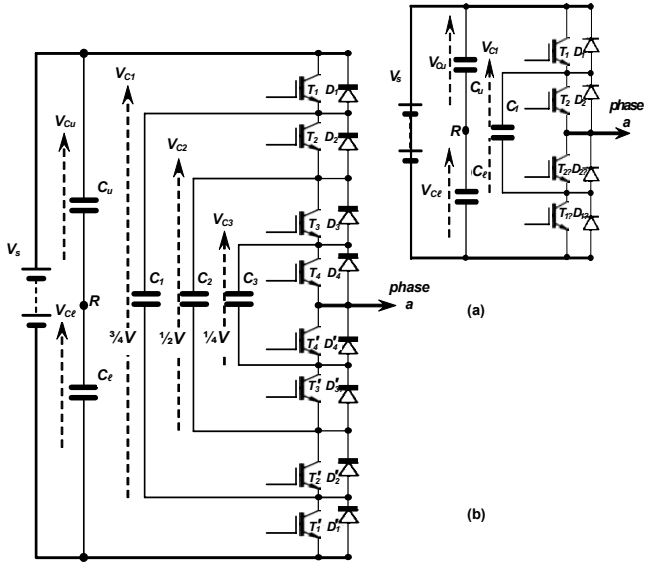


Figure 14.35. *One leg of a voltage-source: (a) three-level and (b) five-level, flying capacitor clamped bridge inverter.*

14.4.3 Cascaded H-bridge multilevel inverter

The *N*-level cascaded H-bridge, multilevel inverter comprises ½(*N*-1) series connected single phase H-bridges per phase, for which each H-bridge has its own isolated dc source. Three output voltages are possible, $\pm V_s$, and zero, giving a total number of states of $3^{½(N-1)}$, where *N* is odd. Figure 14.36 shows one phase of a seven-level cascaded H-bridge inverter.

The cascaded H-bridge multilevel inverter is based on multiple two level inverter outputs (each H-bridge), with the output of each phase shifted. Despite four diodes and switches, it achieves the greatest number of output voltage levels for the fewest switches.

Its main limitation lies in its need for isolated power sources for each level and for each phase, although for VA compensation, capacitors replace the dc supplies, and the necessary capacitor energy is only to replace losses due to inverter losses. Its modular structure of identical H-bridges is a positive feature.

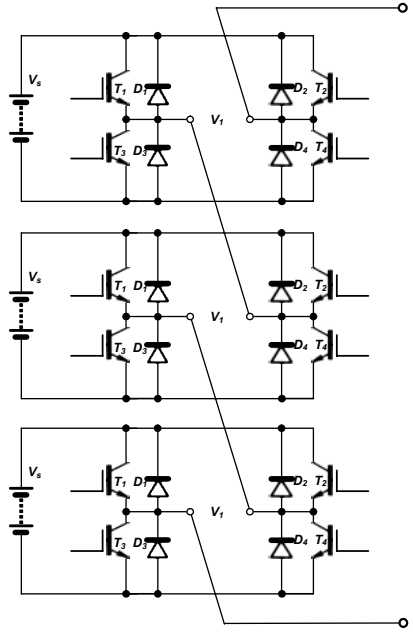


Figure 14.36. *One leg of a voltage-source, seven-level, cascaded H-bridge inverter.*

The number of levels in the line-to-line voltage waveform will be

$$k = 2N - 1 \tag{14.92}$$

while the number of levels in the line to load neutral of a star (wye) load will be

$$p = 2k - 1 \tag{14.93}$$

The number of capacitors or isolated supplies required per phase is

$$N_{cap} = \tfrac{1}{2}(N - 1) \tag{14.94}$$

The number of possible switch states is

$$n_{states} = N^{phases} \tag{14.95}$$

and the number of switches in each leg is

$$S_n = 2(N - 1) \tag{14.96}$$

Table 14.6. Three output states of H-bridge and their current paths.

V_e	On switches	Bidirectional current paths	
		$+ i_L$	$- i_L$
V_s	T_2 T_3	T_2 T_3	D_2 D_3
0	none	D_4 D_1	D_2 D_3
$-V_s$	T_1 T_4	T_1 T_4	D_2 D_3

A comparison between the three basic multilevel inverters is possible from the numerical summary of component numbers for each inverter, as in Table 14.7. The diode clamped inverter requires many clamping diodes; the flying capacitor inverter requires many independent capacitors; while the cascaded inverter requires many isolated power supplies.

Table 14.7. Multilevel inverter component count, per phase.

Inverter type	levels			switches & diodes	diodes clamping	flying capacitors	Level capacitors	Isolated supplies
	$V_{A\text{-}0V}$	$V_{A\text{-}B}$	$V_{A\text{-}N}$					
diode clamped	*N*	*2N-1*	*4N-3*	*2(N-1)*	*(N-1)(N-2)*	0	*(N-1)*	0
fly capacitor	*N*	*2N-1*	*4N-3*	*2(N-1)*	0	*½(N-1)(N-2)*	*(N-1)*	0
cascade	*N*	*2N-1*	*4N-3*	*2(N-1)*	0	0	*½ (N-1)**	*½(N-1)**

* either / or

14.4.4 PWM for multilevel inverters

Two basic approaches can be used to generate the necessary pwm signal for multilevel inverters. Each approach is based on the extension of a two level equivalent.

- Modulating waveform comparison with offset triangular carriers
- Space vector modulation based on a rotating vector in multilevel space

14.4.4i Multiple offset triangular carriers

Various sinusoidal pwm techniques were considered in section 14.1.3v and 14.1.3vi of this chapter. Figure 14.37 shows how a triangular carrier is associate with each complementary switch pair, four carriers (*N*-1) for the five-level inverter as illustrated. The parts of figure 14.37 show how the four individual carriers can be displaced with respect to one another. The figure also shows how triplen injection is incorporated. The appropriate five-level switch states, as in tables 14.4 to 14.6, can be used to decode the necessary switching sequences. To minimise losses, switching only occurs between adjacent levels.

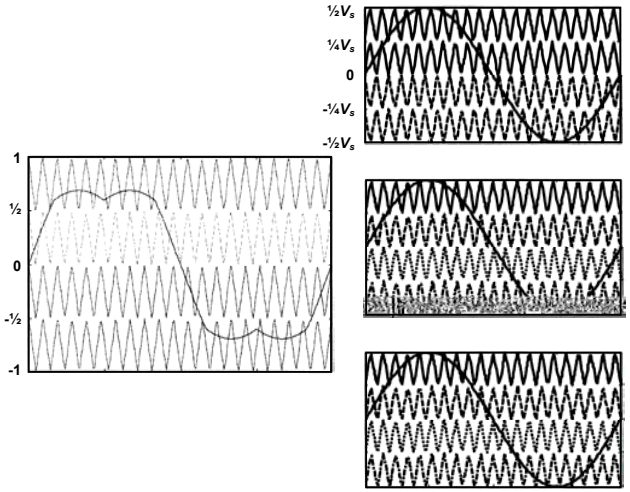


Figure 14.37. *Multi-carrier based pwm generation for one phase of a voltage-source, five-level, inverter.*

14.4.4ii Multilevel rotating voltage space vector

Space vector modulation for the two-level inverter was considered in section 14.1.3vi of this chapter. The basic hexagon shape for two levels is extended to higher levels as shown in figure 14.38, for three levels. The number of triangles, vectors, and states increases rapidly as the level number increases.

Table 14.8. Properties of *N*-level vector spaces

levels	states	triangles	vectors	vectors in each hexagon
N	N^3	$6(N-1)^2$	$3N(N-1)+1$	
2	8	6	7	(1+6)
3	27	24	19	(1+6)+12
5	125	96	61	(1+6)+12+18+24

From table 14.8, the states for the two and three level inverters can be specified as follows.

The 2-level inverter

The zero state matrix is

$$\begin{bmatrix}000 & 111\end{bmatrix}$$

The first and only hexagon is shown in figure 14.18a.

$$\begin{bmatrix}100 & 110 & 010 & 011 & 001 & 101\end{bmatrix}$$

The three level inverter

The zero state matrix is

$$\begin{bmatrix}000 & 111 & 222\end{bmatrix}$$

The first hexagon matrix is

$$\begin{bmatrix}100 & 110 & 010 & 011 & 001 & 101\\ 211 & 221 & 121 & 122 & 112 & 212\end{bmatrix}$$

The second hexagon matrix is

$$\begin{bmatrix}200 & 210 & 220 & 120 & 020 & 021 & 022 & 012 & 002 & 102 & 202 & 201\end{bmatrix}$$

These pole states are shown figure 14.38.

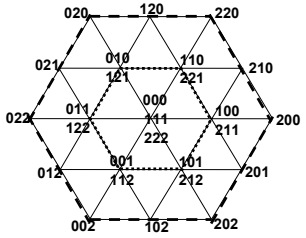


Figure 14.38. *Rotating voltage space vector approached applied to three phases of a voltage-source three-level, inverter.*

A`0´ represents the minimum voltage obtainable from the multilevel converter and *N-1* represents the maximum value. For example, in a two-level converter,`0´ is equivalent to 0V and `1´ is equivalent to $V_s$, where $V_s$ is the converter DC link voltage. In a three-level converter`0´ is equivalent to $-½V_s$,`1´ is equivalent to 0 V, and '2' is equivalent to $½V_s$ where V_s is the link voltage of the multilevel converter.

When the rotating vector is drawn in the vector space, it is decomposed into vectors bordering the triangle it lies in. When operating in the outer hexagon, the vectors states used in the inner most hexagon mean that that level of the converter is operating with a six-step quasi-square output voltage waveform, to which is added a modulated square waveform for the next higher level.

14.5 Reversible converters

Power inversion by phase angle control is attained with a fully controlled single-phase converter as discussed in section 11.3.3. Power regeneration is also possible with the fully controlled three-phase converter shown in figure 11.17. If a fully controlled converter supplies a dc machine, two-quadrant control is possible (QI and QIV), motoring in one direction of rotation and generating in the other direction. Power regeneration into the supply is achieved by reversing the dc output voltage by controlling the converter phase delay angle.

The dual or double converter circuit in figure 14.39a and b will accommodate four-quadrant dc machine operation, where the circuit performs as two fully controlled converters in anti-parallel. Each converter is able to rectify and invert, but because of their inverse parallel connection, one converter (the positive converter P) operates in quadrants QI and QIV, while the other (the negative converter N) operates in quadrants QII and QIII, as shown in figure 14.40.

The two converters can be operated synchronously, called *simultaneous control* or independently where one is always blocking, called *independent control*.

14.5.1 Independent control

Simultaneous converter control can be used if continuous load current can be guaranteed. Only one converter, depending on the quadrant, need operate at anyone time (the other is in a blocking state), as shown in figure 14.39a. No circulating currents arise due to possible mismatched converter output voltages. The continuous current condition may be difficult to ensure at light load levels. Additional series armature inductance, L in figure 14.39a and b, helps with current smoothing and ensuring continuous machine current.

A machine rotational direction change is affected by the following converter operating procedure.

- Initially the motor is operating in quadrant I, with $0° \le \alpha_1 \le 90°$ for the positive converter P. The negative converter, N, is in the fully blocking state, with all thyristors turned off.
- The positive converter is put into the inverting mode with $90° \le \alpha_1 \le 180°$, changing the average output voltage from positive to negative. The machine current rapidly falls to zero. The machine rotational speed slows, the rate depending on the load inertia.
- After a dead time, the positive converter blocks and the negative converter N starts in a motor braking mode in quadrant II. The motor speed falls rapidly to zero.

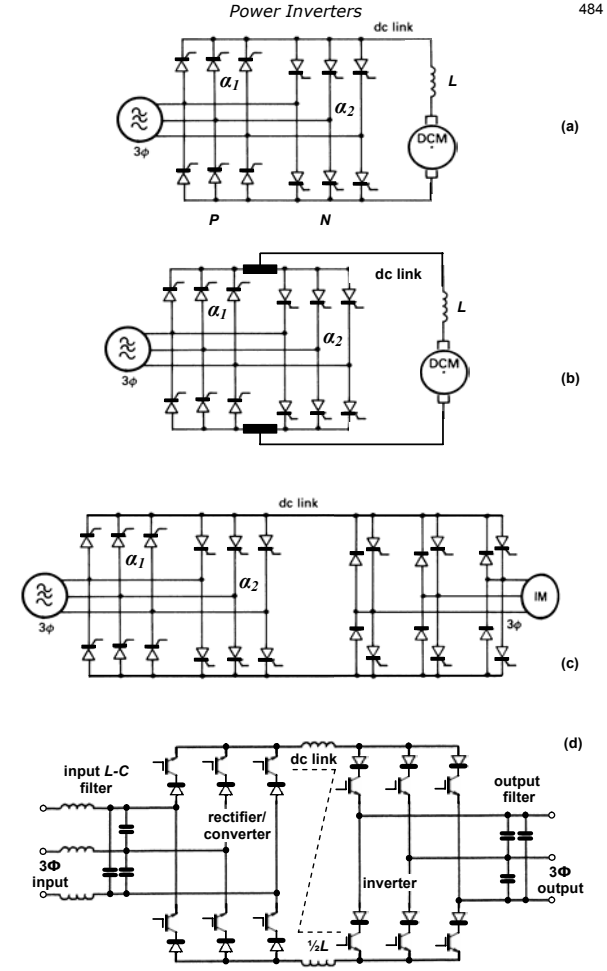


Figure 14.39. *Reversible converter allowing four-quadrant control of: (a) a dc machine with independent converters; (b) a dc machine with simultaneously controlled converters; and (c) voltage and (d) current feed induction machine.*

- The second converter operates in quadrant III and rapidly accelerates the motor in the opposite direction, with $0° \le \alpha_2 \le 90°$.

The dead time before turning on the negative converter N is to ensure the positive converter P is fully off, otherwise the three-phase input voltage lines may short through the converters. Such a current condition cannot be controlled with line-commutated thyristors. Operation is characterised by transitions from QI to QII to QIII for reversal, and transitions from QIII to QIV to QI for returning to the original direction of rotation.

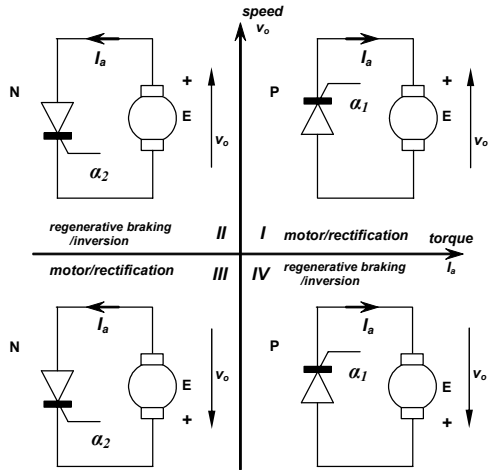


Figure 14.40. *Four quadrants of reversible converter operation.*

14.5.2 Simultaneous control

Simultaneous converter control, also called circulating current control, functions with both converters always in operation which give a faster dynamic response than when the converters are used mutually exclusively. To avoid supply short circuits requires that the output voltage of both converters (rectifier V_r and inverter V_i) be the same in order to minimise circulating currents.

$$\begin{aligned} \overline{V}_r + \overline{V}_i &= 0 \\ V\cos\alpha_1 + V\cos\alpha_2 &= 0 \\ \cos\alpha_1 + \cos\alpha_2 &= 0 \\ \text{that is } \alpha_1 + \alpha_2 &= 180° \end{aligned} \qquad (14.97)$$

As shown in equation (14.97), this implies that both converters operate with firing angles that sum to 180°. Each converter produces the opposite polarity output voltage, which is cancelled by reversing the relative output connections. Under such conditions the load current can be maintained continuous. To minimize any circulating current due to ripple voltage produced by instantaneous voltage difference between the two converters, inductance is usually inserted between each converter and the dc machine load, as shown in figure 14.39b. Adversely the cost and weight are increased, and the supply power factor and drive efficiency are decreased, compared to that obtained with independently controlled converters.

A machine rotational direction change is affected by the following converter operating procedure.

- Initially the motor is operating in quadrant I for the rectifying, positive converter, with $0° \leq \alpha_1 \leq 90°$. The other converter is operating in the inverting mode with $90° \leq \alpha_2 \leq 180°$, such that $\alpha_1 + \alpha_2 = 180°$. The output voltage for both converters is the same, and the negative converter N carries only the circulating current.
- For rotational direction reversal, $\alpha_1 \geq 90°$ and $\alpha_2 \leq 90°$, such that $\alpha_1 + \alpha_2 = 180°$. The armature back emf voltage now exceeds the converter output voltages, and current diverts to the negative converter N and the machine regeneratively brakes, operating in quadrant II. The current rapidly falls to zero and the positive converter P carries only the ac circulating current.
- The speed rapidly falls to zero, with $\alpha_1 = \alpha_2 = 90°$ giving zero output voltage, so as to control the armature current since the back emf is zero. Then with $\alpha_2 < 90°$ the machine rapidly accelerates in quadrant III, in the reverse direction to the original rotation.

For reversing the direction of rotation from Q III the operation sequence is QIII to QIV to QI. Since no converter dead time is introduced, a fast dynamic response can be attained. A small dc circulating current is deliberately maintained, that is greater in magnitude than the peak of the ac ripple current. The ac current can then flow continuously in both converters, both of which can operate in the continuous conduction mode without the need for continuous converter current reversal operation.

14.5.3 Inverter regeneration

The bridge freewheel diodes of a three-phase inverter restrict the dc rail or dc link voltage from reversing. The dual or double converter circuit in figure 14.39c will allow inversion with a three-phase voltage fed inverter. One converter rectifies, the other converter inverts, functioning as a self-commutated inverter, transferring power from the dc link to the ac supply. Complete four-quadrant control of the three-phase ac machine on the inverter is achieved in conjunction with control of the dc to ac inverter. That is, motor reversal is achieved by effectively interchanging the pwm control signals associated with two phases. The real power flow back into the ac supply is controlled by the converter phase delay angle, while the reactive power flow is controlled by the voltage magnitude. The angle and voltage are not independent. In the case of a pwm controlled inverter fed ac

machine, the ac to dc converter can be uncontrolled, using all diodes, since dc output voltage reversal is not utilised.

Figure 14.39d shows a fully reversible current controlled converter/inverter configuration, using self-commutating devices. The use of self-commutated switches (rather than mains commutated converter thyristors) offers the possibility to minimise the input current distortion and to reduce the inductor size hence improve the dynamic current response. The switch series diodes are essential since the shown IGBTs have no useable reverse blocking capability. The use of reverse blocking GCTs avoids the need for the series blocking diodes, which reduces the on-state voltage losses but increases gate drive complexity. Series connection of devices is necessary above a few kV, and above 1 MVA the GCT dominates.

14.6 Standby inverters and uninterruptible power supplies

Standby inverters and uninterruptible power supplies (ups's) provide a 50/60 Hz supply in the event of an ac mains failure. An ups must provide ac output such that mains failure is undetected by the load. To achieve this, an ups continually feeds the load from an inverter. A load that can tolerate a short interruption of the ac supply is fed from a *standby inverter* which becomes operational within 1-5 ms after the ac supply failure. In communications, computing, and automated production lines, ups's are essential for even brownouts (V and f outside bounds for reliable equipment operation), while in lighting and heating applications, standby inverters are used since a few missing ac cycles (due to a blackout – total interruption of the mains power)) may be tolerated. In each power supply case, the alternative energy source is a standby dc battery. The ups keeps the battery charged when the ac input is supplying the output power.

14.6.1 Single-phase UPS

A basic single-phase UPS is shown in figure 14.41. A key safety objective is to retain the supply neutral at both the supply input and the ac output, without resorting to any from of isolating transformer. Consequently, the input ac mains is half-wave rectified by diodes D_R^+ and D_R^-. Boost converters on the positive and negative groups ensure supply sinusoidal input current and unity power factor. The output H-bridge (T_1-T_4) uses pwm and feedback control to produce a fixed frequency and magnitude output (and ac mains phase synchronisation if required), which is filtered by an *L*-*C* filter. In the event of a loss of the ac supply, the backup batteries, V^+ and V^-, provide energy to the boost converters, hence to the output inverter. The battery backup voltage magnitude is much less than the ac supply magnitude and diodes, D_B^+ and D_B^-, isolate the batteries from the rectified ac supply voltage. The shown ups has two basic limitations that manufactures strive to overt.

- If the battery is to be connected to neutral, then two batteries are necessary. Proprietary attempts using only one battery involve circuit complications and limitations. At best, with one battery, it is one forward biased diode voltage drop from neutral.

- Because the batteries supplies are not isolated during normal operation, during part of the mains cycle near zero voltage, the batteries provide energy. This decreases their lifetime and necessitates more complicated trickle charge circuits. The input current is also distorted at the 0V crossover. Replacement of the blocking diodes D_B by switches involves complexity and battery backup operation requires detection and is not fail safe.

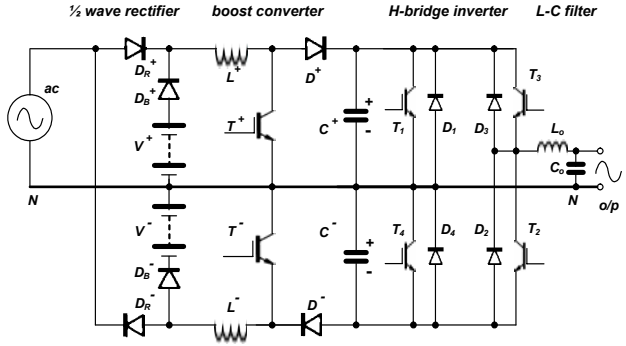


Figure 14.41. *Single-phase uninterruptible power supply.*

14.6.2 Three-phase ups

Figure 14.42 shows a basic three-phase ups, used up to a few tens of kilowatts. The ac supply is rectified and filtered. A forward converter controls the dc link voltage to just above the battery voltage level. This dc voltage is boosted to a dc level such that after inversion it provides the required output voltage magnitude. If the input ac fails or droops, the dc link power is provided by the battery via diode V_B. The output inverter is usually operational in a pwm mode, which allows precise frequency control, voltage control, ac mains phase synchronisation, and mini-misation of low frequency output harmonics. With pwm control minimal filtering is required, which minimises the filter weight, cost, size, and losses. A three-phase ups can utilise third harmonic injection (14.1.4(iv)).
A three-phase boost input converter can be used to maintain sinusoidal ac supply input currents at unity power factor.

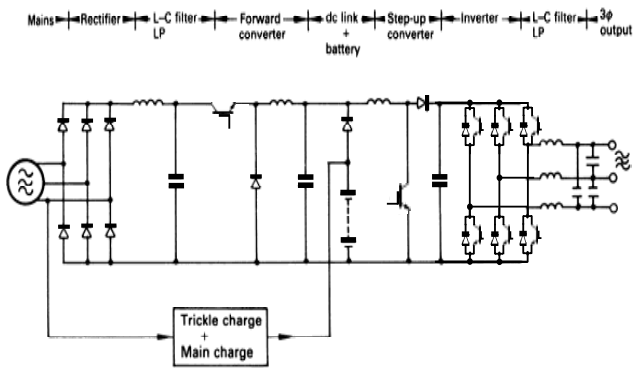


Figure 14.42. *Three-phase uninterruptible power supply.*

14.7 Power filters

Power *L-C* filters are used to reduce harmonics or ripple from

- the rectifier output (dc filter)
- the inverter output (ac filter).

L-C low-pass, second-order filters are shown in figures 14.39, 14.41, and 14.42. In figure 14.42, the *L-C* smoothing filter at the rectifier output, filters the ac mains frequency components leaving dc. The same type of filter is used in the inverter output to filter pwm harmonics, leaving the relative low frequency modulation frequency.
The *L-C* filter fundamental cut-off frequency is dependent on *L, C,* and the load impedance Z_L

$$\frac{v_o}{v_i} = \frac{1}{1 + j\omega L\left(\frac{1}{Z_L} + j\omega C\right)} = \frac{1}{1 - \omega^2 LC + j\frac{\omega L}{Z_L}} \tag{14.98}$$

The simplest design approach is to assume a non-load condition, $Z_L \to \infty$, whence the filter cut-off frequency is $f_o = 1/\left(2\pi\sqrt{LC}\right)$.
Frequency components below f_o, including dc, are passed. Those components above f_o are attenuated by a second order fall-off in gain. Any frequency components inadvertently around the resonant frequency, f_o, will be amplified. For this reason, the filter may be damped with parallel connected *R-C* snubbers.

Reading list

See chapter 11 reading list.

Problems

14.1. The inverter in figure 14.3 is supplied from a 340 V dc source. The load has a resistance of 10 ohms and an inductance of 10 mH. The basic operating frequency is 50 Hz, with three notches per half cycle giving half the maximum output, similar to that shown in figure 14.9.
Determine the load current waveform over the first two cycles and determine the power delivered to the load based on the current waveform of the final half cycle.

14.2. The inverter and load in problem 14.1 are controlled so as to eliminate the third and fifth harmonics in the output voltage.
Determine the load current waveform over the first two cycles and the power delivered to the load based on the current waveform of the last half cycle.

14.3. Output voltage harmonic reduction can be achieved by employing multi-phase, selected notching modulation control on a three-phase bridge as discussed in 14.1.4. An output as in figure 14.10 with $\alpha = 16.3°$ and $\beta = 22.1°$ eliminates the 5th and 7th harmonics.
Determine the fundamental voltage output component and compare it with that of a square wave. Determine the output rms voltage.

14.4. With the aid of figure 14.7 determine the line-to-neutral and line-to-line output voltage of a dc to three-phase inverter employing 120° device conduction.
Calculate the interphase:

i. mean half-cycle voltage
ii. rms voltage
iii. rms voltage of the fundamental.

14.5. The three-phase inverter bridge in figure 14.4 has a 600 V dc rail and a 10 Ω per phase load. For 180° and 120° conduction calculate:

i. the rms phase current
ii. the power delivered to the load
iii. the switch rms current.

[24.5 A, 18 kW, 17.3 A; 28.3 A, 24 kW, 14.15 A]

15

Switched-mode and Resonant dc Power Supplies

A switched-mode power supply (smps) or switching regulator, efficiently converts a dc voltage level to another dc voltage level, usually at power levels below a few kilowatts.

Shunt and series linear regulator power supplies dissipate much of their energy across the regulating transistor, which operates in the linear mode. An smps achieves regulation by varying the on to off time duty cycle of the switching element. This minimises losses, irrespective of load conditions.

Figure 15.1 illustrates the basic principle of the ac-fed smps in which the ac mains input is rectified, capacitively smoothed, and supplied to a high-frequency transistor chopper. The chopped dc voltage is transformed, rectified, and smoothed to give the required dc output voltage. A high-frequency transformer is used if an isolated output is required. The output voltage is sensed by a control circuit that adjusts the duty cycle of the switching transistor in order to maintain a constant output voltage with respect to load and input voltage variation. Alternatively, the chopper can be configured and controlled such that the input current tracks a scaled version of the input ac supply voltage, therein producing unity (or controllable) power factor *I-V* input conditions.

The switching frequency can be made much higher than the 50/60Hz line frequency; then the filtering and transformer elements used can be made small, lightweight, low in cost, and efficient.

Depending on the requirements of the application, the smps can be one of four basic converter types, namely

- forward
- flyback
- balanced
- resonant.

15.1 The forward converter

The basic *forward converter,* sometimes called a *buck converter,* is shown in figure 15.2a. The input voltage E_i is chopped by transistor T. When T is on, because the input voltage is greater than the load voltage v_o, energy is transferred from the dc supply E_i to L, C, and the load R. When T is turned off, stored energy in L is transferred via diode D to C and the load R.

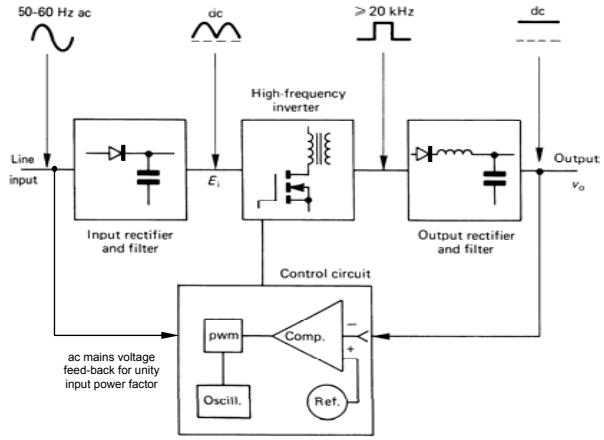


Figure 15.1. *Functional block diagram of a switched-mode power supply.*

If all the stored energy in L is transferred to C and the load before T is turned back on, operation is termed *discontinuous,* since the inductor current has reached zero. If T is turned on before the current in L reaches zero, that is, if continuous current flows in L, operation is termed *continuous.*

Parts b and c respectively of figure 15.2 illustrate forward converter circuit current and voltage waveforms for continuous and discontinuous conduction of L.

For analysis it is assumed that components are lossless and the output voltage v_o is maintained constant because of the large magnitude of the capacitor C across the output. The input voltage E_i is also assumed constant, such that $E_i \geq v_o$.

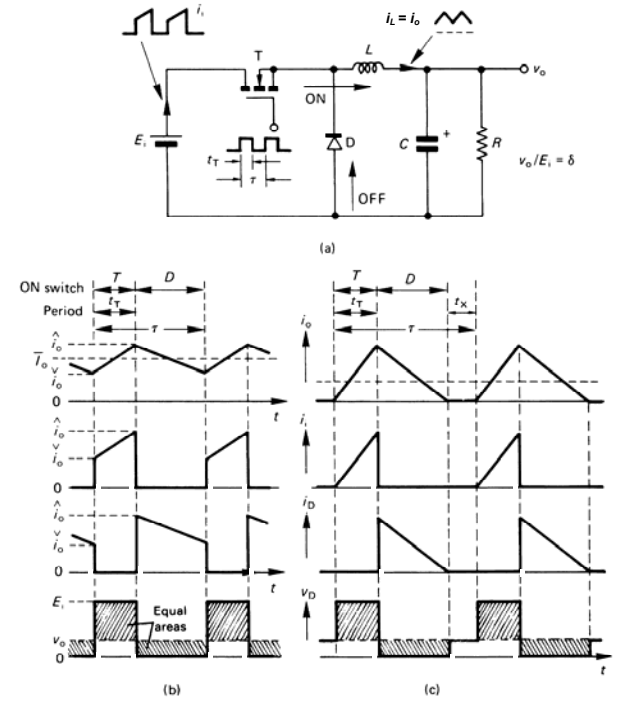


Figure 15.2. *Non-isolated forward converter (buck converter) where $v_0 \le E_1$: (a) circuit diagram; (b) waveforms for continuous output current; and (c) waveforms for discontinuous output current.*

15.1.1 Continuous inductor current

When transistor T is turned on for period t_T, the difference between the supply voltage E_i and the output voltage v_0 is impressed across L. From $V=Ldi/dt=L\Delta i/\Delta t$, the current change through the inductor will be

$$\Delta i_L = \hat{i}_L - \check{i}_L = \frac{E_i - v_o}{L} \times t_T \qquad (15.1)$$

When T is switched off for the remainder of the switching period, τ-t_T, the freewheel diode D conducts and $-v_0$ is impressed across L. Thus, assuming continuous conduction

$$\Delta i_L = \frac{v_o}{L} \times (\tau - t_T) \qquad (15.2)$$

Equating equations (15.1) and (15.2) gives $(E_i - v_o)\, t_T = v_o\, (\tau - t_T)$, which yields

$$\frac{v_o}{E_i} = \frac{\bar{I}_i}{\bar{I}_o} = \frac{t_T}{\tau} = \delta \qquad 0 \le \delta \le 1 \qquad (15.3)$$

This equation shows that for a given input voltage, the output voltage is determined by the transistor conduction duty cycle and the output is always less than the input voltage. This confirms and validates the original analysis assumption that $E_i \ge v_o$. The voltage transfer function is independent of circuit inductance L and capacitance C.
The inductor rms ripple current (and capacitor ripple current in this case) is given by

$$i_{Lr} = \frac{\Delta i_L}{2\sqrt{3}} = \frac{1}{2\sqrt{3}} \frac{v_o}{L}(1-\delta)\tau = \frac{1}{2\sqrt{3}} \frac{E_i}{L}(1-\delta)\delta\tau \qquad (15.4)$$

while the inductor total rms current is

$$i_{Lrms} = \sqrt{\bar{I}_L^2 + i_{Lr}^2} \qquad (15.5)$$

If the average inductor current, hence output current, is $\bar{I}_L$, then the maximum and minimum inductor current levels are given by

$$\hat{i}_L = \bar{I}_L + \tfrac{1}{2}\Delta i_L = \bar{I}_o + \tfrac{1}{2}\frac{v_o}{L}(1-\delta)\tau \qquad (15.6)$$

and

$$\check{i}_L = \bar{I}_L - \tfrac{1}{2}\Delta i_L = \bar{I}_o - \tfrac{1}{2}\frac{v_o}{L}(1-\delta)\tau \qquad (15.7)$$

respectively, where Δi_L is given by equation (15.1) or (15.2). The average output current is $\bar{I}_L = \tfrac{1}{2}\left(\hat{i}_L + \check{i}_L\right) = \bar{I}_o = v_o / R$. The output power is therefore v_o^2 / R. Circuit waveforms for continuous conduction are shown in figure 15.2b.

15.1.2 Discontinuous inductor current

The onset of discontinuous inductor operation occurs when the minimum inductor current $\check{i}_L$, reaches zero. That is, with $\check{i}_L = 0$ in equation (15.7),

$$\bar{I}_L = \bar{I}_o = \tfrac{1}{2}\Delta i_L \qquad (15.8)$$

which, after substituting equations (15.1) or (15.2), yields

$$\bar{I}_L = \bar{I}_o = \frac{(E_i - v_o)}{2L}\tau\delta \quad \text{or} \quad \frac{E_i}{2L}\tau\delta(1-\delta) \qquad (15.9)$$

If the transistor on-time t_T is reduced (or the load current is reduced), the discontinuous condition dead time t_x is introduced as indicated in figure 15.2c. From equations (15.1) and (15.2), with $\hat{i}_L = 0$, the output voltage transfer function is now derived as follows

$$\hat{i}_L = \frac{(E_i - v_o)}{L} t_T = \frac{v_o}{L}(\tau - t_T - t_x) \tag{15.10}$$

that is

$$\frac{v_o}{E_i} = \frac{\delta}{1 - \frac{t_x}{\tau}} \qquad 0 \le \delta < 1 \tag{15.11}$$

This voltage transfer function form may not be particularly useful since the dead time t_x is not expressed in term of circuit parameters. Accordingly, from equation (15.10)

$$\hat{i}_L = \frac{(E_i - v_o)}{L} t_T \tag{15.12}$$

and from the input current waveform in figure 15.2c:

$$\bar{I}_i = \tfrac{1}{2} \hat{i}_L \times \frac{t_T}{\tau} \tag{15.13}$$

Eliminating $\hat{i}_L$ yields

$$\frac{2\bar{I}_i}{\delta} = (1 - \frac{v_o}{E_i}) \frac{\tau \delta E_i}{L} \tag{15.14}$$

that is

$$\frac{v_o}{E_i} = 1 - \frac{2L\bar{I}_i}{\delta^2 \tau E_i} \tag{15.15}$$

Assuming power-in equals power-out, that is, $E_i \bar{I}_i = v_o \bar{I}_o = v_o \bar{I}_L$, the input average current can be eliminated, and after re-arranging yields:

$$\frac{v_o}{E_i} = \frac{1}{1 + \frac{2L\bar{I}_o}{\delta^2 \tau E_i}} = \frac{1}{1 + \frac{2L\bar{I}_i}{\delta^2 \tau v_o}} \tag{15.16}$$

At a low output current or high input voltage, there is a likelihood of discontinuous inductor conduction. To avoid discontinuous conduction, larger inductance values are needed, which worsen transient response. Alternatively, with extremely low on-state duty cycles, a voltage-matching transformer can be used to increase δ. Once using a transformer, any smps technique can be used to achieve the desired output voltage. Figures 15.2b and c show that the input current is always discontinuous.

15.1.3 Load conditions for discontinuous inductor current

As the load current decreases, the inductor average current also decreases, but the inductor ripple current magnitude is unchanged. If the load resistance is increased sufficiently, the bottom of the triangular inductor current, $\check{i}_L$, eventual reduces to zero. Any further increase in resistance causes discontinuous inductor current and the linear voltage transfer function given by equation (15.3) is no longer valid and equations (15.11) and (15.15) are applicable. The critical load resistance for continuous inductor current is specified by

$$R_{crit} \le \frac{v_o}{\bar{I}_o} = \frac{v_o}{\tfrac{1}{2}\Delta i_L} \tag{15.17}$$

Substitution for v_o from equation (15.2) and using the fact that $\bar{I}_o = \bar{I}_L$, yields

$$R_{crit} \le \frac{v_o}{\bar{I}_o} = \frac{\Delta i_L L}{\bar{I}_L(\tau - t_T)} \tag{15.18}$$

Eliminating Δi_L by substituting the limiting condition given by equation (15.8) gives

$$R_{crit} \le \frac{v_o}{\bar{I}_o} = \frac{\Delta i_L L}{\bar{I}_L(\tau - t_T)} = \frac{2\bar{I}_L L}{\bar{I}_L(\tau - t_T)} = \frac{2L}{(\tau - t_T)} \tag{15.19}$$

Divide throughout by τ and substituting $\delta = t_T / \tau$ yields

$$R_{crit} \le \frac{v_o}{\bar{I}_o} = \frac{2L}{(\tau - t_T)} = \frac{2L}{\tau(1 - \delta)} \tag{15.20}$$

The critical resistance can be expressed in a number of forms. By substituting the switching frequency ($f_s = 1/\tau$) or the fundamental inductor reactance ($X_L = 2\pi f_s L$) the following forms result.

$$R_{crit} \le \frac{v_o}{\bar{I}_o} = \frac{2L}{\tau(1-\delta)} = \frac{2f_s L}{(1-\delta)} = \frac{X_L}{\pi(1-\delta)} \qquad (\Omega) \tag{15.21}$$

If the load resistance increases beyond R_{crit}, the output voltage can no longer be maintained with duty cycle control according to the voltage transfer function in equation (15.3).

15.1.4 Control methods for discontinuous inductor current

Once the load current has reduced to the critical level as specified by equation (15.21), the input energy is in excess of the load requirement. Open loop load voltage regulation control is lost and the capacitor *C* tends to overcharge.
Hardware approaches can be used to solve this problem

- increase *L* thereby decreasing the inductor current ripple p-p magnitude
- step-down transformer impedance matching to effectively reduce the apparent load impedance

Two control approaches to maintain output voltage regulation when $R > R_{crit}$ are

- vary the switching frequency f_s, maintaining the switch on-time t_T constant so that Δi_L is fixed or
- reduce the switch on-time t_T , but maintain a constant switching frequency f_s, thereby reducing Δi_L.

If a fixed switching frequency is desired for all modes of operation, then reduced on-time control, using output voltage feedback, is preferred. If a fixed on-time mode of control is used, then the output voltage is control by varying inversely the frequency with output voltage.

15.1.4i - fixed on-time t_T, variable switching frequency f_{var}

The operating frequency f_{var} is varied while the switch-on time t_T is maintained constant such that the ripple current remains unchanged. Operation is specified by equating the input energy and the output energy, thus maintaining a constant capacitor charge, hence output voltage. That is, equating energies

$$½\Delta i_L E_i t_T = \frac{v_o^2}{R}\frac{1}{f_{\text{var}}} \tag{15.22}$$

Isolating the variable switching frequency f_{var} gives

$$\begin{aligned} f_{\text{var}} &= \frac{v_o^2}{½\Delta i_L E_i t_T}\frac{1}{R} \\ f_{\text{var}} &= f_s R_{crit}\frac{1}{R} \\ f_{\text{var}} &\;\alpha\; \frac{1}{R} \end{aligned} \tag{15.23}$$

That is, once discontinuous inductor current occurs, if the switching frequency is varied inversely with load resistance and the switch on-state period is maintained constant, output voltage regulation can be maintained.

Load resistance R is not a directly or readily measurable parameter for feedback proposes. Alternatively, since $v_o = \bar{I}_o R$ substitution for R in equation (15.23) gives

$$\begin{aligned} f_{\text{var}} &= f_s \frac{R_{crit.}}{v_o}\bar{I}_o \\ f_{\text{var}} &\;\alpha\; \bar{I}_o \end{aligned} \tag{15.24}$$

That is, for $\bar{I}_o < ½\Delta i_L$ or $\bar{I}_o < v_o / R_{crit}$, if t_T remains constant and f_{var} is varied proportionally with load current, then the required output voltage v_o will be maintained.

15.1.4ii - fixed switching frequency f_s, variable on-time $t_{T\text{var}}$

The operating frequency f_s remains fixed while the switch-on time $t_{T\text{var}}$ is reduced, resulting in the ripple current being reduced. Operation is specified by equating the input energy and the output energy as in equation (15.22), thus maintaining a constant capacitor charge, hence voltage. That is

$$½\Delta i_L E_i t_{T\text{var}} = \frac{v_o^2}{R}\frac{1}{f_s} \tag{15.25}$$

Isolating the variable on-time $t_{T\text{var}}$ yields

$$t_{T\text{var}} = \frac{v_o^2}{½\Delta i_L E_i f_s}\frac{1}{R}$$

Substituting Δi_L from equation (15.2) gives

$$\begin{aligned} t_{T\text{var}} &= t_T\sqrt{R_{crit}}\frac{1}{\sqrt{R}} \\ t_{T\text{var}} &\;\alpha\; \frac{1}{\sqrt{R}} \end{aligned} \tag{15.26}$$

That is, once discontinuous inductor current commences, if the switch on-time is varied inversely to the square root of the load resistance, maintaining the switching frequency constant, regulation of the output voltage can be maintained.

Again, load resistance R is not a directly or readily measurable parameter for feedback proposes and substitution of $v_o / \bar{I}_o$ for R in equation (15.26) gives

$$\begin{aligned} t_{T\text{var}} &= t_T\sqrt{\frac{R_{crit.}}{v_o}}\sqrt{\bar{I}_o} \\ t_{T\text{var}} &\;\alpha\; \sqrt{\bar{I}_o} \end{aligned} \tag{15.27}$$

That is, if f_s is fixed and t_T is reduced proportionally to $\sqrt{\bar{I}_o}$, when $\bar{I}_o < ½\Delta i_L$ or $\bar{I}_o < v_o / R_{crit}$, then the required output voltage magnitude v_o will be maintained.

15.1.5 Output ripple voltage

Three components contribute to the output voltage ripple

- Ripple charging of the ideal capacitor
- Capacitor equivalent series resistance, ESR
- Capacitor equivalent series inductance, ESL

The capacitor inductance and resistance parasitic series component values decrease as the quality of the capacitor increases. The output ripple voltage is the vectorial summation of the three components that are shown in figure 15.3 for the forward converter.

Ideal Capacitor: The ripple voltage for a capacitor is defined as

$$\Delta v_C = \tfrac{1}{C}\int i\,dt$$

Figures 15.2 and 15.3 show that for continuous inductor current, the inductor current which is the output current, swings by Δi around the average output current, $\overline{I}_o$, thus

$$\Delta v_C = \frac{1}{C}\int i\,dt = \tfrac{1}{2}\frac{1}{C}\frac{\Delta i}{2}\frac{\tau}{2} \qquad (15.28)$$

Substituting for Δi_L from equation (15.2)

$$\Delta v_C = \frac{1}{C}\int i\,dt = \tfrac{1}{2}\frac{1}{C}\frac{\Delta i}{2}\frac{\tau}{2} = \tfrac{1}{8}\frac{1}{C}\frac{v_o}{L}\times(\tau - t_T)\tau \qquad (15.29)$$

If ESR and ESL are ignored, after rearranging, equation (15.29) gives the percentage voltage ripple (peak to peak) in the output voltage

$$\frac{\Delta v_C}{v_o} = \tfrac{1}{8}\frac{1}{LC}\times(1-\delta)\tau^2 = \tfrac{1}{2}\pi^2(1-\delta)\left(f_c/f_s\right)^2 \qquad (15.30)$$

In complying with output voltage ripple requirements, from this equation, the switching frequency f_s=1/τ must be much higher that the cut-off frequency given by the forward converter low-pass, second-order LC output filter, f_c=1/2$\pi\sqrt{LC}$.

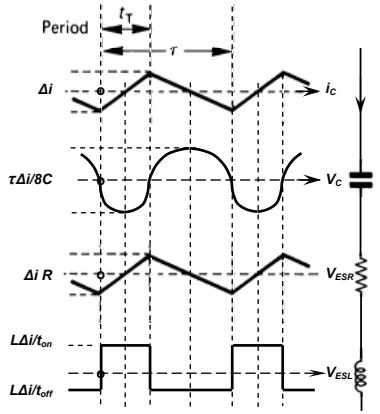


Figure 15.3. *Forward converter, three output ripple components, showing: left -voltage components; centre – waveforms; and right - capacitor model.*

ESR: The equivalent series resistor voltage follows the ripple current, that is, it swings linearly about

$$V_{ESR} = \pm\tfrac{1}{2}\Delta i \times R_{ESR} \qquad (15.31)$$

ESL: The equivalent series inductor voltage is derived from $v = Ldi/dt$, that is when the switch is on

$$V^+_{ESL} = L\Delta i / t_{on} = L\Delta i / \delta\tau \qquad (15.32)$$

When the switch is off

$$V^-_{ESL} = -L\Delta i / t_{off} = -L\Delta i / (1-\delta)\tau \qquad (15.33)$$

The total ripple voltage is

$$\Delta v_o = \Delta v_C + V_{ESR} + V_{ESL} \qquad (15.34)$$

Forming a time domain solution for each component, then differentiating, gives a maximum ripple when

$$t = 2CR_{ESR}(1-\delta) \qquad (15.35)$$

This expression is independent of the equivalent series inductance, which is expected since it is constant during each state. If dominant, the inductor will affect the output voltage ripple at the switch turn-on and turn-off instants.

Example 15.1: ***Buck (step-down forward) converter***

The step-down converter in figure 15.2a operates at a switching frequency of 10 kHz. The output voltage is to be fixed at 48 V dc across a 1 Ω resistive load. If the input voltage E_i=192 V and the choke L = 200μH:

i. calculate the switch T on-time duty cycle δ and switch on-time t_T
ii. calculate the average load current $\overline{I}_o$, hence average input current $\overline{I}_i$
iii. draw accurate waveforms for
   - the voltage across, and the current through L; v_L and i_L
   - the capacitor current, i_c
   - the switch and diode voltage and current; v_T, v_D, i_T, i_D
iv. calculate the mean and rms current ratings of diode D and switch T
v. calculate the capacitor average and rms current, $i_{C\text{rms}}$ and output ripple voltage if the capacitor has an internal equivalent series resistance of 20mΩ (C = ∞).
vi. calculate the maximum load resistance R_{crit} before discontinuous inductor current
vii. if the maximum load resistance is 1Ω, calculate
   - the value the inductance L can be reduced to before discontinuous inductor current and
   - the peak-to-peak ripple and rms, inductor and capacitor currents.
viii. Specify two control strategies for controlling the forward converter in a discontinuous inductor current mode
ix. Output ripple voltage hence percentage output ripple voltage, for C=1000μF and an equivalent series inductance of ESL=0.5uH, assuming ESR = 0Ω

Solution

i. From equation (15.3) the duty cycle δ is

$$\delta = \frac{v_o}{E_i} = \frac{48\text{V}}{192\text{V}} = ¼ = 25\%$$

Also, from equation (15.3), for a 10kHz switching frequency, the switching period τ is 100μs and the transistor on-time t_T is given by

$$\frac{v_o}{E_i} = \frac{t_T}{\tau} = \frac{48\text{V}}{192\text{V}} = \frac{t_T}{100\mu\text{s}}$$

whence the transistor on-time is 25μs and the diode conducts for 75μs.

ii. The average load current is $\overline{I}_o = \frac{v_o}{R} = \frac{48\text{V}}{1\Omega} = 48\text{A} = \overline{I}_L$

From power-in equals power-out, the average input current is

$$\overline{I}_i = v_o \overline{I}_o / E_i = 48\text{V}\times 48\text{A}/192\text{V} = 12\text{A}$$

iii. From equation (15.1) (or equation (15.2)) the inductor peak-to-peak ripple current is

$$\Delta i_L = \frac{E_i - v_o}{L} \times t_T = \frac{192\text{V-}48\text{V}}{200\mu\text{H}} \times 25\mu\text{s} = 18\text{A}$$

From part ii, the average inductor current is the average output current, 48A. The required circuit voltage and current waveforms are shown in the following figure.

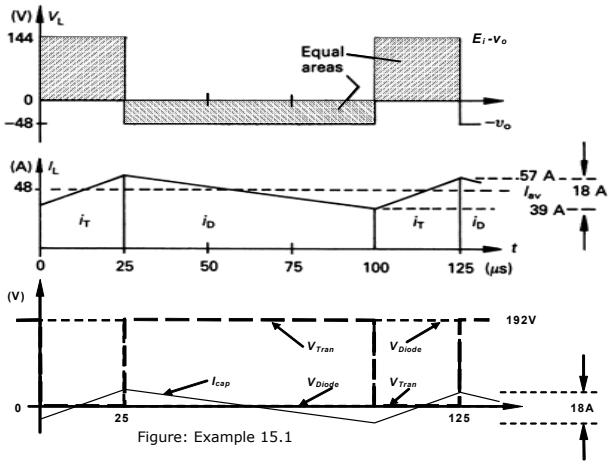


Figure: Example 15.1

iv. Current i_D through diode D is shown on the inductor current waveform. The average diode current is

$$\overline{I}_D = \frac{\tau - t_T}{\tau} \times \overline{I}_L = (1-\delta) \times \overline{I}_L = (1-¼)\times 48\text{A} = 36\text{A}$$

The rms diode current is given by

$$i_{D\text{rms}} = \sqrt{\frac{1}{\tau}\int_0^{\tau - t_T} (\hat{i}_L - \frac{\Delta i_L}{\tau - t_T}t)^2 dt} = \sqrt{\frac{1}{100\mu\text{s}}\int_0^{75\mu\text{s}} (57\text{A} - \frac{18\text{A}}{75\mu\text{s}}t)^2 dt}$$

$$= 41.8\text{A}$$

Current i_T through the switch T is shown on the inductor current waveform. The average switch current is

$$\overline{I}_T = \frac{t_T}{\tau}\overline{I}_L = \delta \overline{I}_L = ¼\times 48\text{A} = 12\text{A}$$

Alternatively, from power-in equals power-out

$$\overline{I}_T = \overline{I}_i = v_o \overline{I}_o / E_i = 48\text{V}\times 48\text{A}/192\text{V} = 12\text{A}$$

The transistor rms current is given by

$$i_{T\text{rms}} = \sqrt{\frac{1}{\tau}\int_0^{t_T} (\check{i}_L + \frac{\Delta i_L}{t_T}t)^2 dt} = \sqrt{\frac{1}{100\mu\text{s}}\int_0^{25\mu\text{s}} (39\text{A} + \frac{18\text{A}}{25\mu\text{s}}t)^2 dt}$$

$$= 24.1\text{A}$$

v. The average capacitor current $\overline{I}_C$ is zero and the rms ripple current is given by

$$i_{C\text{rms}} = \sqrt{\frac{1}{\tau}\left[\int_0^{t_T} (-½\Delta i_L + \frac{\Delta i_L}{t_T}t)^2 dt + \int_0^{\tau - t_T} (½\Delta i_L - \frac{\Delta i_L}{\tau - t_T}t)^2 dt\right]}$$

$$= \sqrt{\frac{1}{100\mu\text{s}}\left[\int_0^{25\mu\text{s}} (-9\text{A} + \frac{18\text{A}}{25\mu\text{s}}t)^2 dt + \int_0^{75\mu\text{s}} (9\text{A} - \frac{18\text{A}}{75\mu\text{s}}t)^2 dt\right]}$$

$$= 5.2\text{A} \quad (= \Delta i_L / 2\sqrt{3})$$

The capacitor voltage ripple (hence the output voltage ripple), is determined by the capacitor ripple current which is equal to the inductor ripple current, 18A p-p, that is

$$v_{o\text{ripple}} = \Delta i_L \times R_{C\text{esr}}$$

$$= 18\text{A}\times 20\text{m}\Omega = 360\text{mV p-p}$$

and the rms output voltage ripple is

$$v_{o\text{rms}} = i_{C\text{rms}} \times R_{C\text{esr}}$$

$$= 5.2\text{A rms}\times 20\text{m}\Omega = 104\text{mV rms}$$

vi. Critical load resistance is given by equation (15.21), namely

$$R_{crit} \le \frac{v_o}{\overline{I}_o} = \frac{2L}{\tau(1-\delta)}$$

$$= \frac{2\times 200\mu H}{100\mu s(1-¼)} = 16/3$$

$$= 5⅓\Omega \text{ when } \bar{I}_o = 9A$$

Alternatively, the critical load current is 9A ($½\Delta i_L$), thus from the equation immediately above, the load resistance must not be greater than $v_o / \bar{I}_o = 48V/9A = 5⅓\Omega$, if the inductor current is to be continuous.

vii. The critical resistance formula given in equation (15.21) is valid for finding critical inductance when inductance is made the subject of the equation, that is, rearranging equation (15.21) gives

$$L_{crit} = ½ \times R \times (1-\delta) \times \tau \qquad \text{(H)}$$

$$= ½ \times 1\Omega \times (1-¼) \times 100\mu s = 37½\mu H$$

This means the inductance can be reduced from 200μH with a 48A mean and 18A p-p ripple current, to 37½μH with the same 48A mean plus a superimposed 96A p-p ripple current. The rms capacitor current is given by

$$i_{C\text{rms}} = \Delta i_L / 2\sqrt{3}$$

$$= 96A/2\sqrt{3} = 27.2A \text{ rms}$$

The inductor rms current requires the following integration

$$i_{L\text{rms}} = \sqrt{\frac{1}{\tau}\left[\int_0^{t_T} (\check{i}_L + \frac{\Delta i_L}{t_T}t)^2 dt + \int_0^{\tau - t_T} (\hat{i}_L - \frac{\Delta i_L}{\tau - t_T}t)^2 dt\right]}$$

$$= \sqrt{\frac{1}{100\mu s}\left[\int_0^{25\mu s} (0 + \frac{96A}{25\mu s}t)^2 dt + \int_0^{75\mu s} (96A - \frac{96A}{75\mu s}t)^2 dt\right]}$$

$$= 96/\sqrt{3} = 55.4 \text{ A rms}$$

or from equation (15.5)

$$i_{L\text{rms}} = \sqrt{\bar{I}_L^2 + i_{L\text{ripple}}^2}$$

$$= \sqrt{48^2 + (96/2\sqrt{3})^2}$$

$$= 55.4 \text{ A rms}$$

viii. For $R > 16/3\Omega$, or $\bar{I}_o < 9A$, equations (15.24) or (15.27) can be used to develop a suitable control strategy.

(a) From equation (15.24), using a variable switching frequency of less than 10kHz,

$$f_{\text{var}} = f_s \frac{R_{crit}}{v_o}\bar{I}_o = 10\text{kHz} \ \frac{5⅓\Omega}{48V} \ \bar{I}_o$$

$$f_{\text{var}} = \frac{10}{9}\times \bar{I}_o \quad \text{kHz}$$

(b) From equation (15.27), maintaining a fixed switching frequency of 10kHz, the on-time duty cycle is reduced for $\bar{I}_o < 9A$ according to

$$t_{T\text{var}} = t_T \sqrt{\frac{R_{crit}}{v_o}}\sqrt{\bar{I}_o} = 25\mu s \sqrt{\frac{5⅓\Omega}{48V}}\sqrt{\bar{I}_o}$$

$$t_{T\text{var}} = \frac{25}{3}\sqrt{\bar{I}_o} \quad \mu s$$

x. From equation (15.28) the output ripple voltage due the pure capacitor is given by

$$\Delta v_C = ½ \frac{1}{C}\frac{\Delta i}{2}\frac{\tau}{2}$$

$$= ½ \times \frac{1}{1000\mu F} \times \frac{18A}{2} \times \frac{100\mu s}{2} = 225\text{mV p-p}$$

The voltage produced because of the equivalent series 0.5 μH inductance is

$$V_{ESL}^{+} = L\Delta i / \delta\tau$$

$$= 0.5\mu H \times 18A/0.25 \times 100\mu s = 360\text{mV}$$

$$V_{ESL}^{-} = -L\Delta i / (1-\delta)\tau$$

$$= -0.5\mu H \times 18A/(1 - 0.25) \times 100\mu s = -120\text{mV}$$

Time domain summation of the capacitor and ESL inductor voltages show that the peak to peak output voltage swing is determined by the ESL inductor, giving

$$\Delta v_o = V_{ESL}^{+} - V_{ESL}^{-}$$

$$= 360\text{mV} + 120\text{mV} = 480\text{mV}$$

The percentage ripple in the output voltage is 480mV/48V = 1%. ♣

15.1.6 Underlying mechanisms of the forward converter

The inductor current is central to the analysis and understanding of any smps. The first concept to appreciate is that the net capacitor charge change is zero over each switching cycle. In so doing, the capacitor provides any load current deficit and stores any load current surplus associated with the inductor current within each complete cycle. Thus, the capacitor is a temporary storage component where the capacitor voltage is fixed on a cycle-by-cycle basis, and because of its large capacitance does not vary significantly within a cycle.

The most enlightening way to appreciate the operating mechanisms is to consider how the inductor current varies with load resistance R and inductance L. The figure 15.4 shows the inductor current associated with the various parts of example 15.1.

For continuous inductor current operation, the two necessary and sufficient equations are $I_o = v_o / R$ and equation (15.2). Since the duty cycle and on-time are fixed for a given output voltage requirement, equation (15.2) can be simplified to show that the ripple current is inversely proportional to inductance, as follows

$$\Delta i_L = \frac{v_o}{L} \times (\tau - t_T)$$
$$\Delta i_L \, \alpha \, \frac{1}{L} \qquad (15.36)$$

Since the average inductor current is equal to the load current, then the average inductor current is inversely proportional to the load resistance, that is

$$\overline{I}_L = \overline{I}_o = v_o / R$$
$$\overline{I}_L \, \alpha \, \frac{1}{R} \qquad (15.37)$$

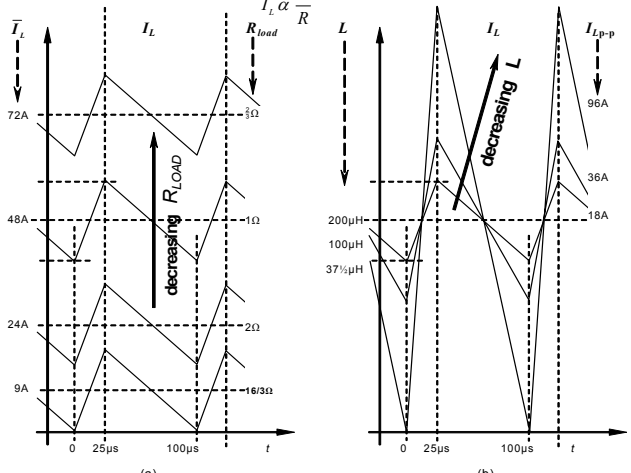


Figure 15.4. *Forward converter (buck converter) operational mechanisms showing that: (a) the average inductor current is inversely proportional to load resistance R and (b) the inductor ripple current magnitude is inversely proportional to inductance L.*

Equation (15.37) predicts that the average inductor current is inversely proportional to the load resistance, as shown in figure 15.4a. As the load is varied, the triangular inductor current moves vertically, but importantly the peak-to-peak ripple current is constant, that is the ripple is independent of load. As the load current is progressively decreased, by increasing R, the peak-to-peak current is unchanged; the inductor minimum current eventually reduces to zero, and discontinuous inductor current operation occurs.

Equation (15.36) indicates that the inductor ripple current is inversely proportional to inductance, as shown in figure 15.4b. As the inductance is varied the ripple current varies inversely, but importantly the average current is constant, and specifically the average current value is not related to inductance L and is solely determined by the load current, v_o /R. As the inductance decreases the magnitude of the ripple current increases, the average is unchanged, and the minimum inductor current eventually reaches zero and discontinuous inductor current operation results.

15.2 Flyback converters

Flyback converters store energy in an inductor, termed 'choke', and transfer that energy to the load storage capacitor such that output voltage magnitudes in excess of the input voltage are attained. Flyback converters are alternatively known as *ringing choke* converters. Two versions of the flyback converter are possible

- The step-up voltage flyback converter, called the *boost converter,* where no output voltage polarity inversion occurs.
- The step-up/step-down voltage flyback converter, called the *buck-boost converter,* where output voltage polarity inversion occurs.

15.3 The boost converter

The *boost converter* transforms a dc voltage input to a dc voltage output that is greater in magnitude but has the same polarity as the input. The basic circuit configuration is shown in figure 15.5a. It will be seen that when the transistor is off, the output capacitor is charged to the input voltage E_i. Inherently, the output voltage v_o can never be less than the input voltage level.

When the transistor is turned on, the supply voltage E_i is applied across the inductor L and the diode D is reverse-biased by the output voltage v_o. Energy is transferred from the supply to L and when the transistor is turned off this energy is transferred to the load and output capacitor. While the inductor is transferring its stored energy into C, energy is also being provided from the input source.

The output current is always discontinuous, but the input current can be either continuous or discontinuous. For analysis, we assume $v_o > E_i$ and a constant input and output voltage. Inductor currents are then linear and vary according to $v = L\, di/dt$.

15.3.1 Continuous inductor current

The circuit voltage and current waveforms for continuous inductor conduction are shown in figure 15.5b. The inductor current excursion, which is the input current excursion, during the switch on-time t_T and switch off-time τ- t_T , is given by

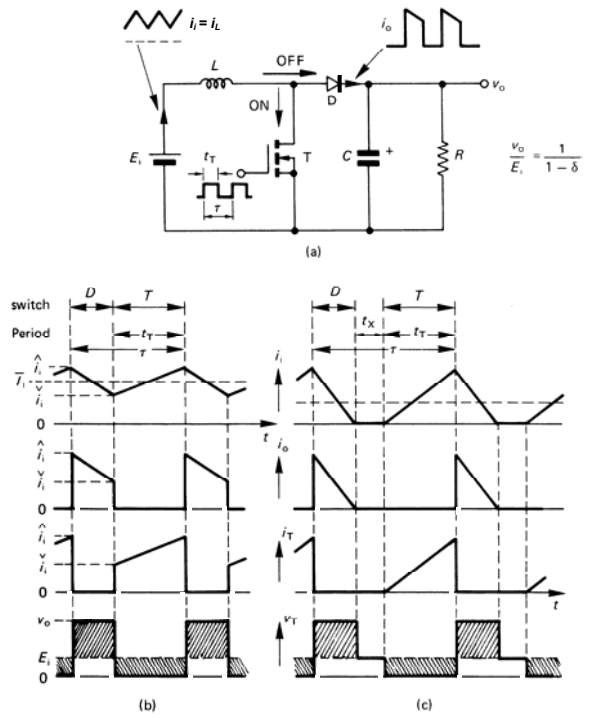


Figure 15.5. *Non-isolated, step-up, flyback converter (boost converter) where $v_0 \geq E_1$: (a) circuit diagram; (b) waveforms for continuous input current; and (c) waveforms for discontinuous input current.*

$$\Delta i_L = \frac{(v_o - E_i)}{L}(\tau - t_T) = \frac{E_i}{L} t_T \tag{15.38}$$

that is, after rearranging, the voltage transfer function is given by

$$\frac{v_o}{E_i} = \frac{\bar{I}_i}{\bar{I}_o} = \frac{1}{1-\delta} \tag{15.39}$$

where $\delta = t_T/\tau$ and t_T is the transistor on-time. The maximum inductor current, which is the maximum input current, $\hat{i}_L$, using equation (15.38), is given by

$$\begin{aligned} \hat{i}_L &= \bar{I}_L + \tfrac{1}{2}\Delta i_L \\ &= \bar{I}_i + \tfrac{1}{2}\frac{E_i t_T}{L} = \frac{\bar{I}_o}{1-\delta} + \tfrac{1}{2}\frac{v_o}{L}(1-\delta)\delta\tau \end{aligned} \tag{15.40}$$

while the minimum inductor current, $\check{i}_L$ is given by

$$\check{i}_L = \bar{I}_i - \tfrac{1}{2}\frac{E_i t_T}{L} = \frac{\bar{I}_o}{1-\delta} - \tfrac{1}{2}\frac{v_o}{L}(1-\delta)\delta\tau \tag{15.41}$$

For continuous conduction $\check{i}_L \geq 0$, that is, from equation (15.41)

$$\bar{I}_L \geq \tfrac{1}{2}\frac{E_i t_T}{L} = \tfrac{1}{2}\frac{v_o(1-\delta)t_T}{L} \tag{15.42}$$

The inductor rms ripple current (and input ripple current in this case) is given by

$$i_{Lr} = \frac{\Delta i_L}{2\sqrt{3}} = \frac{1}{2\sqrt{3}}\frac{v_o}{L}(1-\delta)\delta\tau \tag{15.43}$$

The harmonic components in the input current are

$$I_{in} = \frac{\sqrt{2}\, E_i \tau \sin n\delta\pi}{2\pi^2 n^2 (1-\delta) L} = \frac{\sqrt{2}\, v_o \tau \sin n\delta\pi}{2\pi^2 n^2 L} \tag{15.44}$$

while the inductor total rms current is

$$i_{Lrms} = \sqrt{\bar{I}_L^2 + i_{Lr}^2} \tag{15.45}$$

15.3.2 Discontinuous capacitor charging current in the switch off-state

It is possible that the input current (inductor current) falls below the output (resistor) current during a part of the cycle when the switch is off and the inductor is transferring energy to the output circuit. Under such conditions, towards the end of the off period, part of the load current requirement is provided by the capacitor even though this is the period during which its charge is replenished by inductor energy. The circuit independent transfer function in equation (15.39) remains valid. This discontinuous charging condition occurs when the minimum inductor current and the output current are equal. That is

$$\begin{aligned} &\check{I}_L - \bar{I}_o \leq 0 \\ &\bar{I}_L - \tfrac{1}{2}\Delta i_L - \bar{I}_o \leq 0 \\ &\frac{\bar{I}_o}{1-\delta} - \tfrac{1}{2}\frac{E_i \delta\tau}{L} - \bar{I}_o \leq 0 \end{aligned} \tag{15.46}$$

which yields

$$\delta \le 1-\sqrt{\frac{2L}{\tau R}} \qquad (15.47)$$

15.3.3 Discontinuous inductor current

If the inequality in equation (15.42) is not satisfied, the input current, which is also the inductor current, reaches zero and discontinuous conduction occurs during the switch off period. Various circuit voltage and current waveforms for discontinuous inductor conduction are shown in figure 15.5c.

With $\check{i}_L = 0$, the output voltage is determined as follows

$$\hat{i}_L = \frac{E_i t_T}{L} = \frac{(v_o - E_i)}{L}(\tau - t_T - t_x) \qquad (15.48)$$

yielding

$$\frac{v_o}{E_i} = \frac{1-\frac{t_x}{\tau}}{1-\frac{t_x}{\tau}-\delta} \qquad (15.49)$$

Alternatively, using

$$\hat{i}_L = \frac{E_i t_T}{L}$$

and

$$\bar{I}_L - \bar{I}_o = \tfrac{1}{2}\delta \hat{i}_L$$

yields

$$\frac{2}{\delta}(\bar{I}_L - \bar{I}_o) = \frac{E_i t_T}{L}$$

Assuming power-in equals power-out

$$\frac{2}{\delta}\bar{I}_o(\frac{v_o}{E_i}-1) = \frac{E_i t_T}{L}$$

that is

$$\frac{v_o}{E_i} = 1 + \frac{E_i t_T \delta^2}{2L\bar{I}_o} = 1 + \frac{v_o t_T \delta^2}{2L\bar{I}_i} \qquad (15.50)$$

or

$$\frac{v_o}{E_i} = \frac{1}{1-\frac{E_i t_T \delta^2}{2L\bar{I}_i}} \qquad (15.51)$$

On the verge of discontinuous conduction, these equations can be rearranged to give

$$\bar{I}_o = \frac{E_i}{2L}\tau\delta(1-\delta) \qquad (15.52)$$

At a low output current or low input voltage, there is a likelihood of discontinuous inductor conduction. To avoid discontinuous conduction, larger inductance values are needed, which worsen transient response. Alternatively, with extremely high on-state duty cycles, (because of a low input voltage E_i) a voltage-matching step-up transformer can be used to decrease δ. Figures 15.5b and c show that the output current is always discontinuous.

15.3.4 Load conditions for discontinuous inductor current

As the load current decreases, the inductor average current also decreases, but the inductor ripple current magnitude is unchanged. If the load resistance is increased sufficiently, the bottom of the triangular inductor current, $\check{i}_L$, eventually reduces to zero. Any further increase in load resistance causes discontinuous inductor current and the voltage transfer function given by equation (15.39) is no longer valid and equations (15.49) and (15.50) are applicable. The critical load resistance for continuous inductor current is specified by

$$R_{crit} \le \frac{v_o}{\bar{I}_o} \qquad (15.53)$$

Eliminating the output current by using the fact that power-in equals power-out and $\bar{I}_i = \bar{I}_L$, yields

$$R_{crit} \le \frac{v_o}{\bar{I}_o} = \frac{v_o^2}{E_i \bar{I}_L} \qquad (15.54)$$

Using $\bar{I}_L = \tfrac{1}{2}\Delta i_L$ then substituting with the right hand equality of equation (15.38), halved, gives

$$R_{crit} \le \frac{v_o}{\bar{I}_o} = \frac{v_o^2}{E_i \bar{I}_L} = \frac{v_o^2 2L}{E_i^2 t_T} = \frac{2L}{\tau\delta(1-\delta)^2} \qquad (15.55)$$

The critical resistance can be expressed in a number of forms. By substituting the switching frequency ($f_s = 1/\tau$) or the fundamental inductor reactance ($X_L = 2\pi f_s L$) the following forms result.

$$R_{crit} \le \frac{v_o}{\bar{I}_o} = \frac{2L}{\tau\delta(1-\delta)^2} = \frac{2f_s L}{\delta(1-\delta)^2} = \frac{X_L}{\pi\delta(1-\delta)^2} \quad (\Omega) \qquad (15.56)$$

If the load resistance increases beyond R_{crit}, the output voltage can no longer be maintained with duty cycle control according to the voltage transfer function in equation (15.39).

15.3.5 Control methods for discontinuous inductor current

Once the load current has reduced to the critical level as specified by equation (15.56), the input energy is in excess of the load requirement. Open loop load voltage regulation control is lost and the capacitor C tends to overcharge, thereby increasing v_o.
Hardware approaches can be used to solve this problem

- increase L thereby decreasing the inductor current ripple p-p magnitude
- step-down transformer impedance matching to effectively reduce the apparent load impedance

Two control approaches to maintain output voltage regulation when $R > R_{crit}$ are

- vary the switching frequency f_s, maintaining the switch on-time t_T constant so that Δi_L is fixed or
- reduce the switch on-time t_T , but maintain a constant switching frequency f_s, thereby reducing Δi_L.

If a fixed switching frequency is desired for all modes of operation, then reduced on-time control, using output voltage feedback, is preferred. If a fixed on-time mode of control is used, then the output voltage is control by inversely varying the frequency with output voltage.

15.3.5i - fixed on-time t_T, variable switching frequency f_{var}

The operating frequency f_{var} is varied while the switch-on time t_T is maintained constant such that the ripple current remains unchanged. Operation is specified by equating the input energy and the output energy, thus maintaining a constant capacitor charge, hence output voltage. That is, equating energies

$$½\Delta i_L E_i \tau = \frac{v_o^2}{R}\frac{1}{f_{\text{var}}} \tag{15.57}$$

Isolating the variable switching frequency f_{var} gives

$$f_{\text{var}} = \frac{v_o^2}{½\Delta i_L E_i \tau}\frac{1}{R}$$

$$f_{\text{var}} = f_s R_{crit}\frac{1}{R} \tag{15.58}$$

$$f_{\text{var}} \;\alpha\; \frac{1}{R}$$

Load resistance R is not a directly or readily measurable parameter for feedback proposes. Alternatively, since $v_o = \bar{I}_o R$, substitution for R in equation (15.58) gives

$$f_{\text{var}} = f_s \frac{R_{crit.}}{v_o}\bar{I}_o \tag{15.59}$$

$$f_{\text{var}} \;\alpha\; \bar{I}_o$$

That is, for discontinuous inductor current, namely $\bar{I}_i < ½\Delta i_L$ or $\bar{I}_o < v_o / R_{crit}$, if the switch on-state period t_T remains constant and f_{var} is either varied proportionally with load current or varied inversely with load resistance, then the required output voltage v_o will be maintained.

15.3.5ii - fixed switching frequency f_s, variable on-time $t_{T\text{var}}$

The operating frequency f_s remains fixed while the switch-on time $t_{T\text{var}}$ is reduced such that the ripple current can be reduced. Operation is specified by equating the input energy and the output energy as in equation (15.57), thus maintaining a constant capacitor charge, hence voltage. That is

$$½\Delta i_L E_i t_{T\,\text{var}} = \frac{v_o^2}{R}\frac{1}{f_s} \tag{15.60}$$

Isolating the variable on-time $t_{T\text{var}}$ gives

$$t_{T\,\text{var}} = \frac{v_o^2}{½\Delta i_L E_i f_s}\frac{1}{R}$$

Substituting Δi_L from equation (15.38) gives

$$t_{T\,\text{var}} = t_T\sqrt{R_{crit}}\frac{1}{\sqrt{R}}$$

$$t_{T\,\text{var}} \;\alpha\; \frac{1}{\sqrt{R}} \tag{15.61}$$

Again, load resistance R is not a directly or readily measurable parameter for feedback proposes and substitution of $v_o / \bar{I}_o$ for R in equation (15.61) gives

$$t_{T\,\text{var}} = t_T\sqrt{\frac{R_{crit.}}{v_o}}\sqrt{\bar{I}_o}$$

$$t_{T\,\text{var}} \;\alpha\; \sqrt{\bar{I}_o} \tag{15.62}$$

That is, if the switching frequency f_s is fixed and switch on-time t_T is reduced proportionally to $\sqrt{\bar{I}_o}$ or inversely to $\sqrt{R}$, when discontinuous inductor current commences, namely $\bar{I}_i < ½\Delta i_L$ or $\bar{I}_o < v_o / R_{crit}$, then the required output voltage magnitude v_o will be maintained.

15.3.6 Output ripple voltage

The output ripple voltage is the capacitor ripple voltage. The ripple voltage for a capacitor is defined as

$$\Delta v_o = \tfrac{1}{C}\int i\,dt$$

Figure 15.5 shows that for continuous inductor current, the constant output current $\bar{I}_o$ is provided solely from the capacitor during the period t_{on} when the switch is on, thus

$$\Delta v_o = \tfrac{1}{C}\int i\,dt = \tfrac{1}{C} t_{on}\bar{I}_o$$

Substituting for $\overline{I}_o = v_o / R$ gives

$$\Delta v_o = \tfrac{1}{C}\int i\,dt = \tfrac{1}{C} t_{on} \overline{I}_o = \tfrac{1}{C} t_{on} \,{}^{v_o}\!/_{R}$$

Rearranging gives the percentage voltage ripple (peak to peak) in the output voltage

$$\Delta v_o / v_o = \tfrac{1}{CR} t_{on} = \tfrac{1}{CR}\,\delta\tau \qquad (15.63)$$

The capacitor equivalent series resistance and inductance can be account for, as with the forward converter, 15.1.4. When the switch conducts, the output current is constant and is provided from the capacitor. No ESL effects results during this portion of the switching cycle.

Example 15.2: ***Boost (step-up flyback) converter***

The boost converter in figure 15.5 is to operate with a 50µs transistor fixed on-time in order to convert the 50 V input up to 75 V at the output. The inductor is 250µH and the resistive load is 2.5Ω.

i. Calculate the switching frequency, hence transistor off-time, assuming continuous inductor current.
ii. Calculate the mean input and output current.
iii. Draw the inductor current, showing the minimum and maximum values.
iv. Calculate the capacitor rms ripple current.
v. Derive general expressions relating the operating frequency to varying load resistance.
vi. At what load resistance does the instantaneous input current fall below the output current.

Solution

i. From equation (15.39), which assumes continuous inductor current

$$\frac{v_o}{E_i} = \frac{1}{1-\delta} \quad \text{where} \quad \delta = t_T / \tau$$

that is

$$\frac{75\text{V}}{50\text{V}} = \frac{1}{1-\delta} \quad \text{where} \quad \delta = \frac{50\mu\text{s}}{\tau} = {}^{1}\!/_{3}$$

That is, τ = 150 µs or f_s= 1/τ = 6.66 kHz, with a 100µs switch off-time.

ii. The mean output current $\overline{I}_o$ is given by

$$\overline{I}_o = v_o / R = 75\text{V}/2.5\Omega = 30\text{A}$$

From power transfer considerations

$$\overline{I}_i = \overline{I}_L = v_o \overline{I}_o / E_i = 75\text{V}\times 30\text{A}/50\text{V} = 45\text{A}$$

iii. From $v = L\,di/dt$, the ripple current $\Delta i_L = E_i t_T / L$ = 50V x 50µs /250 µH = 10 A

that is

$$\hat{i}_L = \overline{I}_L + \tfrac{1}{2}\Delta i_L = 45\text{A} + \tfrac{1}{2}\times 10\text{A} = 50\text{A}$$

$$\check{i}_L = \overline{I}_L - \tfrac{1}{2}\Delta i_L = 45\text{A} - \tfrac{1}{2}\times 10\text{A} = 40\text{A}$$

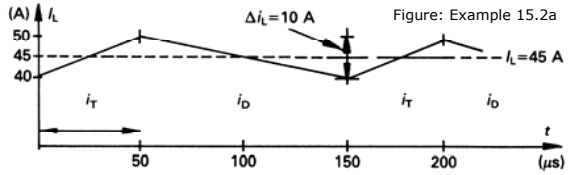


Figure: Example 15.2a

iv. The capacitor current is derived by using Kirchhoff"s current law such that at any instant in time, the diode current, plus the capacitor current, plus the 30A constant load current into *R*, all sum to zero.

$$i_{C\text{rms}} = \sqrt{\frac{1}{\tau}\left[\int_0^{t_T} \overline{I}_o^{\,2} dt + \int_0^{\tau - t_T} \left(\frac{\Delta i_L}{\tau - t_T} t - \hat{i}_L + \overline{I}_o\right)^2 dt\right]}$$

$$= \sqrt{\frac{1}{150\mu\text{s}}\left[\int_0^{50\,\mu\text{s}} 30\text{A}^2 dt + \int_0^{100\,\mu\text{s}} \left(\frac{10\text{A}}{100\mu\text{s}} t - 20\text{A}\right)^2 dt\right]} = 21.3\text{A}$$

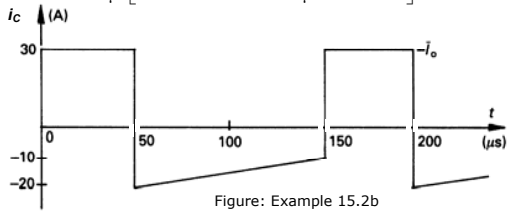


Figure: Example 15.2b

v. The critical load resistance, R_{crit}, produces an input current with Δi_L = 10 A ripple. Since the energy input equals the energy output

$$\tfrac{1}{2}\Delta i \times E_i \times \tau = v_o \times v_o / R_{crit} \times \tau$$

that is

$$R_{crit} = \frac{2v_o^2}{E_i \Delta i} = \frac{2\times 75\text{V}^2}{50\text{V}\times 10\text{A}} = 22\tfrac{1}{2}\Omega$$

Alternatively, equation (15.56) or equation (15.42) can be rearranged to give R_{crit}.
For a load resistance of less than 22½ Ω, continuous inductor current flows and the operating frequency is fixed at 6.66 kHz with $\delta = 1/3$, that is

$$f_s = 6.66 \text{ kHz for all } R \le 22.5\ \Omega$$

For load resistance greater than 22½ Ω, ($< v_o / R_{crit} = 3\tfrac{1}{3}$A), the energy input occurs in 150 μs burst whence from equation (15.57)

$$\tfrac{1}{2}\Delta i_L E_i \times 150\mu\text{s} = \frac{v_o^2}{R}\frac{1}{f_{var}}$$

that is

$$f_{var} = \frac{R_{crit}}{\tau}\frac{1}{R} = \frac{22.5\Omega}{150\mu\text{s}}\frac{1}{R}$$

$$f_{var} = \frac{150}{R} \text{ kHz} \quad \text{for} \quad R \ge 22\tfrac{1}{2}\Omega$$

vi. The ±5A inductor ripple current is independent of the load, provided the critical resistance is not exceeded. When the average inductor current (input current) is less than 5A more than the output current, the capacitor must provide load current not only when the switch is on but also when the switch is off. The transition is given by equation (15.47), that is

$$\delta \le 1 - \sqrt{\frac{2L}{\tau R}}$$

$$\tfrac{1}{3} \le 1 - \sqrt{\frac{2\times 250\mu\text{H}}{150\mu\text{s}\times \text{R}}}$$

This yields $R \ge 7\tfrac{1}{2}\Omega$ and a load current of 10A. The average inductor current is 15A, with a minimum value of 10A, the same as the load current. That is, for $R < 7\tfrac{1}{2}\Omega$ all the load requirement is provided from the input inductor when the switch is off, with excess energy charging the output capacitor. For $R > 7\tfrac{1}{2}\Omega$ insufficient energy is available from the inductor to provide the load energy throughout the whole of the period when the switch is off. The capacitor supplements the load requirement towards the end of the off period. When $R > 22\tfrac{1}{2}\Omega$ (the critical resistance), discontinuous inductor current occurs, and the duty cycle dependent transfer function is no longer valid.

♣

Example 15.3: ***Alternative boost (step-up flyback) converter***

The alternative boost converters (producing a dc supply either above E_i (left) or below 0V (right)) shown in the following figure are to operate under the same conditions as the boost converter in example 15.2, namely, with a 50μs transistor fixed on-time in order to convert the 50 V input up to 75 V at the output. The energy transfer inductor is 250μH and the resistive load is 2.5Ω.

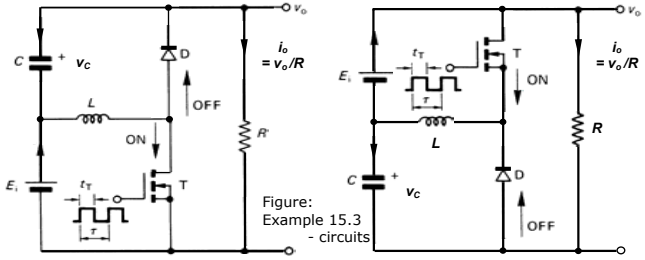


Figure: Example 15.3 - circuits

i. Derive the voltage transfer ratio and critical resistance expression for the alternative boost converter, hence showing the control performance is identical to the boost converter shown in figure 15.5.

ii. By considering circuit voltage and current waveforms, identify how the two boost converters differ.

Solution

i. Assuming non-zero, continuous inductor current, the inductor current excursion, which for this boost converter is not the input current excursion, during the switch on-time t_T and switch off-time τ- t_T, is given by

$$L\Delta i_L = E_i t_T = v_C(\tau - t_T)$$

but $v_C = v_o - E_i$, thus substitution for v_C gives

$$E_i t_T = (v_o - E_i)(\tau - t_T)$$

and after rearranging,

$$\frac{v_o}{E_i} = \frac{\bar{I}_i}{\bar{I}_o} = \frac{1}{1-\delta} \quad \left(= 1 + \frac{\delta}{1-\delta}\right)$$

where $\delta = t_T / \tau$ and t_T is the transistor on-time. This is the same voltage transfer function as for the conventional boost converter, equation (15.39). This result would be expected since both converters have the same ac equivalent circuit. Similarly, the critical resistance would be expected to be the same for each boost converter variation.
Examination of the switch on and off states shows that during the switch on-state, energy is transfer to the load from the input supply, independent of switching action.

This mechanism is analogous to autotransformer action where the output current is due to both transformer action and the input current being directed to the load.
The critical load resistance for continuous inductor current is specified by $R_{crit} \le v_o / \overline{I}_o$.
By equating the capacitor net charge flow, the inductor current is related to the output current by $\overline{I}_L = \overline{I}_o/(1-\delta)$. At minimum inductor current, $\overline{I}_L = \tfrac{1}{2}\Delta i_L$ and substituting with $\Delta i_L = E_i t_T / L$, gives

$$R_{crit} \le \frac{v_o}{\overline{I}_o} = \frac{v_o}{(1-\delta)\overline{I}_L} = \frac{v_o}{(1-\delta)\tfrac{1}{2}\Delta i_L} = \frac{v_o}{(1-\delta)\tfrac{1}{2}E_i t_T / L} = \frac{2L}{\tau\delta(1-\delta)^2}$$

Thus for a given energy throughput, some energy is provided from the supply to the load when providing the inductor energy, hence the discontinuous inductor current threshold occurs at the same load level for both boost converters.

ii. Since the two circuits have the same ac equivalent circuit, the inductor and capacitor, currents and voltages would be expected to be the same for each circuit, as shown in the waveforms in example 15.2. Consequently, the switch and diode voltages and currents are also the same for each boost converter.
The two principal differences are the supply current and the capacitor voltage rating. The capacitor voltage rating for the alternative boost converter is v_o - E_i as opposed to v_o for the convention converter.
The supply current for the alternative converter is discontinuous, as shown in the following waveforms. This will negate the desirable continuous current feature exploited in boost converters that are controlled so as to produce sinusoidal input current.

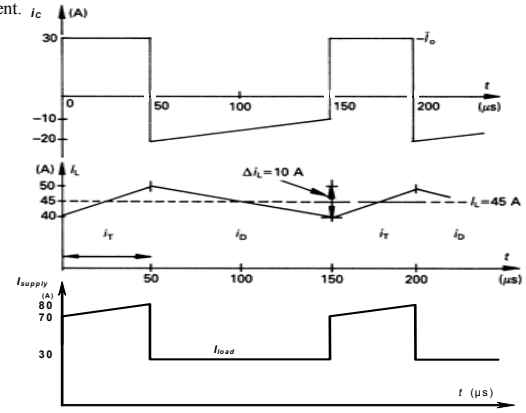
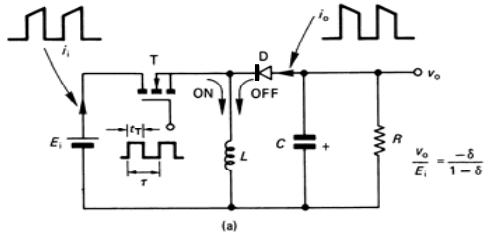


Figure: Example 15.3 - waveforms ♣

15.4 The buck-boost converter

The basic *buck-boost flyback converter* circuit is shown in figure 15.5a. When transistor T is on, energy is transferred to the inductor. When the transistor turns off, inductor current is forced through the diode. Energy stored in *L* is transferred to *C* and the load *R*. This transfer action results in an output voltage of opposite polarity to that of the input. Neither the input nor the output current is continuous, although the inductor current may be continuous or discontinuous.



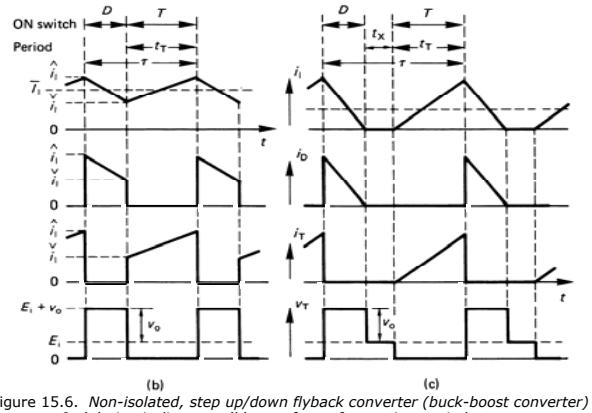


Figure 15.6. *Non-isolated, step up/down flyback converter (buck-boost converter) where $v_o \le 0$: (a) circuit diagram; (b) waveforms for continuous inductor current; and (c) discontinuous inductor current waveforms.*

15.4.1 Continuous choke current

Various circuit voltage and current waveforms for the buck-boost flyback converter operating in a continuous inductor conduction mode are shown in figure 15.6b.
Assuming a constant input and output voltage, the change in inductor current is given by

$$\Delta i_L = \frac{E_i}{L} t_T = \frac{-v_o}{L}(\tau - t_T) \tag{15.64}$$

thus

$$\frac{v_o}{E_i} = \frac{\overline{I}_i}{\overline{I}_o} = -\frac{\delta}{1-\delta} \tag{15.65}$$

where $\delta = t_T/\tau$. For $\delta < ½$ the output magnitude is less than the input voltage magnitude, while for $\delta > ½$ the output is greater in magnitude than the input.
The maximum and minimum inductor current is given by

$$\hat{i}_L = \frac{\overline{I}_o}{1-\delta} + ½\frac{v_o}{L}(1-\delta)\tau \tag{15.66}$$

and

$$\hat{i}_L = \frac{\overline{I}_o}{1-\delta} - ½\frac{v_o}{L}(1-\delta)\tau \tag{15.67}$$

15.4.2 Discontinuous capacitor charging current in the switch off-state

It is possible that the inductor current falls below the output (resistor) current during a part of the cycle when the switch is off and the inductor is transferring energy to the output circuit. Under such conditions, towards the end of the off period, some of the load current requirement is provided by the capacitor even though this is the period during which its charge is replenished by inductor energy. The circuit independent transfer function in equation (15.65) remains valid. This discontinuous charging condition occurs when the minimum inductor current and the output current are equal. That is

$$\begin{aligned} &\overset{\vee}{I}_L - \overline{I}_o \le 0 \\ &\overline{I}_L - ½\Delta i_L - \overline{I}_o \le 0 \\ &\frac{\overline{I}_o}{1-\delta} - ½\frac{\overline{I}_o R}{L}(1-\delta)\tau - \overline{I}_o \le 0 \end{aligned} \tag{15.68}$$

which yields

$$\delta \le 1 + \frac{L}{\tau R} - \sqrt{\left(1+\frac{L}{\tau R}\right)^2 - 1} \tag{15.69}$$

15.4.3 Discontinuous choke current

The change from continuous to discontinuous inductor current conduction occurs when

$$\overline{I}_L = ½\,\hat{i}_L = \Delta i_L \tag{15.70}$$

where from equation (15.64) $\hat{i}_L = v_o(\tau - t_T)/L$

The circuit waveforms for discontinuous conduction are shown in figure 15.6c. The output voltage for discontinuous conduction is evaluated from

$$\hat{i}_L = \frac{E_i}{L} t = -\frac{v_o}{L}(\tau - t_T - t_x) \tag{15.71}$$

which yields

$$\frac{v_o}{E_i} = -\frac{\delta}{1-\delta-\frac{t_x}{\tau}} \tag{15.72}$$

Alternatively, using equation (15.71) and

$$\overline{I}_L = ½\delta\,\hat{i}_L \tag{15.73}$$

yields

$$\overline{I}_L = \frac{E_i \tau \delta}{2L} \tag{15.74}$$

The inductor current is neither the input current nor the output current, but is comprised of components of each of these currents. Examination of figure 15.6b, reveals that these currents are a proportion of the inductor current dependant on the duty cycle, and that on the verge of discontinuous conduction:

$\overline{I}_i = ½\delta\,\hat{i}_L = \delta\overline{I}_L$ and $\overline{I}_o = ½(1-\delta)\hat{i}_L = (1-\delta)\overline{I}_L$ where $\hat{i}_L = \Delta i_L = ½\,\overline{I}_L$

Thus using $\overline{I}_i = \delta\overline{I}_L$ equation (15.74) becomes

$$\overline{I}_i = \frac{E_i \tau \delta^2}{2L} \tag{15.75}$$

Assuming power-in equals power-out, that is $E_i\overline{I}_i = v_o\overline{I}_o$

$$\frac{v_o}{E_i} = \frac{E_i\tau\delta^2}{2L\overline{I}_o} = \frac{v_o\tau\delta^2}{2L\overline{I}_i} = \delta\sqrt{\frac{\tau R}{2L}} \tag{15.76}$$

On the verge of discontinuous conduction, these equations can be rearranged to give

$$\overline{I}_o = \frac{E_i}{2L}\tau\delta(1-\delta) \tag{15.77}$$

At a low output current or low input voltage there is a likelihood of discontinuous conduction. To avoid this condition, a larger inductance value is needed, which worsen transient response. Alternatively, with extremely low on-state duty cycles, a voltage-matching transformer can be used to increase δ. Once using a transformer, any smps

technique can be used to achieve the desired output voltage. Figures 15.6b and c show that both the input and output current are always discontinuous.

15.4.4 Load conditions for discontinuous inductor current

As the load current decreases, the inductor average current also decreases, but the inductor ripple current magnitude is unchanged. If the load resistance is increased sufficiently, the bottom of the triangular inductor current, $\check{i}_L$, eventually reduces to zero. Any further increase in load resistance causes discontinuous inductor current and the voltage transfer function given by equation (15.65) is no longer valid and equations (15.71) and (15.76) are applicable. The critical load resistance for continuous inductor current is specified by

$$R_{crit} \le \frac{v_o}{\bar{I}_o} \tag{15.78}$$

Substituting for, the average input current in terms of $\hat{i}_L$ and v_o in terms of Δi_L from equation (15.64) , yields

$$R_{crit} \le \frac{v_o}{\bar{I}_o} = \frac{2L}{\tau(1-\delta)^2} \tag{15.79}$$

By substituting the switching frequency ($f_s = 1/\tau$) or the fundamental inductor reactance ($X_L = 2\pi f_s L$) the following critical resistance forms result.

$$R_{crit} \le \frac{v_o}{\bar{I}_o} = \frac{2L}{\tau(1-\delta)^2} = \frac{2f_sL}{(1-\delta)^2} = \frac{X_L}{\pi(1-\delta)^2} \quad (\Omega) \tag{15.80}$$

If the load resistance increases beyond R_{crit}, the output voltage can no longer be maintained with duty cycle control according to the voltage transfer function in equation (15.65).

15.4.5 Control methods for discontinuous inductor current

Once the load current has reduced to the critical level as specified by equation (15.80), the input energy is in excess of the load requirement. Open loop load voltage regulation control is lost and the capacitor *C* tends to overcharge.

Hardware approaches can be used to solve this problem

- increase *L* thereby decreasing the inductor current ripple p-p magnitude
- step-down transformer impedance matching to effectively reduce the apparent load impedance

Two control approaches to maintain output voltage regulation when $R > R_{crit}$ are

- vary the switching frequency f_s, maintaining the switch on-time t_T constant so that Δi_L is fixed or

- reduce the switch on-time t_T , but maintain a constant switching frequency f_s, thereby reducing Δi_L.

If a fixed switching frequency is desired for all modes of operation, then reduced on-time control, using output voltage feedback, is preferred. If a fixed on-time mode of control is used, then the output voltage is control by inversely varying the frequency with output voltage.

15.4.5i - fixed on-time t_T, variable switching frequency f_{var}

The operating frequency f_{var} is varied while the switch-on time t_T is maintained constant such that the ripple current remains unchanged. Operation is specified by equating the input energy and the output energy, thus maintaining a constant capacitor charge, hence output voltage. That is, equating energies

$$½\Delta i_L E_i t_T = \frac{v_o^2}{R}\frac{1}{f_{\text{var}}} \tag{15.81}$$

Isolating the variable switching frequency f_{var} gives

$$f_{\text{var}} = \frac{v_o^2}{½\Delta i_L E_i t_T}\frac{1}{R}$$

$$= f_s R_{crit}\frac{1}{R}$$

$$f_{\text{var}} \quad \alpha \quad \frac{1}{R} \tag{15.82}$$

Load resistance *R* is not a directly or readily measurable parameter for feedback proposes. Alternatively, since $v_o = \bar{I}_o R$, substitution for *R* in equation (15.82) gives

$$f_{\text{var}} = f_s \frac{R_{crit}}{v_o}\bar{I}_o$$

$$f_{\text{var}} \quad \alpha \quad \bar{I}_o \tag{15.83}$$

That is, for discontinuous inductor current, namely $\bar{I}_L < ½\Delta i_L$ or $\bar{I}_o < v_o / R_{crit}$, if the switch on-state period t_T remains constant and f_{var} is either varied proportionally with load current or varied inversely with load resistance, then the required output voltage v_o will be maintained.

15.4.5ii - fixed switching frequency f_s, variable on-time $t_{T\text{var}}$

The operating frequency f_s remains fixed while the switch-on time $t_{T\text{var}}$ is reduced such that the ripple current can be reduced. Operation is specified by equating the input energy and the output energy as in equation (15.81), thus maintaining a constant capacitor charge, hence voltage. That is

$$½\Delta i_L E_i t_{T\,\text{var}} = \frac{v_o^2}{R}\frac{1}{f_s} \tag{15.84}$$

Isolating the variable on-time $t_{T\text{var}}$ gives

$$t_{T\,\mathrm{var}} = \frac{v_o^2}{½\Delta i_L E_i f_s}\frac{1}{R}$$

Substituting Δi_L from equation (15.64) gives

$$t_{T\,\mathrm{var}} = t_T\sqrt{R_{crit}}\frac{1}{\sqrt{R}} \qquad t_{T\,\mathrm{var}} \;\alpha\; \frac{1}{\sqrt{R}} \tag{15.85}$$

Again, load resistance R is not a directly or readily measurable parameter for feedback proposes and substitution of $v_o / \overline{I}_o$ for R in equation (15.61) gives

$$t_{T\,\mathrm{var}} = t_T\sqrt{\frac{R_{crit}}{v_o}}\sqrt{\overline{I}_o} \qquad t_{T\,\mathrm{var}} \;\alpha\; \sqrt{\overline{I}_o} \tag{15.86}$$

That is, if the switching frequency f_s is fixed and switch on-time t_T is reduced proportionally to $\sqrt{\overline{I}_o}$ or inversely to $\sqrt{R}$, when discontinuous inductor current commences, namely $\overline{I}_L < ½\Delta i_L$ or $\overline{I}_o < v_o / R_{crit}$, then the required output voltage magnitude v_o will be maintained.

Alternatively the output voltage is related to the duty cycle by $v_o = \delta E_i\sqrt{R\tau / 2L}$.

15.4.6 Output ripple voltage

The output ripple voltage is the capacitor ripple voltage. Ripple voltage for a capacitor is defined as

$$\Delta v_o = \tfrac{1}{C}\int i\,dt$$

Figure 15.6 shows that the constant output current $\overline{I}_o$ is provided solely from the capacitor during the period t_{on} when the switch conducting, thus

$$\Delta v_o = \tfrac{1}{C}\int i\,dt = \tfrac{1}{C}t_{on}\overline{I}_o$$

Substituting for $\overline{I}_o = v_o / R$ gives

$$\Delta v_o = \tfrac{1}{C}\int i\,dt = \tfrac{1}{C}t_{on}\overline{I}_o = \tfrac{1}{C}t_{on}\,v_o/R$$

Rearranging gives the percentage peak-to-peak voltage ripple in the output voltage

$$\Delta v_o/v_o = \tfrac{1}{CR}t_{on} = \tfrac{1}{CR}\delta\tau \tag{15.87}$$

The capacitor equivalent series resistance and inductance can be account for, as with the forward converter, 15.1.5. When the switch conducts, the output current is constant and is provided from the capacitor. No ESL effects result during this portion of the switching cycle.

15.4.7 Buck-boost, flyback converter design procedure

The output voltage of the buck-boost converter can be regulated by operating at a fixed frequency and varying the transistor on-time t_T. However, the output voltage diminishes while the transistor is on and increases when the transistor is off. This characteristic makes the converter difficult to control on a fixed frequency basis.

A simple approach to control the flyback regulator in the discontinuous mode is to fix the peak inductor current, which specifies a fixed diode conduction time, t_D. Frequency then varies directly with output current and transistor on-time varies inversely with input voltage.

With discontinuous inductor conduction, the worst-case condition exists when the input voltage is low while the output current is at a maximum. Then the frequency is a maximum and the dead time t_x is zero because the transistor turns on as soon as the diode stops conducting.

Given	Worst case
$E_{i(\min)}$	$E_i = E_{i(\min)}$
V_o	$\overline{I}_o = \overline{I}_{o(\max)}$
$\overline{I}_{o(\max)}$	$t_x = 0$
$f_{(\max)}$	Δe_o

Assuming a fixed value of peak inductor current $\hat{i}_i$ and output voltage v_o, the following equations are valid

$$E_{i(\min)}t_T = v_o t_D = \hat{i}_i \times L \tag{15.88}$$

$$\tau_{(\min)} = 1/f_{(\max)} \tag{15.89}$$

Equation (15.88) yields

$$t_D = \frac{1}{f_{(\max)}\left(\frac{v_o}{E_{i(\min)}}+1\right)} \tag{15.90}$$

Where the diode conduction time t_D is constant since in equation (15.88), v_o, $\hat{i}_i$, and L are all constants. The average output capacitor current is given by

$$\overline{I}_o = ½\hat{i}_i(1-\delta)$$

and substituting equation (15.90) yields

$$\overline{I}_{o(\max)} ½\hat{i}_i \times f_{(\max)} \times \frac{1}{f_{(\max)}\left(\frac{v_o}{E_{i(\min)}}+1\right)}$$

therefore

$$\hat{i}_i = 2\times\overline{I}_{o(\max)}\times\left(\frac{v_o}{E_{i(\min)}}+1\right)$$

and upon substitution into equation (15.88)

$$L = \frac{t_D v_o}{2\,\overline{I}_{o\,(\max)}(\frac{v_o}{E_{i(\min)}} + 1)} \qquad (15.91)$$

The minimum capacitance is specified by the maximum allowable ripple voltage, that is

$$C_{(\min)} = \frac{\Delta Q}{\Delta e_o} = \frac{\hat{i}_i\, t_D}{2\Delta e_o}$$

that is

$$C_{(\min)} = \frac{\overline{I}_{o\,(\max)} t_D}{\Delta e_o(\frac{v_o}{E_{i(\min)}} + 1)} \qquad (15.92)$$

The ripple voltage is dropped across the capacitor equivalent series resistance, which is given by

$$ESR_{(\max)} = \frac{\Delta e_o}{\hat{i}_i} \qquad (15.93)$$

The frequency varies as a function of load current. Equation (15.89) gives

$$\frac{\overline{I}_o}{f} = \frac{\hat{i}_i\, t_T}{2} = \frac{\overline{I}_{o\,(\max)}}{f_{(\max)}}$$

therefore

$$f = f_{(\max)} \times \frac{\overline{I}_o}{\overline{I}_{o\,(\max)}} \qquad (15.94)$$

and

$$f_{(\min)} = f_{(\max)} \times \frac{\overline{I}_{o\,(\min)}}{\overline{I}_{o\,(\max)}} \qquad (15.95)$$

Example 15.4: ***Buck-boost flyback converter***

The 10kHz flyback converter in figure 15.6 is to operate from a 50V input and produces an inverted non-isolated 75V output. The inductor is 300µH and the resistive load is 2.5Ω.

i. Calculate the duty cycle, hence transistor off-time, assuming continuous inductor current.
ii. Calculate the mean input and output current.
iii. Draw the inductor current, showing the minimum and maximum values.
iv. Calculate the capacitor rms ripple current.

v. Determine
   - the critical load resistance.
   - the minimum inductance for continuous inductor conduction with 2.5 Ω load
vi. At what load resistance does the instantaneous input current fall below the output current.

Solution

i. From equation (15.72), which assumes continuous inductor current

$$\frac{v_o}{E_i} = -\frac{\delta}{1-\delta} \quad \text{where} \quad \delta = t_T / \tau$$

that is

$$\frac{75\text{V}}{50\text{V}} = \frac{\delta}{1-\delta} \quad \text{thus} \quad \delta = \tfrac{3}{5}$$

That is, $\tau = 1/f_s$ = 100 µs with a 60µs switch on-time.

ii. The mean output current $\overline{I}_o$ is given by

$$\overline{I}_o = v_o / R = 75\text{V}/2.5\Omega \;=\; 30\text{A}$$

From power transfer considerations

$$\overline{I}_i = \overline{I}_L = v_o \overline{I}_o / E_i = 75\text{V}\times 30\text{A}/50\text{V} \;=\; 45\text{A}$$

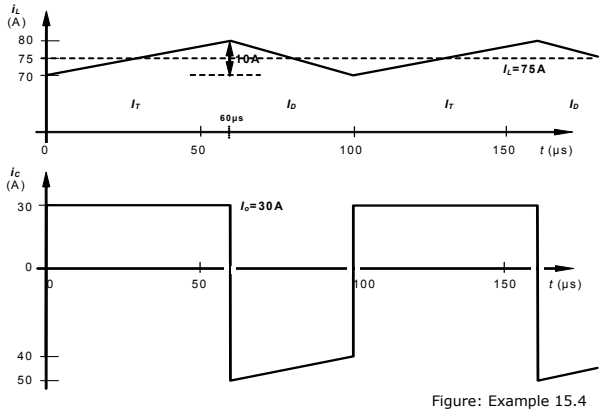


Figure: Example 15.4

iii. The average inductor current can be derived from

$$\overline{I}_i = \delta \overline{I}_L \quad \text{or} \quad \overline{I}_o = (1-\delta)\overline{I}_L$$

That is

$$\overline{I}_L = \overline{I}_i/\delta = \overline{I}_o/(1-\delta)$$
$$= 45\text{A}/\tfrac{3}{5} = 30\text{A}/\tfrac{2}{5} = 75\text{A}$$

From $v = L\,di/dt$, the ripple current $\Delta i_L = E_i t_T/L$ = 50V x 60µs /300 µH = 10 A, that is

$$\hat{i}_L = \overline{I}_L + \tfrac{1}{2}\Delta i_L = 75\text{A} + \tfrac{1}{2}\times 10\text{A} = 80\text{A}$$
$$\check{i}_L = \overline{I}_L - \tfrac{1}{2}\Delta i_L = 75\text{A} - \tfrac{1}{2}\times 10\text{A} = 70\text{A}$$

iv. The capacitor current is derived by using Kirchhoff's current law such that at any instant in time, the diode current, plus the capacitor current, plus the 30A constant load current into R, all sum to zero.

$$i_{C\text{rms}} = \sqrt{\frac{1}{\tau}\left[\int_0^{t_T} \overline{I}_o^2\,dt + \int_0^{\tau-t_T} \left(\frac{\Delta i_L}{\tau - t_T}t - \hat{i}_L + \overline{I}_o\right)^2 dt\right]}$$
$$= \sqrt{\frac{1}{100\mu\text{s}}\left[\int_0^{60\,\mu\text{s}} 30\text{A}^2\,dt + \int_0^{40\,\mu\text{s}} \left(\frac{10\text{A}}{40\mu\text{s}}t - 50\text{A}\right)^2 dt\right]}$$
$$= 36.8\text{A}$$

v. The critical load resistance, R_{crit}, produces an inductor current with Δi_L = 10 A ripple. From equation (15.80)

$$R_{crit} = \frac{2L}{\tau(1-\delta)^2} = \frac{2\times 300\mu\text{H}}{100\mu\text{s}\times(1-\tfrac{3}{5})^2} = 31\tfrac{1}{4}\Omega$$

The minimum inductance for continuous inductor current operation, with a 2½Ω load, can be found by rearranging the critical resistance formula, as follows:

$$L_{crit} = \tfrac{1}{2}R\tau(1-\delta)^2 = \tfrac{1}{2}\times 2.5\Omega\times 100\mu\text{s}\times(1-\tfrac{3}{5})^2 = 20\mu\text{H}$$

vi. The ±5A inductor ripple current is independent of the load, provided the critical resistance of 31¼Ω is not exceeded. When the average inductor current is less than 5A more than the output current, the capacitor must provide load current not only when the switch is on but also when the switch is off. The transition is given by equation (15.69), that is

$$\delta \le 1 + \frac{L}{\tau R} - \sqrt{\left(1+\frac{L}{\tau R}\right)^2 - 1}$$

Alternately, when

$$\overline{I}_i - \overline{I}_o = 5\text{A}$$
$$\frac{\overline{I}_o}{1-\delta} - \overline{I}_o = 5\text{A}$$

For δ=⅗, $\overline{I}_o$ =3⅓A. whence

$$R = \frac{v_o}{\overline{I}_o} = \frac{75V}{10/3\,A} = 22\tfrac{1}{2}\Omega$$

The average inductor current is 8⅓A, with a minimum value of 3⅓A, the same as the load current. That is, for R < 22½Ω all the load requirement is provided from the inductor when the switch is off, with excess energy charging the output capacitor. For R > 22½Ω insufficient energy is available from the inductor to provide the load energy throughout the whole of the period when the switch is off. The capacitor supplements the load requirement towards the end of the off period. When R > 31¼Ω (the critical resistance), discontinuous inductor current occurs, and the duty cycle dependent transfer function is no longer valid.

♣

15.5 The output reversible converter

The basic *reversible converter,* sometimes called an *asymmetrical half bridge converter* (see chapter 13.5), shown in figure 15.7a allows two-quadrant output voltage operation. Operation is characterised by both switches operating simultaneously, being either both on or both off.

The input voltage E_i is chopped by switches T_1 and T_2, and because the input voltage is greater than the load voltage v_o, energy is transferred from the dc supply E_i to L, C, and the load R. When the switches are turned off, energy stored in L is transferred via the diodes D_1 and D_2 to C and the load R but in a path involving energy being returned to the supply, E_i. This connection feature allows energy to be transferred from the load back into E_i when used with an appropriate load and the correct duty cycle.

Parts b and c respectively of figure 15.7 illustrate reversible converter circuit current and voltage waveforms for continuous and discontinuous conduction of L, in a forward converter mode, when δ > ½.

For analysis it is assumed that components are lossless and the output voltage v_o is maintained constant because of the large capacitance magnitude of the capacitor C across the output. The input voltage E_i is also assumed constant, such that $E_i \ge v_o > 0$, as shown in figure 15.7a.

15.5.1 Continuous inductor current

When the switches are turned on for period t_T, the difference between the supply voltage E_i and the output voltage v_0 is impressed across L. From $V=Ldi/dt$, the rising current change through the inductor will be

$$\Delta i_L = \hat{i}_L - \check{i}_L = \frac{E_i - v_o}{L}\times t_T \qquad (15.96)$$

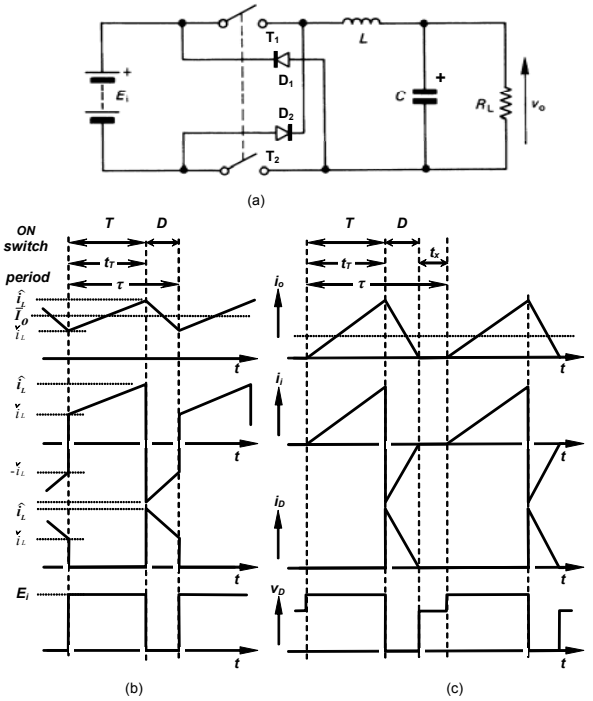


Figure 15.7. *Basic reversible converter with δ>½: (a) circuit diagram; (b) waveforms for continuous inductor current; and (c) discontinuous inductor current waveforms.*

When the two switches are turned off for the remainder of the switching period, τ-t_T, the two freewheel diodes conduct in series and $E_i + v_o$ is impressed across L. Thus, assuming continuous inductor conduction the inductor current fall is given by

$$\Delta i_L = \frac{E_i + v_o}{L} \times (\tau - t_T) \qquad (15.97)$$

Equating equations (15.96) and (15.97) yields

$$\frac{v_o}{E_i} = \frac{\bar{I}_i}{\bar{I}_o} = \frac{2t_T - \tau}{\tau} = 2\delta - 1 \qquad 0 \le \delta \le 1 \qquad (15.98)$$

The voltage transfer function is independent of circuit inductance L and capacitance C. Equation (15.98) shows that for a given input voltage, the output voltage is determined by the transistor conduction duty cycle δ and the output voltage $|v_o|$ is always less than the input voltage. This confirms and validates the original analysis assumption that $E_i \ge |v_o|$. The linear transfer function varies between -1 and 1 for $0 \le \delta \le 1$, that is, the output can be varied between $v_o = -E_i$, and $v_o = E_i$. The significance of the change in transfer function polarity at $\delta = ½$ is that

- for $\delta > ½$ the converter acts as a forward converter, but
- for $\delta < ½$, if the output is a negative source, the converter acts as a boost converter with energy transferred to the supply E_i, from the negative output source.

Thus the transfer function can be expressed as follows

$$\frac{v_o}{E_i} = \frac{\bar{I}_i}{\bar{I}_o} = 2\delta - 1 = 2(\delta - ½) \qquad ½ \le \delta \le 1 \qquad (15.99)$$

and

$$\frac{E_i}{v_o} = \frac{\bar{I}_o}{\bar{I}_i} = \frac{1}{2\delta - 1} = \frac{1}{2(\delta - ½)} \qquad 0 \le \delta \le ½ \qquad (15.100)$$

where equation (15.100) is in the boost converter transfer function form.

15.5.2 Discontinuous inductor current

In the forward converter mode, $\delta \ge ½$, the onset of discontinuous inductor current operation occurs when the minimum inductor current $\check{i}_L$, reaches zero. That is,

$$\bar{I}_L = ½\Delta i_L = \bar{I}_o \qquad (15.101)$$

If the transistor on-time t_T is reduced or the load resistance increases, the discontinuous condition dead time t_x appears as indicated in figure 15.7c. From equations (15.96) and (15.97), with $\check{i}_L = 0$, the following output voltage transfer function can be derived

$$\Delta i_L = \hat{i}_L - 0 = \frac{E_i - v_o}{L} \times t_T = \frac{E_i + v_o}{L} \times (\tau - t_T - t_x) \qquad (15.102)$$

which after rearranging yields

$$\frac{v_o}{E_i} = \frac{2\delta - 1 - \frac{t_x}{\tau}}{1 - \frac{t_x}{\tau}} \qquad 0 \le \delta < 1 \qquad (15.103)$$

15.5.3 Load conditions for discontinuous inductor current

In the forward converter mode, $\delta \geq$ ½, as the load current decreases, the inductor average current also decreases, but the inductor ripple current magnitude is unchanged. If the load resistance is increased sufficiently, the bottom of the triangular inductor current, $\check{i}_L$, eventual reduces to zero. Any further increase in load resistance causes discontinuous inductor current and the linear voltage transfer function given by equation (15.98) is no longer valid. Equation (15.103) is applicable. The critical load resistance for continuous inductor current is specified by

$$R_{crit} \leq \frac{v_o}{\bar{I}_o} \tag{15.104}$$

Substituting $\bar{I}_o = \bar{I}_L$ and using equations (15.96) and (15.101), yields

$$R_{crit} \leq \frac{v_o}{\bar{I}_o} = \frac{v_o}{½\Delta i_L} = \frac{2v_o L}{(E_i - v_o)t_T} \tag{15.105}$$

Dividing throughout by E_i and substituting $\delta = t_T / \tau$ yields

$$R_{crit} \leq \frac{v_o}{\bar{I}_o} = \frac{(2\delta - 1)L}{(1-\delta)\delta\tau} \tag{15.106}$$

By substituting the switching frequency ($f_s = 1/\tau$) or the fundamental inductor reactance ($X_L = 2\pi f_s L$), critical resistance can be expressed in the following forms.

$$R_{crit} \leq \frac{v_o}{\bar{I}_o} = \frac{2(\delta - ½)L}{(1-\delta)\delta\tau} = \frac{2(\delta - ½)f_s L}{(1-\delta)\delta} = \frac{(\delta - ½)X_L}{\pi(1-\delta)\delta} \quad (\Omega) \tag{15.107}$$

If the load resistance increases beyond R_{crit}, the output voltage can no longer be maintained with duty cycle control according to the voltage transfer function in equation (15.98).

15.5.4 Control methods for discontinuous inductor current

Once the load current has reduced to the critical level as specified by equation (15.102) the input energy is in excess of the load requirement. Open loop load voltage regulation control is lost and the capacitor *C* tends to overcharge.

As with the other converters considered, hardware and control approaches can mitigate this overcharging problem. The specific control solutions for the forward converter in section 15.3.4, are applicable to the reversible converter. The two time domain control approaches offer the following operational modes.

15.5.4i - fixed on-time t_T, variable switching frequency f_{var}

The operating frequency f_{var} is varied while the switch-on time t_T is maintained constant such that the magnitude of the ripple current remains unchanged. Operation is

specified by equating the input energy and the output energy, thus maintaining a constant capacitor charge, hence output voltage. That is, equating energies

$$½\Delta i_L E_i t_T = \frac{v_o^2}{R}\frac{1}{f_{\text{var}}} \tag{15.108}$$

Isolating the variable switching frequency f_{var} and using $v_o = \bar{I}_o R$ to eliminate R yields

$$f_{\text{var}} = f_s R_{crit}\frac{1}{R} = f_s \frac{R_{crit}}{v_o}\bar{I}_o$$
$$f_{\text{var}} \quad \alpha \quad \frac{1}{R} \quad \text{or} \quad f_{\text{var}} \quad \alpha \quad \bar{I}_o \tag{15.109}$$

That is, once discontinuous inductor current occurs at $\bar{I}_o < ½\Delta i_L$ or $\bar{I}_o < v_o / R_{crit}$, a constant output voltage v_o can be maintained if the switch on-state period t_T remains constant and the switching frequency is varied

- proportionally with load current, $\bar{I}_o$
- inversely with the load resistance, R_{crit}
- inversely with the output voltage, v_o.

15.5.4ii - fixed switching frequency f_s, variable on-time $t_{T\text{var}}$

The operating frequency f_s remains fixed while the switch-on time $t_{T\text{var}}$ is reduced, resulting in the ripple current magnitude being reduced. Equating input energy and output energy as in equation (15.22), thus maintaining a constant capacitor charge, hence voltage, gives

$$½\Delta i_L E_i t_{T\,\text{var}} = \frac{v_o^2}{R}\frac{1}{f_s} \tag{15.110}$$

Isolating the variable on-time $t_{T\text{var}}$, substituting for Δi_L, and using $v_o = \bar{I}_o R$ to eliminate R, gives

$$t_{T\,\text{var}} = t_T\sqrt{R_{crit}}\frac{1}{\sqrt{R}} = t_T\sqrt{\frac{R_{crit}}{v_o}}\sqrt{\bar{I}_o}$$
$$t_{T\,\text{var}} \quad \alpha \quad \frac{1}{\sqrt{R}} \quad \text{or} \quad t_{T\,\text{var}} \quad \alpha \quad \sqrt{\bar{I}_o} \tag{15.111}$$

That is, once discontinuous inductor current commences, if the switching frequency f_s remains constant, regulation of the output voltage v_o can be maintained if the switch on-state period t_T is varied

- proportionally with the square root of the load current, $\sqrt{\bar{I}_o}$
- inversely with the square root of the load resistance, $\sqrt{R_{crit}}$
- inversely with the square root of the output voltage, $\sqrt{v_o}$.

Example 15.5: ***Reversible forward converter***

The step-down reversible converter in figure 15.7a operates at a switching frequency of 10 kHz. The output voltage is to be fixed at 48 V dc across a 1 Ω resistive load. If the input voltage E_i=192 V and the choke L = 200μH:

i. calculate the switch T on-time duty cycle δ and switch on-time t_T
ii. calculate the average load current $\overline{I}_o$, hence average input current $\overline{I}_i$
iii. draw accurate waveforms for
- the voltage across, and the current through L; v_L and i_L
- the capacitor current, i_c
- the switch and diode voltage and current; v_T, v_D, i_T, i_D

iv. calculate
- the maximum load resistance R_{crit} before discontinuous inductor current with L=200μH and
- the value to which the inductance L can be reduced before discontinuous inductor current, if the maximum load resistance is 1Ω.

Solution

i. The switch on-state duty cycle δ can be calculate from equation (15.98), that is

$$2\delta - 1 = \frac{v_o}{E_i} = \frac{48\text{V}}{192\text{V}} = \tfrac{1}{4} \quad \Rightarrow \quad \delta = \tfrac{5}{8}$$

Also, from equation (15.98), for a 10kHz switching frequency, the switching period τ is 100μs and the transistor on-time t_T is given by

$$\delta = \frac{t_T}{\tau} = \frac{t_T}{100\mu\text{s}} = \tfrac{5}{8}$$

whence the transistor on-time is 62½μs and the diode conducts for 37½μs.

ii. The average load current is $\overline{I}_o = \frac{v_o}{R} = \frac{48\text{V}}{1\Omega} = 48\text{A} = \overline{I}_L$

From power-in equals power-out, the average input current is

$$\overline{I}_i = v_o \overline{I}_o / E_i = 48\text{V} \times 48\text{A}/192\text{V} = 12\text{A}$$

iii. The average output current is the average inductor current, 48A. The ripple current is given by equation (15.98), that is

$$\Delta i_L = \hat{i}_L - \check{i}_L = \frac{E_i - v_o}{L} \times t_T$$

$$= \frac{192\text{V} - 48\text{V}}{200\mu\text{H}} \times 62.5\mu\text{s} = 45\text{A p-p}$$

iv. Critical load resistance is given by equation (15.107), namely

$$R_{crit} \le \frac{v_o}{\overline{I}_o} = \frac{(2\delta - 1)L}{\tau\delta(1-\delta)}$$

$$= \frac{(2\times\tfrac{5}{8}-1)\times 200\mu\text{H}}{100\mu\text{s}\times\tfrac{5}{8}\times(1-\tfrac{5}{8})} = 32/15\Omega$$

$$= 2\tfrac{2}{15}\Omega \text{ when } \overline{I}_o = 22\tfrac{1}{2}\text{A}$$

Alternatively, the critical load current is 22½A (½Δi_L), thus the load resistance must not be greater than $v_o / \overline{I}_o$ = 48V/22.5A=32/15Ω, if the inductor current is to be continuous.

The critical resistance formula given in equation (15.107) is valid for finding critical inductance when inductance is made the subject of the equation, that is, rearranging equation (15.107) gives

$$L_{crit} = R\times(1-\delta)\times\delta\times\tau/(2\delta-1) \quad \text{(H)}$$

$$= 1\Omega\times(1-\tfrac{5}{8})\times\tfrac{5}{8}\times 100\mu\text{s}/(2\times\tfrac{5}{8}-1)$$

$$= 93\tfrac{3}{4}\mu\text{H}$$

That is, the inductance can be decreased from 200μH to 93¾μH when the load is 1Ω and continuous inductor current will flow.

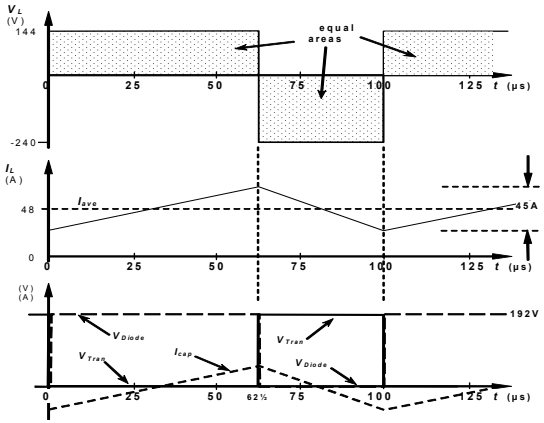


Figure: Example 15.5

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15.5.5 Comparison of the reversible converter with alternative converters

The reversible converter provides the full functional output range of the forward converter when δ>½ and provides part of the voltage function of the buck-boost converter when δ<½ but with energy transferring in the opposite direction.

Comparison of example 15.1 and 15.4 shows that although the same output voltage range can be achieved, the inductor ripple current is much larger for a given inductance L. A similar result occurs when compared with the buck-boost converter. Thus in each case, the reversible converter has a narrower output resistance range before discontinuous inductor conduction occurs. It is therefore concluded that the reversible converter should only be used if two quadrant operation is needed.

The ripple current I_f given by equation (15.2) for the forward converter and equation (15.96) for the reversible converter when $v_o > 0$, yield the following current ripple relationship.

$$\bar{I}_f = (2 - 1/\delta_r) \times \bar{I}_r \quad \text{where } 2\delta_r - 1 = \delta_f \text{ for } 0 \le \delta_f \le 1 \text{ and } ½ \le \delta_r \le 1 \tag{15.112}$$

This equation shows that the ripple current of the forward converter $\bar{I}_f$ is never greater than the ripple current I_r for the reversible converter, for the same output voltage.
In the voltage inverting mode, from equations (15.64) and (15.96), the relationship between the two corresponding ripple currents is given by

$$\bar{I}_{fly} = \frac{2(\delta_r - 1)}{2\delta_r - 1} \times \bar{I}_r \quad \text{where } \frac{2(\delta_r - 1)}{2\delta_r - 1} = \delta_{fly} \text{ for } 0 \le \delta_{fly} \le ½ \text{ and } 0 \le \delta_r \le ½ \tag{15.113}$$

Again the reversible converter always has the higher inductor ripple current. Essentially the higher ripple current results in each mode because the inductor energy release phase involving the diode occurs back into the supply, which is effectively in cumulative series with the output capacitor voltage.

The reversible converter offers some functional flexibility, since it can operate as a conventional forward converter, when only one of the two switches is turned off. (In fact, in this mode, switch turn-off is alternated between T_1 and T_2 so as to balance switch and diode losses.

15.6 The Ćuk converter

The Ćuk converter in figure 15.8 performs an inverting boost converter function with inductance in the input and the output. As a result, both the input and output currents can be continuous. A capacitor is used in the process of transferring energy from the input to the output and ac couples the input boost converter stage (L_1, T) to the output

forward converter (D, L_2). Specifically, the capacitor C_1 ac couples the switch T in the boost converter stage into the output forward converter stage.

15.6.1 Continuous inductor current

When the switch T is on and the diode D is reversed biased

$$i_{C1(on)} = -\bar{I}_{L2} = \bar{I}_o \tag{15.114}$$

When the switch is turned off, inductor currents i_{L1} and i_{L2} are divert through the diode and

$$i_{C1(off)} = \bar{I}_i \tag{15.115}$$

Over one steady-state cycle the average capacitor charge is zero, that is

$$i_{C1(on)}\delta\tau + i_{C1(off)}(1-\delta)\tau = 0 \tag{15.116}$$

which gives

$$\frac{i_{C1(on)}}{i_{C1(off)}} = \frac{\delta}{(1-\delta)} = \frac{\bar{I}_i}{\bar{I}_o} \tag{15.117}$$

From power-in equals power-out

$$\frac{v_o}{E_i} = \frac{\bar{I}_i}{\bar{I}_o} = \frac{\bar{I}_i}{\bar{I}_{L2}} \tag{15.118}$$

Thus equation (15.117) becomes

$$\frac{v_o}{E_i} = \frac{\bar{I}_i}{\bar{I}_o} = \frac{\bar{I}_i}{\bar{I}_{L2}} = -\frac{\delta}{(1-\delta)} \tag{15.119}$$

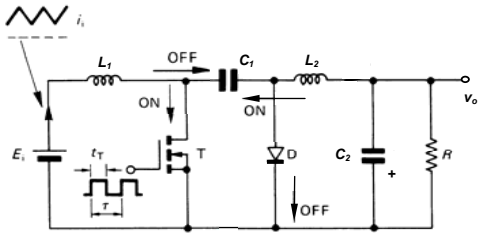

Figure 15.8. *Basic Ćuk converter.*

15.6.2 Discontinuous inductor current

The current rise in L_1 occurs when the switch is on, that is

$$\Delta i_{L1} = \frac{\delta \tau E_i}{L_1} \tag{15.120}$$

For continuous current in the input inductor L_1,

$$\bar{I}_i = \bar{I}_{L1} \geq \tfrac{1}{2}\Delta i_{L1} \tag{15.121}$$

which yields a maximum allowable load resistance, for continuous inductor current, of

$$R_{crit} \leq \frac{v_o}{\bar{I}_o} = \frac{2\delta L_1}{\tau(1-\delta)^2} = \frac{2 f_s L_1 \delta}{(1-\delta)^2} = \frac{\delta X_L}{\pi(1-\delta)^2} \tag{15.122}$$

The current rise in L_2 occurs when the switch is on and the inductor voltage is E_i, that is

$$\Delta i_{L2} = \frac{\delta \tau E_i}{L_2} \tag{15.123}$$

For continuous current in the output inductor L_2,

$$\bar{I}_o = \bar{I}_{L2} \geq \tfrac{1}{2}\Delta i_{L2} \tag{15.124}$$

which yields

$$R_{crit} \leq \frac{v_o}{\bar{I}_o} = \frac{2L_2}{\tau(1-\delta)} = \frac{2 f_s L_2}{(1-\delta)} = \frac{X_{L2}}{\pi(1-\delta)} \tag{15.125}$$

15.7 Comparison of basic converters

The converters considered employ an inductor to transfer energy from one dc voltage level to another voltage level. The basic converters comprise a switch, diode, inductor, and a capacitor. The reversible converter is a two-quadrant converter with two switches and two diodes, while the Cuk converter uses two inductors and two capacitors.

Table 15.1 summarises the main electrical features and characteristics of each basic converter. Figure 15.9 shows a plot of the voltage transformation ratios of the converters considered. With reference to figure 15.9, it should be noted that the flyback step-up/step-down converter and the Cuk converter both invert the input polarity.

Every converter can operate in any one of three inductor current modes:

- discontinuous
- continuous
- both continuous and discontinuous

The main converter operational features of continuous conduction compared with discontinuous inductor conduction are

- The voltage transformation ratio (transfer function) is independent of the load.
- Larger inductance but lower core hysteresis losses and saturation less likely.
- Higher converter costs with increased volume and weight.
- Worse transient response *(L /R)*.
- Power delivered is inversely proportional to load resistance, $P = V_o^2 / R$. In the discontinuous conduction mode, power delivery is inversely dependent on inductance.

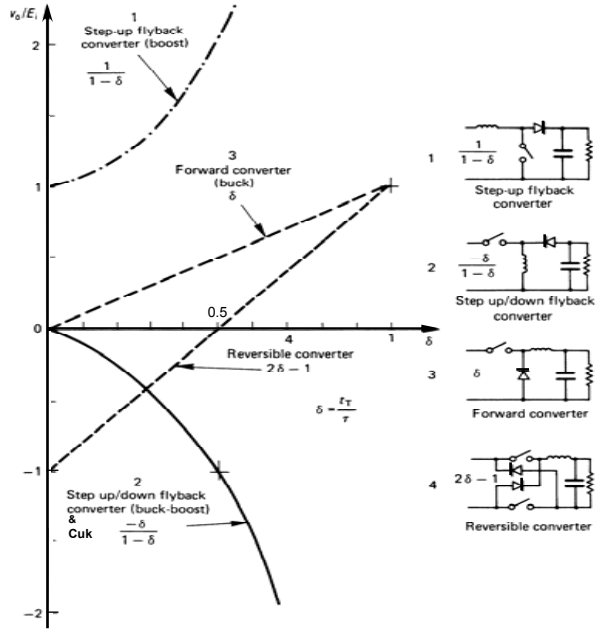

Figure 15.9. *Transformation voltage ratios for five converters when operated in the continuous inductor conduction mode.*

15.7.1 Critical load current

Examination of Table 15.1 show little commonality between the various converters and their performance factors and parameters. One common feature is the relationship between critical average output current $\bar{I}_o$ and the input voltage E_i at the boundary of continuous and discontinuous conduction.

Equations (15.9), (15.52), and (15.77) are identical, (for all smps), that is

$$\bar{I}_{o_{critical}} = \frac{E_i \tau}{2L}\delta(1-\delta) \qquad \text{(A)} \tag{15.126}$$

Table 15.1 Comparison of converter characteristics when inductor current is continuous

			converter			
			Forward Step-down	*Flyback Step-up*	*Flyback Step-up/down*	*Reversible*
Output voltage	v_o/E_i		δ	$\frac{1}{1-\delta}$	$-\frac{\delta}{1-\delta}$	$2\delta-1$
Output polarity with respect to input			Non-inverted	Non-inverted	inverted	any
Current sampled from the supply			discontinuous	continuous	discontinuous	bi-directional
Load current			continuous	discontinuous	discontinuous	continuous
Maximum transistor voltage	V	V	E_i	v_o	E_i+v_o	E_i
Maximum diode voltage	V	V	E_i	v_o	E_i+v_o	E_i
Ripple current	Δi	A	$E_i\delta\tau(1-\delta)/L$	$E_i\delta\tau/L$	$E_i\delta\tau/L$	$2E_i\delta\tau(1-\delta)/L$
Maximum transistor current	$\hat{i}_T$	A	$\bar{I}_o+\frac{v_o\tau(1-\delta)}{2L}$	$\bar{I}_i+\frac{E_i\tau\delta}{2L}$	$\bar{I}_L+\frac{E_i\tau\delta}{2L}$	$\bar{I}_o+\frac{(E_i-v_o)\tau\delta}{2L}$
Transistor rms current			low	high	high	low
Critical load resistance	R_{crit}	Ω	$\frac{2L}{\tau(1-\delta)}$	$\frac{2L}{\tau\delta(1-\delta)^2}$	$\frac{2L}{\tau(1-\delta)^2}$	$\frac{2(\delta-½)L}{\tau\delta(1-\delta)}$
Critical inductance	L_{crit}	H	$½R(1-\delta)\tau$	$½R\tau\delta(1-\delta)^2$	$½R\tau(1-\delta)^2$	$\frac{½R(1-\delta)\delta\tau}{(\delta-½)}$
o/p ripple voltage p-p	Δv_o	V	$\frac{\tau^2(1-\delta)}{8LC}v_o$	$\frac{\pi\delta}{RC}v_o$	$\frac{\pi\delta}{RC}v_o$	$\frac{\pi\delta}{RC}v_o$

This quadratic expression in δ shows that the critical mean output current reduces to zero as the on-state duty cycle δ tends to zero or unity. The maximum critical load current condition, for a given input voltage E_i, is when δ=½ and

$$\bar{I}_{o_c} = E_i\tau/8L \qquad (15.127)$$

Since power in equals power out, then from equation (15.126) the input average current and output voltage at the boundary of continuous conduction are related by

$$\bar{I}_{o_{critical}} = \frac{v_o\tau}{2L}\delta(1-\delta) \quad \text{(A)} \qquad (15.128)$$

The maximum output current at the boundary, for a given output voltage, v_o, is

$$\bar{I}_{i_c} = v_o\tau/8L \qquad (15.129)$$

The reversible converter, using the critical resistance equation (15.107) derived in section 15.5.3, yields twice the critical average output current given by equation (15.126). This is because its duty cycle range is restricted to half that of the other converters considered. Converter normalised equations for discontinuous conduction are shown in table 15.2.

A detailed analysis of discontinuous inductor current operation is given in appendix 15.9.

Table 15.2 Comparison of characteristics when the inductor current is discontinuous

$k=\frac{\delta^2R\tau}{4L}$	converter		
	Forward Step-down	*Flyback Step-up*	*Flyback Step-up/down*
$\delta_{critical}$	$\delta\le 1-\frac{2L}{R\tau}$	$\delta(1-\delta)^2\le\frac{2L}{R\tau}$	$\delta\le 1-\sqrt{\frac{2L}{R\tau}}$
$\frac{v_o}{E_i}$	$k\left[-1+\sqrt{1+\frac{2}{k}}\right]$	$½\left[1+\sqrt{1+8k}\right]$	$\sqrt{2k}$
$\frac{t_x}{\delta\tau}$	$½\left[1+\sqrt{1+\frac{2}{k}}\right]$	$\frac{1}{4k}\left[1+4k+\sqrt{1+8k}\right]$	$1+\frac{1}{\sqrt{2k}}$
$\hat{I}_L\times\frac{\delta R}{E_i}$	$4k\left[1+k-k\sqrt{1+\frac{2}{k}}\right]$	$4k$	$4k$

15.7.2 Isolation

In each converter, the output is not electrically isolated from the input and a transformer can be used to provide isolation. Figure 15.10 shows isolated versions of the three basic converters. The transformer turns ratio provides electrical isolation as well as providing matching to obtain the required output voltage range.

Figure 15.10a illustrates an isolated version of the forward converter shown in figure 15.2. When the transistor is turned on, diode D_1 conducts and L in the transformer secondary stores energy. When the transistor turns off, the diode D_3 provides a current path for the release of the energy stored in L. However when the transistor turns off and D_1 ceases to conduct, the stored transformer magnetising energy must be released. The winding incorporating D_2 provides a path to reset the core flux. A maximum possible duty cycle exists, depending on the turns ratio of the primary winding and freewheel winding. If a 1:1 ratio (as shown) is employed, a 50 per cent duty cycle limit will ensure the required volts-second for core reset.

The step-up flyback isolated converter in part b of figure 15.10 is little used. The two transistors must be driven by complementary signals. Core leakage and reset functions are facilitated by a third winding and blocking diode D_2.

The magnetic core in the buck-boost converter of part c of figure 15.10 performs a bifilar inductor function. When the transistor is turned on, energy is stored in the core. When the transistor is turned off, the core energy is released via the secondary winding into the capacitor. A core air gap is necessary to prevent magnetic saturation and an optional clamping winding can be employed, which operates at zero load.

The converters in parts a and c of figure 15.10 provide an opportunity to compare the main features and attributes of forward and flyback isolated converters. In the comparison it is assumed that the transformer turns ratio is 1:1:1.

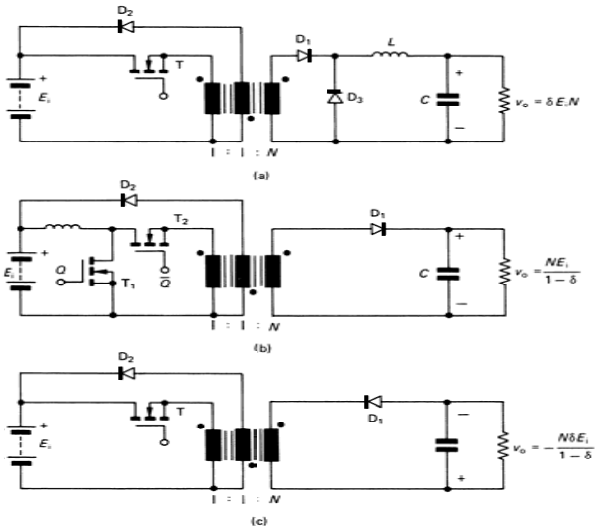

Figure 15.10. *Isolated output versions of the three basic converter configurations: (a) the forward converter; (b) step-up flyback converter; and (c) step up/down flyback converter.*

15.7.2i - *The isolated output,* ***forward converter*** *– figure 15.10a:*

- $v_o = n_T \delta E_i$ or $I_i = n_T \delta I_o$
- The magnetic element acts as a transformer, that is, because of the relative voltage polarities of the windings, energy is transferred from the input to the output, and not stored in the core, when the switch is on.
- The magnetising flux is reset by the current through the catch (feedback) winding and D_3, when the switch is off. The magnetising energy is returned to the supply E_i.
- The necessary transformer Vμs balance requirement (core energy-in equals core energy-out) means the maximum duty cycle is limited to $0 \le \delta \le 1/\left(1+n_{f/b}\right) < 1$ for $1{:}n_{f/b}{:}n_{sec}$ turns ratio. For example, the duty cycle is limited to 50%, $0 \le \delta \le ½$, with a 1:1:1 turns ratio.
- Because of the demagnetising winding, the off-state switch supporting voltage is $E_i + v_o$.
- The blocking voltage requirement of diode D_3 is E_i, v_o for D_1, and $2E_i$ for D_2.

15.7.2ii - *The isolated output,* ***flyback converter*** *– figure 15.10c:*

- $v_o = n_T E_i \delta/(1-\delta)$ or $I_i = n_T I_o \delta/(1-\delta)$
- The magnetic element acts as a storage inductor. Because of the relative voltage polarities of the windings (dot convention), when the switch is on, energy is stored in the core and no current flows in the secondary.
- The stored energy, which is due to the core magnetising flux is released (reset) as current into the load and capacitor C when the switch is off. (Unlike the forward converter where magnetising energy is returned to E_i, not the output, v_o.) Therefore there is no flyback converter duty cycle restriction, $0 \le \delta \le 1$.
- The third winding turns ratio is configured such that energy is only returned to the supply E_i under no load conditions.
- The switch supporting off-state voltage is $E_i + v_o$.
- The diode blocking voltage requirements are $E_i + v_o$ for D_1 and $2E_i$ for D_2.

The operational characteristics of each converter change considerably when the flexibility offered by tailoring the turns ratio is exploited. A multi-winding magnetic element design procedure is outlined in section 9.1.1, where the transformer turns ratio is not necessarily 1:1.

The basic approach to any transformer (coupled circuit) problem is to transfer, or refer, all components and variables to either the transformer primary or secondary circuit, whilst maintaining power and time invariance. Thus, maintaining power-in equals power-out, and assuming a secondary to primary turns ratio of n_T is to one, gives

$$\frac{v_s}{v_p} = \frac{n_s}{n_p} = n_T \qquad \frac{i_p}{i_s} = \frac{n_s}{n_p} = n_T \qquad \frac{Z_s}{Z_p} = \left(\frac{n_s}{n_p}\right)^2 = n_T^2 \qquad (15.130)$$

Time, that is switching frequency, is invariant. The circuit is then analysed. Subsequently, the appropriate parameters are referred back to their original side of the magnetically coupled circuit.

If the coupled circuit is used as a transformer, magnetising current (flux) builds, which must be reset to zero each cycle. Consider the transformer coupled forward converter in figure 15.10a. From Faraday's equation, $v = Nd\phi/dt$, and for maximum on-time duty cycle $\hat{\delta}$ the conduction V-µs of the primary must equal the conduction V-µs of the feedback winding which is returning the magnetising energy to the supply E_i.

$$E_i t_{on} = \frac{E_i}{n_{f/b}} t_{off}$$
$$t_{on} + t_{off} = \tau \qquad (15.131)$$

That is

$$E_i \hat{\delta} = \frac{E_i}{n_{f/b}}\left(1-\hat{\delta}\right)$$
$$\hat{\delta} = \frac{1}{1+n_{f/b}} \qquad (15.132)$$
$$0 \le \delta \le \frac{1}{1+n_{f/b}}$$

From Faraday's Law, the magnetizing current starts from zero and increases linearly to

$$\hat{I}_M = E_i t_{on} / L_M \qquad (15.133)$$

where L_M is the magnetizing inductance referred to the primary. During the switch off period, this current falls linearly, as energy is returned to E_i. The current must reach zero before the switch is turned on again, whence the energy taken from E_i and stored as magnetic energy in the core, has been returned to the supply.

Two examples illustrate the features of magnetically coupled circuit converters. Example 15.6 illustrates how the coupled circuit in the flyback converter acts as an inductor, storing energy from the primary source, and subsequently releasing that energy in the secondary circuit. In example 15.7, the forward converter coupled circuit act as a transformer where energy is transferred through the core under transformer action, but in so doing, self-inductance (magnetising) energy is built up in the core, which must be periodically released if saturation is to be avoided. Relative orientation of the windings, according to the flux dot convention shown in figure 15.10, is thus important, not only the primary relative to the secondary, but also relative to the feedback winding.

Example 15.6: ***Transformer coupled flyback converter***

The 10kHz flyback converter in figure 15.10c operates from a 50V input and produces a 225V dc output from a 1:1:3 (1:$n_{f/b}$:n_{sec}) step-up transformer loaded with a 22½Ω resistor. The transformer magnetising inductance is 300µH, referred to the primary:

i. Calculate the switch duty cycle, hence transistor off-time, assuming continuous inductor current.
ii. Calculate the mean input and output current.
iii. Draw the transformer currents, showing the minimum and maximum values.
iv. Calculate the capacitor rms ripple current.
v. Determine
   - the critical load resistance
   - the minimum inductance for continuous inductor conduction for a 22½ Ω load

Solution

The feedback winding does not conduct during normal continuous inductor current operation. This winding can therefore be ignored for analysis during normal operation.

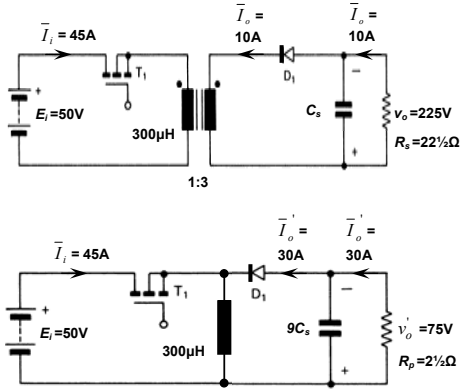

Figure 15.11. *Isolated output step up/down flyback converter and its equivalent circuit when the output is referred to the primary.*

Figure 15.11 shows secondary parameters referred to the primary, specifically

$$v_o = 225\text{V} \quad v_o' = v_o / n_T = 225\text{V}/3 = 75\text{V}$$
$$R_s = 225\Omega \quad R_p = R_s / n_T^2 = 225\Omega/3^2 = 22\tfrac{1}{2}\Omega$$

Note that the output capacitance is transferred by a factor of nine, n_T^2, since capacitive reactance is inversely proportion to capacitance.

It will be noticed that the equivalent circuit parameter values to be analysed, when referred to the primary, are the same as in example 15.4. The circuit is analysed as in

example 15.4 and the essential results from example 15.4 are summarised in Table 15.3 and transferred to the secondary where appropriate. The waveform answers to part iii are shown in figure 15.12.

Table 15.3 Transformer coupled flyback converter analysis

parameter		value for primary analysis	transfer factor $n_T = 3$ →	value for secondary analysis
E_i	**V**	50	3	150
v_o	**V**	75	3	225
R_L	**Ω**	2½	3^2	22½
C_o	**F**	$9C_o$	3^{-2}	C_o
$I_{o(ave)}$	**A**	30	⅓	10
P_o	**W**	2250	invariant	2250
$I_{i(ave)}$	**A**	45A	⅓	15A
δ		⅗	invariant	⅗
τ	**µs**	100	invariant	100
t_{on}	**µs**	60	invariant	60
t_{off}	**µs**	40	invariant	40
f_s	**kHz**	20	invariant	20
Δi_L	**A**	5	⅓	1⅔
$\hat{I}_L$	**A**	80	⅓	80/3
$\check{I}_L$	**A**	70	⅓	70/3
i_{Crms}	**A rms**	21.3	⅓	7.1
R_{crit}	**Ω**	45	3^2	405
L_{crit}	**µH**	20	3^2	180
V_{Dr}	**V**	125	3	375

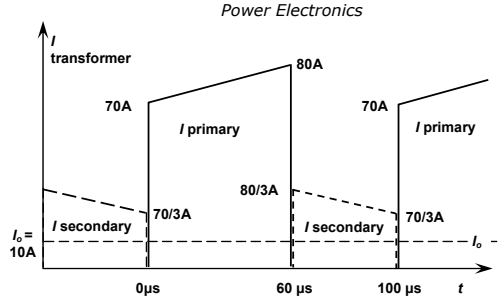

Figure 15.12. *Currents for the transformer windings in example 15.6.*

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Example 15.7: ***Transformer coupled forward converter***

The 10kHz forward converter in figure 15.10a operates from a 192V dc input and a 1:3:2 (1:$n_{f/b}$:n_{sec}) step-up transformer loaded with a 4Ω resistor. The transformer magnetising inductance is 1.2mH, referred to the primary. The secondary smps inductance is 800µH.

i. Calculate the maximum switch duty cycle, hence transistor off-time, assuming continuous inductor current.

At the maximum duty cycle:

ii. Calculate the mean input and output current.

iii. Draw the transformer currents, showing the minimum and maximum values.

iv. Determine
- the critical load resistance
- the minimum inductance for continuous inductor conduction for a 4 Ω load

Solution

The maximum duty cycle is determined solely by the transformer turns ratio between the primary and the feedback winding which resets the core flux. From equation (15.132)

$$\hat{\delta} = \frac{1}{1+n_{f/b}}$$

$$= \frac{1}{1+3} = ¼$$

The maximum conduction time is 25% of the 100µs period, namely 25µs. The secondary output voltage is therefore

$$v_{sec} = \delta n_T E_i$$
$$= ¼ \times 2 \times 192 = 96\text{V}$$

The load current is therefore 96V/4Ω=24A, as shown in figure 15.13a.
Figure 15.13b shows secondary parameters referred to the primary, specifically

$$R_s = 4\Omega \quad R_p = R_s / n_T^2 = 4\Omega / 2^2 = 1\Omega$$
$$v_o = 96\text{V} \quad v_o' = v_o / n_T = 96\text{V}/2 = 48\text{V}$$
$$L_o = 800\mu\text{H} \quad L_o' = L_o / n_T^2 = 800\mu\text{H}/2^2 = 200\mu\text{H}$$

Note that the output capacitance is transferred by a factor of four, n_T^2, since capacitive reactance is inversely proportion to capacitance.
Inspection of example 15.1 will show that the equivalent circuit in figure 15.13b is the same as the circuit in example 15.1, except that a magnetising branch has been added. The various operating condition and values in example 15.1 are valid for example 15.7.

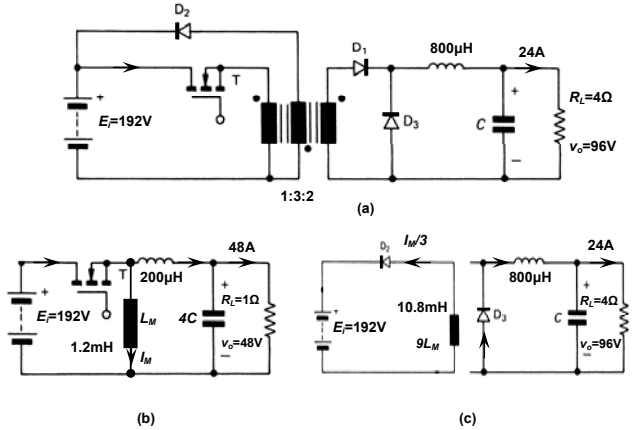

Figure 15.13. *Isolated output forward converter and its equivalent circuits when the output is referred to the primary.*

ii. The mean output current is the same for both circuits, 48A, or 24 A when referred to the secondary circuit. The mean input current from E_i remains 12A, but the switch mean current is not 12A. Magnetising current is provided from the supply E_i through the switch, but returned to the supply E_i through diode D2, which bypasses the switch. The net magnetising energy flow is zero. The magnetising current maximum value is given by equation (15.133)

$$\hat{I}_M = E_i t_{on} / L_M$$
$$= 192\text{V} \times 25\mu\text{s}/1.2\text{mH} = 4\text{A}$$

This current increases the switch mean current to

$$\bar{I}_T = 12\text{A} + ½ \times \delta \times 4\text{A} = 12½\text{A}$$

Figure 15.13c show the equivalent circuit when the switch is off. The output circuit functions independently of the input circuit, which is returning stored core energy to the supply E_i via the feedback winding and diode D2. Parameters have been referred to the feedback winding which has three times the turns of the primary, $n_{f/b}$=3. The 192V input voltage remains the circuit reference. Equation (15.133), Faraday's law, referred to the feedback winding, must be satisfied during the switch off period, that is

$$\frac{\hat{I}_M}{n_{f/b}} = \frac{E_i t_{off}}{n_{f/b}^2 L_M}$$
$$\frac{4}{3} = \frac{192\text{V} \times 75\mu\text{s}}{3^2 \times 1.2\text{mH}}$$

The diode D2 voltage rating is $(n_{f/b}+1) \times E_i$, 768V and its mean current is

$$\bar{I}_{D2} = ½(1-\delta)\frac{I_M}{n_{f/b}} = ½ \times (1 - 0.25) \times \frac{4\text{A}}{3} = ½\text{A}$$

iii. The three winding currents for the transformer are shown in figure 15.14.

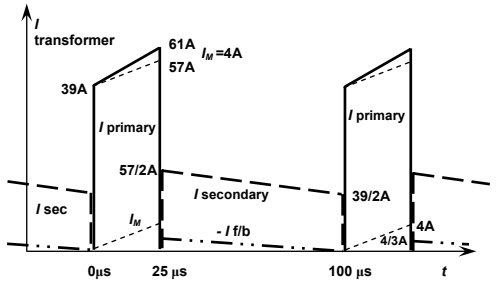

Figure 15.14. *Currents for the three transformer windings in example 15.7.*

iv. The critical resistance and inductance, referred to the primary, from example 15.1 are 5⅓Ω and 37½μH. Transforming into secondary quantities, by multiplying by 2^2 give critical values of R_L = 21⅓Ω and L = 150μH. ♣

15.8 Multiple-switch, balanced, isolated converters

The basic single-switch converters considered have the limitation of using their magnetic components only in a unipolar mode. Since only one quadrant of the *B-H* characteristic is employed, these converters are generally restricted to lower powers because of the limited flux swing, which is reduced by the core remanence flux.

The high-power forward converter circuits shown in figure 15.15 operate the magnetic transformer component in the bipolar or push-pull flux mode and require two or four switches. Because the transformers are fully utilised magnetically, they tend to be almost half the size of the equivalent single transistor isolated converter at power levels above 100 W.

15.8.1 The push-pull converter

Figure 15.15a illustrates a push-pull forward converter circuit which employs two switches and a centre-tapped transformer. Each switch must have the same duty cycle in order to prevent unidirectional core saturation. Because of transformer coupling action, the off switch supports twice the input voltage, $2E_i$, plus any voltage associated with leakage inductance stored energy. Advantageously, no floating gate drives are required.

The voltage transfer function, for continuous inductor conduction, is based on the equivalent secondary output circuit show in figure 15.16. Because of transformer action the input voltage is $N \times E_i$ where N is the transformer turns ratio. When a primary switch is on, current flows in the loop shown in figure 15.16. That is

$$\Delta i_L = \hat{i}_L - \check{i}_L = \frac{N \times E_i - v_o}{L} \times t_T \qquad (15.134)$$

When the primary switches are off, the secondary voltage falls to zero and current continues to flow through the secondary winding due to the energy stored in L. Efficiency is increased if the diode D_f is used to bypass the transformer winding, as shown in figure 15.16. The secondary winding i^2R losses are decreased and minimal voltage is coupled from the secondary back into the primary circuit. The current in the off loop shown in figure 15.16 is given by

$$\Delta i_L = \frac{v_o}{L} \times (\tau - t_T) \qquad (15.135)$$

Equating equations (15.134) and (15.135) gives the following voltage and current transfer functions

$$\frac{v_o}{E_i} = \frac{\bar{I}_i}{\bar{I}_o} = 2N\frac{t_T}{\tau} = 2N\delta \qquad 0 \le \delta \le \tfrac{1}{2} \qquad (15.136)$$

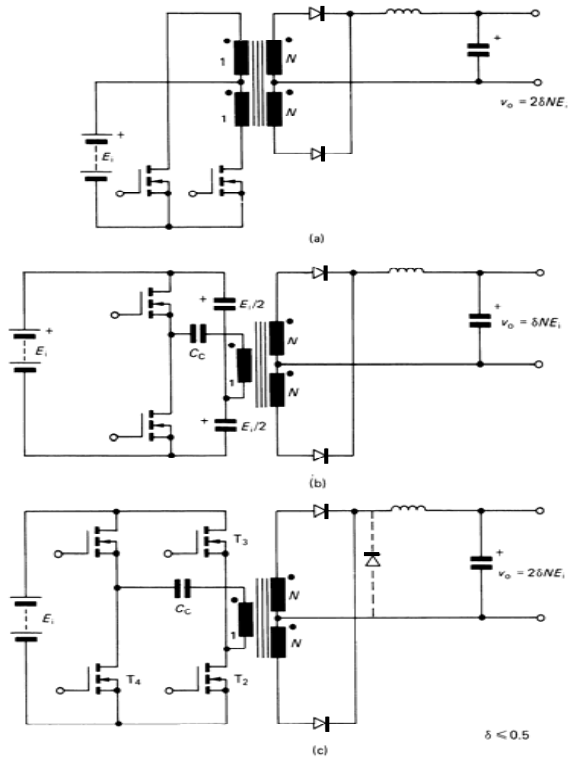

Figure 15.15. *Multiple-switch, isolated output, pulse-width modulated converters: (a) push-pull; (b) half-bridge; and (c) full-bridge.*

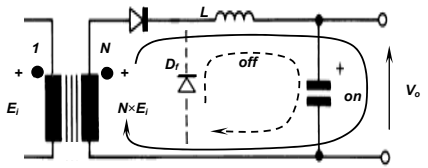

Figure 15.16. *Equivalent circuit for transformer bridge converters based on a forward converter in the secondary.*

15.8.2 Bridge converters

Figures 15.15b and c show half and full-bridge isolated forward converters respectively. In the half-bridge the transistors are switched alternately and must have the same conduction period. This ensures the core volts-second balance requirement to prevent saturation due to bias in one direction.

Using similar analysis as for the push-pull converter in 15.8.1, the voltage transfer function of the half bridge with a forward converter output stage, for continuous inductor conduction, is given by

$$\frac{v_o}{E_i} = \frac{\bar{I}_i}{\bar{I}_o} = N\frac{t_T}{\tau} = N\delta \qquad 0 \le \delta \le ½ \qquad (15.137)$$

A floating base drive is required. Although the maximum winding voltage is $½E_i$, the switches must support E_i in the off-state, when the complementary switch conducts.

The full bridge in figure 15.15c replaces the capacitor supplies of the half-bridge converter with switching devices. In the off-state each switch must support the rail voltage E_i and two floating gate drive circuits are required. This bridge converter is usually reserved for high-power applications.

Using similar analysis as for the push-pull converter in 15.8.1, the voltage transfer function of the full bridge with a forward converter output stage, with continuous conduction is given by

$$\frac{v_o}{E_i} = \frac{\bar{I}_i}{\bar{I}_o} = 2N\frac{t_T}{\tau} = 2N\delta \qquad 0 \le \delta \le ½ \qquad (15.138)$$

Any volts-second imbalance can be minimised by using dc block capacitance C_c, as shown in figures 15.15b and c.

In each forward converter in figure 15.15, a single secondary transformer winding and full-wave rectifier can be used. If the output diode shown dashed in figure 15.15c is used, the off state loop voltage is decreased from two diode voltage drops to one.

If the output inductor is not used, conventional unregulated transformer voltage ratio action occurs for each transformer based smps, where, independent of δ,

$$\frac{v_o}{E_i} = \frac{\bar{I}_i}{\bar{I}_o} = \frac{n_s}{n_o} = N \qquad (15.139)$$

15.9 Resonant dc-to-dc converters

Converter switching losses may be significantly reduced if zero current or voltage switching can be utilised. This switching loss reduction allows higher operating frequencies hence smaller L and C components (in size and value). Also radiated switching noise is significantly reduced.

Two main techniques can be used to achieve near zero switching losses

- a resonant load that provides natural voltage or current zero instances for switching
- a resonant circuit across the switch which feeds energy to the load as well as introducing zero current or voltage instances for switching.

15.9.1 Series loaded resonant dc-to-dc converters

Figure 15.17a shows the circuit diagram of a series resonant converter, which uses an output rectifier bridge to converter the resonant ac oscillation into dc. The converter is based on the series converter in figure 14.27b. The rectified ac charges the dc output capacitor, across which is the dc load, R_{load}. The non-dc-decoupled resistance, which determines the circuit Q, is account for by resistor R_c. The dc capacitor C is assumed large enough so that the output voltage $v_{o/p}$ is maintained constant, without significant ripple voltage. Figures 15.17b and c show how the dc output circuit can be transformed into an ac square wave in series with the L-C circuit, and finally this source is transferred to the dc link as a constant dc voltage source $v_{o/p}$ which opposes the dc supply V_s. These transformation steps enable the series L-C-R resonant circuit to be analysed with square wave inverter excitation, from a dc source V_s - $v_{o/p}$. The analysis in chapter 14.3.2 is valid for this circuit, where V_s is replaced by V_s - $v_{o/p}$. The equations, modified, are repeated for completeness.

The series L-C-R circuit current for a step input voltage V_s-$v_{o/p}$, with initial capacitor voltage v_o, assuming zero initial inductor current, is given by

$$i(\omega t) = \frac{\left(V_s - v_{o/p}\right) - v_o}{\omega L} \times e^{-\alpha t} \times \sin \omega t \qquad (15.140)$$

where

$$\omega^2 = \omega_o^2\left(1-\xi^2\right) \qquad \omega_o = \frac{1}{\sqrt{LC}} \qquad \alpha = \frac{R}{2L} \qquad \frac{1}{2Q_s} = \xi = \frac{R}{2\omega_o L} \qquad Z_o = \sqrt{\frac{L}{C}}$$

ξ is the damping factor. The capacitor voltage is important because it specifies the energy retained in the L-C-R circuit at the end of each half cycle.

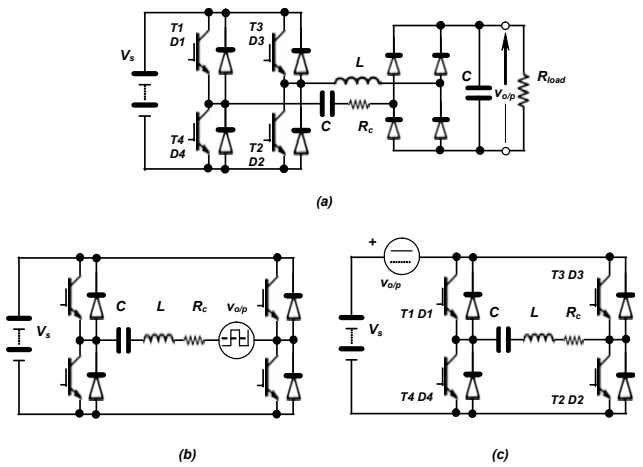

Figure 15.17. *Series resonant converter and its equivalent circuit derivation.*

$$v_c(\omega t) = \left(V_s - v_{o/p}\right) - \left(\left(V_s - v_{o/p}\right) - v_o\right)\frac{\omega_o}{\omega}e^{-\alpha t}\cos\left(\omega t - \phi\right) \tag{15.141}$$

where

$$\tan\phi = \frac{\alpha}{\omega} \quad \text{and} \quad \omega_o^2 = \omega^2 + \alpha^2$$

At the series circuit resonance frequency ω_o, the lowest possible circuit impedance results, $Z = R$. The series circuit quality factor or figure of merit, Q_s is defined by

$$Q_s = \frac{\omega_o L}{R} = \frac{1}{2\xi} = \frac{Z_o}{R} \tag{15.142}$$

Operation is characterised by turning on switches T1 and T2 to provide energy from the source during one half of the cycle, then having turned T1 and T2 off, T3 and T4 are turned on for the second resonant half cycle. Energy is again drawn from the supply, and when the current reaches zero T3 and T4 are turned off.

Without bridge freewheel diodes, the switches support high reverse bias voltages, but the switches control the start of each oscillation half cycle. With freewheel diodes the oscillations can continue independent of the switch states. The diodes return energy to the supply, hence reducing the energy transferred to the load. Correct timing of the switches minimises currents in the freewheel diodes, hence minimises the energy needlessly being returned to the supply. Energy to the load is maximised. The switches can be used to control the effective load power factor. By advancing turn-off to occur before the switch current reaches zero, the load can be made to appear inductive, while delaying switch turn-on produces a capacitive load effect.

The series circuit steady-state current at resonance for the H-bridge with a high circuit Q can be approximated by assuming $\omega_o \approx \omega$, such that:

$$i(\omega t) = \frac{2}{1 - e^{\frac{-\alpha\pi}{\omega}}} \times \frac{\left(V_s - v_{o/p}\right)}{\omega L} \times e^{-\alpha t} \times \sin\omega t \tag{15.143}$$

which is valid for the ± $(V_s$ - $v_{o/p})$ voltage loops of cycle operation at resonance. For a high circuit Q this equation is approximately

$$i(\omega t) \approx \frac{4}{\pi} \times Q \times \frac{\left(V_s - v_{o/p}\right)}{\omega_o L} \times \sin\omega_o t = \frac{4}{\pi} \times \frac{\left(V_s - v_{o/p}\right)}{R} \times \sin\omega_o t \tag{15.144}$$

In steady-state the capacitor voltage maxima are

$$\begin{aligned} \hat{V}_c &= \left(V_s - v_{o/p}\right)\frac{1 + e^{-\alpha\pi/\omega}}{1 - e^{-\alpha\pi/\omega}} = \left(V_s - v_{o/p}\right) \times \coth\left(\alpha\pi/2\omega\right) = -\check{V}_c \\ &\approx \left(V_s - v_{o/p}\right) \times 2\omega_o/\alpha\pi = \frac{4}{\pi} \times Q \times \left(V_s - v_{o/p}\right) \end{aligned} \tag{15.145}$$

The peak-to-peak capacitor voltage, by symmetry is therefore

$$V_{c_{p-p}} \approx \frac{8}{\pi} \times Q \times \left(V_s - v_{o/p}\right) \tag{15.146}$$

The energy transferred to the load R, per half sine cycle (per current pulse) is

$$\begin{aligned} W &= \int_0^{\pi/\omega} i^2 R\, dt \approx \int_0^{\pi/\omega_o} \left(4\frac{2}{\pi} \times \frac{\left(V_s - v_{o/p}\right)}{R} \times \sin\omega_o t\right)^2 R\, dt \\ &= \frac{8}{\pi\omega_o R}\left(V_s - v_{o/p}\right)^2 \end{aligned} \tag{15.147}$$

15.9.1i - Circuit variations

Voltage and impedance matching, for example voltage step-up, can be obtained by using a transformer coupled circuit as shown in figure 15.18a. A parallel resonant circuit approach, with or without transformer coupling, can also be used as shown in figure 15.18b without transformer coupling. When a transformer is used, a centre tapped secondary can reduce the number of high frequency rectifying diodes from four to two, but diode reverse voltage rating is doubled. Secondary Cu utilisation is halved.

Rather than four switching devices and four diodes, as shown in figure 15.17, a half bridge and centre tapped capacitor dc link can be used as shown in figure15.15b. Although the number of semiconductors is halved, the already poor switch utilisation associated with any resonant converter, is further decreased. The bridge output voltage across the *L*-*C* load is $\frac{1}{2}V_s$, while the switches and diodes support V_s. In the full-bridge case the corresponding switch and load voltages are also both V_s.

15.9.1ii - Modes of operation - series resonant circuit

The basic series converter can be operated in any of three difference modes, depending on the switching frequency in relation to the *L*-*C* circuit natural resonant frequency. The switching frequency involves one complete symmetrical square-wave output cycle from the inverter bridge.

i. $f_s < \frac{1}{2}f_o$:- discontinuous inductor current

If the switching frequency is less than half the *L*-*C* circuit natural resonant frequency then discontinuous inductor current results since one complete *L*-*C* resonant ac cycle occurs and current stops, being unable to reverse. Turn-off occurs at zero current. Subsequent turn-on occurs at zero current but the voltage is determined by the voltage retained by the capacitor. Thyristors are therefore applicable switches in this mode of operation. The freewheel diodes turn on and off with zero current.

ii. $f_s < f_o$:- continuous inductor current

If the switching frequency is just less than natural resonant frequency, such that turn-on occurs after half an oscillation cycle but before a complete ac oscillation cycle is complete, continuous inductor current results. Switch turn-on occurs with finite inductor current and voltage conditions, with the diodes freewheeling. Diode reverse recovery losses occur and noise in injected into the circuit at voltage recovery snap. Switch turn-off occurs at zero voltage and current, when the inductor current passes through zero and the freewheel diodes take up conduction. Thyristors are applicable as switching devices with this mode of control.

iii. $f_s > f_o$:- continuous inductor current

If turn-off occurs before the resonance of half a resonant cycle is complete, continuous inductor current flows, hard switching results, and commutable switches must be used. Turn-on occurs at zero voltage and current hence no diode recovery snap occurs. This zero electrical condition at turn-on allows lossless capacitive turn-off snubbers to be employed (a capacitor in parallel with each switch).

15.9.1iii - Modes of operation - parallel resonant circuit

Three modes of operation are applicable to the parallel-resonant circuit, dc-to-dc converter. The discontinuous inductor current mode when $f_s < \frac{1}{2}f_o$ is not preferred.

i. $f_s < f_o$:- continuous inductor current

When switching below resonance, the switches commutate naturally at turn-off, making thyristors a possibility.

Hard turn-on results, necessitating the use of fast recovery diodes.

ii. $f_s > f_o$:- continuous inductor current

When switching at frequencies above the natural resonance frequency, no turn-on losses occur since turn-on occurs when a switches antiparallel diode is conducting. Hard turn-off occurs, with current commutated to a freewheel diode. In mitigation, lossless capacitive turn-off snubber can be used (a capacitor in parallel with each switch).

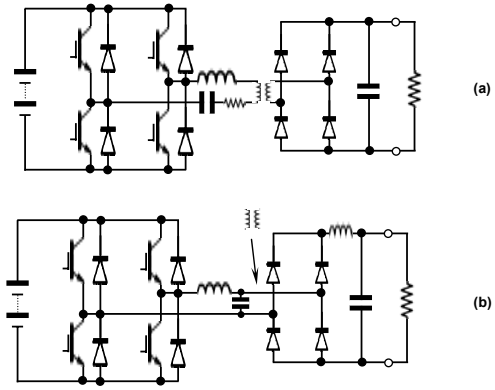

Figure 15.18. *Transformer coupled converters: (a) series resonant converter and (b) an equivalent parallel circuit.*

Example 15.8: ***Transformer- coupled, series-resonant, dc-to-dc converter***

The series resonant dc step down voltage converter in figure 15.17a is used with a step up transformer, 1:2 ($n_T = \frac{1}{2}$), as shown in figure 15.18a. It produces an output voltage for the armature of a high voltage dc motor that has a voltage requirement that is greater than the 50Hz ac mains rectified, 340V dc, with an *L*-*C* dc link filter. The resonant circuit parameters are L=100μH, C=0.47μF, and the coil resistance is R_c = 1Ω. For a 10Ω armature resistance, R_{load}, calculate

i. the circuit Q and ω_o
ii. the output voltage, hence dc armature current and power delivered
iii. the secondary circuit dc filter capacitor voltage and rms current rating
iv. the resonant circuit rms ac current and capacitor rms ac voltage
v. the converter average input current and efficiency
vi. the ac current in the input *L*-*C* dc rectifier filter decoupling capacitor

Solution

i. The resonant circuit Q is

$$Q = \sqrt{\frac{L}{C}} / R_c = \sqrt{\frac{100\mu\text{H}}{0.47\mu\text{F}}} / 1\Omega = 14.6$$

For this high Q, the circuit resonant frequency and damped frequency will be almost the same, that is

$$\begin{aligned}\omega \approx \omega_o &= 1/\sqrt{LC} \\ &= 1/\sqrt{100\mu\text{H} \times 0.47\mu\text{F}} = 146 \text{ krad/s} \\ &= 2\pi f \\ f &= 146 \text{ krad/s} / 2\pi = 23.25 \text{ kHz}\end{aligned}$$

ii. From equation (15.144), which will be accurate because of a high circuit Q of 14.6,

$$\begin{aligned}\bar{I} = \frac{2}{\pi}\hat{I} &= \frac{8}{\pi^2}\frac{\left(V_s - n_T \times v_{o/p}\right)}{R_c} = \frac{8}{\pi^2} \times \frac{\left(340\text{ V} - ½v_{o/p}\right)}{1\Omega} \\ &= 0.81 \times \left(340\text{ V} - ½v_{o/p}\right)\end{aligned}$$

Note that the output voltage $v_{o/p}$ across the dc decoupling capacitor has been referred to the primary by n_T, hence halved, due to the turns ratio of 1:2.
The rectified resonant current provides the load current, that is

$$\begin{aligned}\bar{I} &= \frac{1}{n_T} \times \frac{v_{o/p}}{R_{load}} = 2 \times \frac{v_{o/p}}{10\Omega} \\ &= \frac{v_{o/p}}{5}\end{aligned}$$

Again the secondary current has been referred to the primary. Solving the two average primary current equations gives

$$\bar{I} = 0.81 \times \left(340 - ½v_o\right) = \frac{v_{o/p}}{5}$$

$$v_{o/p} = 456\text{V and } \bar{I} = 91.2\text{A}$$

That is, the load voltage is 456V dc and the load current is 456V/10Ω = 91.2A/2 = 45.6A dc. The power delivered to the load is $456^2/10\Omega = 20.8$kW.
iii. From part ii, the capacitor dc voltage requirement is at least 456V dc. The secondary rms current is

$$\begin{aligned}I_{Srms} = n_T \times I_{Prms} &= n_T \times \frac{1}{\sqrt{2}} \times \hat{I}_p = ½ \times \frac{1}{\sqrt{2}} \times \frac{\pi}{2} \times \bar{I}_p \\ &= 0.555 \times \bar{I}_p = 0.555 \times 91.2\text{A} \\ &= 50.65\text{A rms}\end{aligned}$$

The primary rms current is double the secondary rms current, 101.3A rms.
By Kirchhoff's current law, the secondary current (50.65A rms) splits between the load (45.6A dc) and the decoupling capacitor. That is the rms current in the capacitor is

$$\begin{aligned}I_{Crms} &= \sqrt{I_{Srms}^2 - \bar{I}_S^2} \\ &= \sqrt{50.65^2 - 45.6^2} = 22\text{A rms}\end{aligned}$$

That is, the secondary dc filter capacitor has a dc voltage requirement of 456V dc and a current requirement of 22A rms at 46.5kHz, which is double the resonant frequency because of the rectification process.

iv. The primary rms current is double the secondary rms current, namely from part iii, I_{Prms}=101.3A rms. The 0.47μF resonant capacitor voltage is given by

$$\begin{aligned}v_{cap} = I_{Prms} X_c &= \frac{I_{Prms}}{\omega_o C} \\ &= \frac{101.3\text{A}}{146\text{krad/s} \times 0.47\mu\text{F}} = 1476\text{V rms}\end{aligned}$$

The resonant circuit capacitor has an rms current rating requirement of 101.3A rms and an rms voltage rating of 1476 V rms.

v. From part ii, the average input current is 91.2 A. The supply input power is therefore 340Vdc×91.2A ave = 31kW. The power dissipated in the resonant circuit resistance R_c =1Ω is given by $I_{Prms}^2 \times R_c = 101.3^2 \times 1\Omega = 10.26$kW.. Note that the coil power plus the load power (from part ii) equals the input power (20.8kW+10.26kW = 31kW). The efficiency is

$$\begin{aligned}\eta &= \frac{\text{output power}}{\text{input power}} \times 100\% \\ &= \frac{20.8\text{kW}}{31\text{kW}} \times 100 = 67.1\%\end{aligned}$$

vi. The average input dc current is 91.2A dc while the resonant bridge rms current is 101.3A rms. By Kirchhoff's current law, the 340V dc rail decoupling capacitor ac current is given by

$$\begin{aligned}I_{ac} &= \sqrt{I_{Prms}^2 - I_{Pave}^2} \\ &= \sqrt{101.3^2 - 91.2^2} = 44.1\text{A ac}\end{aligned}$$

This is the same ac current magnitude as the current in the dc capacitor across the load in the secondary circuit, 22A, when the transformer turns ratio, 2, is taken into account.

♣

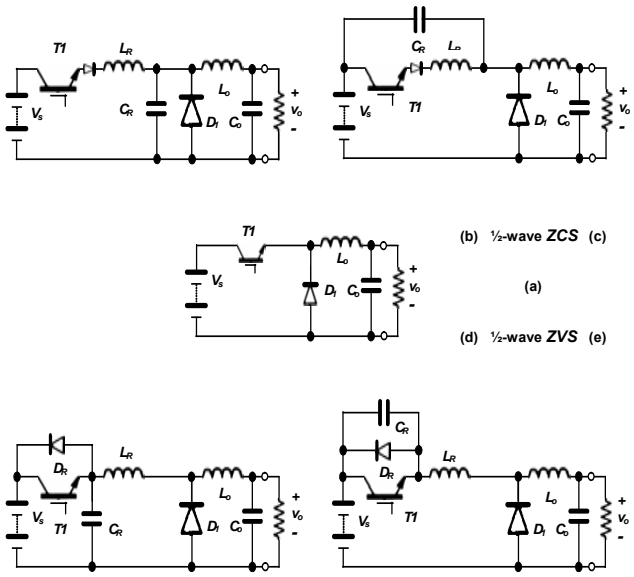

Figure 15.19. *Dc to dc converters:*
(a) conventional switch mode forward step-down converter;
(b) and (c) half-wave zero current switching ***ZCS*** *resonant switch converters; and*
(d) and (e) half-wave zero voltage switching ***ZVS*** *resonant switch converters.*

15.9.2 Resonant-switch, dc-to-dc converters

There are two forms of resonant switch circuit configurations for dc-to-dc converters, namely resonant voltage and resonant current switch commutation. Each type reduces the switching losses to near zero.

- In *resonant current commutation* the switching current is reduced to zero by an *L-C* resonant circuit current greater in magnitude than the load current, such that the switch is turned on and off with zero current.

- In *resonant voltage commutation* the switch voltage is reduced to zero by the capacitor of an *L-C* resonant circuit with a voltage magnitude greater than the output voltage, such that the switch can turn on and off with zero voltage.

Figure 15.19a shows the basic single switch, forward, step-down voltage switch mode dc-to-dc converter. Resonant switch converters are an extension of the standard switch mode forward converter, but the switch is supplement with passive components L_R-C_R to provide resonant operation through the switch, hence facilitating zero current or voltage switching. A common feature is that the resonant inductor L_R is in series with the switch to be commutated. Parasitic series inductance is therefore not an issue with resonant switch converters.

The resonant capacitor C_R, can be either in a parallel or series arrangement as shown in figure 15.19, since small-signal ac-wise the connections are the same. A well-decoupled supply is essential when the capacitor C_R is used in the parallel switch arrangement, as shown in figure 15.19 part b and d. A further restriction is that a diode must be used in series or in antiparallel with T1 if a switch without reverse blocking capability is used. The use of an antiparallel connected diode changes the switching arrangement from half-wave resonant operation with reverse impressed voltage switch commutation to full-wave resonant operation with current displacement commutation, independent of the switch reverse blocking capabilities. Reconnecting the capacitor C_R terminal not associated with V_s, to the other end of inductor L_R in figure 15.19b-e, will create four full-wave resonant switch circuits (the commutation type, namely voltage or current, is also interchanged). An important operational requirement is that the average load current never falls to zero, otherwise the resonant capacitor C_R can never fully discharge when performing its zero switch current turn-off function.

15.9.2i Zero-current, resonant-switch, dc-to-dc converter

The zero current switching of T1 in figure 15.20 (15.19b) can be analysed in five distinctive stages, as shown in the capacitor voltage and inductor current waveforms. The switch is turned on at t_o and turned off after t_4 but before t_5.

The circuit has attained steady state load conditions from one cycle to the next. The cycle commences, before t_o, with both the capacitor voltage and inductor current being zero, and the load current is freewheeling through D1. The current in the output inductor L_o, is large enough such that its current, I_o can be assumed constant. The switch T1 is off.

Time interval I

At t_o the switch is turned on and the series inductor L_R acts as a turn-on snubber for the switch. In the interval t_o to t_1, the supply voltage is impressed across L_R since the switch T1 is on and the diode D1 conducts the output current, thereby clamping the inductor to zero volts. Because of the fixed voltage V_s, the current in L_R increases linearly to I_o.

Time interval II

When the current in L_R reaches I_o at time t_1, the capacitor C_R and L_R are free to resonant. The diode D1 blocks as the voltage across C_R sinusoidally increases. The constant load current component in L_R does not influence its ac performance since a

constant inductor current does not produce any inductor voltage. Its voltage is specified by the resonant cycle, provided $I_o > V_s / Z_o$. The capacitor resonantly charges to twice the supply V_s when the inductor current falls back to the load current level I_o, at time t_3.

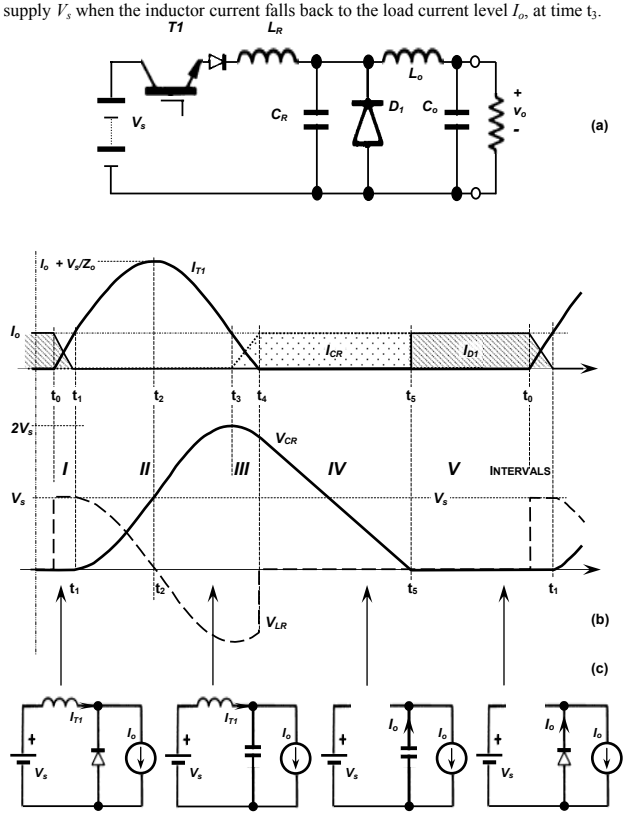

Figure 15.20. *Zero current switching, ZCS, resonant switch dc to dc converter: (a) circuit; (b) waveforms; and (c) equivalents circuits.*

Time interval III

Between times t_3 and t_4 the load current is displaced from L_R by charge in C_R, in a quasi resonance process. The resonant cycle cannot reverse through the switch once the inductor current reaches zero at time t_4, because of the series blocking diode (the switch must have uni-directional conduction characteristics).

Time interval IV

At time t_4 the input current is zero and the switch T1 can be turned off with zero current, ZCS. The constant load current requirement I_o is provided by the capacitor, which discharges linearly to zero volts and time t_5. The time for interval *IV* is therefore load current dependant.

Time interval V

After t_5, the switch is off, the current freewheels through D1, the capacitor voltage is zero and the input inductor current is zero. At time t_1 the cycle recommences. The interval *V*, t_5 to t_0, is used to control the rate at which energy is transferred to the load.

The circuit has a number of features:

i. Turn-on and turn-off occur at zero current, hence switching losses are minimal.
ii. At light load currents the switching frequency may become extreme low.
ii. The basic half resonant period is given by $t_{II} = \pi\sqrt{L_R C_R}$
iii. The capacitor discharge time is $t_{IV} \leq 2 \times V_s \times C_R / I_o$
iv. L_R and C_R are dimensioned such that the capacitor voltage is greater than V_s at time t_4, at maximum load current I_o.
v. Supply inductance is inconsequential, decreasing the inductance L_R requirement.

Operation of the ZCS circuit in figure 15.19c, where the capacitor C_R is connected in parallel with the switch, is essentially the same as the circuit in figure 15.20. The capacitor connection produces the result that the capacitor voltage has a dc offset of V_s, meaning its voltage swings between $\pm V_s$ rather than zero and twice V_s, as in the circuit just considered. Any dc supply inductance must be decoupled when using the ZVS circuit in figure 15.19c.

15.9.2ii Zero-voltage, resonant-switch, dc-to-dc converter

The zero voltage switching of T1 in figure 15.21 (15.19e) can be analysed in five distinctive stages, as shown in the capacitor voltage and inductor current waveforms. The switch is turned off at t_o and turned on after t_4 but before t_5.

The circuit has attained steady state load conditions from one cycle to the next. The cycle commences, before t_o, with the capacitor C_R voltage being V_s and the load current I_o being conducted by the switch and the resonant inductor, L_R. The output inductor L_o is large enough such that its current, I_o can be assumed constant. The switch T1 is on.

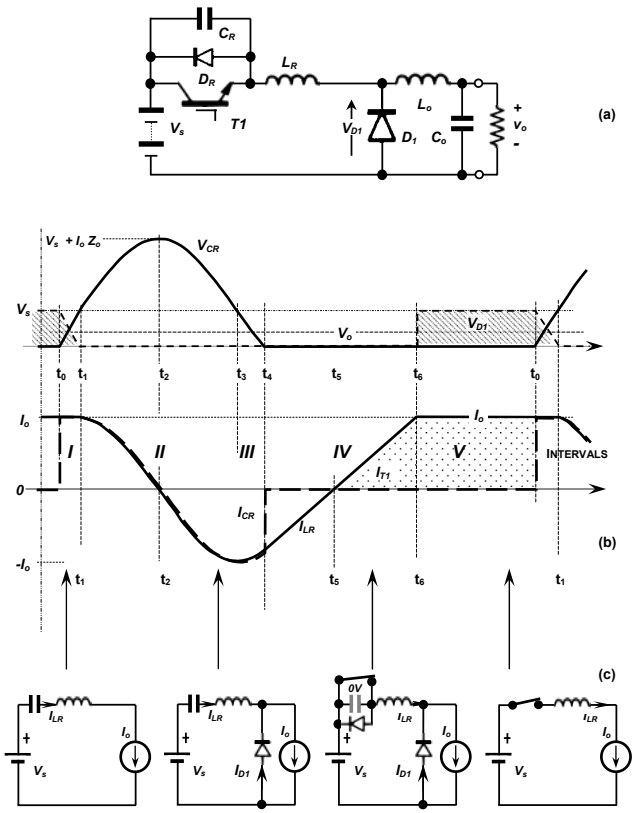

Figure 15.21. *Zero voltage switching, ZVS, resonant switch dc to dc converter: (a) circuit; (b) waveforms; and (c) equivalents circuits.*

Time interval I

At tome t_o the switch is turned off and the parallel capacitor C_R acts as a turn-off snubber for the switch. In the interval t_o to t_1, the supply current is provided from V_s through C_R and L_R. Because the load current is constant, I_o, due to large L_o, the capacitor charges linearly from 0V until its voltage reaches V_s.

Time interval II

When the voltage across C_R reaches V_s at time t_1, the load freewheel diode conducts, clamping the load voltage to zero volts. The capacitor C_R and L_R are free to resonant, where the initial inductor current is I_o and the initial capacitor voltage is V_s. The energy in the inductor transfers to the capacitor, which increases its voltage from V_s to $V_s + I_o Z_o$ at time t_2. The capacitor energy transfers back to the inductor which has resonated from $+ I_o$ to $- I_o$ between times t_1 to time t_3. For the capacitor voltage to resonantly return to V_s, $I_o > V_s / Z_o$. Between t_3 and t_4 the voltage V_s on C_R is resonated through L_R, which conducts $- I_o$ at t_3, as part of the resonance process.

Time interval III

At time t_4 the voltage on C_R attempts to reverse, but is clamped to zero by diode D_R. The inductor energy is returned to the supply V_s via diode D_R and the freewheel diode D_1. The inductor current decreases linearly to zero during the period t_4 to t_5. During this period the switch T1 is turned on. No turn-on losses occur because the diode D_R in parallel with T1 is conducting during the period the switch is turned on, that is, the switch voltage is zero and the switch T1 can be turned on with zero voltage, ZVS. With the switch on at time t_5 the current in the inductor L_R reverses and builds up, linearly to I_o at time t_6. The current slope is supply V_s dependant, according to $V_s = L_R \, di/dt$ and the time of period *III* is load current dependant, $t_{III} = I_o L_R / V_s$.

Time interval V

At t_6, the supply V_s provides all the load current and the diode D1 recovers with a controlled di/dt given by V_s / L_R. The switch conduction interval *IV*, t_6 to t_o, is used to control the rate at which energy is transferred to the load.

The circuit has a number of features:

i. Switch turn-on and turn-off both occur at zero voltage, hence switching losses are minimal.

ii. At light load currents the switching frequency may become extreme high.

iii. The basic half-resonant period is approximately given by $t_{1-4} = \pi\sqrt{L_R C_R}$

iv. The inductor discharge time is $t_{III} \leq 2 \times I_o \times L_R / V_s$

v. L_R and C_R are dimensioned such that the inductor current is less than zero (being returned to the supply V_s) at time t_5, at maximum load current I_o.

Operation of the ZVS circuit in figure 15.19d, where the capacitor C_R is connected in parallel with the load circuit (the freewheel diode D1), is essentially the same as the circuit in figure 15.21. The capacitor connection produces the result that the capacitor voltage has a dc offset of V_s, meaning its voltage swings between $+ V_s$ and $-I_o Z_o$, rather than zero and $V_s - I_o Z_o$, as in the circuit just considered. Any dc supply inductance must be decoupled when using the ZVS circuit in figure 15.19d.

It will be noticed that a ZCS converter has a constant on-time, while a ZVS converter has a constant off-time.

Example 15.9: ***Zero-current, resonant-switch, dc-to-dc converter***

The ZCS resonant dc step-down voltage converter in figure 15.20a produces an output voltage for the armature of a high voltage dc motor and operates from the voltage produced from the 50Hz ac mains rectified, 340V dc, with an *L-C* dc link filter. The resonant circuit parameters are L = 100μH, C = 0.47μF, and the high frequency ac resistance of the circuit is $R_c = 1\Omega$.
Calculate

i. the circuit Z_o, Q, and ω_o
ii. the minimum output current to ensure ZCS
iii. the maximum operating frequency, represented by the time between switch turn on and the freewheel diode recommencing conduction, at minimum load current
iv. the average diode voltage, hence load voltage at the maximum frequency.

Solution

i. The characteristic impedance is given by

$$Z_o = \sqrt{\frac{L}{C}} = \sqrt{\frac{100\mu\text{H}}{0.47\mu\text{F}}} = 14.6\Omega$$

The resonant circuit Q is

$$Q = Z_o / R_c = \sqrt{\frac{100\mu\text{H}}{0.47\mu\text{F}}} / 1\Omega = 14.6$$

For this high Q, the circuit resonant frequency and damped frequency will be almost the same, that is

$$\omega \approx \omega_o = 1/\sqrt{LC}$$
$$= 1/\sqrt{100\mu\text{H} \times 0.47\mu\text{F}} = 146 \text{ krad/s}$$
$$= 2\pi f$$
$$f = 146 \text{ krad/s} / 2\pi = 23.25 \text{ kHz}$$
$$\text{or} \quad T = 43\mu\text{s}$$

ii. For zero current switching, the load current must be greater than the resonant current, that is

$$I_o > V_s / Z_o = 340\text{V}/14.6\Omega = 23.3\text{A}$$

iii. The commutation period comprises the four intervals, *I* to *IV*, shown in figure 15.20b.

Interval I
The switch turns on and the inductor current rises from 0A to 23.3A in a time given by

$$t_I = L_R \Delta I / V_s$$
$$= 100\mu\text{H} \times 23.3\text{A}/340\text{V} = 6.85\mu\text{s}$$

Intervals *II* and *III*
These two interval take just over half a resonant cycle, which takes 43μs/2 = 21.5μs to complete. Assuming action is purely sinusoidal resonance with a 23.3A offset, from 0A to a maximum of 23.3A and down to -23.3A then from

$$I_o = V_s / Z_o \sin \omega t \quad \text{for} \quad \omega t > \pi$$
$$23.3A = -23.3A \sin \omega t \text{ gives}$$
$$t = \tfrac{3}{4} \times 43\mu\text{s}$$
$$= 32.25\mu\text{s}$$

The capacitor voltage at the end of this period is given by

$$V_{cIV} = V_s(1 - \cos \omega t)$$
$$= 340\text{V} \times (1 - \cos \tfrac{3}{2}\pi)$$
$$= 340\text{V}$$

Interval *IV*
The capacitor voltage must discharge from 340V dc to zero volts, providing the 23.3A load current. That is

$$t_{IV} = V_{cIV} \times C_R / I_o$$
$$= 340\text{V} \times 0.47\mu\text{F}/23.3\text{A} = 6.86\mu\text{s}$$

The minimum commutation cycle time is therefore 6.85+32.25+6.86 = 46μs. Thus the maximum operating frequency is 21.7kHz.

iv. The output voltage v_o is the average reverse voltage of freewheel diode D_1, which is in parallel with the resonant capacitor C_R. Integration of the capacitor voltage shown in figure 15.20b gives

$$v_o = \frac{1}{t_5}\left[\int_{t_1}^{t_4} V_s(1 - \cos \omega t)\, dt + \int_{t_4}^{t_5} V_s \frac{t}{t_5 - t_4} dt\right]$$
$$== \frac{1}{46\mu\text{s}} \times \left[\int_o^{32.25\mu\text{s}} 340\text{V} \times (1 - \cos \omega t)\, d\omega t + \int_0^{6.86\mu\text{s}} 340\text{V} \times \frac{t}{6.86\mu\text{s}} dt\right]$$
$$= \frac{1}{46\mu\text{s}} \times \left[340\text{V} \times \left(\frac{3\pi}{2} + 1\right) \times \frac{43\mu\text{s}}{2\pi} \quad + \tfrac{1}{2} \times 340\text{V} \times 6.86\mu\text{s}\right]$$
$$= \frac{1}{46\mu\text{s}} \times [13291.8\text{V}\mu\text{s} \quad + 1166.2\text{V}\mu\text{s}] = 314\text{Vdc}$$

The maximum output voltage is 314V dc.

♣

15.10 Appendix: Analysis of non-continuous inductor current operation

Operation with constant input voltage, E_i

In applications were the input voltage E_i is fixed, as with rectifier ac voltage input circuits, the output voltage v_o can be controlled by varying the duty cycle.

In the continuous inductor conduction region, the transfer function for the three basic converters is determined solely in terms of the on-state duty cycle, δ. Operation in the discontinuous current region, for a constant input voltage, can be characterised for each converter in terms of duty cycle and the normalised output or input current, as shown in figure 15.22. Key region and boundary equations, for a constant input voltage E_i, are summarised in tables 15.4 and 15.5.

Operation with constant output voltage, v_o

In applications were the output voltage v_o is fixed, as with regulated dc power supplies, the effects of varying input voltage E_i can be controlled and compensated by varying the duty cycle.

In the inductor continuous current conduction region, the transfer function is determined solely in terms of the on-state duty cycle, δ. Operation in the discontinuous region, for a constant output voltage, can be characterised in terms of duty cycle and the normalised output or input current, as shown in figure 15.23.

Key region and boundary equations, for a constant output voltage v_o, are summarised in table 15.6.

Because of the invariance of power, the output current $\bar{I}_o$ characteristics for each converter with a constant input voltage E_i , shown in figure 15.22, are the same as those for the input current $\bar{I}_i$ when the output voltage v_o is maintained constant, as shown in figure 15.23.

Table 15.4. Transfer functions with constant input voltage, E_i, with respect to $\bar{I}_o$

E_i constant	converter		
	step-down	step-up	step-up/down
reference equation	(15.3)	(15.39)	(15.65)
current conduction	$\frac{v_o}{E_i}=\delta$	$\frac{v_o}{E_i}=\frac{1}{1-\delta}$	$\frac{v_o}{E_i}=\frac{-\delta}{1-\delta}$
reference equation	(15.16)	(15.50)	(15.76)
discontinuous current	$\frac{v_o}{E_i}=\frac{1}{1+\frac{2L\bar{I}_o}{\delta^2\tau E_i}}$	$\frac{v_o}{E_i}=1+\frac{\delta^2 E_i t_T}{2L\bar{I}_o}$	$\frac{v_o}{E_i}=-\frac{\delta^2 E_i \tau}{2L\bar{I}_o}$
normalised $\hat{\bar{I}}_o=\frac{E_i\tau}{8L}$ @ δ = ½	$\frac{v_o}{E_i}=\frac{1}{1+\frac{1}{4\delta^2}\times\frac{\bar{I}_o}{\hat{\bar{I}}_o}}$	$\frac{v_o}{E_i}=1+4\delta^2/\frac{\bar{I}_o}{\hat{\bar{I}}_o}$	$\frac{v_o}{E_i}=-4\delta^2/\frac{\bar{I}_o}{\hat{\bar{I}}_o}$
change of variable	$\frac{\bar{I}_o}{\hat{\bar{I}}_o}=\frac{4\delta^2\left(1-\frac{v_o}{E_i}\right)}{\frac{v_o}{E_i}}$	$\frac{\bar{I}_o}{\hat{\bar{I}}_o}=\frac{4\delta^2}{\frac{v_o}{E_i}-1}$	$\frac{\bar{I}_o}{\hat{\bar{I}}_o}=\frac{-4\delta^2}{\frac{v_o}{E_i}}$
boundary	$\frac{\bar{I}_o}{\hat{\bar{I}}_o}=4\frac{v_o}{E_i}\left(1-\frac{v_o}{E_i}\right)$	$\frac{\bar{I}_o}{\hat{\bar{I}}_o}=\frac{4\left(\frac{v_o}{E_i}-1\right)}{\left(\frac{v_o}{E_i}\right)^2}$	$\frac{\bar{I}_o}{\hat{\bar{I}}_o}=\frac{-4\frac{v_o}{E_i}}{\left(1+\frac{v_o}{E_i}\right)^2}$
duty cycle all with boundary $\frac{\bar{I}_o}{\hat{\bar{I}}_o}=4\delta(1-\delta)$	$\delta=½\sqrt{\frac{\frac{\bar{I}_o}{\hat{\bar{I}}_o}\times\frac{v_o}{E_i}}{1-\frac{v_o}{E_i}}}$	$\delta=½\sqrt{\frac{\bar{I}_o}{\hat{\bar{I}}_o}\times\left(\frac{v_o}{E_i}-1\right)}$	$\delta=½\sqrt{\frac{\bar{I}_o}{\hat{\bar{I}}_o}\times\frac{v_o}{E_i}}$

Table 15.5. Transfer functions with constant input voltage, E_i, with respect to $\overline{I}_i$

v_o constant	converter		
	step-down	step-up	step-up/down
reference equation	(15.3)	(15.39)	(15.65)
current conduction	$\frac{v_o}{E_i}=\delta$	$\frac{v_o}{E_i}=\frac{1}{1-\delta}$	$\frac{v_o}{E_i}=\frac{-\delta}{1-\delta}$
reference equation	(15.15)	(15.51)	(15.76)
equation	$\frac{v_o}{E_i}=1-\frac{2L\overline{I}_i}{\delta^2\tau E_i}$	$\frac{v_o}{E_i}=\frac{1}{1-\frac{E_i t_r \delta^2}{2L\overline{I}_i}}$	$\frac{v_o}{E_i}=\frac{v_o\tau\delta^2}{2L\overline{I}_i}$
normalised	$\frac{v_o}{E_i}=1-\frac{4}{27\delta^2}\times\frac{\overline{I}_i}{\hat{\overline{I}}_i}$	$\frac{v_o}{E_i}=\frac{1}{1-\delta^2/\left(\frac{\overline{I}_i}{\hat{\overline{I}}_i}\right)}$	$1=\delta^2/\frac{\overline{I}_i}{\hat{\overline{I}}_i}$
$\hat{\overline{I}}_i$ max @ δ =	$\delta = ⅔$	$\delta = 1$	$\delta = 1$
$\hat{\overline{I}}_i$	$\hat{\overline{I}}_i=\frac{4}{27}\times\frac{E_i\tau}{2L}$	$\hat{\overline{I}}_i=\frac{E_i\tau}{2L}$	$\hat{\overline{I}}_i=\frac{E_i\tau}{2L}$
change of variable	$\frac{\overline{I}_i}{\hat{\overline{I}}_i}=27/4\,\delta^2\left(1-\frac{v_o}{E_i}\right)$	$\frac{\overline{I}_i}{\hat{\overline{I}}_i}=\frac{\delta^2\frac{v_o}{E_i}}{\left(\frac{v_o}{E_i}-1\right)}$	$\frac{\overline{I}_i}{\hat{\overline{I}}_i}=-\delta^2$
boundary	$\frac{\overline{I}_i}{\hat{\overline{I}}_i}=27/4\left(1-\frac{v_o}{E_i}\right)\left(\frac{v_o}{E_i}\right)^2$	$\frac{\overline{I}_i}{\hat{\overline{I}}_i}=\frac{\left(\frac{v_o}{E_i}-1\right)}{\frac{v_o}{E_i}}$	$\frac{\overline{I}_i}{\hat{\overline{I}}_i}=-\left(\frac{\frac{v_o}{E_i}}{\frac{v_o}{E_i}+1}\right)^2$
duty cycle	$\delta=\sqrt{\frac{\frac{\overline{I}_i}{\hat{\overline{I}}_i}}{4/27\left(1-\frac{v_o}{E_i}\right)}}$	$\delta=\sqrt{\frac{\frac{v_o}{E_i}-1}{\frac{\overline{I}_i}{\hat{\overline{I}}_i}\times\frac{v_o}{E_i}}}$	$\delta=\sqrt{\frac{\overline{I}_i}{\hat{\overline{I}}_i}}$
boundary	$\frac{\overline{I}_i}{\hat{\overline{I}}_i}=27/4\,\delta^2(1-\delta)$	$\frac{\overline{I}_i}{\hat{\overline{I}}_i}=\frac{\delta}{(1-\delta)^2}$	$\delta=\sqrt{\frac{\overline{I}_i}{\hat{\overline{I}}_i}}$

Table 15.6. Transfer functions with constant output voltage, v_o, with respect to $\overline{I}_o$

v_o constant	converter		
	step-down	step-up	step-up/down
reference equation	(15.3)	(15.39)	(15.65)
current conduction	$\frac{v_o}{E_i}=\delta$	$\frac{v_o}{E_i}=\frac{1}{1-\delta}$	$\frac{v_o}{E_i}=\frac{-\delta}{1-\delta}$
reference equation	(15.15)	(15.51)	(15.76)
equation	$\frac{v_o}{E_i}=1-\frac{2L\overline{I}_i}{\delta^2\tau E_i}$	$\frac{v_o}{E_i}=\frac{1}{1-\frac{E_i t_r \delta^2}{2L\overline{I}_i}}$	$\frac{v_o}{E_i}=\frac{v_o\tau\delta^2}{2L\overline{I}_i}$
normalised	$\frac{v_o}{E_i}=1-\frac{1}{4\delta^2}\times\frac{\overline{I}_o}{\hat{\overline{I}}_o}\times\left(\frac{v_o}{E_i}\right)^2$	$\frac{v_o}{E_i}=\frac{1}{1-4\delta^2/\left(\frac{\overline{I}_o}{\hat{\overline{I}}_o}\times\left(\frac{v_o}{E_i}\right)^2\right)}$	$\frac{v_o}{E_i}=\delta^2/\left(\frac{\overline{I}_o}{\hat{\overline{I}}_o}\times\frac{v_o}{E_i}\right)$
$\hat{\overline{I}}_o$ max @ δ =	$\delta = 0$	$\delta = ⅓$	$\delta = 0$
$\hat{\overline{I}}_o$	$\hat{\overline{I}}_o=\frac{v_o\tau}{2L}$	$\hat{\overline{I}}_o=\frac{4}{27}\times\frac{v_o\tau}{2L}$	$\hat{\overline{I}}_o=\frac{v_o\tau}{2L}$
change of variable	$\frac{\overline{I}_o}{\hat{\overline{I}}_o}=\frac{\delta^2\left(1-\frac{v_o}{E_i}\right)}{\left(\frac{v_o}{E_i}\right)^2}$	$\frac{\overline{I}_o}{\hat{\overline{I}}_o}=\frac{27/4\,\delta^2}{\left(\frac{v_o}{E_i}-1\right)\frac{v_o}{E_i}}$	$\frac{\overline{I}_o}{\hat{\overline{I}}_o}=\frac{-\delta^2}{\left(\frac{v_o}{E_i}\right)^2}$
boundary	$\frac{\overline{I}_o}{\hat{\overline{I}}_o}=1-\frac{v_o}{E_i}$	$\frac{\overline{I}_o}{\hat{\overline{I}}_o}=\frac{27/4\left(\frac{v_o}{E_i}-1\right)}{\left(\frac{v_o}{E_i}\right)^3}$	$\frac{\overline{I}_o}{\hat{\overline{I}}_o}=\frac{-1}{\left(1+\frac{v_o}{E_i}\right)^2}$
duty cycle	$\delta=\frac{v_o}{E_i}\sqrt{\frac{\frac{\overline{I}_o}{\hat{\overline{I}}_o}}{1-\frac{v_o}{E_i}}}$	$\delta=\sqrt{4/27\times\frac{\overline{I}_o}{\hat{\overline{I}}_o}\left(\frac{v_o}{E_i}-1\right)\frac{v_o}{E_i}}$	$\delta=\frac{v_o}{E_i}\sqrt{\frac{\overline{I}_o}{\hat{\overline{I}}_o}}$
boundary	$\delta=1-\frac{\overline{I}_o}{\hat{\overline{I}}_o}$	$\frac{\overline{I}_o}{\hat{\overline{I}}_o}=27/4\,\delta(1-\delta)^2$	$\delta=1-\sqrt{\frac{\overline{I}_o}{\hat{\overline{I}}_o}}$

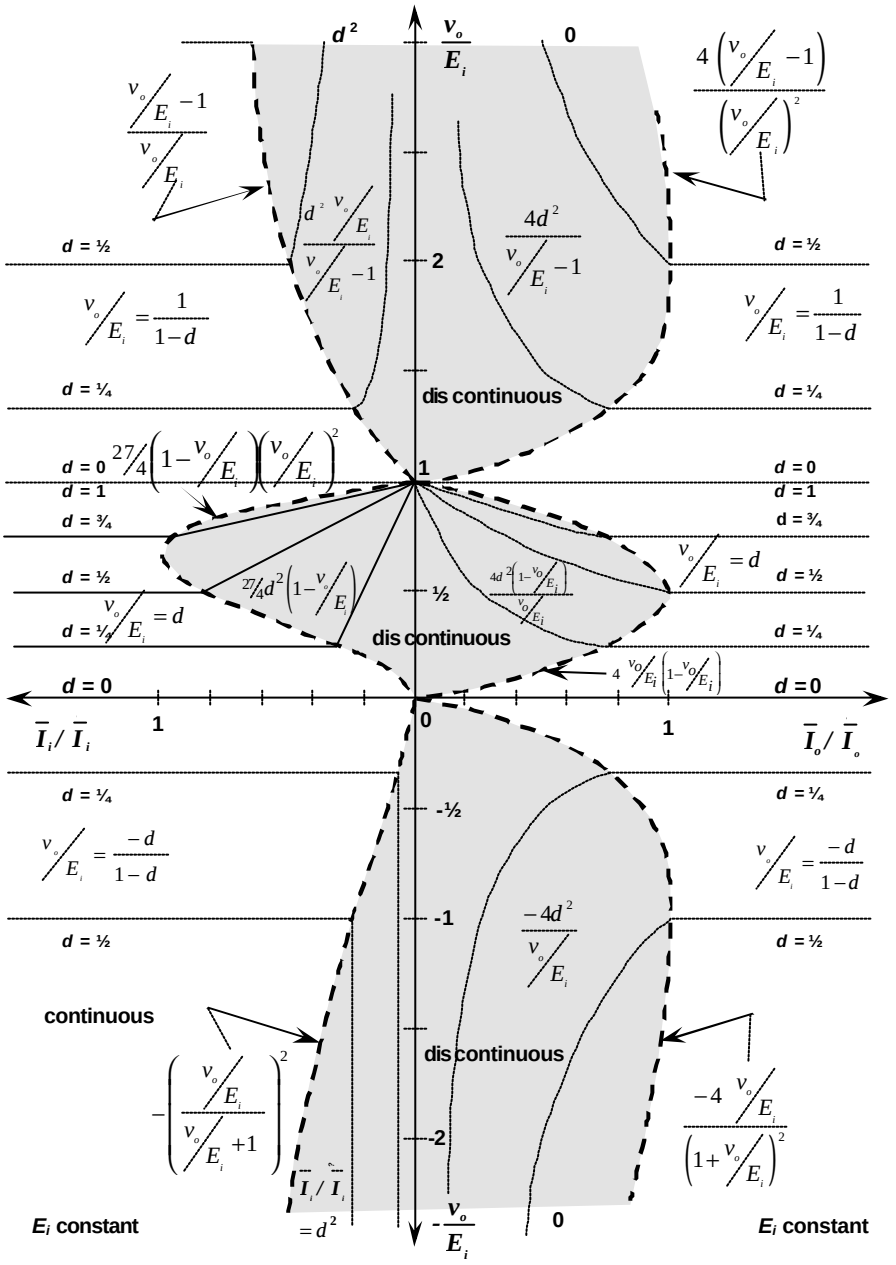

Figure 15.22. *Characteristics for three dc-dc converters, when the input voltage E_i is held constant.*

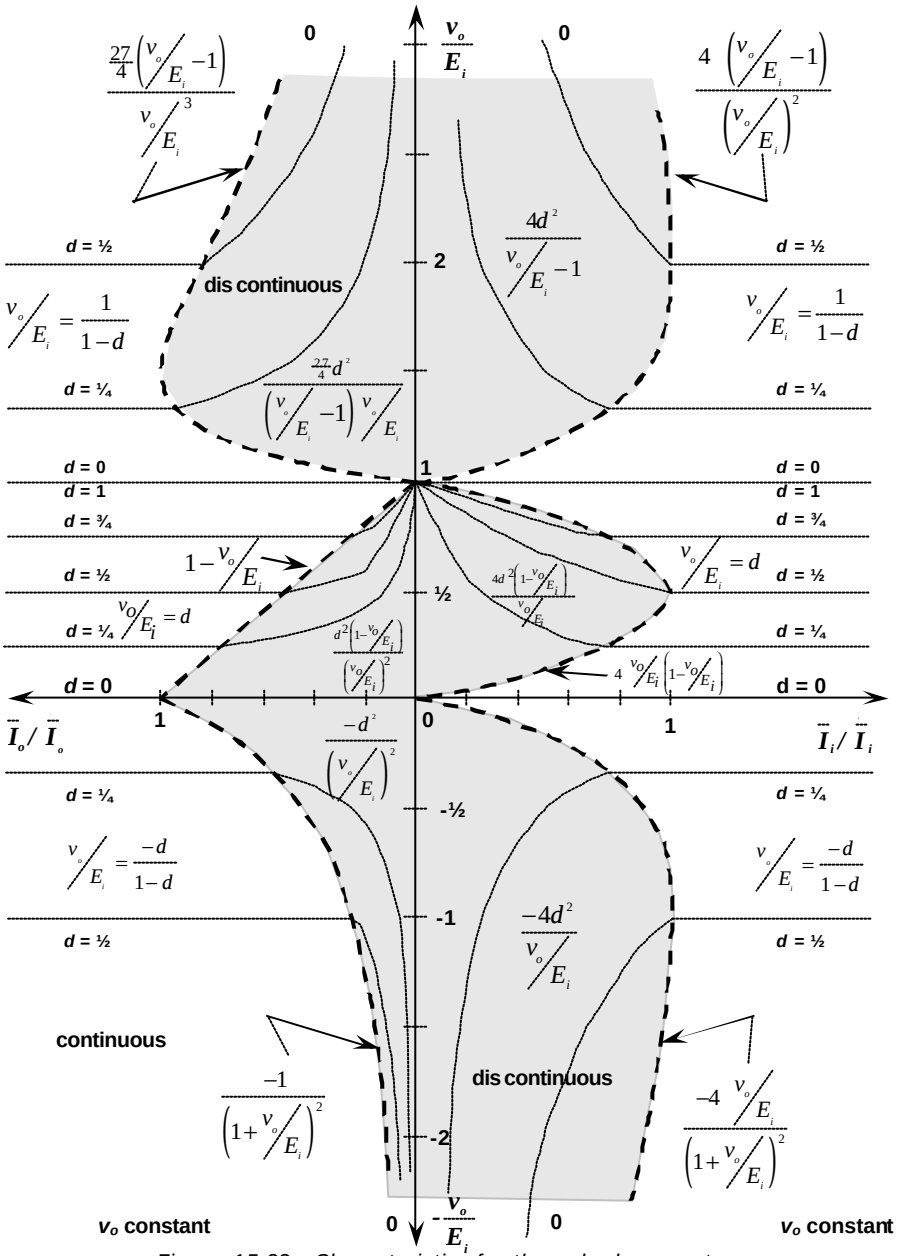

Figure 15.23. *Characteristics for three dc-dc converters, when the output voltage v_o is held constant.*

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Problems

15.1. An smps is used to provide a 5V rail at 2.5A. If 100 mV p-p output ripple is allowed and the input voltage is 12V with 25 per cent tolerance, design a flyback buck-boost converter which has a maximum switching fre quency of 50 kHz.

15.2. Derive the following design equations for a flyback boost converter, which operates in the discontinuous mode.

$$\hat{i}_i = 2 \times \overline{I}_{o\,(\max)} \times \frac{v_o}{E_{i\,(\min)}} = \text{ constant} \qquad t_D = \frac{1}{f_{(\max)} \dfrac{v_o}{E_{i\,(\min)}}}$$

$$L = t_{T\,(\min)} \frac{v_o - E_{i(\min)}}{\hat{i}_i} \qquad f = \frac{1}{t} = f_{(\max)} \frac{\overline{I}_o}{\overline{I}_{o\,(\max)}} \times \frac{v_o - E_i}{v_o - E_{i(\min)}}$$

$$C_{(\min)} = \frac{\Delta Q}{\Delta e_o} = \frac{\hat{i}_i \, t_{T(\min)}}{2\Delta e_o} \qquad ESR_{(\max)} = \frac{\Delta e_o}{\hat{i}_i}$$

15.3. Derive design equations for the forward non-isolated converter, operating in the continuous conduction mode.

15.4. Prove that the output rms ripple current for the forward converter in figure 15.2 is given by $\Delta i_o / 2\sqrt{3}$.

16

Capacitors

Selection of the correct type of capacitor is important in all applications. Just satisfying capacitances and voltage requirements is usually insufficient. In previous chapters, capacitors have been used to perform the following functions:

- turn-off snubbering (8.3.1)
- *dv/dt* snubbering (8.1)
- (RFI filtering (10.2.4, 14.7)
- transient voltage sharing of series connected devices (10.1.1)
- switched-mode power supply output filtering and dc blocking (15)
- dc rail splitting for multilevel converters (14.4)
- power *L*-*C* filters

as well as

- ac power factor correction and compensation
- dc rail decoupling
- voltage multipliers
- motors for single phase supplies
- cascaded multilevel inverters for VAr compensation

which is just to name a few uses of capacitors in electrical power applications. In each application, the capacitor is subjected to stresses, such as high temperature, *dv/dt* or high ripple current, which must be taken into account in the design and selection process. To make the correct capacitor selection it is necessary to consider various capacitor types, their construction, features, and uses.

Two broad capacitor types are found extensively in power electronic circuits, namely:

- liquid and solid (wet and dry) electrolyte, oxide dielectric capacitors, for example an aluminium electrolytic capacitor
- plastic film dielectric capacitors, for example a polyester capacitor.

The first capacitor group has a metal oxide dielectric which offers large capacitance for a small volume. The second capacitor group, which uses a thin plastic film as a dielectric, offers high ac electrical stress properties.

Ceramic and mica dielectric capacitors are also considered. Ceramic capacitors are used extensively in high power, high frequency switched mode power supplies where they offer small size, low cost, and good performance. The voltage and capacitance ranges for the four main types of dielectric capacitors are shown in figure 16.1.

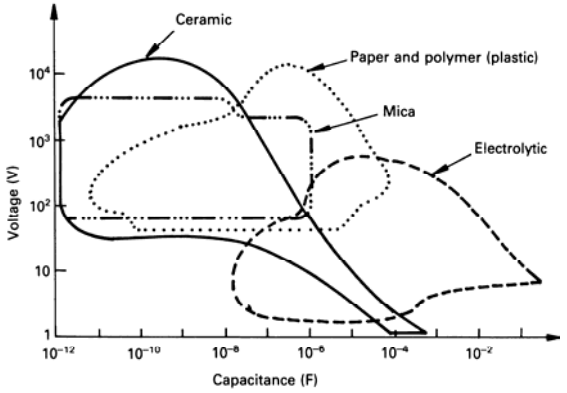


Figure 16.1. *Voltage/capacitance boundaries for the principal types of capacitors.*

16.1 Capacitor general properties

The following general principles, properties, and features are common to all capacitor dielectric types.

16.1.1 Capacitance

The primary function of a capacitor is to store electrical energy in the form of a charge. The amount of electrical charge, Q, is given by

$$Q = CV \quad \text{(C)} \tag{16.1}$$

while the stored energy is given by

$$E = \tfrac{1}{2}QV = \tfrac{1}{2}CV^2 \quad \text{(J)} \tag{16.2}$$

The value of capacitance, C, is directly proportional to surface area, A, and inversely proportional to the thickness of the dielectric layer, W; that is

$$C = \varepsilon_r \varepsilon_o \frac{A}{W} \quad \text{(F)} \tag{16.3}$$

The dielectric constants ε_r or alternatively K for materials in common usage, are summarised in table 16.1.

Table 16.1. Dielectric constants for common dielectric materials.

Dielectric material	*Relative dielectric constant* ε_r
Vacuum	1
Air (1 atmosphere)	1.00059
Polystyrene	2.5
Polypropylene	2.5
Polycarbonate	2.8
Polyethylene-terephthalate	3
Impregnated paper	2 - 6
Mica	6.5 - 8.7
Al_20_3	7
Glass	4 - 9.5
Ta_20_3	10 - 25
Ceramic	20 -12,000

16.1.2 Equivalent circuit

The impedance of a capacitor can be modelled by the capacitor equivalent circuit shown in figure 16.2. In series with the ideal capacitor, C_R, termed *rated capacitance,* is an *equivalent series resistor* R_s (ESR) and *equivalent series inductor* L_s (ESL). R_s is determined by lead and junction resistances, while L_s is the inductance of the electrodes due to the construction and the supply lines. The value of L_s is usually given for a specific package and capacitor type, and is generally neglected at lower frequencies, below the self-resonant frequency, which is given by

$$\omega_r = \frac{1}{\sqrt{L_s C_R}} \qquad \text{(rad/s)} \tag{16.4}$$

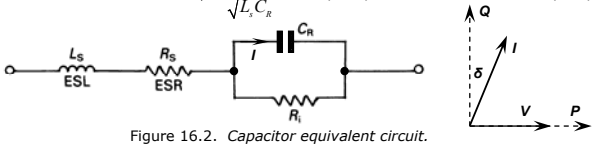


Figure 16.2. *Capacitor equivalent circuit.*

The electrical impedance Z of a capacitor, neglecting R_i the insulation resistance which is usually large, is

$$Z = R_s + jX \qquad (\Omega) \tag{16.5}$$

Since the ESL is neglected, at lower frequencies, since ωL is small

$$Z = R_s - \frac{j}{\omega C_R} \qquad (\Omega) \tag{16.6}$$

and

$$\tan\delta = \omega C_R R_s = \frac{R_s}{X_c} = \frac{1}{Q} = \frac{\text{real power}}{\text{reactive power}} \tag{16.7}$$

where δ is the loss angle and tan δ is termed the *dissipation factor,* which is the inverse of the circuit quality factor, Q. The angle δ is that necessary to make the capacitor current lead the terminal voltage by 90°, figure 15.2, as for the ideal capacitor.
If the insulating or dielectric dc resistance, R_i *(= $\rho_i \ell/A$),* is included, then

$$\tan\delta = \frac{1}{\omega C_R R_i} + \omega C_R R_s \tag{16.8}$$

and at low frequency

$$\tan\delta_l = \frac{1}{\omega C_R R_i} \tag{16.9}$$

while at high frequency

$$\tan\delta_u \approx \omega C_R R_s \tag{16.10}$$

Both R_s and X_c are dependent on temperature and frequency as shown in figure 16.3. Figure 16.3a shows that the rated capacitance illustrated has a positive temperature coefficient, the value of which also depends on capacitance and rated voltage. Also shown is the negative temperature dependence of equivalent series resistance ESR. Figure 16.3b shows that C_R and ESR both decrease with frequency.
Since C_R and ESR are temperature and frequency dependent, and are related to tan δ and Z, then tan δ and Z are frequency and temperature dependent as illustrated in figures 16.3c and 16.3d. Figure 16.3c shows the typical characteristics of the impedance of an oxide dielectric capacitor versus frequency, at different temperatures. At low frequencies the negative slope of Z is due to the dominance of the capacitive reactance, $Z \approx X_c = 1/\omega C_R$, whereas the horizontal region, termed the resonance region, is where Z is represented by the ohmic resistance R_s, that is $Z \approx R_s$. At higher frequencies the inductive reactance begins to dominate, whence $Z \approx \omega L_s$ and tan $\delta = R_s/\omega_s L$.
Figure 16.3d shows how the dissipation factor, tan δ, increases approximately proportionally with frequency to a high value at resonance, as would be expected from equation (16.9). At lower frequencies tan δ may be considered as having a linear frequency dependence, according to tan δ = tan $\delta_o + kf$.
The service life of a capacitor occurs when its parameters fall outside the specification limit, termed *degradation.* Such parameters are usually the capacitance, dissipation factor, impedance, and leakage current. The service life is specified under specific operating conditions such as voltage, ambient temperature, and current, and will increase

- the lower the ambient temperature, T_a
- the lower the ripple current or voltage, I_r
- the lower the operating voltage in proportion to the rated voltage, V_{op}/V_R
- the higher the ac load frequency, f.

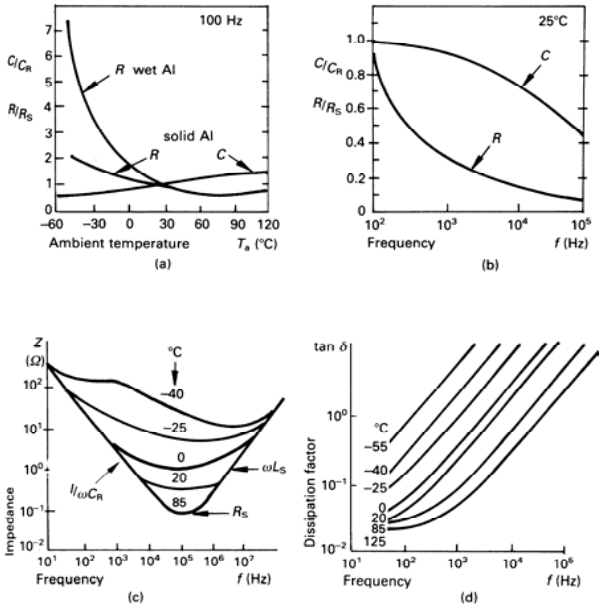


Figure 16.3. *Variation of capacitor equivalent circuit parameters with frequency and temperature for a high voltage (47 μF, 350 V) metal oxide liquid dielectric: (a) R_s and C_R as a function of temperature; (b) R_s and C_R as a function of frequency; (c) impedance Z as a function of frequency and temperature; and (d) tan δ as a function of frequency and temperature.*

16.1.3 Lifetime and failure rate

Other factors may be relevant to specific dielectrics.
Lifetime is the period until a given failure rate is reached. The failure rate, λ, is the ratio of the number of failures to the service life expected. It is usually indicated in failures per 10^9 component hours and is an indicator of equipment reliability.
If, in a large number N of identical components, percentage ΔN fail in time Δt, then the failure rated λ, averaged over Δt is expressed as

$$\lambda = \frac{\Delta N}{N \times \Delta t} \quad (/\text{h}) \tag{16.11}$$

If the sample N is large, then the failure rate in time can be represented by a continuous 'bathtub'-shaped curve as shown in figure 16.4, such that

$$\lambda = \frac{1}{N}\frac{dN}{dt} \quad (/\text{h}) \tag{16.12}$$

This figure shows the three distinct failure periods, and the usual service life is specified according to the failure λ_o, which is constant.

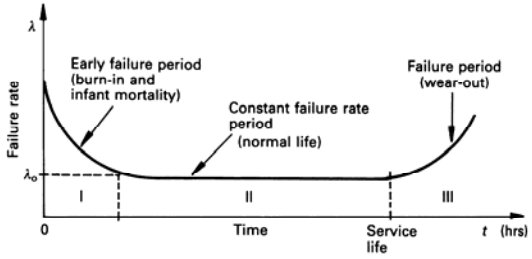


Figure 16.4. *The bathtub curve showing variation of failure rate with operating hours.*

In the case of voltage, current, and other stresses including temperature, which differ from those under which λ_o is specified, *conversion* or *acceleration factors* are used to calculate the new failure rate.
Typical conversion factors are given in table 16.2 for ambient temperature T_a, and operating voltage V_{op}, in relation to rated voltage V_R. Alternatively conversion graphs are also used or the Arrhenius' law

$$\lambda = \lambda_o \left(\frac{V_{op}}{V_R}\right)^n e^{-E\left(\frac{1}{KT} - \frac{1}{KT_o}\right)} \tag{16.13}$$

Table 16.2. Stress conversion factors for an aluminium electrolytic capacitor

$\frac{V_{op}}{V_R}$ %	*Conversion factor*	*Temperature* T_a *(°C)*	*Conversion factor*
100	1	≤40	1
75	0.4	55	2
50	0.2	70	5
25	0.06	T_{jmax}	10
10	0.04		
(a)		(b)	

Example 16.1: ***Failure rate***

A component has a failure rate $\lambda_o = 2 \times 10^9$/h, commonly termed 2 fit (failures in time) using 10^9/h as reference.
With reference to table 16.2, what is the failure rate if

i. the ambient temperature, T_a, is increased to 55°C
ii. the operating voltage is halved
iii. i. and ii. occur simultaneously?

Solution

Assume λ_o applies to conditions at $T_a \leq 40$°C and V_R.

i. If the ambient temperature is increased from 40°C to 55°C, then using a conversion factor of 2 from table 16.2b

$$\lambda_{55} = 2 \times \lambda_o$$
$$= 4 \quad \text{fit}$$

that is, the failure rate has doubled, from 2 fit to 4 fit.

ii. Similarly, by halving the operating voltage, a conversion factor of 0.2 is employed from table 16.2a. The new failure rate is

$$\lambda_{½V} = 0.2 \times \lambda_o$$
$$= 0.4 \quad \text{fit}$$

that is, the failure rate has decreased by a factor of 5, from 2 fit to 0.4 fit.

iii. If simultaneously both the ambient temperature is increased to 55°C and the operating voltage is halved, then

$$\lambda_{55,½V} = 2 \times 0.2 \times \lambda_o$$
$$= 0.8 \quad \text{fit}$$

The conversion factors are cumulative and the failure rate decreases from 2 fit to 0.8 failures in time.

♣

If the number of units surviving decreases exponential with time, then the probability of failure after a service time t is given by

$$F(t) = 1 - e^{-\lambda t} \tag{16.14}$$

Equipment failure rate can be calculated by summing the failure rates of the individual components, that is

$$\lambda_{total} = \lambda_1 + \lambda_2 ..... + \lambda_n \tag{16.15}$$

If the failure rate is to be constant, then the instantaneous failure rate of the number of faults per unit time divided by the number of non-failure components must yield a constant

$$\frac{1}{1-F(t)} \frac{dF(t)}{dt} = \lambda \tag{16.16}$$

For n components in a system the probability of system survival is

$$1 - F(t) = \left(1 - F_1(t)\right) \times \left(1 - F_2(t)\right) \times .... \left(1 - F_n(t)\right) = e^{-\lambda_1 t} \times e^{-\lambda_2 t} \times .... e^{-\lambda_n t}$$
$$= n\lambda \tag{16.17}$$

if, since the units are identical, $\lambda_1 = \lambda_2 = ... = \lambda_n$.
The *meantime between failure* (*mtbf*) is given by

$$mtbf = \frac{1}{\lambda_{total}} = \int_0^\infty 1 - F(t)\, dt = \int_0^\infty e^{-\lambda t}\, dt = \frac{1}{\lambda} \tag{16.18}$$

The service operating life τ for a specified probability of failure is therefore given by

$$\tau = \frac{1}{\lambda} \ell n \frac{1}{1-F} \tag{16.19}$$

Example 16.2: ***Capacitor reliability***

A capacitor has a failure rate λ of 200 x 10^{-9} failure/hour, 200 fit. Calculate

i. the probability of the component being serviceable after one year
ii. the service life if the probability of failure is chosen to be 1% or 0.1%
iii. the mean time between failure
iv. the mean time between failure for 10 parallel connected capacitors
v. the probability of survival for 1 year and of failure for units, if 1000 units each have 10 parallel connected capacitors.

Solution

i. The probability of the capacitor being serviceable after 8760 h (1 yr) is given by

$$1 - F(1\,yr) = e^{-\lambda t}$$

$$= e^{-200\times10^{-9}\times8760} = 0.998 \quad (99.8\%)$$

ii. Component lifetime is given by

$$\tau = \frac{1}{\lambda}\,\ell n\frac{1}{1-F}$$

$$\tau(1\%) = \frac{10^9}{200}\,\ell n\frac{1}{1-0.01} = 50{,}000 \text{ h} = 5.7 \text{ years}$$

$$\tau(0.1\%) = \frac{10^9}{200}\,\ell n\frac{1}{1-0.001} = 5{,}000 \text{ h} = 0.57 \text{ years}$$

iii. The mean time between failure, given by equation (16.18) is

$$mtbf = 1/\lambda = \frac{10^9}{200} = 5 \text{ x } 10^6 \text{ h} = 570 \text{ years}$$

iv. The failure rate for 10 capacitors is 10λ = 2000 fit and the mtbf is

$$\frac{1}{10\lambda} = \frac{10^9}{2000} = 57 \text{ years}$$

v. For 1000 units, each with a failure rate of 10λ, the probability of one unit surviving 1 year is

$$1 - F(1 \text{ yr}) = e^{-10\,x\,200\,x\,10^{-9}\,x\,8760} = 98.2 \text{ per cent}$$

The probable number of first year failures with 1000 units is

$$F(1 \text{ yr}) = 1 - e^{-200\,x\,10^{-9}\,x\,8760} = 0.002 \text{ pu} = 2 \text{ units}$$

♣

The reliability concepts considered are applicable to all electronic components and have been used to illustrate capacitor reliability.

16.1.4 Self-healing

One failure mode of a capacitor is voltage breakdown in a defective area of the dielectric. As a result of the applied voltage, the defective area experiences an abnormally high electric field which may cause failure by arcing. Oxide capacitors using an electrolyte and plastic film dielectric capacitors exhibit self-healing properties, which in the case of plastic film dielectrics allow the capacitor to remain functional after voltage breakdown.

In the case of a defect in the dielectric oxide layer of an electrolytic capacitor, the maximum field strength is reached first in the defective region. This is effectively the process which occurs during the formation of the oxide layer, which results in the formation of new oxide, thereby repairing the defect. The reforming process is relatively slow compared with the healing time for non-polarised capacitors.
By contrast, the high electric field at the defect in a plastic film capacitor causes an arc which evaporates the metallisation in the breakdown region, thereby isolating the faulty dielectric within a few microseconds.

16.1.5 Temperature range

The operating temperature upper and lower limits are either dictated by expected service life or the allowable variation limits on the nominal capacitance. Most capacitors can be used outside their nominal temperature limits, but at reduced lifetime, hence with reduced reliability. The extremes -55°C to 125°C are common, but obviously electrolytic capacitors must be restricted to a smaller range if the electrolyte is not either to freeze or to boil.

16.2 Liquid and solid, metal oxide dielectric capacitors

The oxides of metals such as aluminium and tantalum are capable of blocking current flow in one direction and conducting in the other. Operation of metal oxide dielectric capacitors is based on the so-called *valve effect* of these two metals.

16.2.1 Construction

The capacitor dielectric layer consists of aluminium oxide Al_20_3 or tantalum oxide Tn_20_3 which is formed by an electrochemical oxidising process of aluminium foil or sintered tantalum powder. These starting metals form the capacitor anode. The oxide layer withstands high electric field strengths, typically 8 x 10^8 V/m for Al_20_3 which represents 1.25 nm per volt, and are excellent insulators (hence result in a high capacitor loss factor). This field strength is maintained during the oxidising process, so that the oxide thickness is dependent and practically proportional to the *forming voltage* V_F. To avoid changing the oxide thickness during normal use, the component *operated rated voltage* V_R should always be lower than the forming voltage, as shown in figure 16.5. The difference V_F - V_R is the *over-oxidisation voltage* and substantially determines the capacitor operational reliability. For general-purpose electrolytic capacitors, the value of V_R / V_F is about 0.8, while solid capacitors are rated at 0.25.

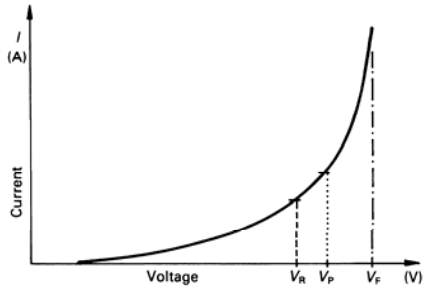


Figure 16.5. *Current dependence on voltage of Al electrolytic capacitors.*

The oxide dielectric constant ε_r is approximately 10 for Al_20_3 and 25 for Ta_20_3, while in comparison paper-based dielectrics have a value of approximately 5. An oxide thickness of $W = 0.7$ μm is sufficient for high voltage capacitors (≥ 160 V) as compared with minimum practical paper dielectric thickness of about 6 μm. The metal oxide type capacitors potentially offer high capacitance per unit volume. To further improve the capacitance per unit volume, before oxidation, the aluminium anode surface area is enlarged 10-300 times by electrochemical deep etching processes. In the case of tantalum capacitors, the sintered tantalum structure results in the same increase of area effect.

The capacitor is formed by the placement of the cathode on to the oxide layer. In the case of the electrolytic capacitor, a highly conductive organic acid electrolytic (based on dimethylacetamide) which is impregnated into porous paper forms the capacitor cathode. The electrolyte largely determines the ESR hence it must have a low resistivity over a wide temperature range. It must also have a breakdown voltage well above the capacitor rated voltage at maximum operating temperature. For long life, electrolytes with a water content must be avoided. Teflon spacers are sometimes used rather than paper. In the case of solid capacitors, a high conductive cathode is formed by a solid semiconductor metal oxide, such as manganese dioxide. The electrical contact to the cathode is a layer of etched aluminium, which has a thin oxide layer. In solid oxide capacitors, the manganese dioxide is dipped into graphite which is coated with silver epoxy for soldering.

The four possibilities are shown in figure 16.6. A porous paper or glass fibre is used as a space keeping agent in order to avoid short circuits and direct mechanical contact.

Long strips of the cross-sections are wound into cylindrical bodies and encased as shown in figure 16.6. Operation at high voltages causes oxide growth and the production of hydrogen. Any gas pressure relief valve should be orientated upwards.

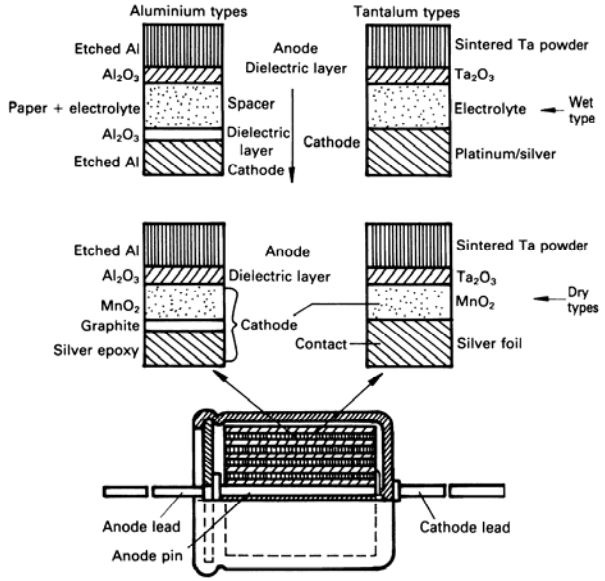


Figure 16.6. *Construction of metal oxide capacitors.*

16.2.2 Voltage ratings

Basic electrolyte (electrolytic) capacitors are suitable only for unipolar voltages, where the anode is positive with respect to the cathode. In the case of the aluminium electrolytic capacitor, the cathode connection metal does have a thin air-oxide layer which corresponds to an anodically generated layer with a blocking voltage capability of about 2 V. Above this voltage level, an electrolytic generated dielectric oxide film would be formed on the cathode foil. The effect is to decrease the capacitance and cause high internal heating and gas formation, which can lead to failure.

Solid, oxide capacitors are in principle capable of supporting bipolar voltage since the cathode is a semiconductor, manganese oxide. In practice, impurities such as moisture

restrict the reverse voltage limits to 5-15 per cent of V_F. The usable reverse voltage decreases with increased ambient temperature.
The rated voltage V_R may be exceeded under specified intermittent conditions, resulting in a maximum or peak voltage limit V_P, as shown in figure 16.5, where

for $V_R \leq 315V$ $\quad V_P = 1.15\ V_R$
for $V_R > 315V$ $\quad V_P = 1.1\ V_R$

Both V_R and V_P, are derated with increasing temperature.

16.2.3 Leakage current

When a dc voltage is applied to capacitors, a low current, I_{lk} called the *leakage current,* flows through every capacitor, as implied by the presence of R_i in the equivalent circuit model in figure 16.2. With oxide dielectric capacitors, this current is high at first and decreases with working time to a final value, as shown in figure 16.7.
A low final leakage current is the criterion of a well designed dielectric, thus leakage current can be considered as a measure for the quality of the capacitor. The current is a result of the oxidising activity within the capacitor. The leakage current depends on both dc voltage and ambient temperature, as shown in figure 16.8. The purity of the anode metal, hence oxide dielectric determines the leakage current.

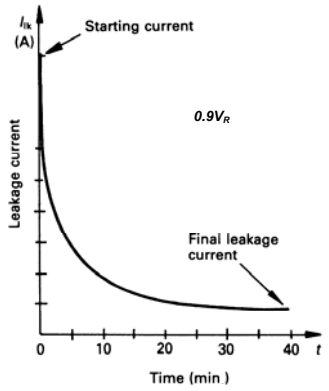


Figure 16.7. *Leakage current variation with working time for a liquid aluminium oxide capacitor.*

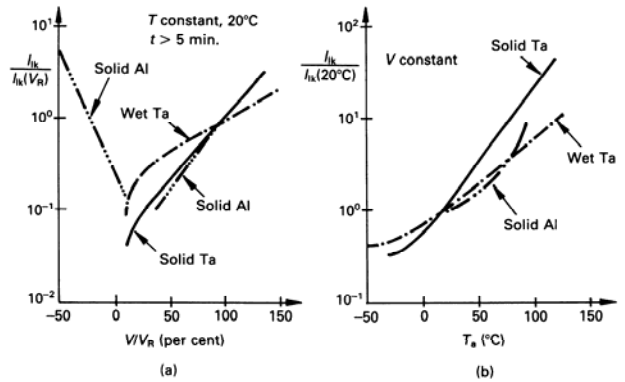


Figure 16.8. *Typical leakage current of oxide capacitors versus: (a) voltage and (b) temperature.*

Liquid, oxide capacitors have the lower leakage currents at rated voltage since when a voltage is applied; anions in the electrolyte maintain the dielectric electrochemical forming process. The $Mn0_2$ in solid oxide capacitors has lower reforming capabilities.
From figure 16.8 it will be seen that leakage increases with both temperature and voltage. The increase in leakage current with temperature is lower in liquid capacitors than in the solid because, once again, the electrolyte can provide anions for the dielectric reforming process.
For an aluminium electrolyte capacitor at 85°C, an expected lifetime of 2000 hours is achieved by selecting $V_R / V_F = 0.8$. However, V_F is inversely proportional to absolute temperature so for the same leakage current at 125°C, the ratio of V_R / V_F must be decreased to

$$\frac{V_R}{V_F} = 0.8 \times \frac{273+85}{273+125} = 0.7$$

For higher temperature operation, a higher forming voltage is required. But since $V_F \times C_R$ is constant for any dielectric/electrode combination, C_R is decreased.
When connecting electrolytic capacitors in series, parallel sharing resistors are necessary to compensate for leakage current variation between the capacitors. The design of the sharing network is as for the steady-state voltage sharing for semiconductors presented in 10.1.1. Additionally, the resistors provide a discharge path for the stored energy at power-off. When parallel connecting capacitors, highest reliability is gained if identically rated capacitors (voltage and capacitance) are used.

16.2.4 Ripple current

The maximum superimposed alternating current, or ripple current $\hat{I}_r$ is the maximum rms value of the alternating current with which a capacitor is loaded, which produces a temperature difference of 10 K between the core and ambient. Ripple current results in power being dissipated in the ESR, according to

$$P_d = \hat{I}_r^2 R_s \qquad \text{(W)} \qquad (16.20)$$

which results in an internal temperature rise until equilibrium with the ambient occurs.

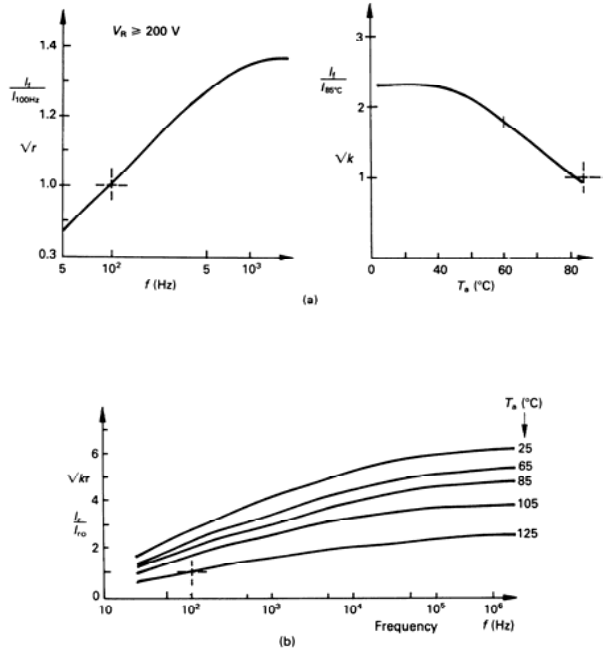


Figure 16.9. *Frequency and temperature ripple current conversion multipliers for: (a) liquid and (b) solid $A1_20_3$ capacitors.*

The maximum power dissipation $\hat{P}_d$ is dependent on the thermal dissipation properties of the capacitor, and from equation (5.4)

$$\hat{P}_d = h\,A\,\Delta T \qquad \text{(W)} \qquad (16.21)$$

where h = heat transfer coefficient (W/m^{2}K)
A = capacitor outer surface area (m^2)
ΔT = temperature difference between capacitor surface, T_s, and ambient, T_a (K)

Thus the maximum ripple current is given by

$$\hat{I}_r = \sqrt{\frac{\hat{P}_d}{R_s}} = \sqrt{\frac{hA\Delta\hat{T}}{R_s}} \qquad \text{(A)} \qquad (16.22)$$

The ESR, R_s, is both temperature and frequency dependent, hence rated ripple current I_{ro}, is specified at a given temperature and frequency, and at rated voltage V_R. Due to the square root in equation (16.22), conversion to other operating conditions is performed with the frequency multiplier $\sqrt{r}$ and temperature multiplier $\sqrt{k}$, such that

$$I_r = \sqrt{k}\sqrt{r} I_{ro} = \sqrt{k\,r}\; I_{ro} \qquad \text{(A)} \qquad (16.23)$$

Typical multiplier characteristics for aluminium oxide capacitors are shown in figure 16.9. It will be seen from figure 16.9a that electrolytic capacitors are rated at 85°C, while as seen in figure 16.9b solid types are characterised at 125°C. For each type, a reference frequency of 100 Hz is used. Electrolytic capacitors usually have a thermal time constant of minutes, which can be exploited to allow intermittent overloads.

Example 16.3: ***Capacitor ripple current rating***

A 1000 µF, 385 V liquid, aluminium oxide capacitor has an rms ripple current rating I_{ro} of 3.7 A at 100 Hz and 85°C.
Use figure 16.9a to calculate the allowable ripple current at

i. 60°C and 1 kHz
ii. lowest stress conditions.

Solution

i. Using equation (16.23)

$$I_r = \sqrt{k}\sqrt{r} I_{ro} = \sqrt{k\,r}\; I_{ro} \qquad \text{(A)}$$

where from figure 16.9a at 60°C, $\sqrt{k} = 1.85$
at 1 kHz, $\sqrt{r} = 1.33$

whence $\hat{I}_r = 1.33 \times 1.85 \times 3.7$A
$= 9.1$ A

ii. This capacitor experiences lowest stressing at temperatures below 40°C, where $\sqrt{k}$ =2.25 and at frequencies in excess of 2 kHz when $\sqrt{r}$ = 1.37. Under these conditions the ripple current rating is

$$\hat{I}_r = 2.25 \times 1.37 \times 3.7\text{A}$$
$$= 11.4\text{A}$$
♣

Non-sinusoidal ripple currents have to be analysed such that the individual frequency components satisfy

$$\hat{I}_r^2 \geq \sum_n \frac{I_n^2}{r_n} \qquad (16.24)$$

where $\hat{I}_r$ is for the appropriate rated ambient and reference frequency as indicated in figure 16.9.
Liquid tantalum capacitors have a ripple current rating which is determined by the physical dimensions, independent of temperature over a wide range, and independent of frequency above 50 Hz.

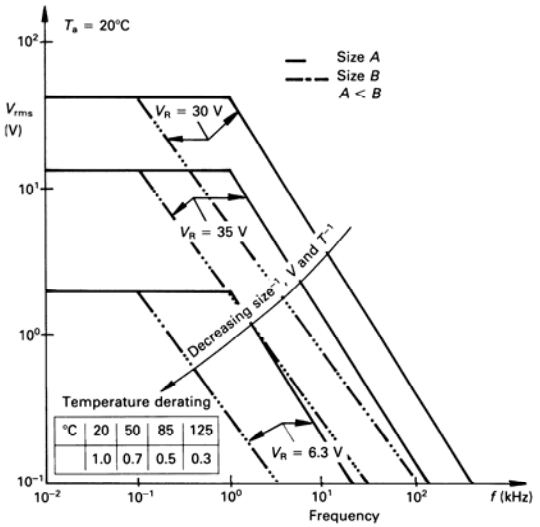


Figure 16.10. *Rms voltage limits of solid tantalum capacitors for different physical dimensions, temperature, voltage rating, and frequency.*

Ripple current ratings may not be specifically given for some capacitor types, for example solid tantalum capacitors. In this case an indirect approach is used. In satisfying ac voltage limitations as illustrated in figure 16.10, and any series resistance requirement, allowable ripple currents can be specified for a given temperature.

16.2.5 Service lifetime and reliability

16.2.5i - Liquid, oxide capacitors

As considered in 16.1.3, the reliability and lifetime of a capacitor can be significantly improved by decreasing the thermal and electrical stresses it experiences. Stress reduction is of extreme importance in the case of liquid aluminium oxide capacitors since it is probably the least reliable commonly used component.
The reliability and service lifetime of an aluminium oxide electrolytic capacitor are dominated by its ripple current, operating temperature, and operating voltage. Figure 16.11 in conjunction with figure 16.9a can be used to determine service life.

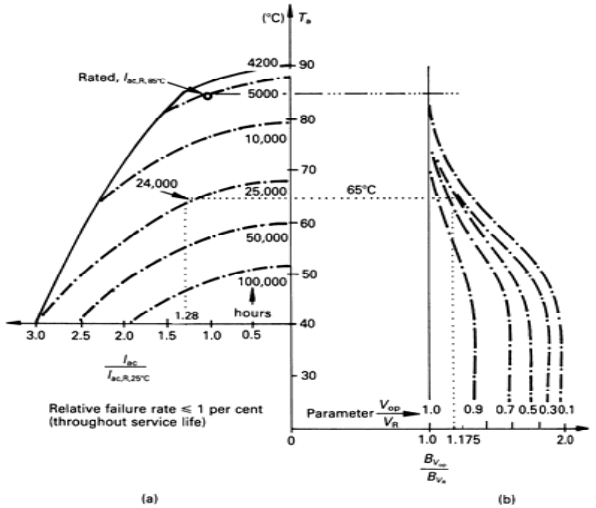


Figure 16.11. *Service life for an aluminium oxide liquid capacitor. Temperature dependence of lifetime variation with: (a) ripple current and (b) operating voltage.*

Example 16.4: $A1_20_3$ *capacitor service life*

A 1000 μF, 385 V dc aluminium oxide liquid capacitor with a ripple current rating I_{ro} of 2.9 A at 100 Hz and 85°C ambient is used at 5 A, 4 kHz, in a 65°C ambient and on a 240 V dc rail. What is the expected service lifetime of the capacitor?

Solution

From figure 16.9a at 4 kHz, √r =1.35, whence

$$\frac{I_o}{I_{ro}} \times \frac{1}{\sqrt{r}} = \frac{5\text{A}}{2.9\text{A}} \times \frac{1}{1.35} = 1.28$$

From figure 16.11a, the coordinates 1.28 and 65°C correspond to a 24,000 hour lifetime with less than 1 per cent failures. Since a 385 V dc rated capacitor is used on a 240 V dc rail, that is, a ratio 0.64, an increase in service lifetime of 17½ per cent can be expected, according to figure 16.11b. That is, a service lifetime of 28,000 hours or greater than 3½ years is expected with a relative failure rate of less than 1 per cent.
Generally, between 40 and 85°C aluminium electrolytic capacitor lifetime doubles for every 10°C decrease in ambient temperature. A service lifetime of 7 years could be obtained by decreasing the ambient temperature from 65°C to 55°C.

♣

With aluminium electrolytic capacitors, degradation failures are mostly due to factors such as

- aggressiveness of the acidic electrolyte
- diffusion of the electrolyte
- material impurities.

16.2.5ii - Solid, oxide capacitors

The failure rate of solid aluminium and tantalum capacitors is determined by the occurrence of open and short circuits as a result of dielectric oxide layer breakdown or field crystallisation. In general, for a given oxide operating at rated conditions, liquid capacitors have a shorter lifetime than the corresponding solid type. Solid aluminium capacitors are more reliable than solid tantalum types and failure is usually the degradation of leakage current rather than a short circuit.
In comparison with liquid, electrolytic capacitors, solid types, and, in particular, tantalum type capacitors, have a number of desirable characteristics:

- higher capacitance per unit/volume due to the higher permittivity of Ta_20_3 and the intrinsically high effective area per unit volume due to the sintered construction
- changes in parameters (C, tan δ) are less because the specific resistance of $Mn0_2$ and hence temperature coefficient, is lower than that of liquid electrolytes
- electrolyte is stable, does not evaporate or corrode.

The failure rate of all capacitors can be improved by decreasing the stress factors such as temperature and operating voltage. But reliability of solid tantalum capacitors can be increased by placing a series resistor (low inductance) in the circuit. The improvement is illustrated by the following design example, which compares the lifetime of both liquid and solid tantalum capacitors based on the conversion curves in figure 16.12.

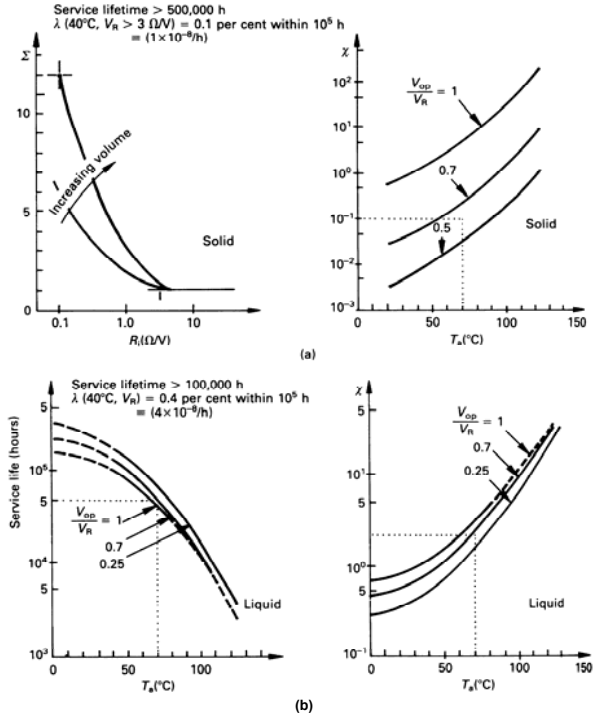


Figure 16.12. *Stress conversion factors for:*
(a) solid tantalum capacitors and (b) liquid tantalum capacitors.

Example 16.5: ***Lifetime of tantalum capacitors***

A 22 μF tantalum capacitor is required to operate under the following conditions:
ambient temperature T_a, 70°C
operating voltage V_{op}, 15 V
circuit resistance i. 1 Ω
ii. 100 Ω

Calculate the expected lifetime for solid and liquid tantalum capacitors.

Solution

Capacitor used $C_R = 22$ μF
$V_R = 25$ V
For each capacitor type (solid or liquid) the voltage stress factor is
$V_{op}/V_R = 0.60$
For the solid tantalum, the circuit resistance factor is given by
i. $R_i' = 1\ \Omega/15\ \text{V} = 0.07\ \Omega/\text{V}$ which is < 0.1 Ω/V
ii. $R_i' = 100\ \Omega/15\ \text{V} = 6.6\ \Omega/\text{V}$ which is > 3 Ω/V
Based on figure 16.12, the capacitor lifetime calculation is summarised below.

		Liquid tantalum	*Solid tantalum*	
R	Ω	1 and 100	1	100
R_i	Ω	n/a	0.1	3
ΣR_i		(1)	12	1
X at V_{op}/V_R=0.6 and 70°C		2.2	0.10	0.10
λ_o	/h	4×10^{-8}	1×10^{-8}	1×10^{-8}
λ $= \lambda_o \times \Sigma$	/h	$2.2\times4\times10^{-8}$ 8.8×10^{-8}	$12\times0.1\times10^{-8}$ 1.2×10^{-8}	$1\times0.1\times10^{-8}$ 0.1×10^{-8}
fit		88	12	1
τ (% failures) within $\lambda\Delta t$	h	45,000 (0.4%)	83,000 (0.1%)	100,000 (0.1%)

♣

16.3 Plastic film dielectric capacitors

Plastic (polymer) dielectric type capacitors are non-polarised capacitors and in general offer high dv/dt and pulse rating capability compared with oxide type capacitors.
The most common dielectric plastics used are:

poly***e*** ***t*** hylene-terephthalate (polyester or PEPT)	T
poly ***c*** arbonate	C
poly ***p*** ropylene	P
poly ***s*** tyrene	S
polyphenylene sulph ***i*** de	I

The letter shown after each type is the symbol generally used to designate the film type. The symbol K is used to designate plastic, which is *Kunststoff* in German.
Two basic types of plastic film dielectric capacitors are common. The first type involves *metallisation* deposited on to the plastic and the metal forms the electrodes. Typically such a capacitor would be termed MKP, that is metallised - M, plastic - K, polypropylene - P. A foil capacitor, the second type, results when metal foil is used for the electrode. Typically such a capacitor would be termed KS, that is plastic - K, polystyrene - S. The plastic type is generally designated by the fifth letter of the plastic name, that is the letter after poly, with two exceptions.

16.3.1 Construction

16.3.1i - Metallised plastic film dielectric capacitors

The dielectric of these capacitors consists of plastic film on to which metal layers of approximately 0.02-0.1 μm are vacuum deposited. A margin of non-coated film is left as shown in figure 16.13a. The metallised films are either wound in a rolled cylinder or flattened to form a stacked block construction. In this construction, the metallised films are displaced so that one extends out at one end of the roll and the next layer extends out the other end as shown in figure 16.13a. This displaced layer construction is termed *extended metallisation* and facilitates electrical contact with the electrodes. A hot metal spray technique, called s*chooping,* is used for making electrical contact to the extended edges of the metallised plastic winding. This large disk area contact method ensures good ohmic contact, hence low loss and low impedance capacitor characteristics result.
The most common metallised plastic film capacitors are those employing polyester, MKT and polypropylene, MKP.
Polyester has a higher dielectric constant than polypropylene, and because of its stronger physical characteristics it is available in thinner gauges than is polypropylene. Very high capacitance values result in the smallest possible space. But polypropylene has a higher dielectric strength and lower dielectric losses, hence is favoured at higher ac voltages.

16.3.1ii - Foil and plastic film capacitors

Foil capacitors normally use a plastic film dielectric which is a flexible bi-axially aligned electro-insulator, such as polyester. Aluminium foils and/or tin foils are used as the electrodes. The thin strips are wound to form the capacitor as shown in figure 16.13b. An *extended foil* technique similar to the extended metallisation method is used to enable contact to be made to the extended foil electrodes.

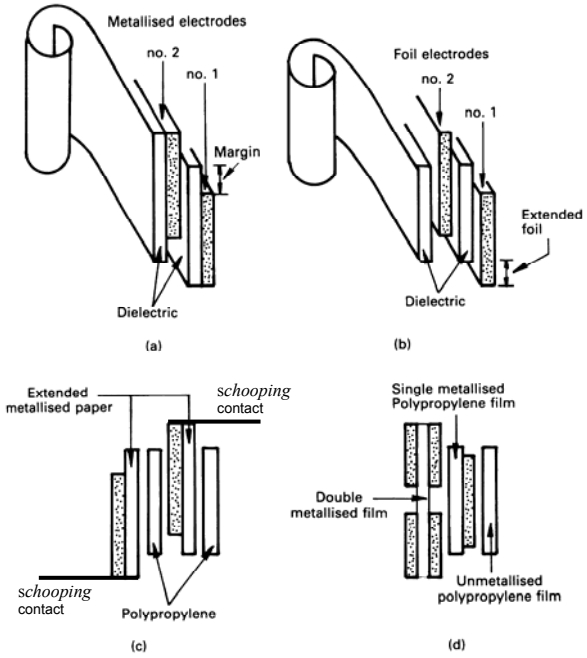


Figure 16.13. *Plastic capacitor constructions: (a) extended single metallisation; (b) extended foil; (c) mixed dielectric; and (d) mixed dielectric, double metallisation.*

16.3.1iii - *Mixed dielectric capacitors*

To further improve the electrical stress capabilities of a capacitor, combinations of different dielectrics are commonly used. Such capacitors use combinations of metallised plastics, metallised paper, discrete foils and dielectrics, and oil impregnation.
Figure 16.13c shows the layers of a mixed dielectric paper and polypropylene capacitor. A thin gauge of polypropylene dielectric is combined with textured

metallised paper electrodes. The coarse porous nature of the paper allows for improved fluid impregnation of the dielectric material, which counters the occurrence of gas air bubbles in the dielectric. This construction has the electrical advantages of high dielectric strength, low losses, and a self-healing mechanism, all at high voltages.
Two plastic dielectrics can be combined, as shown in figure 16.13d, to form a *mixed layer* capacitor. It involves a double metallised polyethyleneterephthalate film and polypropylene films. These dielectric combinations give low inductance, high dielectric strength, and low losses with high ac voltage capability.

16.3.2 Insulation

The insulation characteristics of a capacitor are indicated either as a resistance value R_i as shown in Figure 16.2 or as a time constant, $\tau = R_i C_R$. The resistance comprises the insulation resistance of the dielectric (layer to layer) and the insulation resistance between layer and case. This later resistance is determined by the quality of the case insulating material and by the length of the surface leakage paths.
Both the time constant and resistance are dependent on voltage and temperature, as is shown in figure 16.14. These characteristics illustrate that extremely high insulation resistance values can be obtained.

16.3.3 Electrical characteristics

16.3.3i - *Temperature dependence*

The capacitance of plastic film capacitors changes with both temperature and frequency, as shown in figure 16.15. The dependence is strongly dependent on the dielectric film although some foil types are virtually independent of frequency. Table 16.3 summarises capacitance temperature dependence for a wide range of dielectrics. The temperature coefficient is measured in parts per million per degree Kelvin, ppm/K. The temperature dependence of dissipation factor is shown in figure 16.21a.

16.3.3ii - *Dissipation factor and impedance*

Figure 16.16a shows the typical frequency dependent characteristics of the dissipation factor for a range of plastic dielectric capacitor types. It is important to note that polyester types have 50-100 times the losses of polypropylene capacitors. A low loss characteristic is important in power pulse applications where capacitor package heat dissipation may be a limiting factor.
Generally, tan δ rises with increased frequency and increased capacitance. Tan δ is dominated by dielectric losses and the contact resistance of the leads. The extended foil/metallisation and schooping contact methods provide not only a low and constant ohmic contact, but because of the large contact area, result in a low self-inductance. The resonant frequency of such capacitors, because of their self-inductance and their capacitance, is high as shown by the minimum impedance in figure 16.16b. Minimum

impedance decreases with increased capacitance and each capacitor in the range, here 1.5 nF to 4.7 μF, has its own Y-shaped impedance curve. The self-resonant frequency decreases with increased capacitance. In figure 16.16b, the full impedance curves for maximum and minimum capacitance only have been shown.

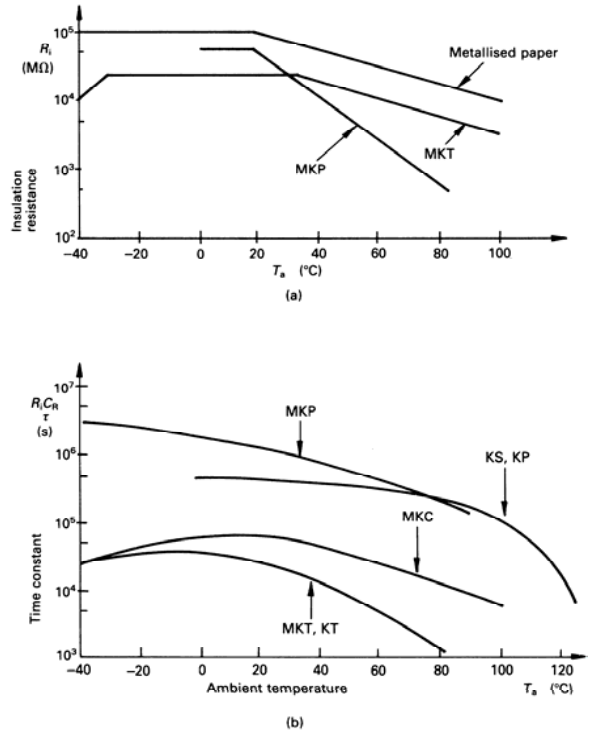


Figure 16.14. *Plastic dielectric insulation resistance temperature dependence characteristics:(a) resistance R_i and (b) time constant τ.*

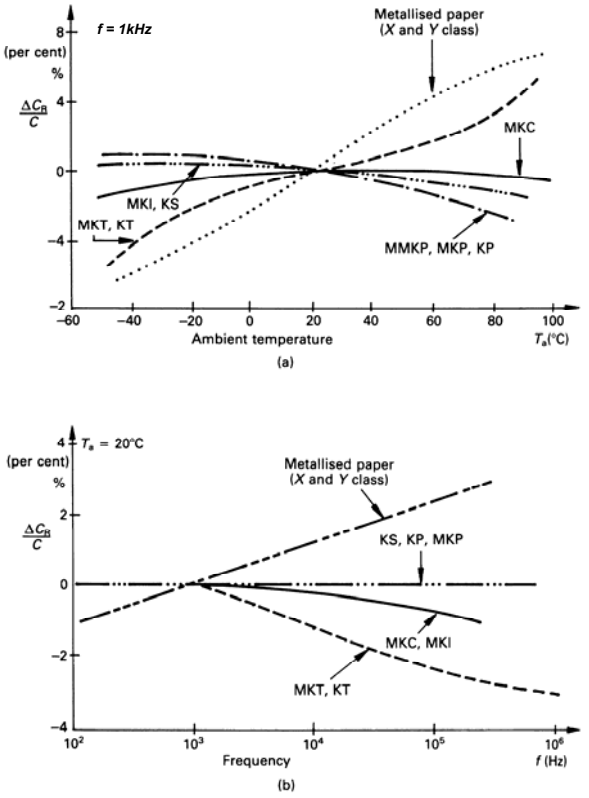


Figure 16.15. *Plastic film dielectric capacitance variation with: (a) ambient temperature and (b) frequency.*

Table 16.3. Capacitor temperature coefficient for various dielectric materials

Dielectric type	*Temperature coefficient (ppm/K)*		
	metallised	*other*	*film/foil*
Polypropylene	-170		-120
Polyester	400		400 (non-linear)
Polycarbonate	150		-50 to -150
Polystyrene			-125
Paper	300		300
Mica		100	
Ceramic		+ 1000 to -1000	(non-linear)
Aluminium		1500	
Tantalum (solid and liquid)		+200 to +1000	

16.3.3iii - *Voltage derating*

The ac and dc voltages which may be applied continuously to a capacitor vary with ambient temperature and also frequency in the case of ac voltage rating. Typical characteristics showing frequency and temperature dependence are shown in figure 16.17 for plastic dielectric capacitor types. It will be seen that the ac voltage rating is significantly less than the dc voltage rating, while both voltage ratings are derated above 85°C and at higher frequencies. In all situations, the sum of the dc voltage and peak value of superimposed ac voltage must not exceed the rated dc voltage.
An alternative approach for calculating the maximum ac voltage, allowable V_{ac}, for a capacitor is based on the power dissipation limits, P, of the package.
If we neglect R_i and ESL in the capacitor equivalent circuit shown in figure 16.2, then

$$P = \frac{V_{R_s}^2}{R_s} = I^2 R_s \qquad \text{(W)} \tag{16.25}$$

and

$$V_{R_s}^2 = \frac{R_s^2}{R_s^2 + \dfrac{1}{\omega^2 C_R^2}} V_{ac}^2 \tag{16.26}$$

Since from equation (16.10) for plastic dielectric capacitors

$$\tan\delta = \omega C_R R_s$$

then equation (16.25) can be written as

$$P = \left(R_s C_R\right) \omega^2 C_R V_{ac}^2 \qquad \text{(W)} \tag{16.27}$$

or alternatively

$$P = \tan\delta \;\; \omega C_R V_{ac}^2 \qquad \text{(W)} \tag{16.28}$$

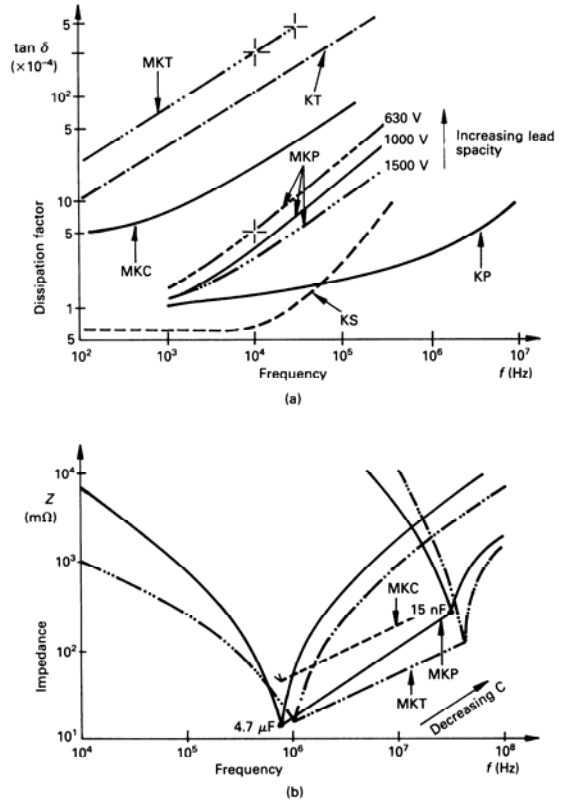


Figure 16.16. *Frequency characteristics for plastic dielectric capacitors: (a) maximum dissipation factor, tan δ and (b) typical impedance characteristics, Z, for metallised plastic dielectric capacitors.*

The value of tan δ for equation (16.28) is available from figure 16.16a or, alternatively, the value of R_sC_R for equation (16.27) is available from figure 16.18.
The maximum permissible power dissipation, $\hat{P}$ which depends on the package dimensions and ambient temperature, is given in figure 16.19. Thus when the power dissipation, for a given ac voltage, has been calculated, figure 16.19 can be used to specify the minimum size (dimensions) capacitor capable of dissipating that power.
The following example illustrates the design approach outlined.

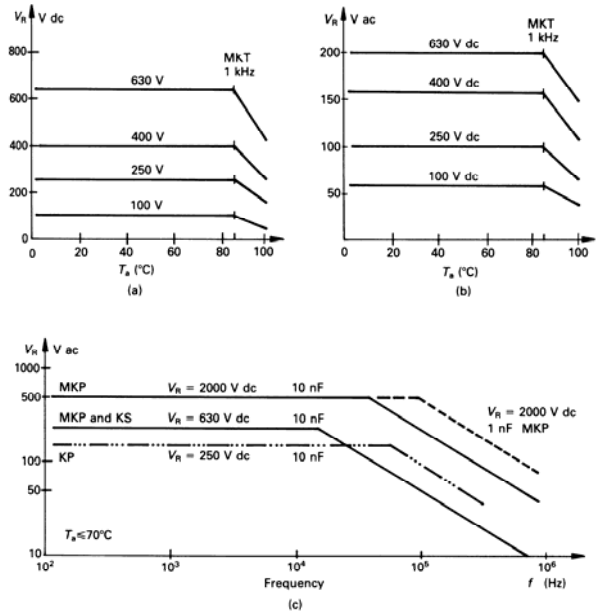


Figure 16.17. *Plastic dielectric capacitor, voltage derating characteristics: (a) dc voltage derating with ambient temperature; (b) ac voltage derating with temperature; and (c) ac voltage derating with frequency.*

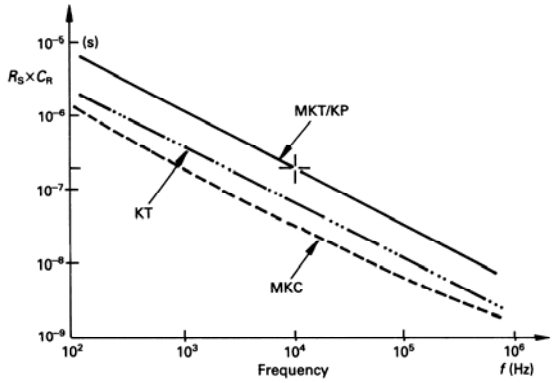


Figure 16.18. *Maximum product of series resistance, R_s, and rated capacitance, C_R, as a function of frequency.*

Example 16.6: ***Power dissipation limits - ac voltage***

A 0.1 µF plastic capacitor is used in a 100 V ac, 10 kHz and 50°C ambient application. Select suitable metallised polypropylene and polyester capacitors for this application.

Solution

i. Metallised polyester capacitor (MKT)
From equation (16.27)

$$P = (R_sC_R)\,\omega^2 C_R V_{ac}^2 \qquad \text{(W)}$$

From figure 16.18, $R_sC_R = 2 \times 10^{-7}$ at 10 kHz. Thus

$$P = (2\times10^{-7}) \times (2\pi\times10^4)^2 \times (0.1\times10^{-6}) \times (100)^2$$
$$= 780 \text{ mW}$$

From figure 16.19, at 50°C a MKT capacitor of dimensions 11×20×31 (mm) can dissipate 930 mW. The applicable capacitor must have an ac voltage rating in excess of 100 V ac. From figure 16.17b, it can be seen that a 0.1 µF, 400 V dc MKT capacitor is necessary, given that the dimension constraints are met.

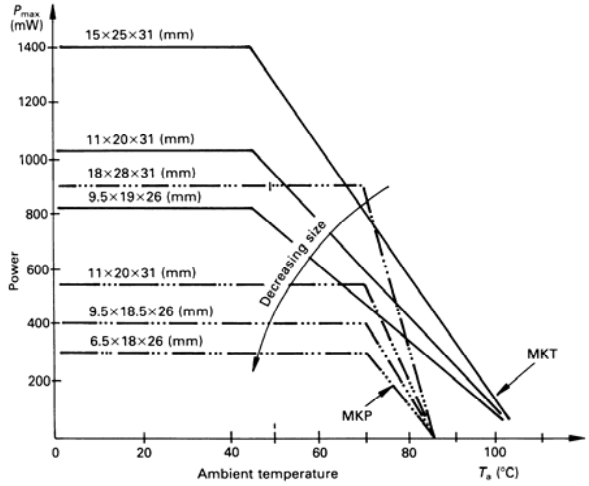


Figure 16.19. *Maximum power dissipation for metallised plastic capacitors as a function of ambient temperature and capacitor dimensions.*

ii. Metallised polypropylene capacitor (MKP)

From equation (16.28)

$$P = \tan\delta \;\; \omega C_R V_{ac}^2 \qquad \text{(W)}$$

From figure 16.16a, $\tan\delta = 4.0 \times 10^{-4}$ at 10 kHz, for a 600 V dc type. Thus

$$P = (4.0\times10^{-4}) \times (2\pi\times10^{4}) \times (0.1\times10^{-6}) \times 100^2$$
$$= 25.6 \text{ mW}$$

From figure 16.19, at 50°C, the smallest volume MKP capacitor, of dimensions 6.5×15×26 mm, can dissipate 300 mW. From figure 16.17c it can be seen that a 0.1 μF, 630 V dc (250 V ac) MKP capacitor is necessary.

From figure 16.17c it can be seen that a 250 V dc 0.1 μF polypropylene foil capacitor (KS) is capable of 160 V ac at 10 kHz. Figure 16.16a shows the dissipation factor of KP type capacitors to be under half that of the metallised equivalent. That is, the expected losses are only

$$P = (1.4\times10^{-4}) \times (2\pi\times10^{4}) \times (0.1\times10^{-6}) \times 100^2$$
$$= 9 \text{ mW}$$

♣

16.3.3iv - *Pulse dV_R/dt rating*

Related to the ac voltage rating and power handling capabilities of a capacitor is the rated pulse slope dV_R/dt, which from $i = C_R\, dv/dt$ is specified by

$$R = \frac{V_R}{C_R\, dV/dt_{\max}} = \frac{V_R}{\hat{I}} \qquad (16.29)$$

where R is the minimum series resistance including the ESR. Generally for a given C_R, dv/dt capability increases with rated voltage V_R, and decreases as the distance between the metallised electrode contacts increases. If the capacitor operating voltage V_{op} is decreased below V_R, at which voltage, dv/dt capability is specified, dv/dt capability increases according to

$$\frac{dV_{op}}{dt} = \frac{dV_R}{dt} \times \frac{V_R}{V_{op}} \qquad \text{(V/s)} \qquad (16.30)$$

The dv/dt capability depends on both the dielectric type and layer construction. Generally polystyrene (KS) and polyester (KT) foil type capacitors are not applicable to high dv/dt applications. Metallised polycarbonate capacitors offer slightly better dv/dt properties than those of metallised polyester. Metallised paper capacitors can withstand very high levels of dv/dt, 30-50 times higher than those for metallised polyester. Capacitors using polypropylene, or even better a mixed dielectric involving polypropylene, offer extremely high dv/dt capability. With the construction shown in figure 16.13d, a 1 μF metallised polypropylene capacitor with V_R of 2000 V dc and 1000 V ac, a 2500 V/μs capability is attainable. Practically the dv/dt limit may be restricted by the external connections. Such ratings are obtainable with polypropylene because of its extremely low losses, tan δ, as indicated in figure 16.16a. Under such high dv/dt stresses, it is important to ensure that the power dissipated does not exceed the package limit.

16.3.4 Non-sinusoidal repetitive voltages

Capacitors used for repetitive transient suppression, and for turn-off snubbers on GTO thyristors and diodes, experience high-magnitude short-duration voltage and current pulses which are not sinusoidal. High dv/dt capacitors based on metallised polypropylene are used, which are limited by their internal power losses, hence temperature rise and package power dissipation limit.

A restrictive graphical design approach for capacitor selection with sinusoidal, sawtooth, and trapezoidal pulse trains is shown in figure 16.20. The design approach is illustrated by the following example.

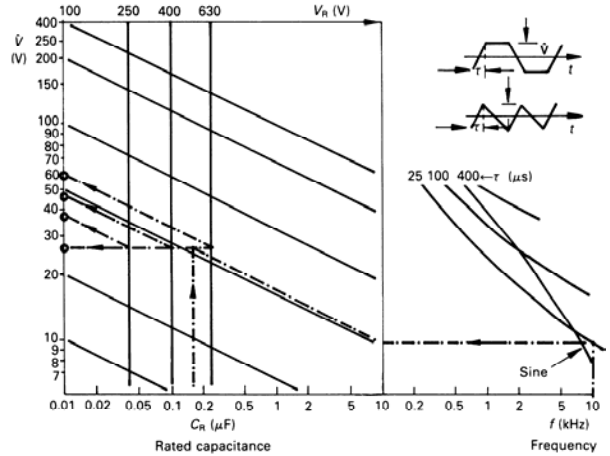


Figure 16.20. *Metallised polyester capacitor selection graph for sinusoidal and non-sinusoidal voltages.*

Example 16.7: ***Capacitor non-sinusoidal voltage rating***

A 0.15 μF MKT capacitor is used to generate a 10 kHz maximum and 25 μs risetime minimum, sawtooth ac voltage waveform. What voltage rated capacitor is applicable if the output voltage maximum is 100 V p-p?

Solution

Worst-case conditions are at maximum frequency, 10 kHz, and minimum risetime, 25 μs.
With reference to figure 16.20, use
f = 10 kHz (repetition frequency)
τ = 25 μs (risetime)
C = 0.15 μF (capacitance)
According to the dashed line in figure 16.20, starting from f = 10 kHz, yields
V_R = 100 V dc gives maximum peak voltage of 27 V
V_R = 250 V dc gives maximum peak voltage of 38 V
V_R = 400 V dc gives maximum peak voltage of 47 V
V_R = 630 V dc gives maximum peak voltage of 59 V

The peak to peak requirement is 100 V, hence only a 630 V dc 0.1 μF MKT capacitor can fulfil the specification.

♣

An alternative approach to specify the voltage limits for non-sinusoidal repetitive voltages is to sum the power contribution due to each voltage harmonic. The total power due to all harmonics must not exceed the capacitor package power limits.
The non-sinusoidal voltage v can be expressed in the form

$$v = \sum_{V_i} V_i \sin\left(i\omega t + \phi_i\right) \tag{16.31}$$

where V_i is the magnitude of the *ith* voltage harmonic, which has an rms value of

$$v_i = \frac{V_i}{\sqrt{2}}$$

From equations (16.10) and (16.27), assuming capacitance is frequency independent

$$P_i = \left(R_S C_R\right)_i \omega_i^2 C_{R_i} v_i^2 \tag{16.32}$$

or

$$P_i = \tan\delta_i \ \omega_i C_{R_i} v_i^2 \tag{16.33}$$

The total power dissipated is the sum of the powers associated with each frequency. The near-linear frequency dependence of tan δ and $R_S C_R$, as shown in figures 16.16a and 16.18, may be utilised to simplify the calculation procedure. Assuming the rated capacitance is independent of frequency may be a valid and helpful simplification, while the temperature dependence of C_R initially could be accounted for by using a value at 10 K above ambient.

Example 16.8: ***Capacitor power rating for non-sinusoidal voltages***

The applied voltage across a 1 μF MKP capacitor, at 40°C ambient is $\sqrt{2}$ 100 sin($2\pi \times 10^4 t$) + $\sqrt{2}$ Y sin($2\pi \times 3 \times 10^4 t$)
What is the maximum allowable voltage Y?

Solution

From equation (16.33), the total power is given by

$$P_i = \tan\delta_1 \ \omega_1 C_{R_1} v_1^2 + \tan\delta_3 \ \omega_3 C_{R_3} v_3^2$$

From figure 16.15b we may assume that capacitance is independent of frequency for polypropylene types. From figure 16.15a, at 50°C, rated capacitance has reduced by only 1 per cent - thus temperature effects on C_R may be neglected.
From figure 16.16, for a 600 V MKT capacitor
tan δ_1 at 10 kHz (ω_1) = 2.5×10^{-4}
tan δ_3 at 30 kHz (ω_3) = 4.2×10^{-4}
From figure 16.19b it can be seen that 880 mW can be dissipated in the largest

package at 50°C. Total power is given by

$$0.88\text{W} = 2.5\times10^{-4} \times 2\pi\times10^{4} \times 1\times10^{-6} \times 100^{2} + 4.2\times10^{-4} \times 6\pi\times10^{4} \times 1\times10^{-6} \times Y^{2} \quad \text{(W)}$$

Solving for Y, $Y = 30.2$ V rms.

♣

The key properties of plastic type non-polarised capacitors are summarised in table 16.4. The excellent dielectric properties of the polypropylene lead to metallised polypropylene capacitors being extensively used in power applications.

Table 16.4. Properties of non-polarised plastic type capacitors

dielectric type	ε_r	tanδ	λ_o	*dv/dt*	self-healing
polypropylene	low	low	good	high	good
polyester	medium	high	poor	medium	good
polystyrene	low	low	good	high	poor
polycarbonate	low	medium	good	medium	good
mixed dielectric	medium	medium	good	medium	good
paper	high	high	very good	high	very good

16.4 Emi suppression capacitors

Non-polarised capacitors are used in rfi filters for electrical appliances and equipment, as was introduced in 10.2.4. The capacitors used between line and neutral are termed class X while those used to earth are termed class Y.

16.4.1 Class X *capacitors*

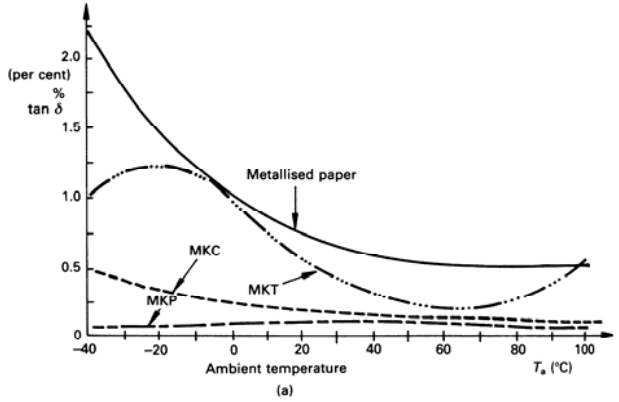
X capacitors are suitable for use in situations where failure of the capacitor would not lead to danger of electric shock. X capacitors are divided into two subclasses according to the ac power line voltage applied.

- The Xl subclass must support a peak voltage in excess of 1.2 kV in service, while
- X2 capacitors have peak service voltage capabilities of less than 1.2 kV.

In order to obtain the peak voltage requirement of Xl capacitors, a construction comprising impregnated paper dielectric and metal foil electrodes is essential. The common capacitance range is 10 nF to 0.2 μF.

The lower peak voltage requirement of X2 capacitors allows the use of a metallised plastic dielectric, of which polyester and polypropylene are common. Impregnated paper dielectrics may also be employed. Advantageously, metallised plastic film suppression capacitors yield high *dv/dt* capability with low associated losses, tan δ, as

shown in figure 16.16a. These films also offer good insulation properties as shown in figure 16.14. Variation of capacitance with frequency and temperature is shown in figure 16.15, while percentage variation of losses, tan δ, with frequency and temperature is shown in figure 16.21. The typical capacitance range of X2 capacitors is from 10 nF to l μF, rated for 250 V ac application.



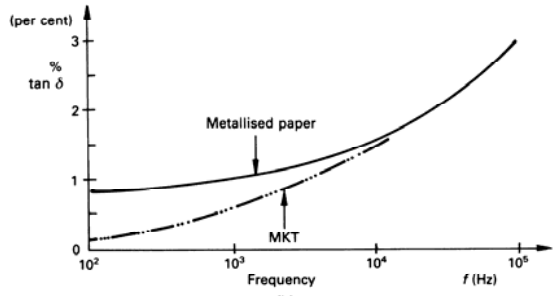


Figure 16.21. *RFI capacitance variation with: (a) ambient free-air temperature and (b) frequency.*

16.4.2 Class Y capacitors

Class Y capacitors are suitable for use in situations where failure of the capacitor could lead to danger of electric shock. These capacitors have high electrical and mechanical safety margins so as to increase reliability and prevent short circuit. They are limited in capacitance so as to restrict any ac current flowing through the capacitor, hence decreasing the stored energy to a non-dangerous level.

An impregnated paper dielectric with metal foil electrodes is a common construction and values between 2.5 nF and 35 nF are extensively used. Capacitance as low as 0.5 nF is not uncommon.

A Y-class capacitor for 250 V ac application can typically withstand over 2500 V dc for 2s, layer to layer. On an ac supply, 425 V ac ($\sqrt{3}\ V_R$) for 1000 hours is a common continuous ac voltage test.

If *dv/dt* capability is required, polypropylene film dielectric Y-class capacitors are available, but offer lower withstand voltage capability than paper types. Generally paper dielectric capacitors offer superior insulation resistance properties, as shown in figure 16.14a.

Metallised paper capacitors are also preferred to metallised plastic types because they have better self-healing characteristics. Breakdown in metallised plastic film dielectrics causes a reduction of the insulation resistance because of a higher carbon deposit in the breakdown channel than results with paper dielectrics.

16.4.3 Feed-through capacitors

Feed-through or four-terminal capacitors are capacitors in which the operating current flows through or across the electrodes. High frequency rfi is attenuated by the capacitors and the main power is transmitted unaffected. That is they suppress emi penetration into or from shielded equipment via the signal or power path.

Figures 16.22a and b show three terminal feed-through capacitors while figure 16.22c is a four-terminal capacitor. A three-terminal coaxial feed-through, wound capacitor cross-section is shown in figure 16.22d. The feed-through rod is the central current-carrying conductor: the outer case performs the function of an electrode plate and connector to produce an RF seal between the capacitor case and shielding wall.

These capacitors are effective from audio frequencies up to and above the SW and VHF band (>300 MHz). Current ratings from signal levels to 1600 A dc, 1200 A ac are available, in classes Xl and X2, rated at 240 V ac, 440 V ac and 600 V dc. Class Y feed-through capacitors rated at 25 A and 440 V ac, 600 V dc are available.

Important note: *This section on emi-suppression capacitors does not imply those requirements necessary to conform with governmental safety and design standards.*

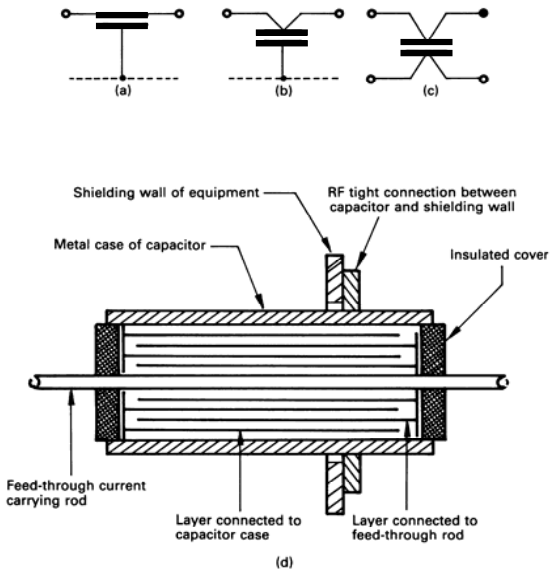


Figure 16.22. *Feed-through capacitors for RFI attenuation: (a), (b) three user terminals; (c) four terminals; and (d) coaxial feed-through capacitor construction.*

16.5 Ceramic dielectric capacitors

Ceramic capacitors as a group have in common an oxide ceramic dielectric. The dielectric is an inorganic, non-metal polycrystalline structure formed into a solid body by high temperature sintering at 1000 to 1300°C. The resultant crystals are usually between 1 and 100 μm in diameter.

The basic oxide material for ceramic capacitors is titanium dioxide ($Ti0_2$) which has a relative permittivity of about 100. This oxide together with barium oxide ($Ba0_2$) forms barium titanate ($BaTi0_3$) which is a ferro-electric material with a high permittivity, typically 10^4. Alternatively strontium titanate may be utilised. These same materials are used to make positive temperature coefficient resistors - thermistors, where dopants are added to allow conduction.

Table 16.5. Ceramic dielectric capacitor characteristics

Dielectric class			*I* (ε_r < 500) *Low K*	*II* (ε_r > 500) *Moderately high K*		*High K*
EIA designation* IEC/CECC designation			COG CG	X7R 2C1		Z5U 2F4
Temperature range		°C	-55 to 125	-55 to 125		+ 10 to 85
Dielectric constant	ε_r		13 - 470	700	to	50,000
Temperature coefficient of C_R (typical)			(N150) -150 ± 60 ppm	(X7R) ±15%		(Z5U) +22% / -56%
Dissipation factor	tan δ		0.15% @ 1 MHz	2.5%		3%
C		nF	< 0.2	< 4.7		< 40
V_R		V	500-1k	100 to >2k		

* In EIA designation, first letter and number indicate temperature range while last letter indicates capacitance change.

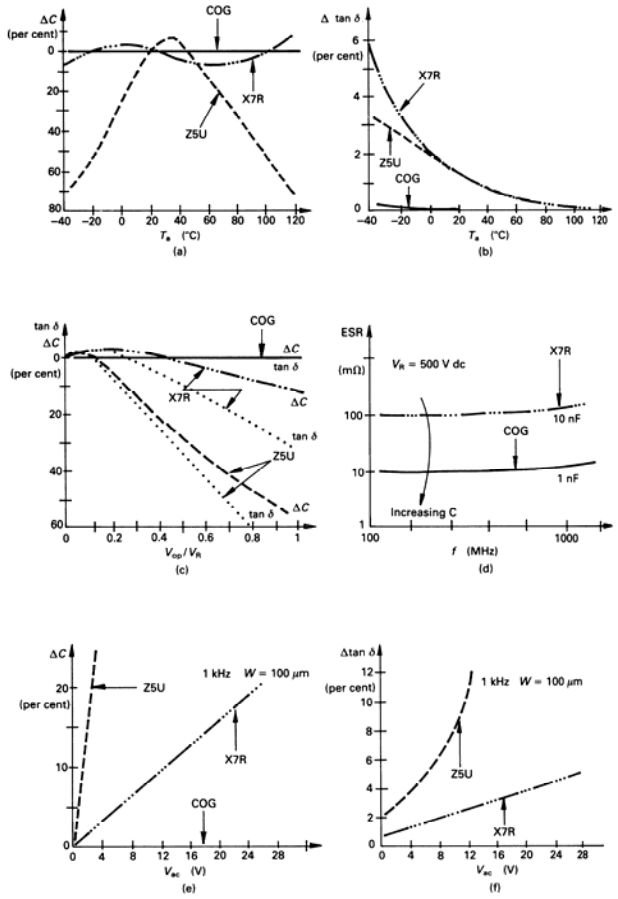
Metal plates of silver or nickel (with minimal palladium and platinum) are used to form the capacitor. Single plate, or a disc construction, is common as is a multi-layer monolithic type construction.
The ceramic dielectric is split into two classes, as shown in table 16.5.

16.5.1 *Class I dielectrics*

This class of dielectric consists mainly of $Ti0_2$ and additions of Ba0, La_20_3 or Nd_20_5, which provides a virtually linear, approximately constant and low temperature coefficient as shown in figure 16.23a.
COG capacitors belong to the class 1 dielectrics and have a low temperature coefficient over a wide temperature range, as seen in table 16.5. They provide stability and minimum dissipation properties. In attaining these properties, a low dielectric constant results and these capacitors are termed *low K*. Because of the low dielectric constant, capacitance is limited.

16.5.2 *Class II dielectrics*

Ceramic capacitors in this class are usually based on a high permittivity ferroelectric dielectric, $BaTi0_3$, hence termed *hi K*. Large capacitance in a small volume can be attained, but only by sacrificing the temperature, frequency, and voltage properties, all of which are non-linear. Typical characteristics are shown in figure 16.23. Their characteristics are less stable, non-linear, and have higher losses than class I ceramic, as seen in table 16.5. Also see table 16.6.



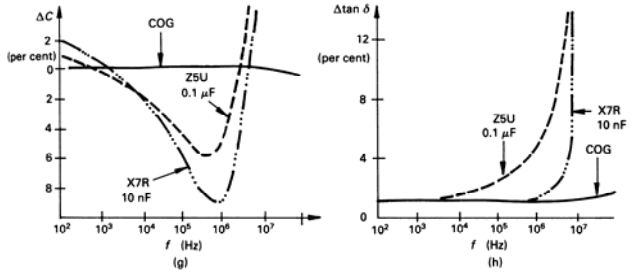


Figure 16.23. *Typical properties of commercial ceramic capacitors: (a) capacitance change with temperature; (b) dissipation variation with temperature; (c) capacitance change with dc voltage; (d) ESR change with frequency; (e) capacitance change with ac voltage; (f) dissipation factor variation with ac voltage; (g) capacitance change with frequency; and (h) dissipation factor variation with frequency.*

Table 16.6. Characteristics of class I and II type dielectrics

Class I	*Class II*
Almost linear capacitance/temperature function	Non-linear capacitance/temperature function
No voltage dependency of capacitance and loss angle	
No ageing	Slight ageing of capacitance
High insulation resistance	High insulation resistance
	Extremely high capacitance value per unit volume
Very small dielectric loss	
High dielectric strength	
Normal capacitance tolerance ±1% to ±10%	Normal capacitance tolerance ±5% to -20+80%

16.5.3 *Applications*

Flat circular disc ceramic (Z5U dielectric, high K) capacitors have a 2000 V dc, 550 V ac rating with capacitances of up to 47 nF. An exploitable drawback of such a ceramic capacitor is that its permittivity decreases with increased voltage. That is, the capacitance decreases with increased voltage as shown in figure 16.23c. Such a capacitor can be used in the turn-off snubber for the GTO thyristor and diodes which are considered in 8.1.3 and 8.1. High snubbering action is required at the commencement of turn-off, and can subsequently diminish without adversely affecting losses or the switching area trajectory tailoring. The capacitor action is a dual to that

performed by a saturable reactor, as considered in 8.3.4. Exploitation of voltage dependence capacitance is generally outside the capacitor specification. Advantageously, the disc ceramic capacitor has low inductance, but the high dissipation factor may limit the frequency of operation. Multi-layer ceramic capacitors can be used in switched mode power supply input and output filters.

16.6 Mica dielectric capacitors

The dielectric mica is a mineral which has a plane of easy cleavage enabling large sheets of single crystal to be split into thin plates, typically 50 μm thick. Stacks of mica plates are interleaved with silver metal foils as shown in figure 16.24.

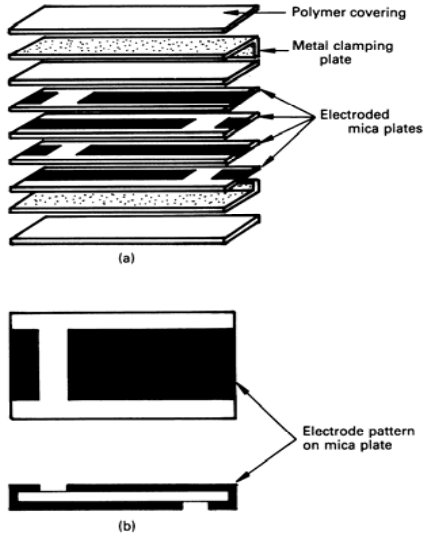


Figure 16.24. *Silver mica capacitor: (a) exploded construction view and (b) electrode pattern of a silvered mica plate.*

The metal foils, to which the leads are spot-welded, are made of silver, copper, brass, tin or lead. The stack is held together either by the encapsulation or a metal crimp. The assembled unit is encapsulated by dipping it into high melting temperature microcrystalline wax or by coating it with epoxy resin.

16.6.1 *Properties and applications*

Mica capacitors are non-polar, low loss, and stable up to about 30 MHz, where the lead length and electrodes dominate as inductance. Because of their relatively high cost of manufacture, as a result of the high labour content and diminishing number of mines, the ceramic capacitor, particularly the monolithic multi-layer type, is favoured.
Maximum ratings are a few nanofarads at 5000 V, with dissipation factors of 0.1 per cent at 1 kHz. For capacitance less than 1 nF, a 0.1 per cent dissipation factor is obtainable at 1 MHz. An insulation resistance of 10^5 MΩ at 20°C down to 10^4 MΩ at 125°C is common for capacitance to 10 nF, after which resistance falls off. Typical operating temperature range is from -55°C to 125°C, with a capacitance temperature coefficient of 0 to +70 ppm/K.
The maximum current depends on the edge connections and electrodes, so for each physical design the factor is different and is expressed in mA/pF. This rating may range between 1.6 mA/pF for smaller packages (9×8×8 mm) down to 0.12 mA/pF for larger packages (44×32×33 mm). A maximum VA limit must also be observed, typically 50 VA for smaller sizes up to 820 VA for the larger sizes.
Mica dielectric capacitors are sensitive to pressure.

16.7 Appendix: Minimisation of stray capacitance

Unexpected component stray capacitance, and inductance, can have disastrous circuit consequences. Figure 16.25 shows four examples of electronic components which have stray capacitance between two parts of the component used at different potentials. When the isolated part rapidly changes its relative potential, a charging current flows according to $i = C\,dv/dt$. With just 1 pF of capacitance, and at 10,000 V/µs, which is possible with MOSFETs and IGBTs, 10 mA of current flows. This current coupled from the power level to the signal level would affect cmos or ttl circuitry, leading to malfunction and possible failure, if precautions are not taken.
Figure 16.25a shows a power package electrically isolated from its heatsink, which is grounded (to 0V or V_s) in order to minimise rfi radiation. Large power blocks have over 100 pF of isolation capacitance. Other than injecting noise, the level may be sufficient to activate earthing leakage circuitry, if connected to ground. Increasing the ceramic substrate or mica thickness decreases capacitance according to equation (16.3), but at the expense of increasing thermal resistance. Al_2O_3 reduces the thermal impedance compared to aluminium nitride, but at the expense of increased cost.

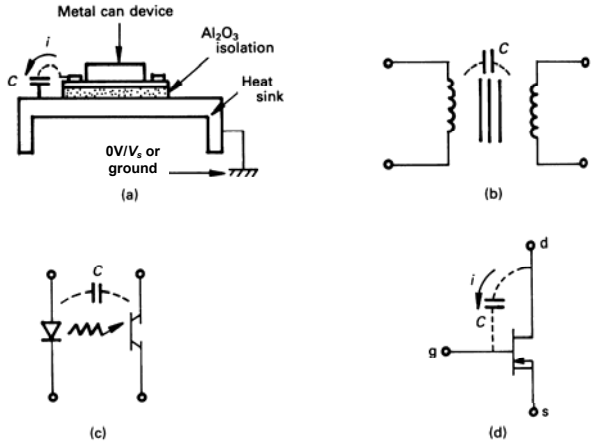


Figure 16.25 *Component stray capacitance C:*
(a) when isolating power devices; (b) between transformer windings; (c) in opto-couplers; and (d) between terminals of metal oxide semiconductor devices.

Interwinding capacitance, shown in figure 16.25b, is important in switch mode power supplies and other applications using transformers. By winding the primary and secondary in different bobbin sections, the interwinding capacitance is decreased since their physical separation is increased. Alternatively, an overlapped copper foil ground shield layer is wrapped between the two windings. The copper strip is a connected to a supply rail or earthed so that charging currents bypass sensitive circuitry. Experimentation will reveal the best connection potential and location position. The copper foil overlapped turn ends must not make electrical contact, otherwise a short circuit turn results. Minimise winding start to finish turns capacitance by using the winding method shown in figure 17.19b.
A similar solution is used in opto-coupler packages. A grounded Faraday's grid is placed between the emitter and receiver in order to divert charging current. High *dv/dt* opto-couplers, with less than 1 pF capacitance input to output, are guaranteed to 15000 V/µs at 200 V dc levels. This *dv/dt* limit decreases to 1000 V/µs on a 600 V dc rail. The effects of capacitive charging current can be minimised by driving the emitting diode from a low impedance source, both when on and off. Speed and current transfer ratio can be traded for higher *dv/dt* capability by increasing separation. For high

voltages and high *dv/dt* a fibre optic is an expensive alternative, but unlike the pulse transformer, has now lower cut-off frequency.

Figure 16.25d shows the Miller capacitance associated with the MOSFET and IGBT. During switching, the Miller capacitance charging and discharging currents slow the switching transition as power level current is injected into and from the gate level circuitry. A low impedance gate drives reduces the Miller capacitance effects.
A commonly overlooked capacitively injected current is that associated with the use of oscilloscope probes, when measuring power level signals. The scope probe ground should be physically connected to an appropriate power ground point, rather than signal ground. Always use the highest voltage step-down ratio probes as possible, since capacitance tends to decrease with increased step down ratio.

Reading list

Siemens, *Components,* 1986.

Mullard, *Book 3 Parts 1b and 1e,* 1984/85.

Rifa, *Capacitors,* 1986.

17

Soft Magnetic Materials

Soft magnetic materials are used extensively in power electronic circuits, as voltage and current transformers, saturable reactors, magnetic amplifiers, inductors, and chokes. These magnetic devices may be required to operate at only 50/60 Hz, or at frequencies down to dc or over 1 MHz. For example, a steel lamination ac mains voltage transformer operates at 50/60 Hz, while its ferrite switch-mode power supply equivalent may operate at 500 kHz. Soft magnetic materials have been utilised in other chapters for the following applications:

switching aid circuits	
- linear inductor	(8.3.3)
- saturable inductor	(8.3.4)
- snubber discharge	(figure 8.5)
- unified energy recovery	(9.2.1)
- thyristor *di/dt* control	(figure 8.5)
pulse transformers	(figures 7.7f)
current transformer	
turn-on snubber energy recovery	(figures 9.2a)
L-C resonator circuits	(figure 9.5c)
transient current sharing	(figure 10.8)
rfi filtering	(10.4.2)
single and three phase transformers	(11, 12)
cycloconverter intergroup reactors	(12.5)
phase shifting transformers	(14.1.3ii)
current source inductance	(14.2)
smps inductance and transformers	(15)

Hard magnetic materials, which are used for permanent magnets and ferrite beads for rfi suppression, are not specifically considered.

17.1 Material types

Two basic types of soft magnetic materials are extensively used, depending on the application and its requirements. These materials are:

- Ferromagnetic materials based on iron and nickel, which are for lower frequencies, < 2kHz, while
- Ferrimagnetic materials, which are based on ceramic oxides of metals, are applicable to frequencies from a few kilohertz to well over 80 MHz.

17.1.1 Ferromagnetic materials

17.1.1i - Steel

Cold-rolled grain-oriented steel is a 3-4 per cent silicon iron, cold reduced to develop a high degree of grain orientation, which gives

- increased flux for a given magnetising force and
- decreased size for a given rating, hence reduced weight.

Normally cores are produced in a number of material lamination thicknesses

- 0.3 mm for frequencies up to 200 Hz
- 0.1 mm for frequencies between 200 Hz to 2 kHz and
- 0.05 mm for higher frequencies and pulse applications.

Steel laminations for low frequency applications are available in different shapes. E and I laminations or strip C cores or toroids are extensively used for mains transformers and ac line inductors. Non-orientated silicon steels are extensively used for machine laminations.

17.1.1ii - Iron powders

Two general forms of iron powder cores are employed

- Cores are made by highly compacting insulated high quality spongy iron powder.
- High resistivity is required to reduce eddy current losses and so the iron powder is subjected to an acid treatment to produce an insulating oxide layer on the surface of each individual particle. This fine carbonyl iron is mixed with a bonding material and highly compressed. The bonding material used limits the maximum core temperature. Minute gaps appear between the particles, severely reducing the permeability. It is difficult to saturate such materials.

17.1.1iii - Alloy powders

These cores are made by highly compacting insulated alloy powder. The alloy is usually 50-75 per cent nickel, the remainder being iron with a small percentage of copper and molybdenum. The higher the iron percentage, the higher the saturation flux density and the higher the losses.

Powder iron and alloy cores are available in toroidal or ring shapes, cylindrical and hollow cylindrical cores, as well as cup cores, bobbins, pot cores, and beads.

17.1.2 Ferrimagnetic materials - soft ferrites

Ferrites are black, hard, brittle, chemically inert ceramic materials, which have a magnetic cubic structure.
The most general ferrites are polycrystalline magnetic ceramic oxides, which are compounds of iron oxide, Fe_20_3 mixed with one or more oxides of bivalent transition metals such as Fe0, Ni0, Zn0, Mn0, Cu0, Ba0, Co0, and Mg0. At lower frequencies, below a few MHz, a Mn-Zn combination is added to iron oxide, while for higher frequencies, above a MHz, Ni-Zn is the additive.
The raw oxide materials are mixed, pre-sintered at 1000°C if required, and ground. The powder material is shaped by means of pressing and sintering at between 1150°C and 1300°C. The sintering process involves raising the temperature to 1300°C in about 3 h, with 15 per cent oxygen present. The cores are cooled slowly without oxygen present to about 200°C in 20 h after entry. A 15 per cent linear, and 40 per cent by volume shrinkage occurs during sintering.
A diverse range of ferrite core shapes is available, which include, E, I, U, toroid, drum, pot, rod, tube, and screw. Where appropriate, diamond-wheel-ground air gaps are available on the centre pole. Manufacturing yields limit the physical component in size. Toroid cores of 152 mm outside diameter are not uncommon, and exotic shapes such as motor stators are made for special applications.

17.2 Comparison of material types

Table 17.1 shows typical comparative data for the main classes of soft ferro and ferri magnetic materials. Generally, those materials with higher saturating flux densities, B_s, have higher initial permeability μ_i, and hence offer higher inductance but at the expense of higher core eddy current and hysteresis losses.
Typical *B-H* curve characteristics are shown in figure 17.1 for the different soft magnetic materials shown in table 17.1. In the case of a transformer, the advantage of a high core flux density is that more volts v, per turn N, for a given frequency f, results. This is seen from Faraday's Law:

$$v = N\frac{d\phi}{dt} = NA\frac{d\,B}{dt} \qquad \text{(V)} \qquad (17.1)$$

whence for sinusoidal flux

$$v = 4.44NB_s A_c f \qquad \text{(V)} \qquad (17.2)$$

Table 17.1. Typical comparative data of soft magnetic materials

		Silicon steel	Iron		Alloys	Ferrites	
			powder	carbonyl		Mn-Zn	Ni-Zn
Frequency range, Δf	Hz	20-1k	400-10k	50k-1M	40-70k	400-250k	200k-10M
Temperature range, ΔT	°C	-55 to 300	-55 to 125	-55 to 105	-55 to 200	-30 to 105	-55 to 250
Initial permeability, μ_i		500	90	35	160	2700	100
flux density, B_s @ 25°C	T	1.75	0.86	0.86	0.63	0.47	0.24
remanence, B_r	T	1.2	0.2	0.001	0.02	0.2	0.12
Intrinsic mmf strength $H_i = (B_s - B_r)/2\mu_i$	A/m	440	2560	9120	1448	40	350
Resistivity, ρ	Ωcm	0.1				100	10^5 - 10^6
Curie temperature, T_c	°C	300	200	150	500	200	450

Inductance is specified from equation (17.1) and from

$$v = L\frac{di}{dt} \qquad \text{(V)} \qquad (17.3)$$

$$L = N\frac{d\phi}{di} \qquad \text{(H)} \qquad (17.4)$$

Using $\phi = BA_e$ and $H\ell_e = Ni$, equation (17.4) becomes

$$L = \frac{N^2 A_e}{\ell_e} dB\Big/dH \qquad \text{(H)} \qquad (17.5)$$

where dB/dH is the slope of the *B-H* curve, according to $B = \mu_o\mu_i H$. Therefore, before core saturation

$$L = \frac{N^2 A_e}{\ell_e}\mu_o\mu_i \qquad \text{(H)} \qquad (17.6)$$

The subscript ***e*** is used to denote the effective core parameter, as shown in table 17.2.
In rfi suppression and filtering applications, silicon steel is not effective since the initial permeability, μ_i, falls rapidly with frequency hence at the high suppression frequency, inductance is small. Thus iron powder or a high iron alloy may be used, which have relatively high flux densities and high losses. For rfi suppression, a high core loss aids suppression.
At inaudible frequencies, >20 kHz, for a low core loss, ferrites are extensively used. Although ferrite flux densities are relatively low, typically 0.4 T, eddy current and hysteresis losses are low. The low eddy current loss results from the high core material resistivity. With ferromagnetic materials, the eddy current loss is reduced by using thinner laminations or electrically isolated powder particles. A major disadvantage of a ferrite core is its poor temperature stability and low allowable core temperature. On the other hand, high initial permeabilities, >12,000, are obtainable.

Ferrite materials, application, and component design are specifically considered, although the concepts developed are generally applicable to ferromagnetic materials.

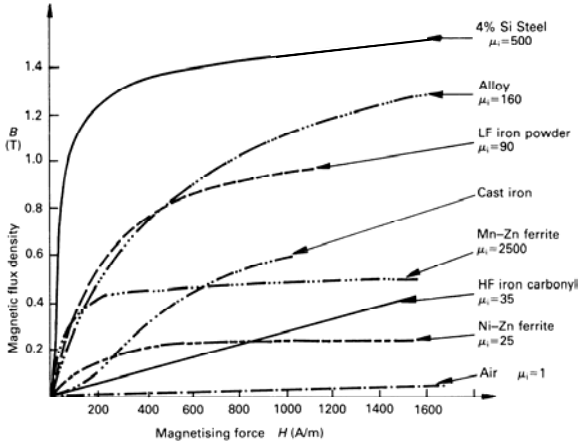


Figure 17.1. *Magnetisation curves for soft magnetic materials.*

17.3 Ferrite characteristics

The definitions and explanations given are applicable to soft magnetic materials in general and are illustrated specifically by reference to ferrite materials.
General mechanical and thermal properties of ferrites are given in appendix 17.6.

17.3.1 Dimensions and parameters

The effective magnetic dimensions are constant for a given core and are defined in table 17.2. These effective constants are based on the length ℓ and area A of the individual limbs comprising the complete core. These effective dimensions are used for magnetic component design, such as transformer core loss, which is given per unit effective volume, V_e.

Table 17.2. Core effective dimensions and parameters

core factor			
ℓ_e/A_e	c_1	$\Sigma\ell/A$	m^{-1}
effective area	A_e	$c_1/\Sigma\ell/A^2$	m^2
effective length	l_e	$A_e c_1$	m
effective volume	V_e	$\ell_e A_e$	m^3
core permeance	c	μ_o/c_1	H

From the parameters in table 17.2, inductance is calculated from equation (17.6) as

$$L = \mu_i c N^2 \quad \text{(H)} \tag{17.7}$$

17.3.2 Permeability

Figure 17.1 shows that a non-linear relationship exists between B and H for magnetic materials, and is characterised by the dimensionless parameter μ_r - the relative permeability - according to $B = \mu_o \mu_r H$ (where $\mu_o = 4\pi\times10^{-7}$ H/m). Figure 17.2 shows a detailed B-H magnetising curve for a ferrite material along with its hysteresis loop. The case of an air core magnetic circuit, for which $\mu_r = 1$, is also shown.
Figure 17.2 illustrates various definitions for μ_r based on

$$\mu_r = \frac{1}{\mu_o}\frac{B}{H} \tag{17.8}$$

17.3.2i - Initial permeability, μ_i

The initial permeability, which is dependant on temperature and frequency, is the permeability at weak field strengths at $H = 0$ and ΔH tends to zero, that is

$$\mu_i = \left[\frac{1}{\mu_o}\frac{\Delta B}{\Delta H}\right]_{H=0,\,\Delta H\to 0} \tag{17.9}$$

17.3.2ii - Amplitude permeability, μ_a and maximum permeability, $\hat{\mu}$

The amplitude permeability applies to large magnitude sinusoids, with no dc field applied, and is the ratio of the sinusoid peak B and H

$$\mu_a = \left[\frac{1}{\mu_o}\frac{\hat{B}}{\hat{H}}\right]_{H=0} \tag{17.10}$$

$\hat{\mu}$ is the maximum μ_a obtainable for any H, that is, $\hat{\mu}$ = max [μ_a] for all values of H. The variation of amplitude permeability with magnetising force or flux density is shown in figure 17.3. Because of the non-linear nature of the B-H curve loop, the amplitude permeability is highly dependant of the applied field strength magnitude.

This figure 17.3 is representative of a ferrite material suitable for a wide range of power electronic applications. More technical data for this material is presented in Appendix 17.7 and in the figures that follow.

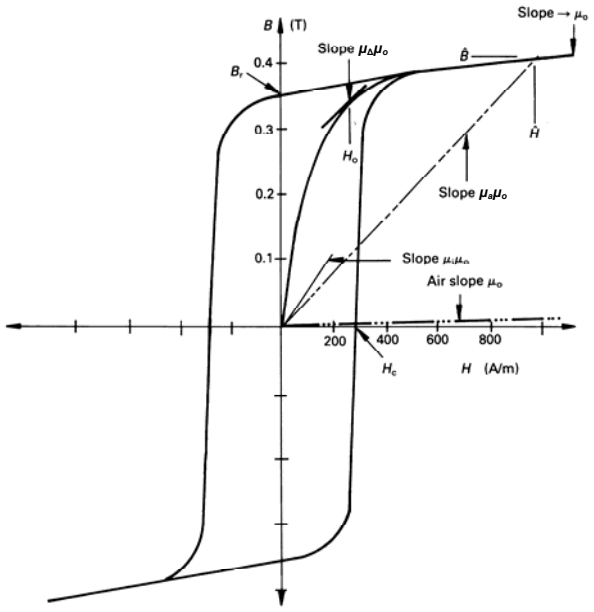


Figure 17.2. *Hysteresis loop illustrating permeability definitions, remanence B_r, and coercive force H_c.*

17.3.2iii - Reversible or incremental permeability, μ_{rev}, μ_Δ

When a core is magnetised with a polarising dc offset field upon which a small ac field is superimposed, the ac *H* field produces a small lancet-shape hysteresis loop which reduces to a straight line as the ac *H* field is reduced. The slope of this line, shown in figure 17.2, is called the incremental or reversible permeability

$$\mu_\Delta = \frac{1}{\mu_o} \lim_{\Delta H \to 0} \left[\frac{\Delta B}{\Delta H} \right]_{H\ =\ \text{constant}} \qquad (17.11)$$

The incremental permeability, μ_Δ is a function of the dc magnetic bias, as shown in figure 17.4. It is usually a maximum when no dc field is present, while for a toroid it is identical with the initial permeability, μ_i. With increased current, μ_Δ, hence inductance, decreases.

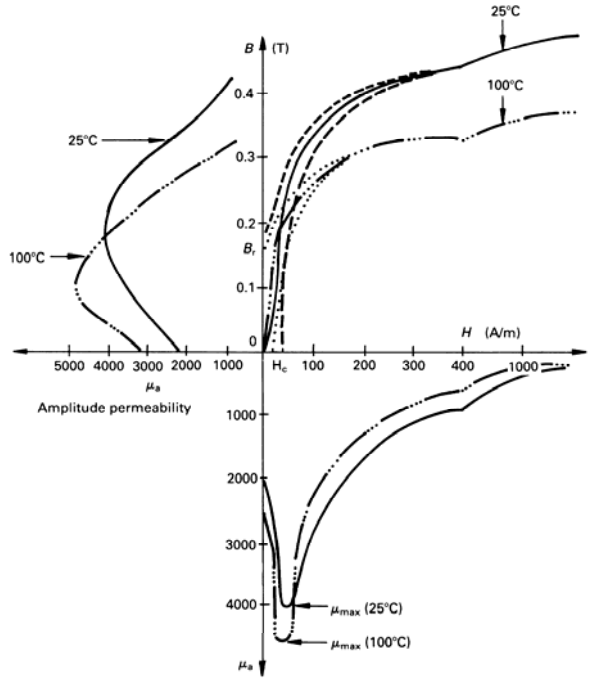


Figure 17.3. *Temperature dependence of flux density and permeability, μ_a.*

17.3.2iv - Effective permeability, μ_e

The inductance of a coil with a gapped core of effective permeability μ_e is given by

$$L = \frac{\mu_o \mu_e N^2}{\sum \ell / A} = \mu_e c N^2 = \mu_e L_o = A_L N^2 \qquad \text{(H)} \tag{17.12}$$

hence

$$\mu_e = L / cN^2 = L / L_o \tag{17.13}$$

where L_o is the coil inductance if the core is removed, whence the permeability drops. The term A_L is the inductance factor and is equal to $\mu_e c$. Conversely

$$N = \alpha \sqrt{L} \tag{17.14}$$

where $\alpha = 1/\sqrt{A_L}$ and is termed the turns factor.

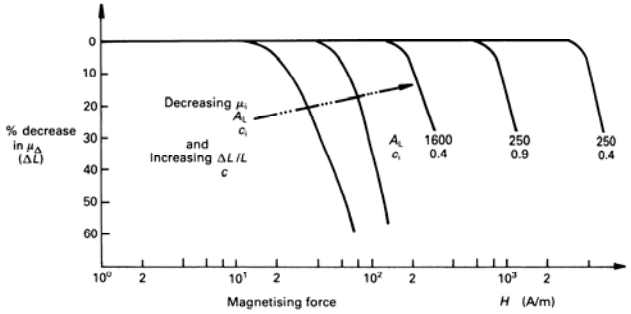


Figure 17.4. *Variation of permeability with field strength.*

If the air gap, ε, is small compared with the core of length, l_e, such that $\varepsilon << \ell_e$, the effective permeability approximates to

$$\frac{1}{\mu_e} = \frac{1}{\mu} + \frac{\varepsilon}{l_e} \tag{17.15}$$

The introduction of an air gap is equivalent to connecting two inductors in parallel: one without an air gap, μL_o; the other also without a gap but having an inductance $(l_e/\varepsilon)\, L_o$. The effective permeability of a gapped core at low flux levels is specified by the initial permeability, μ_i, and is given by

$$\frac{1}{\mu_e} = \frac{1}{\mu_i} + \frac{\varepsilon}{l_e} \tag{17.16}$$

The effective permeability for high flux densities is expressed in terms of the amplitude permeability, μ_a, that is

$$\frac{1}{\mu_e} = \frac{1}{\mu_a} + \frac{\varepsilon}{l_e} \tag{17.17}$$

That is

$$\mu_e = \frac{\mu_a}{1 + \frac{\varepsilon\, \mu_a}{\ell_e}} \tag{17.18}$$

A fringing factor, ε/β, must be introduced for significant gap widths, to account for the effective increase in permeability due to the fringing flux effect.

17.3.2v - Complex permeability, $\overline{\mu}$

Because of core losses, a coil can be represented by

- a series L_s - R_s circuit for an inductor
- a parallel R_p // L_p circuit for a transformer.

Core losses are modelled by the inclusion of resistance and the associated losses can be accounted for by considering the coil permeability as a complex variable, $\overline{\mu}$. For the inductor series equivalent circuit

$$Z = R_s + j\omega L_s = j\omega \overline{\mu} c N^2 \qquad (\Omega) \tag{17.19}$$

such that

$$\begin{aligned} \overline{\mu} &= \mu_s' - j\mu_s'' \\ &= \frac{L_s}{cN^2} - j\frac{R_s}{\omega c N^2} \end{aligned} \tag{17.20}$$

while for the transformer parallel equivalent circuit

$$\frac{1}{Z} = \frac{1}{R_p} + \frac{1}{j\omega L_p} \qquad \text{(S)} \tag{17.21}$$

such that

$$\begin{aligned} \frac{1}{\overline{\mu}} &= \frac{1}{\mu_p'} - \frac{1}{j\mu_p''} \\ &= \frac{1}{L_p / cN^2} - \frac{1}{jR_p / \omega c N^2} \end{aligned} \tag{17.22}$$

Since the parallel and series circuits are equivalent

$$\frac{\mu_s''}{\mu_s'} = \frac{\mu_p'}{\mu_p''} = \tan\delta \tag{17.23}$$

where tan δ is the core loss factor

$$\tan\delta = \frac{R_s}{\omega L_s} = \frac{\omega L_p}{R_p} = \frac{1}{Q} \qquad (17.24)$$

The complex permeability components are related according to

$$\mu_p' = \mu_s' \left(1 + \tan^2\delta\right)$$
$$\mu_p'' = \mu_s'' \left(1 + 1/\tan^2\delta\right) \qquad (17.25)$$

For low losses, namely at low frequencies, $\tan^2\delta \rightarrow 0$ in equation (17.25), whence $\mu_p' = \mu_s'$, while at high losses, at high frequencies, $\mu_p'' = \mu_s''$ since $\tan^2\delta \rightarrow \infty$ in equation (17.25). Complex permeability characteristics are shown in figure 17.5. The cut-off frequency, f_c is defined as the frequency at which the permeability is half the initial permeability, μ_s', at low frequency. At 25°C, f_c for Mn-Zn materials is approximated by $f_c \approx 4000/\mu_i$ (MHz), for μ_i at low frequency.
The complex permeability components are measured at low flux densities. Mn-Zn ferrites applicable to power application usually have high permeability, low resistivity, and a high dielectric constant. In such cases, the complex permeability is highly dependent on the core dimensions, as shown in figure 17.5, which characterises stacked toroids. Because of the associated large volume, volume resonance occurs where eddy currents dominate losses.

17.3.3 Coercive force and remanence

The coercive force H_c is the field strength at which the hysteresis loop cuts the H-axis as shown in figures 17.2 and 17.3. It is representative of the static hysteresis loss of the material. The point where the hysteresis loop intersects the B-axis is called the remanence, B_r. Where a core is operated with a magnetic field strength bias, for example, as with an inductor carrying dc current, the value of flux density is reduced to B_s - B_r for calculations. The area within the hysteresis loop represents core hysteresis loss, in Joules per unit volume.

17.3.4 Core losses

17.3.4i - Core losses at low H

At low magnetising forces, the total losses, represented by R_t, can be separated into three core components (magnetic components, R_m) and a copper turns component, R_{Cu}. The components are

- frequency dependent eddy currents, R_F
- frequency dependent hysteresis, R_h
- magnetic drag, remanence loss, or residual loss, R_r
- copper winding loss including both dc and ac components, R_{Cu}, where

$$R_t = R_m + R_{Cu}$$
$$R_t = R_F + R_h + R_r + R_{Cu} \quad (\Omega) \qquad (17.26)$$

The coil is represented by the series R_t - L_s circuit where L_s is the lossless self-inductance. Empirical formulae, called *Jordan formulae* can be used to calculated R_t at low magnetic forces.

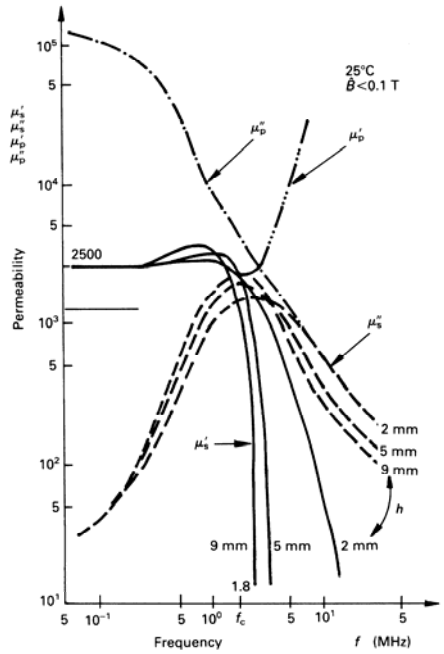


Figure 17.5. *Influence of core size (h) on the frequency characteristics of the complex permeability for a toroid.*

The series coil model impedance is given by

$$Z = R_t + j\omega L_s \qquad (\Omega) \tag{17.27}$$

whence

$$\begin{aligned}\tan\delta_t &= R_m + R_{Cu} \Big/ \omega L_s = R_t \Big/ \omega L_s \\ &= \frac{R_F}{\omega L_s} + \frac{R_h}{\omega L_s} + \frac{R_r}{\omega L_s} + \frac{R_{Cu}}{\omega L_s} \\ &= \tan\delta_F + \tan\delta_h + \tan\delta_r + \tan\delta_{Cu}\end{aligned} \tag{17.28}$$

where $\tan\ \delta_t$ is the loss factor for the coil. The reciprocal of the loss factor is the inductor quality factor, namely

$$Q = \frac{1}{\tan\delta_t} = \frac{\omega L_s}{R_t} \tag{17.29}$$

The copper loss is usually excluded so as to characterise the core material specifically, whence

$$Q = \frac{1}{\tan\delta} = \frac{\mu_s''}{\mu_s'} = \frac{\mu_p'}{\mu_p''} \tag{17.30}$$

An alternative core loss factor is $\tan\delta\ /\mu$ or $1/\mu Q$, which is generally characterised only for high frequency Ni-Zn ferrites. The loss factor for a gapped core, $\tan\ \delta_e$, can be found by multiplying the core loss factor by the gapped core effective permeability, μ_e, that is

$$\tan\delta_e = \frac{\tan\delta}{\mu}\mu_e \tag{17.31}$$

17.3.4ii - Core losses at high *H*

1 **- Ferrites**

Core losses, P_V, with high flux densities in Mn-Zn ferrites are applicable to power electronic application. Empirical formulae are not practical, and ferrites used for choke and transformer cores are provided with experimentally characterised total core loss per unit volume data, as indicated in figure 17.6. This loss, for a power Mn-Zn ferrite, is given as a function of frequency, temperature, and flux density.

For a specified and limited operating range, core losses in figure 17.6 can be approximated by

$$\begin{aligned}P_V\,(25°\text{C}) &= P_h + P_F \\ &= 5.8\times10^{-5}\times f^{1.2}\times\hat{B}^{2.11} + \ 3.32\times10^{-7}\times f^2\times\hat{B}^2 \qquad (\text{mW/cm}^3)\end{aligned} \tag{17.32}$$

where f is in kHz for 10 kHz $\le f \le$ 500 kHz

and $\hat{B}$ is the peak flux density in mT for 50mT $\le \hat{B} \le$ 250mT.

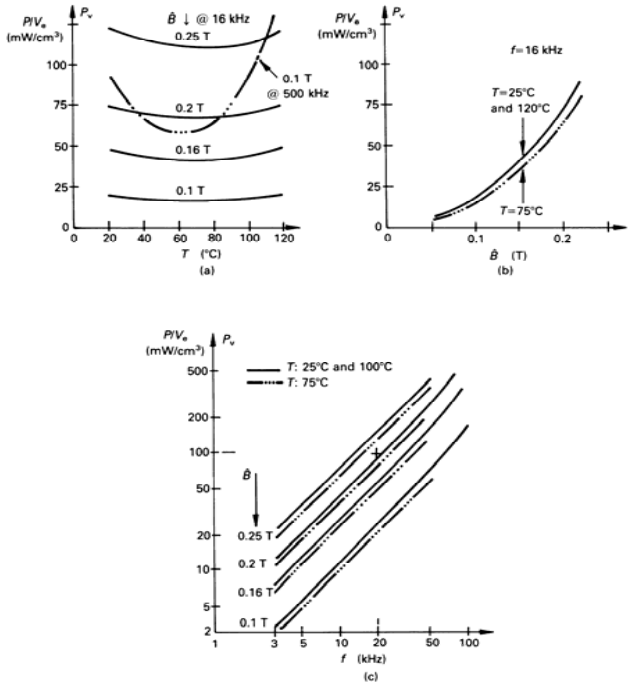


Figure 17.6. *Total per unit volume core losses as a function of: (a) core temperature, T; (b) maximum flux density, $\hat{B}$; and (c) frequency, f.*

Temperature dependence is modelled according to

$$P_V = \kappa \times P_V\,(25°\text{C}) \tag{17.33}$$

where

$$\kappa = 1.48\times10^{-4}\times T^2 - 21.2\times10^{-3}\times T\ + 1.44$$

for f < 200 kHz and $\hat{B} \ge$ 100 mT

$$\kappa = 1.2\times10^{-4}\times T^2 - 17.8\times10^{-3}\times T + 1.38$$

for $f \geq 200$ kHz and $\hat{B} \leq 100$ mT

where temperature T is with respect of 0°C.

The per unit volume loss $P_V(T)$ is applicable to a square wave. For a half wave sine, power losses are reduced by 0.7-0.8 while for a full wave rectified sine wave, losses are increased by 1.8 to 2.2.

2 - Laminated silicon steel

Hysteresis and eddy current losses for silicon steel can be calculated by using well established, classical empirical formulae.

(a) Hysteresis loss

Steinmetz equation predicts hysteresis loss according to

$$P_h = \lambda_h \hat{B}^n f V_e \quad \text{(W)} \qquad (17.34)$$

where λ_h and n are characteristics of the core

$n = 1.7$

$\lambda_h = 500$ for 4 per cent silicon steel

$= 3000$ for cast iron

(b) Eddy current loss

Eddy current loss is predicted by

$$P_F = \frac{\left(\pi \hat{B} f t\right)^2}{6\rho} V_e \quad \text{(W)} \qquad (17.35)$$

where t is the thickness of the lamination, parallel to the flux path, and ρ is the magnetic material resistivity. This formula illustrates why high resistivity ferrites have low eddy current loss, even at high frequencies. In the case of iron, the addition of 3-4 per cent silicon increases the resistivity by about four times, reducing both eddy current and hysteresis losses.

Eddy currents produce magnetic fields in the magnetic material, by Lenz's law, which will oppose the applied field. This reduces the flux density in the core centre such that most of the flux is confined to a thin layer or skin near the surface, termed *skin effect*.

Within a magnetic material with an ac flux, the flux density distribution is given by

$$B(x) = B(0)e^{\frac{-x}{\delta}} \quad \text{(T)} \qquad (17.36)$$

where x is the distance from the surface

$\delta = \sqrt{(\rho/\mu_o \pi f)}$ is called the skin depth.

Laminations should be less than $\frac{1}{2}\delta$ thick. The skin effect in metals can be used to absorb radiated and conducted rfi by using laminations $>2\delta$ thick.

A similar effect occurs within conductors carrying ac current, where the current is minimal at the conductor centre. The current density, J, is given by

$$J(x) = J(0)e^{\frac{-x}{\delta}} \quad (\text{A/m}^3) \qquad (17.37)$$

Below 20-50 kHz and above a few megahertz, solid wire is preferred. In between these frequencies, stranded wire, *Litz wire* (after *Litzendraht*) is preferred; decreasing from 0.07 mm to 0.03 mm in strand diameter as the frequency increases and interwinding capacitance dominates. Copper foil can also be employed.

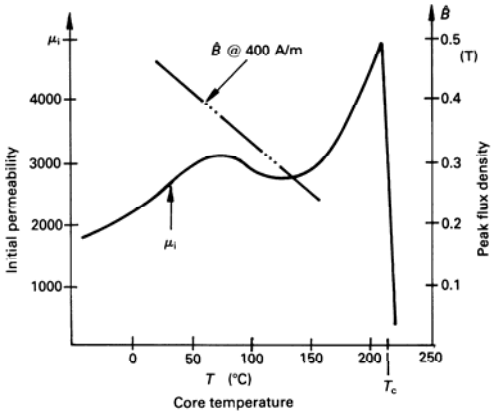


Figure 17.7. *Permeability, μ_i, and maximum density, $\hat{B}$, as a function of core temperature, T.*

17.3.5 Temperature effects on core characteristics

Generally ferrites have poor characteristic temperature stability. At higher temperatures, at the *Curie point*, cores lose their magnetic properties, abruptly. The phenomenon is reversible and below the Curie temperature, T_c, the material becomes magnetic again. The temperature effect on initial permeability in figure 17.7 illustrates the sudden loss of permeability at 212°C. Generally Curie temperature is inversely proportional to the initial permeability, μ_i. For most ferrites the initial permeability increases with temperature, and reaches a maximum just below the Curie temperature, as shown in figure 17.7.

Other ferrite parameters are also affected by temperature. Increased temperature decreases flux density and hysteresis loss as shown in figures 17.3 and 17.7. The effects of temperature on total core loss per unit volume are shown in figure 17.6a.

17.3.6 Inductance stability

Three factors affect inductance stability:

- *Parameter effects*
- *Time effects*
- *Temperature effects*

17.3.6i *- Parameter effects*

From the differential of equation (17.12)

$$\frac{dL}{L} = \frac{d\mu_e}{\mu_e} \tag{17.38}$$

while differentiating equation (17.16) yields

$$\frac{d\mu_e}{\mu_e^2} = \frac{d\mu_i}{\mu_i^2} \tag{17.39}$$

Substituting equation (17.39) into equation (17.38) gives

$$\frac{dL}{L} = \frac{d\mu_i}{\mu_i^2}\frac{A_L}{c} \tag{17.40}$$

The factor $d\mu_i / \mu_i^2$ is constant for a given temperature, hence any change in inductance is due to variations in A_L and c. Thus in order to increase the stability of an inductor in a given material with $\varepsilon << \ell_e$, it is necessary to increase the magnetic circuit air gap (to reduce the inductance factor A_L) or to select a bigger core (to increase the core permeance factor c).

17.3.6ii *- Time effects*

Initial permeability of a ferrite decreases with time under constant operating conditions, including constant temperature. A *disaccommodation factor*, *df*, independent of effective permeability, is introduced, which characterises the material such that the change in inductance is defined by

$$\frac{dL}{L} = df\ \mu_e \log_{10}\frac{t_1}{t_o} \tag{17.41}$$

This expression is based on the fact that permeability is proportional to the logarithm of time. The *df* increases slightly with temperature. Generally the *df* decreases, as shown in table 17.3:

- as the initial permeability increases for a given resistivity
- as resistivity decreases.

Example 17.1: ***Inductance variation with time***

A pot ferrite core with an effective permeability of 100 (A_L = 250) and a disaccommodation factor $df < 35 \times 10^{-6}$ has been in satisfactory operation for five weeks after production. What is the expected inductance variation after 10 years?

Table 17.3. Factors affecting the disaccommodation factor

			ρ(Ω cm)		
			10^5	500	≈ 20
μ_i			11-250	800-2000	4000
T_c		°C	450-300	250-170	145
df	× 10^{-6}		50-10	20-2	3

Solution

From equation (17.41)

$$\frac{dL}{L} = df\ \mu_e \log_{10}\frac{t_1}{t_o} < 35\times10^{-6}\times100\times\log\frac{520\text{ weeks}}{5\text{ weeks}}$$

that is, $dL < 0.7$ per cent can be expected.

♣

17.3.6iii *- Temperature effects*

Figure 17.7 shows that between +5°C and +55°C the permeability μ_i variation as a function temperature is approximately linear for this ferrite. The temperature coefficient α is given by

$$\alpha = \frac{1}{\mu_{i1}}\frac{\Delta\mu_i}{\Delta T} \qquad (\text{K}^{-1}) \tag{17.42}$$

where $\Delta\mu_i = \mu_{i2} - \mu_{i1}$ is the initial permeability variation over the temperature range $\Delta T = T_2 - T_1$.

In a magnetic circuit with an air gap and effective permeability, μ_e, the temperature coefficient of the core is reduced according to

$$\alpha_e = \alpha\frac{\mu_e}{\mu_i} = \alpha_F\mu_e \qquad (\text{K}^{-1}) \tag{17.43}$$

The term $\alpha_F = \alpha_i / \mu_i$ is called the relative temperature coefficient. The relative inductance change between two temperatures can be determined by

$$\frac{dL}{L} = \alpha_F\mu_e\Delta T \tag{17.44}$$

For effective permeability $\mu_e < 80$, the temperature coefficient $\alpha_e = \mu_e\alpha_F$ should be increased by 10 to 30 × 10^6/K to account for the temperature influence of the winding.

Example 17.2: ***Temperature effect on inductance***

The gapped pot core in example 17.1 is specified by a relative temperature coefficient of 1 x 10^6/K. What is the expected inductance variation over the temperature range 25-55°C?

Solution
From example 17.1

$$\mu_e = \frac{A_L}{c} = \frac{250}{2.5} = 100$$
$$\Delta T = 55 - 25 = 30°\text{C}$$

From equation (17.44)

$$\frac{dL}{L} = \alpha_F \mu_e \Delta T$$
$$= 1\times10^{-6}\times100\times30$$
$$= 0.3 \text{ per cent inductance variation}$$

♣

17.3.7 Stored energy in inductors

The energy stored in the magnetic field is given by

$$E = ½BH\breve{V}_e \quad \text{(J)} \tag{17.45}$$

where $\breve{V}_e$ is the effective minimum volume. It can be shown that the stored magnetic energy is equivalent to the stored electrical energy, whence

$$E = ½BH\breve{V}_e = ½Li^2 \quad \text{(J)} \tag{17.46}$$

For un-gapped cores, like a toroid, the ferrite effective volume, V_e, is equal to the minimum effective volume, $\breve{V}_e$. Inductors meeting this requirement may make the core size excessive. However the introduction of an air gap, ε, can reduce the core size significantly, since a significant amount of the energy can be stored in the gap volume. The minimum effective volume is now larger than the ferrite core effective volume, and is given by

$$\begin{aligned}\breve{V}_e &= V_e + A_e\mu_i\varepsilon \\ &= A_e\left(l_e + \mu_i\varepsilon\right) \quad (\text{m}^3)\end{aligned} \tag{17.47}$$

Figure 17.8 shows modified *B-H* characteristics for inductors with an air gap. The line curve o-b represents the core without an air gap, which results in the largest inductance. The energy stored in the core for a flux BA_e, in the linear portion of the curve, is the area of the shaded triangle 0-a-b, as defined by equation (17.45). When an air gap is introduced, the effective permeability falls as shown by the slope of line o-c. The figure

shows that as the air gap increases, the inductance decreases. It can be shown that the stored energy in the air gap and core is represented by the shaded area o-a-c, for a given flux, BA_e. It can be seen that the energy stored in the gap of length ε, although its length is much smaller than the core length, ℓ_c, its stored energy is much greater than that stored in the core.

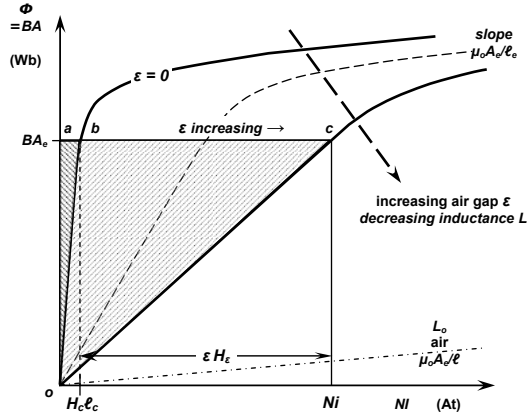


Figure 17.8. *Effects of air gap on inductance and stored energy.*

The total energy stored, E_T, in the magnetic circuit comprises the energy stored in the air gap, E_ε, plus the energy stored in the magnetic core material, E_{core}. It can be shown that these two energies are equal to the areas of the shaded triangles, o-b-c and o-a-b, respectively in figure 17.8. That is

$$\begin{aligned}E_T &= E_{core} + E_\varepsilon \\ &= ½B_cH_cV_c + ½B_\varepsilon H_\varepsilon V_\varepsilon\end{aligned} \tag{17.48}$$

If leakage is neglected, then the air gap flux is the same as the core flux. If fringing is neglected then the area of the core at the air gap is the same as the area of gap. Then

$$\begin{aligned}E_T &= ½BH_cA_e\ell_c + ½BH_\varepsilon A_e\,\varepsilon \\ &= ½BA_e\left(H_c\ell_c + H_\varepsilon\,\varepsilon\right)\end{aligned} \tag{17.49}$$

For a gapped core, as shown in figure 17.11

$$Ni = H_c\ell_c + H_\varepsilon\,\varepsilon \tag{17.50}$$

Therefore, on substituting equation (17.50) into equation (17.49) gives the total stored energy as

$$E_T = \tfrac{1}{2}BA_e\left(H_c\ell_c + H_\varepsilon\varepsilon\right) = \tfrac{1}{2}BA_e\left(Ni\right) \tag{17.51}$$

which is equal to the area of the shaded triangle o-a-b.
The inductance L is given by equation (17.4), that is

$$L = \frac{N\phi}{i} \tag{17.52}$$

Substitution of equation (17.50) for the current i gives

$$L = \frac{N^2\phi}{H_c\ell_c + H_\varepsilon\varepsilon} = \frac{N^2A_e\mu_o}{\frac{\ell_c}{\mu_r}+\varepsilon} = \frac{N^2A_e\mu_e}{\ell_c+\varepsilon}\left[\frac{\left(\ell_c+\varepsilon\right)\mu_r}{\ell_c+\mu_r\varepsilon}\right] = \frac{N^2A_e\mu_o\mu_e}{\ell_{total}} \tag{17.53}$$

where $\ell_{total} = \ell_c + \varepsilon$ and

$$\mu_e = \frac{\left(\ell_c+\varepsilon\right)\mu_r}{\ell_c+\mu_r\varepsilon} \tag{17.54}$$

Making the usual assumption that the length of the core is much greater than the length of the air gap, $\ell_c >> \varepsilon$, yields equation (17.18) for the effective permeability.

17.4 Ferrite inductor and choke design, when carrying dc current

Air gaps in magnetic circuits are introduced in order to reduce the influence of a superimposed dc current, manufacturing dispersion or to improve parameter stability. Saturable inductors for a semiconductor switch turn-on snubber normally do not employ an air gap, in order to reduce the stored energy, which may be subsequently dissipated, and to minimise the magnetising current magnitude.
Empirical equations have been derived for cylindrical inductors with a cylindrical core, which give an inductor with a large air gap. Design equations and examples are given in appendix 17.7.

17.4.1 Linear inductors and chokes

The introduction of an air gap reduces the effective permeability, μ_e such that the coil inductance is given by the equation (17.12)

$$L = \mu_e cN^2 = \mu_e L_o = A_L N^2 \qquad \text{(H)} \tag{17.55}$$

Figure 17.9a shows the variation of the effective permeability, μ_e at both low flux levels and without a dc bias, as a function of the relative air gap, ε/ℓ_e as specified by equation (17.17). As the air gap and the superimposed dc field are varied, the incremental permeability, μ_Δ varies as shown in figure 17.9b. This figure indicates how inductance varies with dc bias current (H).

Figure 17.9 does not specify the optimum inductor design since for a given inductance and dc current the optimum air gap and number of turns are not specified. The minimum number of turns and air gap requirements can be determined by means of the Hanna curves in figure 17.10.

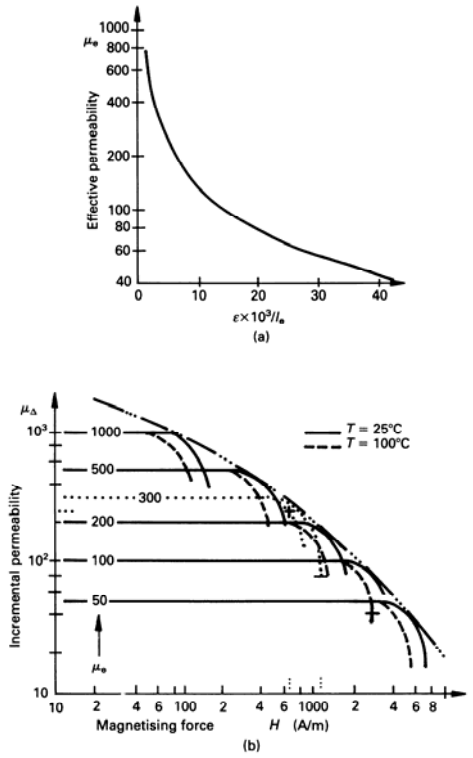


Figure 17.9. *Permeability as a function of:*
(a) air gap, ε and (b) superimposed dc field and air gap.

This figure shows experimental families of curves of per unit core energy against magnetomotive force per unit length, for different air gaps. The resultant curves are ferrite type dependent and dimensionally independent. Hanna curves therefore allow the determination of minimum turns N and air gap ε, from the required inductance L and dc current I.

Three distinct energy levels are shown in the Hanna curves in figure 17.10.

i. At low dc currents (H) the per unit energy increases linearly with H. This region corresponds to the horizontal regions in figure 17.9b, where

$$L = \mu_\Delta c N^2 \quad \text{(H)} \tag{17.56}$$

and as H varies, μ_Δ is constant.

ii. In the mid energy region, the per unit energy can decrease with increased H. The incremental permeability decreases, causing L to decrease at a greater rate than the increase in the dc current squared, I^2. This region is characterised by the fall off in μ_Δ, hence inductance, as H increases as shown in figure 17.9b.

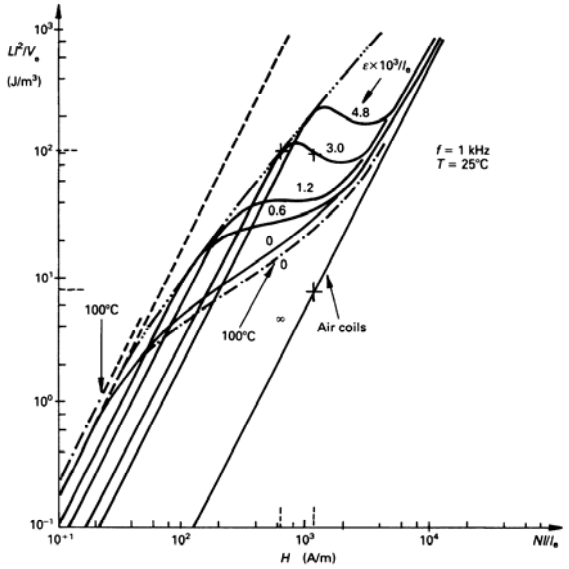


Figure 17.10. *Hanna curves, showing trajectories for different air gaps.*

iii. At high dc currents, the core material saturates, and μ_Δ tends to unity. An air core inductance results, where

$$L = L_o = c N^2 \tag{17.57}$$

Example 17.3: ***Inductor design with Hanna curves***

A 20 μH, 10 A choke is required for a forward converter. The inductance must be constant for unidirectional currents to 10 A. An available E-core pair has the following effective parameters

$\ell_e = 0.11$ m, $A_e = 175 \times 10^{-6}$ m^2, $V_e = 19.3 \times 10^{-6}$ m^3

and

$\mu_i = 2500$ @ 25°C and 3000 @ 100°C (from figure 17.7)

i. At a core temperature of 25°C, determine the required air gap and turns. Allow a 5 per cent decrease in inductance at rated conditions.

ii. Estimate the inductance at 20A dc.

iii. Calculate the inductance at 10A and 20A dc, both at 100°C.

Solution

i. Evaluate $\dfrac{LI^2}{V_e} = \dfrac{20\times10^{-6}\times10^2}{19.3\times10^{-6}} = 104$ J/m^3

From figure 17.10, restricted to the constant-L region, 104 J/m^3 corresponds to

(a) $\varepsilon/\ell_e = 3 \times 10^{-3}$

whence $\varepsilon = 3 \times 10^{-3} \times \ell_e = 3 \times 10^{-3} \times 0.11$

The required total air gap is 0.33 mm

(b) $H = 650$A/m

Since $H = NI/\ell_e$

$N = H\ell_e/I = 650 \times 0.11/10 = 7.15$ turns

Use 7 turns and a 0.33 mm total air gap.

ii. At 20 A, 25°C

$H = NI/\ell_e = 7 \times 20/0.11 = 1270$A/m

Two alternative design approaches may be used to estimate the inductance.

(a) The effective permeability, μ_e, before saturation can be evaluated from equation (17.17)

$$\frac{1}{\mu_e} = \frac{1}{\mu_a} + \frac{\varepsilon}{l_e} = \frac{1}{2500} + 3\times10^{-3}$$

that is

$$\mu_e \approx 300$$

From figure 17.9b, for μ_e = 300 it can be seen that the incremental permeability μ_Δ is constant, as required to 650A/m, then μ_Δ decrease as

saturation commences. At H = 1270A/m, μ_Δ has fallen to 75, from 300. The incremental inductance at 20 A is about ¼ of 20μH, namely 5.0μH.
(b) Alternatively, a simpler approach uses only figure 17.10. H = 1270A/m projects 100 J/m^3. Solving $100.0 = L_{20A} I^2/V_e$ with I = 20A yields L_{20A} = 5μH.

iii. The effective permeability at 100°C is

$$\frac{1}{\mu_e} = \frac{1}{\mu_i} + \frac{\varepsilon}{l_e} = \frac{1}{3000} + 3\times10^{-3}$$

that is

$$\mu_e \approx 300$$

It is seen that, although the initial permeability varies significantly with temperature, here the effective permeability is dominated by the air gap, and hence is essentially temperature independent. Figure 17.9b, with H = 640A/m, projects μ_Δ = 220 at 100°C. Using $L\ \alpha\ \mu_\Delta$, the inductance falls to about 15μH at 100°C, 10 A.
At 20A, 100°C, the effects of saturation are highly significant, and figure 17.9b indicates that the incremental permeability is low. The best approximation is to use the air coil curve in figure 17.10. Hence H = 1270A/m projects 9J/m^3. At 20A, 100°C, an inductance of at least 0.43μH can be expected.

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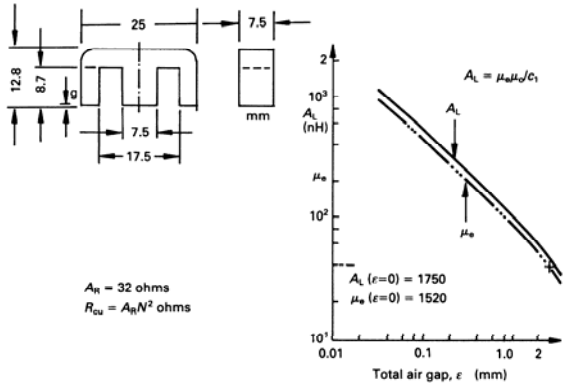

Figure 17.11. *Characteristics of a pair of gapped E-cores. Core dimensional parameters are given in table 17.5.*

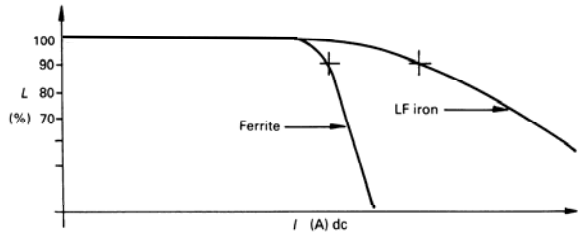

Figure 17.12. *Comparison of inductance characteristics illustrating how inductance falls off faster with ferrite cores than with iron cores, at higher currents.*

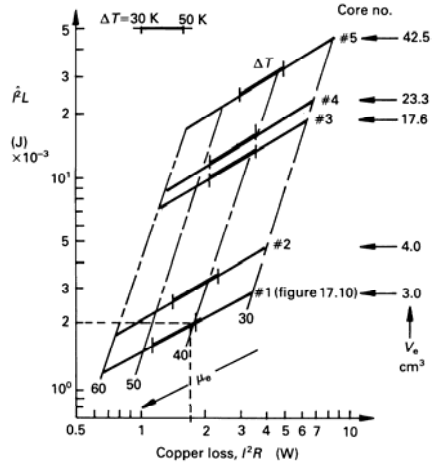

Figure 17.13. *Magnetic biasing capability $\hat{I}^2L$, copper loss I^2R, effective permeability μ_e and over-temperature ΔT of five different effective volume V_e ferrite cores.*

Figure 17.4 shows how μ_Δ and hence the inductance, falls off as H, and hence the current, increases for ferrite core materials. The larger the air gap, and hence the lower A_L, the higher H before inductance rolls off. Inductance rolls off faster, the wider the air gap, hence the higher the magnetic field strength, H. The decrease in effective permeability, μ_e and inductance factor, A_L, with increase of air gap, ε, is shown in figure 17.11 for two E-cores.

Figure 17.12 shows typical curves for the decrease in μ_Δ, hence inductance, with increased H, hence current, for both ferrites and alloy or iron powder cores. Because power ferrites have a squarer B-H curve than powder cores, the inductance of ferrites falls off faster. By increasing the core volume, the fall off rate of inductance can be reduced. Depending on core loss for a given volume, a powder core may be more effective than a ferrite; and would have better utilisation of the copper window area. The design approach previously considered in example 17.3 in fact neglects the optimisation of core size and copper I^2R loss.

17.4.Ii - Core temperature and size considerations

Figure 17.13 relates stored energy, LI^2, and copper loss, I^2R, for different cores of the same ferrite type. Once L and I are fixed, figure 17.13 can be used to determine the optimum core size and air gap. This figure shows that with increasing air gap (decreasing μ_e), the magnetic biasing capability increases along with the associated copper loss, I^2R. A flowchart is shown in figure 17.14, which outlines the design procedure to be used in conjunction with figure 17.13.

Example 17.4: ***Inductor design including copper loss***

With the aid of figure 17.13, design a 20 μH, 10 A dc inductor, calculating the copper loss and temperature rise for the predicted optimum air gap and number of turns.

Solution

Following the procedure outline in the flowchart of figure 17.14

Evaluating $LI^2 = 20 \times 10^{-6} \times 10^2$

$= 2$ mJ

From the nomogram in figure 17.13 use core no. 1, which must have $\mu_e = 40$ and $I^2R = 1.8$ W. This copper loss will produce a 50°C temperature rise above ambient on the core surface, beneath the winding. The thick bars in figure 17.13 represent a 30-50°C temperature increase range.

The core type no. 1 has A_L and μ_e values versus total air gap, and effective parameters as shown in figure 17.11 and table 17.5. For $\mu_e = 40$, $A_L = 45$ nH, a total air gap of 2.7 mm is required.

From $L = A_L N^2$

$N = \sqrt{20 \times 10^3/45}$

$= 21$ turns

For $I = 10$ A dc, $I^2R_{Cu} = 1.8$ W, then $R_{Cu} = 18$ mΩ. The copper turns diameter is determined from

$$R_{Cu} = N \ell_N R_L \quad (\Omega) \tag{17.58}$$

where R_L is the resistance per meter, Ω/m

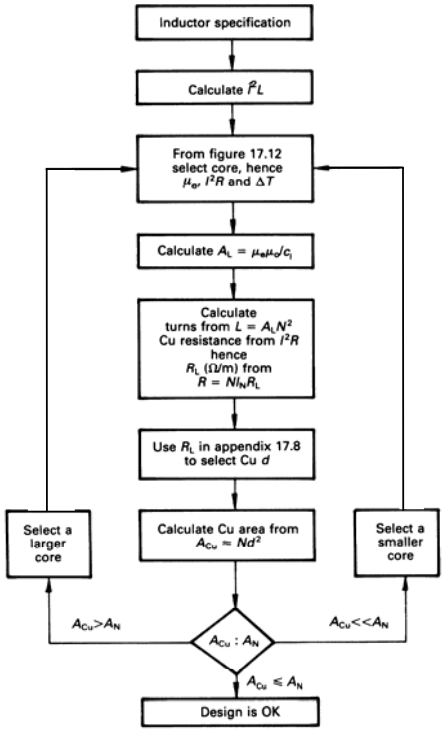

Figure 17.14. *Linear inductor design flowchart.*

ℓ_N is the mean turn length which is either provided for a given former or may be estimated from core physical dimensions. From table 17.5:

$$\ell_N = 52 \text{ mm}$$
$$R_L = R_{Cu} / N\,\ell_N$$
$$= 18 \times 10^{-3}/21 \times 52 \times 10^{-3} = 0.165\ \Omega/\text{m}$$

Using standard wire tables, appendix 17.9 for 0.165 Ω/m, use 28 SWG (0.154 Ω/m) which has a diameter of 0.36 mm and 0.434 when enamelled. The resultant copper current density is 77 A/mm^2. In many applications 4 A/mm^2 is used for finer gauge wires up to 20 A/mm^2 for heavier gauge wires. These current densities represent about 5 per cent of the fusing current , I_{fusing} which is approximated by

$$I_{\text{fusing}} = 80\,d^{1.5}$$

The diameter d is in mm.

This recommendation is unrealistic and inductor and transformer design is based on temperature rise.

The approximate copper area is

$$A_{Cu} = N \times d^2$$
$$= 21 \times 0.434^2$$
$$= 3.88\text{mm}^2$$

From table 17.5, the useful winding cross-section is

$$A_N = 56 \text{ mm}^2$$

Only 8 per cent of the former window area is filled, hence the actual copper length is overestimated and I^2R loss, hence temperature rise, will be less than the allowed 1.8 W and 50°C respectively.

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Comparing the design of examples 17.3 and 17.4, it will be seen that the same design specification can be fulfilled with the latter core of 20 per cent the volume of the former. The bigger core required an 0.33 mm air gap to give μ_e = 300, while the smaller core required a larger gap of2.7 mm to give μ_e = 40. Both cores are of the same ferrite type. The incremental inductance of the smaller core will fall off with current, much faster than with the larger core, as indicated by figure 17.4.

For a switch mode power supply application, the rms value of current is less than the peak current at which the inductance is specified. The copper loss, hence temperature rise, is then based on an rms current basis.

17.4.2 Saturable inductors

Saturable inductors are used in series with semiconductor switching devices in order to delay the rise of current, thereby reducing switch turn-on stress and loss. In the case of a power transistor, the collector current is delayed until the collector voltage has fallen (see 8.3.4). For thyristor devices, the delay time allows the gate activated cathode area

to spread hence giving a high initial di/dt capability. In each case the inductor supports the supply voltage, then after a finite time saturates to a very low inductance, supporting little voltage, and does not influence the switch current.

Ferrites are ideal as the core of a saturable inductor because of their low magnetic field strength, H_s, at the onset of flux density saturation, B_s. While the inductor supports voltage, v, the flux density increases, moving up the B-H curve according to Faraday's law

$$v = NA_e \frac{dB}{dt} \tag{17.59}$$

A low magnetising current results. After a finite time the flux density reaches the knee of the B-H curve (B_s, H_s), the core saturates and the incremental permeability falls from an initially high value to that of air, μ_Δ = 1. The high initial permeability, hence high inductance, limits the current. The time t_s, for the core to saturate should be equal to the switch voltage fall time, t_{fi}. The low saturation inductance allows the switch current rapidly to build up to a level dictated by the load.

If the switch voltage fall is assumed linear then the inductor voltage is $V_s\,t/t_{fi}$. The time t_s, taken to reach saturation (B_s, H_s) from integration of Faraday's law is

$$t_s = \frac{2NA_eB_s}{V_s} \tag{17.60}$$

for $t_s \le t_{fi}$.

The flux density, hence H, and current increase quadratically with time. At saturation the magnetising current magnitude (hence switch current) is

$$I_s = \frac{H_s\ell_e}{N} \quad \left(= \frac{2B_sH_sV_e}{t_sV_s}\right) \quad \text{(A)} \tag{17.61}$$

which should be small compared with the switch on-state current magnitude.

The inductance before saturation is given by

$$L = A_L N^2 \quad \text{(H)} \tag{17.62}$$

and falls to

$$L_{sat} = c\,N^2 \quad \text{(H)} \tag{17.63}$$

after saturation, when leakage and lead length will, in practice, dominate inductance.

The energy stored in the core and subsequently dissipated at core reset is given by

$$E = \tfrac{1}{2}B_sH_sV_e \quad \left(= \tfrac{1}{4}I_sV_st_s\right)$$
$$= \tfrac{1}{2}B_sH_sA_e\ell_e \quad \text{(J)} \tag{17.64}$$

which must be minimised.

Table 17.4 summarises saturable inductor requirements based on equations (17.60) to (17.64).

Table 17.4. Design requirement of a saturable inductor

	Material dependent		Shape dependent		
	H_s	B_s	A_e	ℓ_e	N
Minimise E $E = ½ B_s H_s A_e \ell_e$	low	low	low	low	×
Maximise t_s $t_s = 2NA_eB_s/V_{sec}$	×	high	high	×	high
Minimise I_s $I_s = H_s\ell_e/N$	low	×	×	low	high
Maximise L $L_a = N^2A_eB_s/\ell_eH_s$	low	high	high	low	high
Requirement	low H_s (high μ_r)	-	-	short ℓ_e	high N
Compromise	-	high B_s if H_s is low	high A_e if ℓ_e is short		

17.4.3 Saturable inductor design

Figure 17.15 shows a saturable inductor design flowchart. The design starting point is the type of ferrite. The desired ferrite should have minimal high frequency loss, associated with a small magnetic field strength, H_s, at saturation. These features would be associated with ferrites having a low coercive force, H_c and remanence, B_r. The ferrite material shown in figure 17.3 fulfils these requirements with

$$H_c = 12\text{A/m} \qquad B_r = 0.18\text{T}$$
$$H_s = 200\text{A/m} \qquad B_s = 0.4\text{T}$$

Ferrites with lower magnetic field strengths are available but tend to be limited in size.
A material with a high initial permeability is one indicator of a suitable ferrite type.
The next considerations are core shape and effective core parameters such as effective length, ℓ_e and area, A_e. The core should have a short effective length, ℓ_e. The area and length are traded in maintaining sufficient copper window area, A_N.
A core shape without an air gap will produce the highest possible initial, hence effective, permeability. Example 17.5, which follows, illustrates that a toroid core offers a good solution.
A high number of turns, N, is desirable, and preferred to an increase in area, A_e.
Design should be based on the maximum core temperature. An increase in temperature decreases H_s at a faster rate than B_s, as shown in figure 17.3. From equation (17.60), many turns are required which, in combination with decreased H_s, advantageously decrease the magnetising current, I_s.

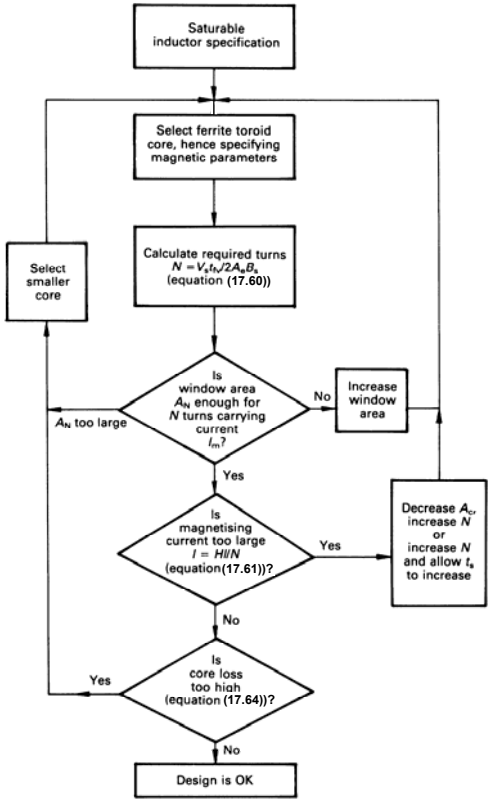

Figure 17.15. *Saturable inductor design flowchart.*

Table 17.5. Pot, toroid, and E-core design data.
Applicable magnetic data are presented in appendix 17.8

		Physical dimensions (mm)		
		Pot core d_o = 25 h = 16	Toroid d_o = 39 d_i = 24.77 h = 6.61	E-core (pair) See figure 17.11
V_e	cm^3	3.63	3.86	3.02
A_e	cm^2	0.999	0.398	0.525
ℓ_e	cm	3.64	9.71	5.75
c_1	cm^1	3.64	24.4	10.9
A_{min}	cm^2	0.95	0.398	0.45
A_L	nH	4300	1540	(ε = 0)1750
μ_e		1245	(μi) 3000	(ε = 0)1500
c	nH	3.45	0.51	1.15
A_N	cm^2	0.357 (0.266)	4.75	0.56
ℓ_N	cm	5.3 (5.35)	7.6	5.2
S_A	cm^2	18.4	48.7/58	20
Weight	g	23.4	19.3	2 × 8

Example 17.5: ***Saturable inductor design***

A pot, toroid and E-shaped core of the same Mn-Zn ferrite as characterised in appendix 17.8, and of similar volume, have characteristics and parameters as shown in table 17.5, with H_s = 200At/m.
Design a saturable inductor for each core shape, for a switch having a 200 ns linear voltage fall time and operating on a 600 V dc supply rail.
The core is to saturate when the switch voltage reaches saturation (0 V).
Estimate the core power removed at reset if the switching frequency is 20 kHz.

Solution

		Pot	Toroid	E-cores (ε = 0)
From equation (17.60) $N = V_s t_{fv}/2A_eB_s = 1.875/A_e$ A_e is in cm^2		2	5	4
From equation (17.61) $I_s = H_s\ell_e/N = 2\ell_e/N$ ℓ_e is in cm	(A)	3.64	3.85	2.83
From equation (17.62) $L = A_L N^2 \times 10^{-3}$	(μH)	17.2	38.5	28.0
From equation (17.63) $L_{sat} = cN^2$	(nH)	13.8	12.75	18.4
From equation (17.64) $P_d = V_e \times 8 \times 10^{-1}$ V_e is in cm^3	(W)	2.90	3.09	2.42

Based on the available copper window area, A_N and number of turns, the cores would be applicable to switching currents in excess of 100 A. Smaller cores could be used for lower current levels, although A_N tends to dictate the required core.
From equation (17.64), the power dissipated at 20 kHz is given by $P_d = \frac{1}{2}B_s H_s V_e f_s$.

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17.5 Power ferrite transformer design

A Mn-Zn ferrite material is almost exclusively used for power transformer cores, and has been optimised by manufacturers for a wide frequency range. Specific core shapes have also been developed to cover a wide power range. In the case of voltage transformers, at 20 kHz and below 100 W, pot cores are used, or when low flux leakage and low emi are important. Such cores can be processed on automatic machines which wind and assemble the whole unit. At powers above 100 W, E-E and E-I cores are extensively used.
The usable power range of the pot core is increased by increasing frequency and at 500 kHz no alternative exists, because of the low leakage flux, low self-capacitance, and good shielding offered by pot cores.

17.5.1 Ferrite voltage transformer design

To simplify ferrite core selection, manufacturers provide the characteristic curves given in figure 17.16 which show the power that can be transmitted by various core shapes. Specifically, these curves show power for the modes of operation commonly used in switch-mode power supplies; such as push-pull, forward, and flyback, as considered in

chapter 15, versus the core plus copper volume.
A formal transformer design approach based on copper and core losses is shown in the flowchart in figure 17.17 and is applicable to all smps types.

Stage 1 and stage 2

The transformer, primary and secondary voltages, currents, and powers, hence efficiency, must be specified or determined. Other requirements are frequency, ambient temperature, and allowable temperature rise at the core to copper interface. The final specification should include

$$\begin{matrix} V_p & V_s \\ I_p & I_s \\ P_p & P_s \end{matrix} \qquad \eta, f, T_a, \Delta T$$

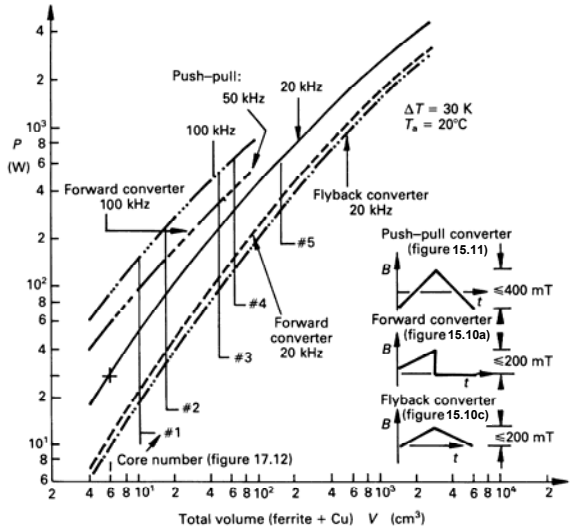


Figure 17.16. *Transmissible power, P, versus volume (ferrite plus copper), V, of transformers with ferrite Mn-Zn cores.*

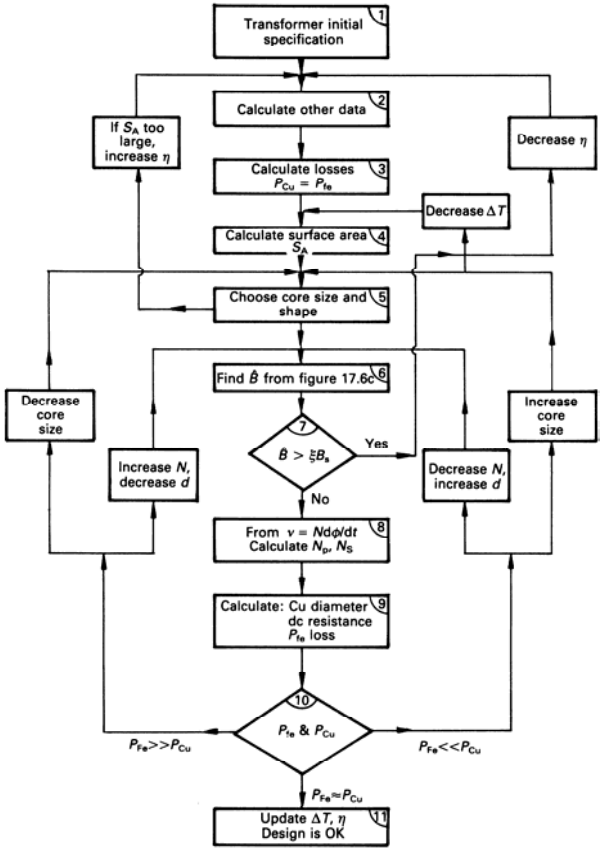


Figure 17.17. *Voltage transformer design flowchart.*

Stage 3

The difference between input power and output power is the total power loss, P_L, which comprises copper and core losses. The maximum efficiency is obtained when the copper loss equals the core loss.

Stage 4

The total power loss, P_L, ambient temperature, T_a, and temperature rise, ΔT, specify the exposed copper and core surface area requirements, S_A, according to (see equation 5.4)

$$S_A = \frac{P_L}{\Delta T\, S_d} \quad (\text{m}^2) \tag{17.65}$$

where S_d is a surface dissipation factor.
Empirical equations are commonly provided for S_d. Based on the assumption that thermal stability is reached half by convection and half by radiation, the surface area requirement can be approximated by

$$S_A = 145 \times \left[\frac{1000}{T_a + 273}\right]^{2.06} \frac{P_L}{\Delta T^{1.22}} \quad (\text{cm}^2) \tag{17.66}$$

Stage 5

A core with the minimum surface area, S_A, is selected using manufacturers' data, ensuring that the ferrite type is appropriate to the operating frequency and that the core shape meets any engineering, cost or other special requirements. The manufacturers' data required include the effective dimensional parameters, copper winding area, A_N, and average turn length, ℓ_N.
Some manufacturers provide transformer design data for each core. This specific data can be employed, rather than the general procedure that follows.

Stage 6

Using the core volume, V_e, and core loss $P_c = ½P_L$, whence core loss per cm^3, $P_w = P_c / V_e$ the maximum allowable operating flux density, B_{op}, for the specified frequency can be determined from the power loss curves in figure 17.6c.

Stage 7

The rated saturation flux density, B_s, cannot safely be used. For a transformer using both quadrants of the *B-H* characteristics, for example, a push-pull smps transformer

$$B_{op} \le 0.8\, B_s$$

while for a core used with a flux bias

$$B_{op} \le 0.4\, B_s$$

These limits avoid operational saturation of the core in one direction. If the working flux density, B_{op}, is too high, either

- reduce the efficiency and go to stage 1/2, or
- reduce the allowable temperature rise and go to stage 4.

Stage 8

The required number of primary turns, N_p, can be calculated from Faraday's law, which yields

$$N_p = \frac{V_p}{k\, B_{op} A_e f} \tag{17.67}$$

where $k = 4$ for a square-wave voltage
$k = 4.44$ for a sine wave.
If $B_{op} > 100$ mT, the effective area, A_e, in equation (17.67) is replaced by the core minimum area section, A_{min}, since that portion experiences the highest flux density.
The number of secondary turns is calculated according to

$$N_s = N_p \frac{V_s}{V_p} \tag{17.68}$$

Stage 9

The winding diameter, d_p, for the allotted primary for a window area, A_p, is calculated according to

$$d_p = 2\sqrt{\frac{A_p k_w}{\pi N_p}} \quad (\text{m}) \tag{17.69}$$

where k_w is a winding space factor, 0.7, which accounts for insulation, winding taps, shielding, air space, etc. A similar expression for the diameter of the secondary, d_p, involves the number of secondary turns, N_s, and allotted area, A_N. The total winding area $A_p + A_s$ must not exceed the available winding area, A_N.
Standard copper wire tables, appendix 17.9, provide the resistance per meter, R_L, for the calculated diameters. From equation (17.58), the dc resistance of the primary can be calculated according to

$$R_p = N_p\, \ell_N\, R_{Lp} \quad (\Omega) \tag{17.70}$$

Similarly for calculating the secondary dc resistance, R_s. The total copper loss can be calculated as

$$P_{Cu} = I_p^2 R_p + I_s^2 R_s \quad (\text{W}) \tag{17.71}$$

Stage 10

The core loss, P_c, and the copper loss, P_{Cu} are compared. If

(i) $P_{Cu} > P_c$

Either decrease the number of turns and increase the copper diameter. This will reduce the copper loss and increase B_{op}, and hence P_c. Recalculate from stage 6.

or select a larger core, which will increase the copper window area, A_N, hence increasing the allowable wire diameter. Recalculate from stage 5.

(ii) $P_{Cu} < P_c$

Either increase the number of turns which will reduce d, B_{op} hence P_c, and then recalculate from stage 6.

or select a smaller core, which will require d to be reduced, and then recalculate from stage 5.

Proceed if $P_{Cu} \approx P_c$.

Stage 11

Update the value of total losses, P_L, and hence recalculate the power requirements and resultant efficiency.

Calculate the actual core temperature rise from equation (17.66), rearranged

$$\Delta T = 59\left(\frac{1000}{T_a + 273}\right)^{1.69} \times \left(\frac{P_L}{S_A}\right)^{0.82} \quad \text{(K)} \qquad (17.72)$$

where S_A is the heat dissipating area in cm^2 of the chosen core.

Example 17.6: ***Ferrite voltage transformer design***

Consider the design requirements for the split rail push-pull smps shown in figure 15.7b, which is specified as follows

$v_o = 5$ V — $V_{sec} = 48$ V ± 15 per cent
$i_o = 4$A — $f = 20$kHz
$P_o = 20$ W — $T_a = 25$°C, $\Delta T \leq 35$ K
$\eta = 97$ per cent

Solution

Based on the flowchart in figure 17.17 and the eleven stages outlined, design proceeds as follows.

Stage 1

The transformer must deliver 20 W plus losses associated with an output inductor and the pair of Schottky diodes in the output rectifier. The inductor loss is estimated at 4 per cent of the output power, 0.8 W, while the diode total loss is 0.6 V × 4 A = 2.4 W. Thus the transformer output power requirement P_s is 23.2 W (20 W + 0.8 W + 2.4 W). With a 97 per cent efficiency, the transformer input power, P_p, requirement is 1/97 per cent of 23.2 W, namely 23.9 W. The nominal primary current, I_p, at the nominal voltage, 24 V is

$$I_p = \frac{P_p}{V_{pn}} = \frac{23.9\text{W}}{24\text{V}} = 1\text{A}$$

The maximum primary voltage, V_p, is $1.15 \times V_{sec}/2 = 27.6$ V, since the 48 V supply is centre tapped and has + 15 per cent regulation. For worst case, it is assumed that the voltage drop across the switches is zero.

The transformer secondary voltage, V_{sec}, for the centre tapped full-wave rectifier circuit, must be large enough to overcome the diode voltage drop, V_d, and must allow for averaging of the nominal low duty cycle switching action of the primary input power. With pwm regulation each input switch operates for approximately 25 per cent of the time, thus

$$\tfrac{1}{2}V_s = 2 \times (V_o + V_d)$$

where the ½ indicates that half of the secondary winding conducts at any one time, while the 2 approximates the pwm average on-time. Thus for $V_d = 0.6$ V and $V_o = 5$ V

$$V_{sec} = 4 \times (5 + 0.6) = 22.4\text{V}$$

Stage 2

Extracting the transformer data from stage 1

$I_p = 1$A — $I_s = 4$A
$V_p = 27.6$ V — $V_{sec} = 22.4$ V
$P_p = 23.9$ W — $P_s = 23.2$ W

$\eta = 97$ per cent, $f = 20$ kHz, $T_a = 25$°C, $\Delta T = 35$ K

Stage 3

The total transformer power loss, P_L, from $P_s - P_p$, is 0.7 W.
Thus $P_c = P_{Cu} = 0.7/2 = 0.35$ W each.

Stage 4

The surface area requirement is calculated from equation (17.66)

$$S_A = 145 \times \left[\frac{1000}{25 + 273}\right]^{2.06} \times \frac{0.7\text{W}}{35^{1.22}}$$

$= 16.1$ cm^2 for a 35 K temperature rise

Stage 5

Either the pot core in table 17.5 or the pair of E-cores in figure 17.11 have sufficient surface area, 18.4 and 20 cm^2 respectively, and both are of a ferrite material suitable for a 10 to 100 kHz operating frequency range.
At the low power level of 23.9 W, choose the pot core.

Stage 6

Using the technical data given in table 17.5, the core loss per unit volume is calculated

$$P_w = \frac{P}{V_e} = \frac{0.35\text{W}}{3.63\text{V}} = 0.096\text{W/cm}^3$$

Stage 7

From figure 17.6c, an operating flux density of 0.21 T at 20 kHz will result in the allowable core loss of 0.1 W/cm^3. For push-pull operation the maximum allowable flux density is about 80 per cent of B_s, that is, 80 per cent of 0.48 T, namely 0.38 T. Since 0.21 T < 0.38 T, a working flux density of 0.21 T is acceptable.

Stage 8

Since the operating flux density is greater than 100 mT, the pot core minimum area, A_{min} (0.95 cm^2) is used for calculations, rather than the effective area, A_e (0.999 cm^2). From equation (17.67), the required number of primary turns is given by

$$N_p = \frac{27.6\text{V}}{4 \times 0.21\text{T} \times 0.95 \times 10^{-4} \times 20 \times 10^3} = 17.3$$

Use 17 turns.
The number of secondary turns is given by equation (17.68)

$$N_s = \frac{22.4}{24} \times 17 = 15.7$$

where the nominal primary voltage is used. Use 16 turns per secondary winding.

Stage 9

From table 17.5, the available winding area, A_N, is either 0.357 cm^2 for a one-section former or 0.266 cm^2 for a two-section former. Since the primary and secondary voltages are relatively low, insulation and isolation present few difficulties, hence single enamel copper wire and a single section former can be used. The available copper area, 0.357 cm^2, is divided between the primary and secondary so as to provide a uniform current density within the winding area. The primary to secondary currents are in the ratio of 1:4, hence 0.285 cm^2 is allocated to the secondary (approximately 80 per cent) while 0.072 cm^2 is allocated to the primary winding. The copper wire diameter is calculated using equation (17.69)

$$d_p = 2\sqrt{\frac{A_p k_w}{\pi N_p}} = 2 \times \sqrt{\frac{0.072 \times 10^{-4} \times 0.8}{17\pi}} = 0.66 \text{ mm}$$

$$d_s = 2\sqrt{\frac{A_s k_w}{\pi N_s}} = 2 \times \sqrt{\frac{0.285 \times 10^{-4} \times 0.8}{32\pi}} = 0.95 \text{ mm}$$

Using the standard wire tables in appendix 17.9 and equation (17.58) to calculate the winding resistance

		Primary	Secondary	
d_{Cu}	mm	0.6	0.95	bare Cu
d_{Cu+en}	mm	0.65	1.017	single enamel
R_L	Ω/m	0.06098	0.02432	
R_{Cu}	Ω	0.055	0.0206/16 turns	

The total power copper loss is given by equation (17.71)

$$\begin{aligned} P_{Cu} &= I_p^2 R_p + I_s^2 R_s \\ &= 1^2 \times 0.055 + 4^2 \times 0.0206 \\ &= 0.055 + 0.330 = 0.385\text{W} \end{aligned}$$

Stage 10

The core loss is 0.35 W while the copper loss is only slightly higher at 0.385 W. No iterative change is necessary. The updated total loss, P_{L_s} is 0.735 W.

Stage 11

The secondary power requirement remains 23.2 W while the primary requirement has increased to 23.94 W. The efficiency has been reduced to

$$\eta = \frac{23.3\text{W}}{23.94\text{W}} \equiv 96.9\,\text{per cent}$$

from 97 per cent.
Using the actual core surface area, 18.4 cm^2, and loss, 0.735 W, the core temperature rise can be calculated from equation (17.72)

$$\begin{aligned} \Delta T &= 59 \times \left(\frac{1000}{25+273}\right)^{1.69} \times \left(\frac{0.735}{18.4}\right)^{0.82} \\ &= 32.6 \text{ K} \end{aligned}$$

which is less than the 35 K allowable temperature rise limit.

♣

The transformer design of example 17.6 could be based on figure 17.16. The volume of the core plus copper, for the pot core in table 17.5, can be estimated from its diameter of 25 mm and height of 16 mm. This yields a total volume of 6 cm^3, after allowing for slots.
Using figure 17.16, for a total volume of 6 cm^3, at 20 kHz, for a push-pull converter, 28 watts can be transmitted in a 20°C ambient, producing a 30 K core temperature rise. These results and those from example 17.6 compare as follows.

		Figure 17.16	Example 17.6
P	W	28	23.2
ΔT	K	30	32.6
T_a	°C	20	25

All other operating conditions are identical. Any design discrepancy is accounted for by

- the higher ambient temperature
- the poorer winding slot utilisation.

A centre tapped secondary represents poorer slot utilisation compared with using a single winding, which requires four rectifying diodes since, because of a limited core size range, the same core would be used independent of the type of secondary circuit. A centred tapped secondary would result in the cost saving associated with two fewer Schottky diodes.

17.5.2 Ferrite current transformer

By adding a secondary winding, a linear inductor can be converted into a voltage transformer, while a saturable inductor can be converted into a current transformer. The linear inductor and voltage transformer (of E-I laminations) are characterised by a core with an air gap (inherent in transformers which use E-I laminations). The saturable inductor and current transformer generally use an un-gapped core.
A given transformer can operate either in the voltage mode or the current mode depending on the load impedance. The voltage transformer operates into a high impedance circuit, while the current transformer requires a low impedance load. Current and voltage transformer action both cease at core saturation.
The equivalent circuit model is identical for each transformer mode, and the same basic equations apply in each case. A saturable inductor is required to support a large voltage for a short period, while a current transformer supports a low voltage for a long period. In each case, the primary voltage-time product is equal for a given core and primary turns.

17.5.3 Current transformer design requirements

The basic requirement of a current transformer is a fixed ratio between the primary and secondary currents according to

$$I_p N_p = I_s N_s \quad \text{(A)} \tag{17.73}$$

Ideally the load impedance is zero, hence zero secondary voltage is developed. Practically, a secondary voltage, V_{sec}, exists, whence from Faraday's law

$$V_{sec} = N_s \frac{d\phi}{dt} = N_s A \frac{dB}{dt}$$

For a constant secondary voltage (a short circuit), the core flux density increases linearly, effectively moving up the *B-H* curve and reaches saturation, B_s, in time

$$t_s = \frac{N_s B_s A_e}{V_{sec}} \quad \text{(s)} \tag{17.74}$$

Where a core is operated with an *H* offset, for example, as with an inductor carrying dc current or a unidirectional current transformer, the maximum value of flux density used for analysis should be reduced because of remanence to B_s - B_r, whence

$$t_s = \frac{N_s \left(B_s - B_r\right) A_e}{V_{sec}} \quad \text{(s)} \tag{17.75}$$

The lower the secondary voltage, V_{sec}, the longer the time before saturation, at which point current transformer action ceases. The core is fully reset by a negative voltage of sufficient duration for which the voltage-time product must equal that of the on-period. Fortunately, a high reset voltage can generally be employed, which produces a very short reset time. Effectively, the reset voltage forces the magnetising current, or stored energy, to zero.
This magnetising current, $\check{I}_P$ should be minimal and its presence modifies the ideal ampere-turns balance according to

$$\left(I_p - \check{I}_p\right) N_p = N_s I_s \quad \text{(A)} \tag{17.76}$$

where the magnetising current $\check{I}_P$ is given by

$$\check{I}_p = \frac{H \ell_e}{N_p} \quad \text{(A)} \tag{17.77}$$

The initial magnetising current is zero, and increases linearly with time. Low leakage core shapes should be used to minimise leakage inductance.
At all times the primary voltage is related to the secondary voltage according to

$$V_p = V_{sec}\left(\frac{N_p}{N_s}\right) = \frac{V_{sec}}{n_T} \quad \text{(V)} \tag{17.78}$$

The requirements of the previous equations are summarised in table 17.6 where the maximum on-time is $\hat{t}_{on}$, while the time available for reset is the minimum off-time

$\check{t}_{off}$. The secondary reset voltage V_{sr} requirement and associated dissipated energy W are also included. This table summarises key current transformer requirements as follows

- use a core material which has a low magnetising force, H_s, at saturation
- use a core with a short effective core path length, ℓ_e
- use a high number of turns, N_p and N_s, for a given turns ratio
- operate the transformer with a low secondary voltage, V_{sec}.

Table 17.6. Current transformer requirements showing how magnetic parameter variation affects the electrical characteristics

		core parameters					*circuit parameters*		
		H_s	B_s	B_r	A_e	ℓ_e	N_s	N_p	V_{sec}
Equation (17.75) $t_s = \frac{N_s (B_s - B_r) A_e}{V_{sec}}$	s	*	↑	↓	↑	*	↑	↑	↓
Equation (17.77) $\check{I}_p = \frac{H_s \ell_e}{N_p} \frac{\hat{t}_{on}}{\check{t}_{off}}$	A	↓	*	*	*	↓	*	↑	*
Equation (17.81) $V_{sr} = V_p \frac{\hat{t}_{on}}{\check{t}_{off}}$	V	*	*	*	*	*	*	*	↓
$W = H_s (B_s - B_r) A_e \ell_e \left(\frac{\hat{t}_{on}}{t_s} \right)^2$	J	↓	↓	*	↓	↓	*	*	*
Design requirements		low H_s	—	low B_r	—	low ℓ_e	high turns		low V_{sec}

17.6.5 Current transformer design procedure

Figure 17.18 shows a flowchart design procedure for a current transformer and the design stages are as follows.

Stage 1/stage 2

The current transformer primary and secondary currents, hence turns ratio $n_T = N_s/N_p$, must be specified with the limits on duty cycle times, $\hat{t}_{on}$ and $\check{t}_{off}$. The expected secondary voltage V_{sec} must be specified.

Stage 3

Select a ferrite toroid with an internal diameter, hence window area A_N, sufficient to accommodate the required minimum turns, $n_T + 1$. The copper turns current ratings must be taken into account. The core specifies the effective parameters ℓ_e, A_e, and V_e. The ferrite type specifies B_s, B_r, and H_s.

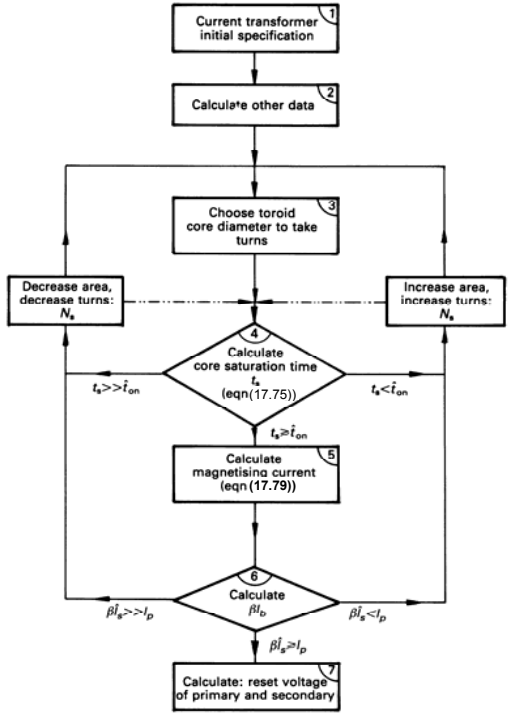


Figure 17.18. *Current transformer design flowchart.*

Stage 4

Calculate the time t_s, before the core saturates from equation (17.75). This time must be greater than the required maximum output current pulse width, $\hat{t}_{on}$.

(i) If $\hat{t}_{on} > t_s$
Either increase the number of turns, using a core with a larger window A_N if necessary.
or increase the core area, A_e, which can be achieved with the same window area, A_N, either with a core of increased thickness or by using two stacked cores.
go to stage 3

(ii) If $t_s >> \hat{t}_{on}$
Either decrease the number of turns which may allow a smaller core size.
or decrease the core cross-sectional area.
go to stage 3

(iii) If $t_s \geqq \hat{t}_{on}$, proceed to stage 5

Stage 5

Calculate the magnetising current at $\hat{t}_{on}$

$$\breve{I}_p = \frac{H_s \ell_e \hat{t}_{on}}{N_p t_s} \quad \text{(A)} \tag{17.79}$$

Stage 6

Calculate the secondary current, taking the magnetising current $\breve{I}_p$ into account

$$\hat{I}_s = \frac{\hat{I}_p - \breve{I}_p}{n_T} \tag{17.80}$$

Is $\beta = \hat{I}_p / I_s$ sufficiently large?
(i) If $\hat{I}_p > \beta \hat{I}_s$
Either decrease the magnetising current by increasing core area.
or increase the turns ratio, n_T.
go to stage 3
(ii) If $\hat{I}_p \ll \beta \hat{I}_s$
Either decrease the turns ratio, n_T.
or decrease the core cross-sectional area.
go to stage 3
(iii) If $\hat{I}_p \lesssim \beta \hat{I}_s$, proceed to stage 7

Stage 7

Calculate the core reset voltage

$$V_{sr} = V_p \frac{\hat{t}_{on}}{\breve{t}_{off}} \quad \text{(V)} \tag{17.81}$$

Calculate the reflected primary on-state voltage

$$e_p = \frac{V_{sr} N_p}{N_s} \tag{17.82}$$

Example 17.7: ***Ferrite current transformer design***

A current transformer primary is used in the collector of a bipolar junction transistor switching circuit and the secondary is used to provide transistor base current as shown in figure 17.20. The maximum collector current is 100 A and the transistor has a gain of 8 at 100 A, in saturation.
The transistor maximum on-time is 46 μs while the minimum off-time is 4 μs. Design a suitable current transformer using the toroid ferrite core, which has low flux leakage and is specified by the data in table 17.5 and appendix 17.7. Assume a core temperature of 25°C.

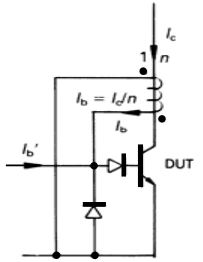


Figure 17.20. *Current transformer for bjt base drive.*

Solution

Based on the flowchart in figure 17.18 and the procedure previously outlined:

Stage 1

The required turns ratio factor is $n_T = N_p/N_s = \beta = 8/1$. In allowing for the magnetising current component, choose $n_T = 15/2$.
The secondary winding voltage is the maximum transistor base to emitter voltage plus the maximum voltage drop across a series diode. Maximum voltage occurs at maximum current.

$$\begin{aligned} V_s &= V_{be_{sat}} + V_D \\ &= 1.2\text{V} + 1.2\text{V} \\ &= 2.4\text{ V} \end{aligned}$$

Stage 2

The current transformer requirements can be summarised as follows

$n_T = N_p/N_s = 15/2$ $\quad\quad$ $\hat{t}_{on} = 46\mu\text{s}$

$V_{sec} = 2.4\text{V}$ $\quad\quad$ $\check{t}_{off} = 4\mu\text{s}$

Stage 3

The ferrite toroid core specified in table 17.5, fulfils the following requirements

$B_s = 0.4$ T at $H_s = 200$ A/m
and $A = 0.398$ cm^2, $\ell_e = 9.71$cm

while the available window area, A_N, is 4.75 cm^2. This window must accommodate two conductor turns of 100 A (plus magnetising current) each and fifteen conductor turns of 12 A each.

Stage 4

The time, t_s, before core saturation is given by equation (17.75), and assuming $B_r = 0$

$$t_s = \frac{15\times0.4\times0.4\text{T}\times10^{-4}}{2.4\text{V}} = 100\ \mu\text{s}$$

Since $t_s > \hat{t}_{on}$, that is 100 μs > 46 μs, proceed to stage 5.

Stage 5

The maximum primary magnetising current, $\hat{I}_p$ is specified by equation (17.79)

$$\hat{I}_p = \frac{46}{100}\times\frac{200\times9.71\times10^{-2}}{2} = 4.47\text{A}$$

Stage 6

The 4.47 A of magnetising current detracts from the primary current available for current transformer action. The maximum available secondary current under worst-case conditions is given by equation (17.80)

$$\hat{I}_s = \frac{100\text{A} - 4.47\text{A}}{15/2} = 12.7\text{A}$$

The maximum allowable collector current is this base current, 12.7 A, multiplied by the transistor gain, 8, which yields 102 A. This is larger than the specified maximum collector current of 100 A, hence the design is correct.

Stage 7

In the on-state, the secondary voltage is 2.4V and the reflected primary voltage is 0.32V.
The maximum secondary voltage, V_{sr}, required to reset the core is given by equation (17.81)

$$V_{sr} = 2.4\text{V}\times\frac{46\mu\text{s}}{4\mu\text{s}} = 27.6\text{V}$$

The reflected primary voltage is 3.7 V.
The reset voltage is usually much larger and is clamped by a base circuit diode in avalanche. Therefore the core reset time will be shorter than 4 μs.
At currents much lower than 100 A, the secondary voltage is decreased, hence the magnetising current is reduced. This reduced magnetising current could consume the full collector current at collector currents of a few amperes. It is therefore necessary to add extra base current to compensate for this deficiency at low currents. The minimum secondary voltage, V_{sec}, specifies the extra requirement according to

$$I_b' = \frac{\check{V}_s}{\hat{V}_s}\times\frac{\hat{I}_p}{n_T} \qquad (17.83)$$

For $\check{V}_s = 1.2$ V, the extra base current requirement is

$$I_b' = \frac{1.2}{2.4}\times\frac{4.47}{7.5} = 300\text{mA}$$

This current can be delivered from an inductive circuit since zero extra current is initially required, and the requirement rises linearly to 300 mA in 46 μs.
A base start pulse of a few microseconds duration is required initially to turn the transistor on, whence collector current is established and current transformer action commences.

♣

17.6 Appendix: Soft ferrite general technical data

Tensile strength	20	N/mm^2
Resistance to compression	100	N/mm^2
Vickers hardness HV_{15}	8000	N/mm^2
Modulus of elasticity	150,000	N/mm^2
Breakage modulus	80-120	N/mm^2
Thermal conductivity	4 - 7× 10^{-3}	J/mm s K (W/mm/K)
Linear expansion coefficient	7-10×10^{-6}	/K
Specific heat	0.75	J/g K
Density	4 - 5	g/cm^3 (4 per cent Si, 7.63 g/cm^3)

Resistivity ρ	$\lambda_s = \frac{\Delta\ell^*}{\ell}$	$\varepsilon_r^{\P} / \rho^{\S}(pu)$				
Ω cm	×10^{-16}	10 kHz	100 kHz	1 MHz	100 MHz	300 MHz
10^5	-18	30/1	15/1	12/1	11/0.97	11/0.95
1	-1.5	140×10^3/1	50×10^3/0.95	30×10^3/0.65	-	-

* Magnetostriction, at saturation, contraction.
¶ Dielectric constant, $\varepsilon_r \rightarrow$ 10-20 at high frequency.
§ Resistivity normalised at low frequency.

17.7 Appendix: Technical data for a ferrite applicable to power applications

Symbol	Unit	Test condition	
μ_i		25°C	2500±20%
$\hat{B}$	T T	25°C 100°C	0.48 0.37
H_s	A/m	B_s = 0.4T, 25°C	200
H	A/m		1600
H_c/B_r	A/m /T	25°C 100°C	12/0.18 9.6/0.11
T_c	°C		>200
ρ	Ω cm		100
η_B^*	mT^{-1} × 10^{-6}	10 kHz	0.9
Density	g/cm^3		4.8
f_c	MHz	25°C	1.8

* - Maximum hysteresis coefficient
10 G (gauss) = 1 mT (milliTesla)
l0 e = 80A/m

17.8 Appendix: Cylindrical inductor design

Figures 17.19a and b show cross-sectional views of single-layer and multi-layer cylindrical inductors. The inductance of a single-layer cylindrical inductor is given by

$$L = \frac{\mu_{eff}(rN)^2}{228.6r + 254\ell} \quad (\mu H) \tag{17.84}$$

while for the multi-layer cylindrical inductor shown in figure 17.19b, inductance is given by

$$L = \frac{\mu_{eff}(rN)^2}{152.4r + 228.6\ell + 254b} \quad (\mu H) \tag{17.85}$$

Figure 17.19c shows a family of curves used to give the effective permeability from the former *l/d* ratio and the core material permeability. These curves are applicable to the single-layer inductor but are a fair approximation of the multi-layer inductor. The winding is assumed to be closely wound over 95 per cent of the core length.

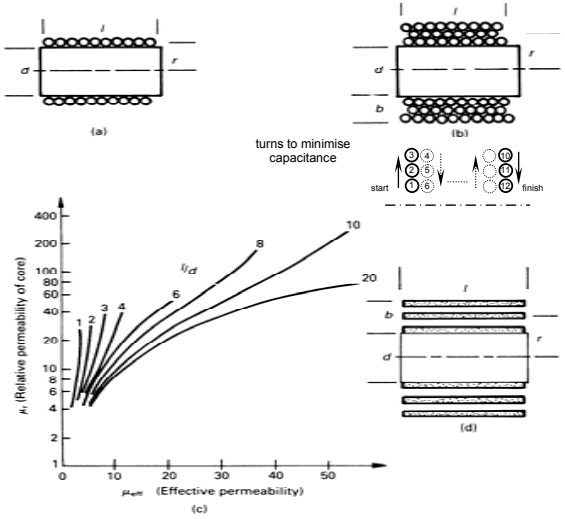


Figure 17.19. *Cylindrical inductors:*
(a) single-layer coil; (b) multi-layer coil; (c) effective permeability for different aspect ratios, lid; and (d) core strip wound air core inductor.

For inductance levels below 100 μH, an air core strip wound inductor as shown in figure 17.19d, has an inductance approximated by

$$L = \frac{r^2 N^2}{225r + 250\ell + 250b + 82.5\dfrac{lb}{r}\left(\dfrac{\ell + 2r}{\ell + 4r}\right)} \quad (\mu H) \qquad (17.86)$$

Inductor design using these equations may require an iterative solution. Always attempt to maximise the winding surface area ($S_A \approx \pi(d + 2b)\ell$) for better cooling.

Example 17.8: ***Wound strip air core inductor***

An air core inductance of 50 μH is made as a wound strip of copper, 40 mm wide and 1.5 mm thick. For cooling purposes, a 0.5 mm spacing is used between each turn with an inner diameter of 60 mm and an outer diameter of 160 mm as physical constraints: Can the required inductance be achieved?

Solution

First calculate the parameters shown in figure 17.18b.

$$r = ¼(d_o + d_i) = ¼ \times (160 + 60) = 55 \text{ mm}$$

$$b = ¼(d_o - d_i) = ¼ \times (160 - 60) = 25 \text{ mm}$$

$$\ell = 40 \text{ mm}$$

$$N = \frac{b}{t_{Cu} + t_{air}} = \frac{50}{1.5 + 0.5} = 25 \text{turns}$$

Substitution of the appropriate parameters into equation (17.86) yields L = 51.6 μH.

♣

Example 17.9: ***Multi-layer air core inductor***

An air core inductor is to have the same dimensions as the inductor in example 17.8. The same conductor area (40 mm × 1.5 mm) but circular in cross-section and number of turns is to be used. Calculate the inductance. If a ferrite cylindrical core 42 mm long and 60 mm in diameter with a relative permeability of 25 is inserted, what will the inductance increase to?

Solution

From example 17.8

r = 55 mm $\qquad$ ℓ = 40 mm

b = 50mm $\qquad$ N = 25

Substitution of these parameter values into equation (17.85) yields 62.5 μH.

From figure 17. 18c, ℓ/d = 40/60 = 0.66, whence $\mu_{eff} \approx 3$. That is, with a cylindrical core inserted, a three fold increase in inductance would be expected (188 μH).

The use of end-caps and an outer magnetic sleeve would increase inductance, but importantly also help to contain the stray magnetic field.

♣

17.9 Appendix: Copper wire design data

Nominal wire diameter d	Outer diameter enamelled grade 2	Approximate dc resistance at 20°C	Bare copper weight	Fusing current
mm	mm	Ω/m	gm/m	A
0.1	0.129	2.195	0.070	2.5
0.2	0.245	0.5488	0.279	7
0.376	0.462	0.136	1.117	18
0.5	0.569	8.781×10^{-2}	1.746	27.5
0.6	0.674	6.098×10^{-2}	2.50	36
0.8	0.885	3.430×10^{-2}	4.469	57
0.95	1.041	2.432×10^{-2}	6.301	79
1	1.093	2.195×10^{-2}	6.982	82
1.5	1.608	9.67×10^{-3}	15.71	145
2	2.120	5.44×10^{-3}	27.93	225
2.5	2.631	3.48×10^{-3}	43.64	310
3	3.142	2.42×10^{-3}	62.84	>
4	4.160	1.36×10^{-3}	111.7	>
4.5	4.668	1.08×10^{-3}	141.4	>
5.0	5.177	8.70×10^{-4}	174.6	>

17.10 Appendix: Minimisation of stray inductance

In many circuit layouts, it is essential to minimise stray and residual inductance. With high *di*/*dt* currents during switching, large voltages occur ($v = L\ di/dt$) which may impress excessive stresses on devices and components. Stray inductance within a package reduces its usable voltage rating. Stray inductance in the drain circuit of the MOSFET, within the package as shown in figure 4.17, reduces the usable voltage rail while source inductance increases the transient gate voltage. In the case of capacitors, residual inductance reduces the effectiveness of turn-off snubbers and can result in an unintentional resonant circuit.

Inductance of a straight wire of length ℓ and radius r is

$$L = \frac{\mu_o \ell}{2\pi}\left(\ell n\frac{2\ell}{r} - \tfrac{3}{4}\right) \quad \text{(H)} \qquad (17.87)$$

which as a rule of thumb is about 1μH/m.

17.10.1 Reduction in wiring residual inductance

Wiring inductance can be decreased by cancelling magnetic fields in a number of ways

- coaxial cable
- parallel plates
- parallel wiring conductors.

In each case, the go and return paths are made parallel and physically close. Figure 17.21 shows the per unit length inductance for each wiring method.

coaxial cable

Minimum inductance results with coaxial cable, which is available for power application. The per unit inductance and capacitance are given by

$$L = \frac{\mu_o \mu_r}{2\pi}\ell n\frac{r_o}{r_i} \quad \text{(H/m)}$$
$$C = 2\pi\varepsilon_o\varepsilon_r / \ell n\frac{r_o}{r_i} \quad \text{(F/m)} \qquad (17.88)$$

where r_i is the inner radius and r_o the outer radius.

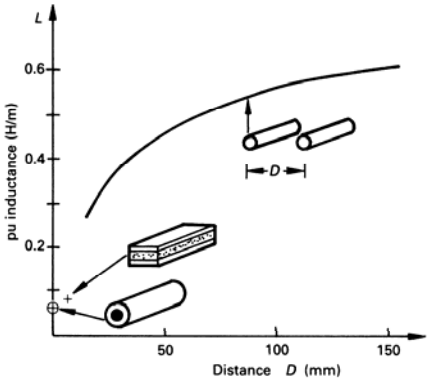


Figure 17.21. *Inductance of go and return wiring conductors.*

parallel plates

Very low inductance can be achieved by using parallel conducting copper plates separated by a thin insulation layer. The inductance per unit length, neglecting skin effects, is approximated by

$$L = \mu_o \frac{d}{w} \quad \text{(H/m)} \qquad (17.89)$$

where d is the separation of the plates and
w is the plate width.

The parallel plate capacitance is

$$C = \varepsilon_o\varepsilon_r\, w/d \quad \text{(F/m)} \qquad (17.90)$$

A complete analysis of the laminated parallel bus bar configuration is presented in appendix 17.11

parallel wiring conductors

For parallel wiring cylindrical conductors of radius r and separation D, in air,

$$C = \frac{2\pi\varepsilon_o}{\ell n\left(\frac{D}{r}\right)} \quad \text{(F/m)}$$
$$L = \frac{\mu_o}{\pi}\ell n\left(\frac{D}{r}\right) \quad \text{(H/m)} \qquad (17.91)$$

When the separation is small over a long distance, ℓ, that is $D/\ell \ll 1$, the capacitance, inductance, and mutual coupling inductance are

$$C = \frac{\pi\varepsilon_o}{\cosh^{-1}\left(\frac{D}{2r}\right)} \quad \text{(F/m)}$$
$$L = \frac{\mu_o \ell}{\pi}\left\{\ell n\left(\frac{D}{r}\right) - \frac{D}{\ell} + \tfrac{1}{4}\right\} \quad \text{(H)} \qquad (17.92)$$
$$M = \frac{\mu_o \ell}{2\pi}\left\{\ell n\left(\frac{D}{r}\right) - \frac{D}{\ell} - 1\right\} \quad \text{(H)}$$

parallel wiring conductors over a conducting ground plane

The self inductance and mutual inductance between two conductors height h over a ground plane carrying the return current are given by

$$L = \frac{\mu_o}{2\pi}\ell n\frac{2h}{r} \quad \text{(H/m)}$$
$$M = \frac{\mu_o}{4\pi}\ell n\left(1 + \left(\frac{h}{r}\right)^2\right) \quad \text{(H/m)} \qquad (17.93)$$

Figure 17.21 shows that go and return power cable residual inductance decreases as separation decreases. Physical and mechanical constraints may dictate which wiring technique is most viable. All other wiring should cross perpendicularly, in order to minimise coupling effects.

Inductance of other conductor profiles

The self-inductance of a rectangular conductor, not associated with a return path in close proximity is

$$L = \frac{\mu_o}{2\pi}\left[\ell n\left(\frac{2\ell}{w+t}\right) + \tfrac{1}{2} + \frac{2}{9}\frac{w+t}{\ell}\right] \quad \text{(H/m)} \qquad (17.94)$$

When the bus bar and its return path are side-by-side in the same plane

$$L = \frac{\mu_o}{2\pi}\left[\ell n\left(\frac{D}{w+t}\right) + \frac{3}{2}\right] \quad \text{(H/m)} \qquad (17.95)$$

or long cylindrical wire and its return path are side-by-side in the same plane

$$L = \frac{\mu_{wire}}{8\pi} + \frac{\mu}{2\pi}\ell n\frac{D}{r} \quad \text{(H/m)} \qquad (17.96)$$

where w is the width of the conductors
t is the thickness of the conductors
D is the distance between the midpoints of the conductors
ℓ is the conductor length.

The first component in equation (17.96) is the internal self-inductance component, which for copper and aluminium, $\mu_{wire} = \mu_o$, gives 50nH per metre.

17.10.2 Reduction in component residual inductance

17.10.2i - Capacitors

The inductance of a cylindrical capacitor winding, employing extended foils and scooping connections is given by

$$L = \frac{\mu_o}{2\pi}\left[\ell n\frac{2b}{r} - \tfrac{3}{4}\right] \quad \text{(H)} \qquad (17.97)$$

where b is the length of the cylinder winding and $2r$ is its diameter. This equation shows that inductance is decreased by decreasing the length and by increasing the diameter.

17.10.2ii - Capacitors - parallel connected

Capacitors are extensively parallel connected, by manufacturers before potting, or by the user after potting, in order to increase capacitance. The low inductance feature of an extended foil, scoop connected capacitor can be obliterated by poor lead connection. Consider the parallel-connected capacitors shown in figure 17.22a, which shows the

relative residual wiring inductance for three connections. Minimum inductance results when using a thin, double-sided copper printed circuit board arrangement, such that connections alternated between the top and bottom copper layers (go and return conductors). Cutouts in the pcb, for the capacitors to fit into, only marginally decrease the inductance.

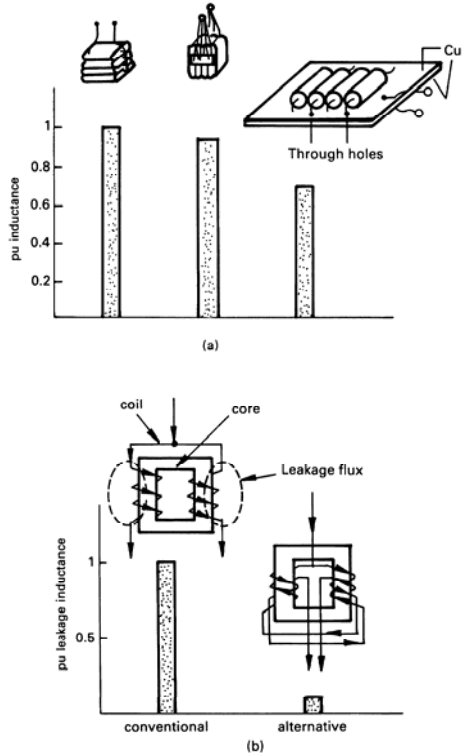


Figure 17.22. *(a) Parallel connected capacitors, inductance and (b) leakage inductance of a current balancing transformer.*

***17.10.2iii* -** Transformers

A current balancing transformer may be used to equalise the principal currents of two parallel-connected power devices, as shown in figure 10.8. Conventionally each coil is wound on separate legs of the core, resulting in a large leakage inductance. This large leakage inductance can result in high voltage transients, which are to be avoided.
Leakage can be significantly decreased if two coils are bifilar wound on each limb and connected as shown in figure 17.22b. The same leakage flux cancelling technique can be used on the centre-tapped, push-pull transformer for the switch mode power supply shown in figure 15.8. Because of the close proximity of bifilar wound conductors, high interwinding capacitance and high dielectric fields may be experienced.

17.11 Appendix: *Laminated bus bar design*

As shown in figure 17.21, the use of a parallel laminated bus bar arrangement shown in figure 17.23a for go and return paths, results in a low inductance loop. If the gap between the bus bars is laminated with a dielectric material, distributed capacitance properties are gained.
A laminated bus bar arrangement offers the following features:

- high packing density
- better conductor cooling because of flat surface area
- low voltage drop
- high voltage and current capability
- reliable and eliminates wiring errors
- space saving
- increased capacitance for better noise suppression
- low inductance because thin parallel conductors allow flux cancellation

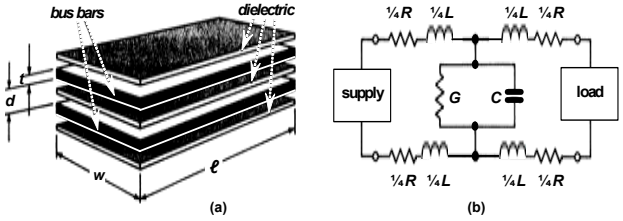


Figure 17.23. *Laminated bus bar:*
(a) Parallel planar construction and (b) equivalent circuit distributed components.

The physical bus bar dimensions are related to the electrical parameters and characteristics. The two level bus bar comprises two parallel conducting plates of aluminium, brass or copper with resistivity σ, separated by a dielectric, with dielectric constant ε_r, and permeability μ_o, giving a conductance G, capacitance C, and resistance R which are uniformly distributed along the bus, as shown in figure 17.23b.

Capacitance, C
The capacitance C is given by

$$C = \varepsilon_o \varepsilon_r \frac{w}{d} \qquad \text{(F/m)} \tag{17.98}$$

where w is the width of the conductors
d is the distance between the bars, which is the dielectric thickness.
An increase in capacitance decreases the characteristic impedance, $Z_o = \sqrt{L/C}$. A lower impedance gives greater effective signal suppression and noise elimination. This is achieved with

- a smaller bar separation, d,
- a higher permittivity dielectric material, ε_r,
- wider conductors, w.

Shunt conductance, G
The shunt conductance G depends on the quality of the dielectric, specifically its conductivity at the operating frequency.

$$G = \frac{1}{\sigma}\frac{w}{d} \qquad \text{(℧/m)} \tag{17.99}$$

Skin effect
Both the resistance and inductance are affected by the ac skin effect, which is frequency dependant. This was briefly treated in section 17.3.4ii, and specifically equation (17.36). The skin effect is when at high frequencies the current tends to flow on the surface of the conductor. The skin depth δ, from equation (17.36)

$$\delta(f) = \sqrt{\rho / \mu_o \pi f} \tag{17.100}$$

where ρ is the resistivity of the conductor at frequency f.
The skin depth for copper and brass are

$$\delta_{Cu} = \frac{0.066}{\sqrt{f}} \quad \text{(m)} \qquad \delta_{Brass} = \frac{0.126}{\sqrt{f}} \quad \text{(m)} \tag{17.101}$$

As the frequency increases L decreases and R increases.

Inductance, L

There two inductive components,

- L_{int} - inside the conductor due to internal flux linkages,
- L_{ext} - external inductance between the two conductors due to the orientation of the two conductor carrying current.

In power applications and at the associated frequencies, the external inductance is more dominant.

$$L_{ext} = \mu_o \frac{d}{w} \quad \text{(H/m)} \tag{17.102}$$

At high frequency (taking the skin effect into account) the effective inductance is

$$L_e = \mu_o \frac{d+\delta}{w} \quad \text{(H/m)} \tag{17.103}$$

Thus to decreased inductance

- decrease the dielectric thickness, d
- increase the conductor width, w
- decrease the skin depth δ by using a conductor of lower resistivity.

Resistance, R

The dc resistance R_{dc} of the two conductors is

$$R_{dc}(20°\text{C}) = 2\rho \frac{1}{wt} \quad (\Omega/\text{m}) \tag{17.104}$$

where t is the thickness of the conductors

The resistivity of copper and brass at 20°C are 1.7×10^{-8} and 7.0×10^{-8} Ωm, respectively.

The temperature effects on resistance for copper are accounted for by

$$R_{T_o} = R_{20°C}\left(1 + 0.0043\times(T_o - 20°C)\right) \quad (\Omega) \tag{17.105}$$

At high frequency, taking the skin effect into account, assuming that the conductor thickness is at least twice the skin depth,

$$R_{ac} = 2\rho \frac{2}{\delta w} \quad (\Omega/\text{m}) \tag{17.106}$$

Characteristic impedance, Z

The characteristic impedance Z of the go-and return bus bar arrangement is given by

$$Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (\Omega) \tag{17.107}$$

when the conductor resistance R and insulation conductance G are negligible

$$Z = \sqrt{\frac{L}{C}} \quad (\Omega) \tag{17.108}$$

This equation illustrates that increasing the capacitance and decreasing the inductance reduces bus bar noise problems. Common to decreased inductance and increased

capacitance are

- decrease the dielectric thickness d and
- increase the bus bar width w

That is, characteristic impedance Z is proportional to d/w.

Figure 17.24 compares the electrical parameters obtained for one metre of twist pair plastic coated 1mm diameter solid copper wire and one metre of laminated bus bar. The copper cross section area is the same in each case, giving a dc resistance of 44mΩ per metre. The most significant electrical factor is the reduction in inductance when a bus bar arrangement is used. Better electrical parameters are gained for a significant cost increase.

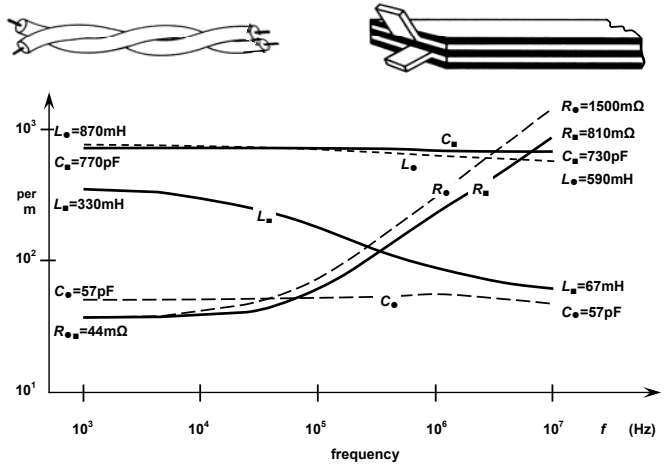


Figure 17.24. *Comparison between electrical parameters for a twisted pair and a laminated bus bar, each with the same copper cross sectional area, that is, the same dc resistance.*

Reading list

McLyman, W. T., *Transformer and Inductor Design Handbook*,
Marcel Dekker Inc., 1978.

Snelling, E. C., *Soft Ferrites*,
CRC Press, Cleveland, Ohio, 1969.

Manufacturers Data Handbooks and Catalogues

Siemens	Thomson CSF	Philips
SEI	Telmag	Neosid
Magnetics Inc	Krystinel Corp	Stackpole
Ferroxcube Inc	Arnold Eng. Co.	Micrometals Co.
Pyroferric Inc	Fuji	

Problems

17.1. Rework example 17.7, taking $B_r = 0.18$ T into account.

17.2. Rework example 17.7, when the core temperature is 100°C.

17.3. Rework example 17.3 when

$V_e = 7.3 \times 10^{-6}$ m^3 $\quad A_e = 66$ mm^2

$\ell_e = 110$ mm $\quad c = 0.75$ nH

What are the effects of decreasing the core volume for a given L and I?
[10A: 274 J/m^3, 0.53 mm, 1200 A/m, 13 turns; 20A: 2360 A/m, $\mu_e = 185$]

17.4. Show that the maximum flux density for a square-wave-excited transformer is given by

$$\hat{B} = \frac{V}{4NAf}$$

17.5. A 2:1 step-down transformer with an effective area of 10 cm^2 is driven from a 240 V, 1 kHz square-wave source. The transformer has 240 primary turns and magnetising inductance of 10 mH.

i. Calculate the maximum flux density.

ii. Calculate the peak primary current when the secondary is loaded with a 5 Ω resistor. Sketch the primary and secondary current waveforms.
[0.25 T, 30 A]

18

Resistors

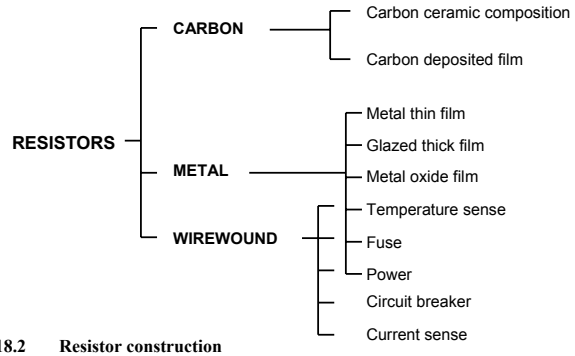
Power resistors (≥1W) are used extensively in power electronic circuits, either as a pure dissipative element, or to provide a current limiting path for charging/discharging currents. These energy transfer paths may be either inductive or non-inductive. Resistors are used for the following non-inductive resistance applications.

Series *R-C* circuit for diode, mosfet and thyristor snubbers	(6.1.2, 8.1, 8.3)
Series turn-on *L-R-D* snubbers	(6.1.2, 8.3.3)
R-C-D turn-off snubbers for GTO thyristors	
- inductance in *R* is allowable	(8.2)
Static voltage sharing for series connected capacitors and semiconductors	(10.1.1)
Static current sharing for parallel connected semiconductors	(10.1.2)
Resistor divider for proportional voltage sensing	(10.2.3)
Current sensing	(10.2.3)
Damping, clamping, and voltage dropping circuits	

The resistive element specification can be more than just fulfilling resistance and power dissipation requirements. For example, a current shunt resistor should be non-inductive in order to give good high frequency performance. Conversely, the resistor of the *R-C-D* turn-off snubber considered in 8.3 can be inductive thereby reducing the high initial peak current associated with an *R-C* discharge. An important resistor requirement is working voltage and the dielectric withstand voltage. High voltages (>200 V) are common in power circuits and the physical construction of a resistor places a limit to allowable voltage stress levels. Certain applications within the realm of power electronics may necessitate a power resistor with a low temperature coefficient of resistance (or even a negative temperature coefficient), a high operating temperature, a high pulse power ability or even a low thermoelectric voltage. Any one of these constraints would restrict the type of resistor applicable.

18.1 Resistor types

The tree below illustrates the main types of resistors used in electrical power applications. The three main resistor types are carbon film, metal film and wire wound. The main electrical and thermal properties of each resistor type are summarised in table 18.1. Typical values for power resistors are shown, which may vary significantly with physical size and resistance value.



18.2 Resistor construction

Almost all types of power resistors (≥1W) have a cylindrical high purity ceramic core, either rod or tube as shown in figure 18.1. The core has a high thermal conductivity, is impervious to moisture penetration, is chemically inert, and is capable of withstanding thermal shock. The resistive element is either a carbon film, a homogeneous metal-based film or a wound wire element around the ceramic body. For high accuracy and reliability, a computer-controlled helical groove is cut into the film types in order to trim the required ohmic resistance.

The terminations are usually nickel-plated steel, or occasionally brass, force fitted to each end of the cylindrical former in order to provide excellent electrical contact between the resistive layer and the end-cap. Tinned connecting wires of electrolytic copper or copper-clad iron are welded to the end-caps, thereby completing the terminations.

All fixed resistance resistor bodies are coated with a protective moisture-resistant, high dielectric field strength, and some times conformal coating, such that the wire terminations remain clear and clean.

The resistors are either colour coded by colour bands or provided with an identification stamp of alphanumeric data.

Table 18.1. The main characteristics of electrical power resistors

			carbon composition	carbon deposited film	metal thin film	glazed thick film		metal oxide film	power wire wound	fusible	circuit breaker	temperature sense	current sense
						LV	*HV*						
Resistance range	R	Ω	10-22M	1-10M	1-5M	1-2M	300k-1G	15-100k	1-1.5M	0.1-3.9k	0.27-82k	0.1-300	0.01 - 10
Watts @ 70°C	P_R	W	1	2	2.5	2	90	7	>300	2	6	2	9
Maximum temperature	T_h	°C	150	125	300	175	100	235	275	160	150	200	250
Working voltage	V_m	V	500	500	500	1k	100k	650	2.5k	160	500	700	$\sqrt{PR}$
Voltage coefficient	φ	10^{-6}/V	200	50	5	10	-	0.1	<1	-	-	-	-
Residual capacitance	C_R	pF	¼	½	-	-	$\frac{1}{5}$	½	-	-	-	-	-
Temperature coefficient	α	10^{-6}/K	-500 -1000	+50 -350	±350	±200	±150	±500	50	500	-80 +500	-3000 +5500	100
Thermal resistance	R_θ	K/W	80	27	90	35	13	26	0.3	50	14	0.55	20
Reliability	λ	10^{-9}/hr fit	1	10	1		-	3	300	-	-	-	-
Stability $\frac{\Delta R}{R}$%	@ P_R, T_a = 70°C, @10^3 hours		5	3	5	½	2	3	3	5	2 @ 150°C	0.1	3

18.2.1 Film resistor construction

Figure 18.la shows a sectional view of a typical film resistor having a construction as previously described. The resistive film element is produced in one of four ways:

- cracked carbon film
- glaze of glass powder mixed with metals and metal compounds fired at 1000°C, giving a firmly bonded glass-like film on the core
- precisely controlled thin film of metal alloy (Cr/Ni or Au/Pt) evaporated, baked or vacuum sputtered on to the inert core and of thickness between 10^{-8}m and 10^{-7}m
- metal oxide ($Sn0_2$) resistive film deposited or sintered on to the core.

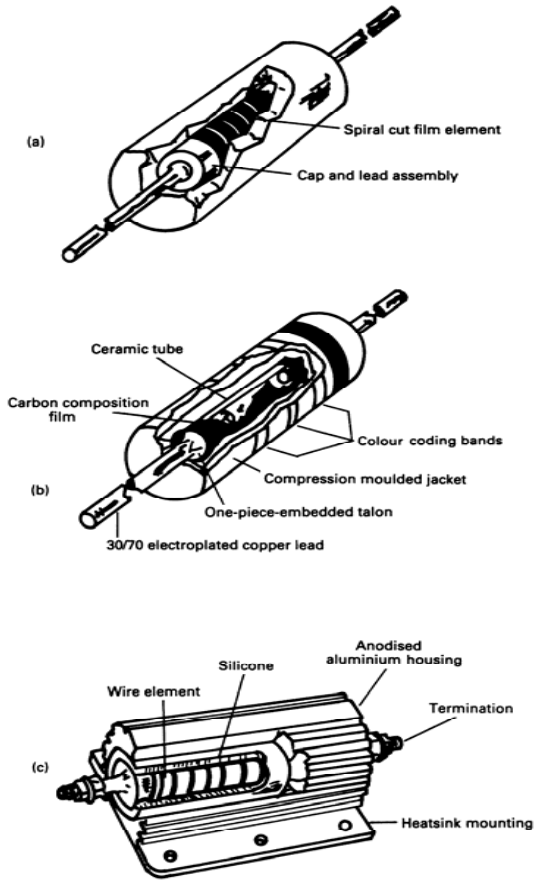


Figure 18.1. *Power resistor construction: (a) metal glaze, thick film; (b) moulded carbon composition film; and (c) wire wound aluminium clad.*

The film materials exhibits a wide range of resistivity, ρ, which extends from 40×10^{-6} Ω cm for gold/platinum to in excess of 10^2 Ω cm for layers of thick film mixture. The thinnest possible film, for maximum resistance, is limited by the need for a cohesive conductive film on the ceramic substrate while the thickest film, for minimum resistance, is associated with the problem of adhesion of the resistance film to the substrate.
The helical groove shown in figure 18.la, used to trim resistance, is shown clearly and is either laser or diamond cut. The residual inductance is significantly increased because of the formed winding which is a spiral around the core. Below 100 Ω, a helical groove may not be used.
Resistive materials such as polymer and ruthenium oxide are used for high voltage and high resistance resistors up to 100 kV, 1 GΩ and 20 kV, 150 GΩ respectively.

18.2.2 Carbon composition film resistor construction

A sectional view of a moulded carbon composition film resistor is shown in figure 18.lb. The resistive carbon film is cured at 500°C and is unspiralled, and hence non-inductive with excellent high frequency characteristics. The resistance value is obtained by variation of film composition and thickness, which may be between 0.01 μm and 30 μm. A component with a wide nominal value tolerance results since the film is not helically trimmed.
A special formed one-piece talon lead assembly is deeply imbedded into the substrate for good uniform heat dissipation. These terminations are capless.
The following example illustrates typical parameters and dimensions for carbon film resistors.

Example 18.1: ***Carbon film resistor***

A 470 Ω resistor is constructed from a film of carbon with a resistivity 3.5×10^{-5} Ω m, deposited on a non-conducting ceramic bar 3 mm diameter and 6 mm long.
Calculate the thickness of film required, ignoring end connection effects.

Solution

Let thickness of the film be t metre, then
cross-sectional area $\approx \pi \times 3 \times 10^{-3} \times t$ (m^2)

Now $R = \rho\ell$/area, that is
$470\Omega = 3.5\times10^{5}\times6\times10^{3}/\pi\times3\times10^{3}\times t$

$t = 0.0474$ μm

♣

18.2.3 Wire-wound resistor construction

The sectional view of an aluminium-housed power wire-wound resistor, shown in figure 18.1c can dissipate up to 300 W with a suitable heatsink in air or up to 900 W when water-cooled.
The former is a high purity, high thermal conductivity ceramic, of either Steatite or Alumina tube, depending on size. The matching resistive element is iron-free, 80/20 nickel-chromium for high resistance values or copper-nickel alloy for low resistance. These alloys result in a wire or tape which has a high tensile strength and low temperature coefficient. The tape or wire is evenly wound on to the tube former with an even tension throughout. This construction is inductive but gives a resistor which can withstand repeated heat cycling without damage.
The assembled and wound rod is encapsulated in a high temperature thermal conducting silicone moulding material and then cladded in an extruded, hard, anodised aluminium housing, ensuring electrical stability and reliability.
Alternatives to the aluminium-clad resistor are to encapsulate the wound rod in a vitreous enamel or a fire-proof ceramic housing.
Power wire-wound resistors with a low temperature coefficient, of less than $\pm20\times10^{-6}$ /K, use a resistive element made of Constantan (Nickel and Copper) or Nichrome (Nickel and Chromium). Constantan is used for lower resistance, up to several kilo-ohm, while Nichrome is applicable up to several hundred kilo-ohm. The resistance ranges depend on the ceramic core dimensions, hence power rating. The element is wound under negligible mechanical tension, resulting in a reliable, low temperature coefficient resistor which at rated power can safely attain surface temperatures of over 350°C in a 70°C ambient. Because these resistors can be used at high temperatures, the thermally generated emf developed at the interface between the resistive element and the copper termination can be significant, particularly in the case of Constantan which produces -40 μV/K. Nichrome has a coefficient of only + 1 μV/K.
Ayrton-Perry wound wire elements can be used for low inductance applications. The resistive element is effectively wound back on itself, such that the current direction in parallel conductors oppose. Either a bifilar winding or an opposing chamber winding is used. The net effect is that a minimal magnetic field is created, hence residual inductance is low. The maximum resistance is one-quarter that for a standard winding, while the limiting element voltage is reduced, by dividing by √2. The low inductance winding method is ineffective below 4.7 Ω. This winding style also lowers the maximum permissible winding temperature, called *hot spot temperature*, T_h. The hot spot temperature is the resistor surface temperature at the centre of its length.

18.3 Electrical properties

An electrical equivalent circuit for a wirewound resistor is shown in figure 18.2. The ideal resistor is denoted by the rated resistance, R_R, and the lumped residual capacitance and residual inductance are denoted by C_r and L_r respectively. A film type

resistor is better modelled with the capacitance in parallel with the resistive component. The terminal resistance of a homogeneous element of length ℓ and area A is given by

$$R(v,f,T) = \rho(v,f,T)\frac{\ell}{A} = \frac{\ell}{\sigma A} \qquad (\Omega) \tag{18.1}$$

where ρ is the resistivity of the resistive element and σ is the conductivity (= $1/\rho$). The terminal resistance is a function of temperature, voltage, and frequency. Temperature dependence is due to the temperature dependence of resistivity α, typical values of which are shown in table 18.1. The temperature coefficient may vary with either or both temperature, as with carbon and metal film resistors, or resistance, as with thick film and noble metal film resistors. A reference for measurement is usually 25°C. Frequency dependence is due to a number of factors, depending on the type of resistive element and its resistance value. Typical factors are due to skin effects in the case of wire-wound resistors or residual capacitance in film types. Frequency dependent resistance, R_{ac}, for carbon composition film and metal glaze thick film resistors, is shown in figure 18.3.

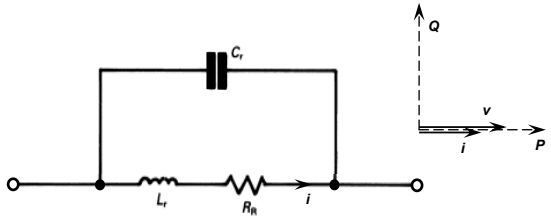


Figure 18.2. *Equivalent model of a resistor.*

A voltage dependence factor, which is called ϕ, is given in table 18.1 and is resistive element type dependent. For operation at low frequencies, resistance is given by

$$R(v,T) = R(0,25°\text{C})(1+\phi v)(1+\alpha T) \qquad (\Omega) \tag{18.2}$$

Values for non-linearity coefficients ϕ and α are given in table 18.1.
Electrically, the terminal voltage and current are related by Ohm's law, namely

$$v = i \times R \qquad (\text{V}) \tag{18.3}$$

where it is assumed that R is constant. This electrical relationship is shown in the phase diagram in figure 18.2. In practice when a pure sinusoidal current is passed through a resistor its terminal voltage may not be a pure sinusoid, and may contain harmonic components. This voltage distortion is termed nonlinearity and is the harmonic deviation in the behaviour of a fixed resistor from Ohm's law, equation (18.3). Another resistor imperfection is *current noise* which is produced by fluctuation of conductivity in the resistive element. The noise is proportional to current flow. Wire-wound resistors

generate negligible current noise. The resistance value itself can change: *long term drift* due to chemical-physical processes such as oxidation, recrystallisation corrosion, electrolysis, and diffusion, as may be appropriate to the particular resistive element.
The power dissipated, P_d, in an ideal resistor, is specified by

$$P_d = vi = i^2R = v^2/R \qquad (\text{W}) \tag{18.4}$$

where the power dissipated is limited by the power rating, P_R, of the resistor. In turn, the power limit also sets the maximum voltage that can be withstood safely.

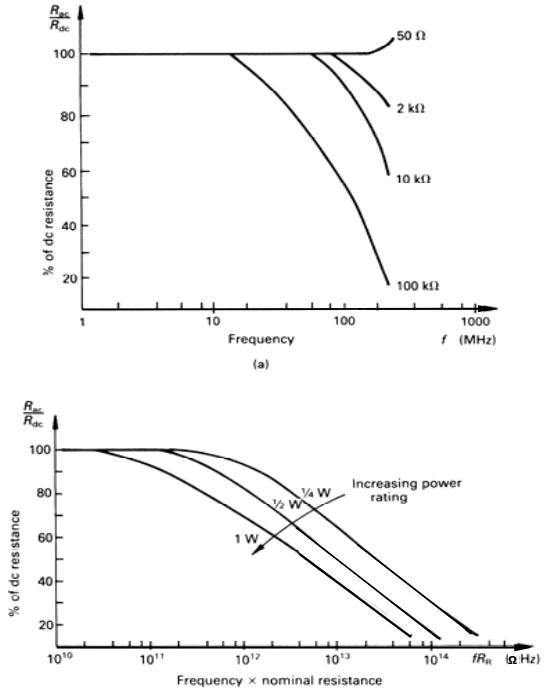


Figure 18.3. *Resistor high frequency characteristics: (a) of a metal glaze thick film 3 W resistor and (b) moulded carbon composition film resistors.*

18.3.1 Maximum working voltage

The maximum working voltage $\hat{V}$, either dc or ac rms, is the limiting element voltage that may be continuously applied to a resistor without flashover, subject to the maximum power rating P_R not being exceeded. A typical characteristic is shown in figure 18.4, which illustrates the allowable voltage bounds for a 10 W resistor range, having a limiting flashover voltage of 300 V rms.
At lower resistance, power dissipation capability limits the allowable element voltage, and above a certain resistance level, termed critical resistance, R_c, the maximum working voltage, $\hat{V}$, is the constraint. Maximum working voltage decreases with decreased air pressure, typically a 30 per cent reduction for low pressures.

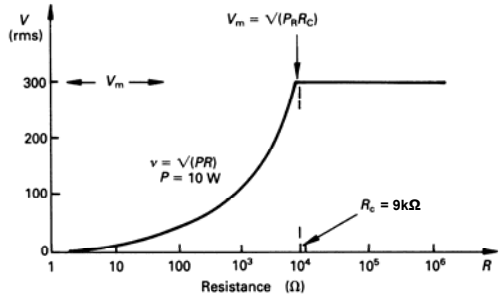


Figure 18.4. *Resistor voltage limits for a given power rating.*

18.3.2 Residual capacitance and residual inductance

Generally all resistors have residual inductance and shunt capacitance. Inductance increases with both resistance and power rating as shown by figure 18.5, while residual capacitance increases mainly with increased pulse rating. For example, a 2 W metal oxide film resistor (typical of film resistors) has ½ pF residual capacitance and inductance varying from 16 nH to 200 nH. A ¼ W family member has 0.13 pF of capacitance and 3 to 9 nH of inductance.
Film resistors, with resistance above 1 kΩ, having a helical grove, tend to be dominated by interspiral capacitance effects at frequencies above 10 MHz, as seen in figure 18.3a.
Non-inductive elements have low shunt capacitance, such as in the case of carbon composition, while wire-wound resistors can have microhenries of inductance. For

example from figure 18.5, a 25 W, 47 Ω, wire-wound resistor may have 6 μH of inductance. Residual inductance increases with resistance and decreases with frequency.

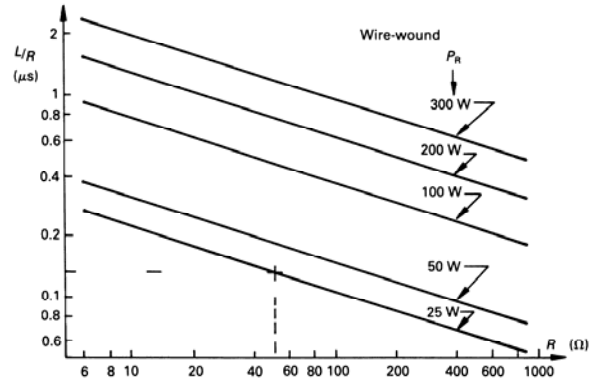


Figure 18.5. *Resistor time constant versus resistance and power rating.*

18.4 Thermal properties

The continuous power rating of a resistor, P_R, is based on three factors:

- Maximum surface temperature, in free air, over the usable ambient temperature range, typically from -55°C to well over 100°C.
- Stability of resistance when subjected to a dc cyclic load. Typical power dissipation is limited to give 5 per cent resistance change for 2000 hours continuous operation in a 70°C ambient air temperature.
- Proximity of other heat sources and the flow of cooling air.

The temperature rise of a resistor due to power dissipation is determined by the laws of conduction, convection, and radiation (see Chapter5). The maximum body temperature, the hot spot temperature, occurs on the surface - at the middle of the resistor length. As previously considered, any temperature rise will cause a change in resistance, depending on a temperature coefficient; examples are given in table 18.1.
Within the nominal operating temperature range of a resistor, the hot spot temperature, T_h, is given by (equation 5.10)

$$T_h = T_a + R_{\theta_{h-a}} P_d \qquad \text{(K)} \tag{18.5}$$

The hot spot temperature is limited thus as the ambient temperature, T_a, increases the allowable power dissipated decreases, as shown in figure 18.6a for four different elements. These curves show that:

- No power can be dissipated when the ambient temperature reaches the hot spot temperature.
- No derating is necessary below 70°C.
- Some resistors, usually those with higher power ratings, can dissipate higher power at temperatures below 70°C.

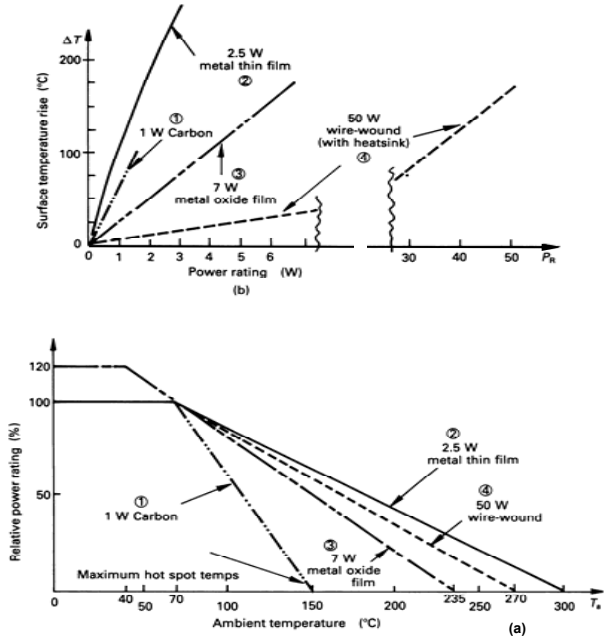


Figure 18.6. *Power resistor thermal properties: (a) power derating with increased temperature and (b) surface temperature increase with increased power dissipation.*

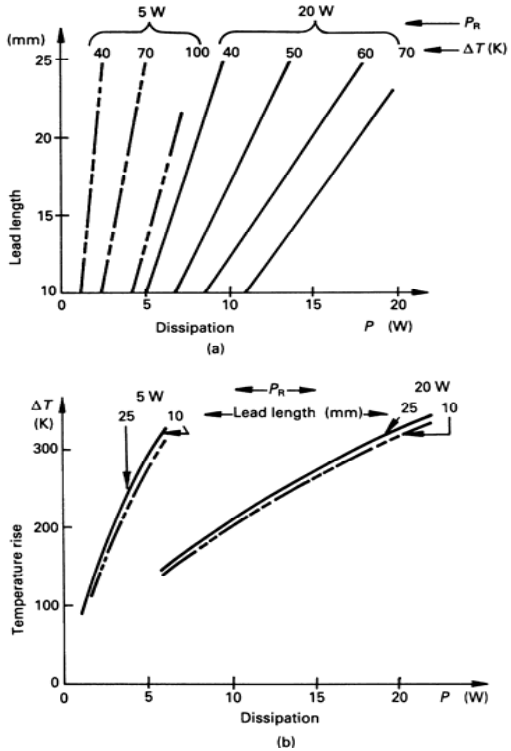


Figure 18.7. *Wire-wound 5 W and 20 W resistor dissipation as a function of: (a) lead length and temperature rise at the end of the lead (soldering spot) and (b) temperature rise of the resistor body, for two lead lengths.*

Figure 18.6b shows the resistor surface temperature rise above ambient, nominally 20°C, at different levels of power dissipation. The lead lengths can significantly affect the thermal dissipation properties of resistors and an increase in lead length

- decreases the end of the lead, or soldering spot temperature
- increases the body temperature.

These characteristics are shown for 5 W and 20 W 'cemented' wire-wound resistors in figure 18.7. Figure 18.7a shows how the soldering spot temperature is affected by lead length. Figure 18.7b, on the other hand, is based on the assumption that the soldering spot is represented by an infinite heatsink. Therefore the shorter the lead length, the lower the body temperature for a given power dissipation. It is important to limit the solder pad temperature in order to ensure the solder does not melt.

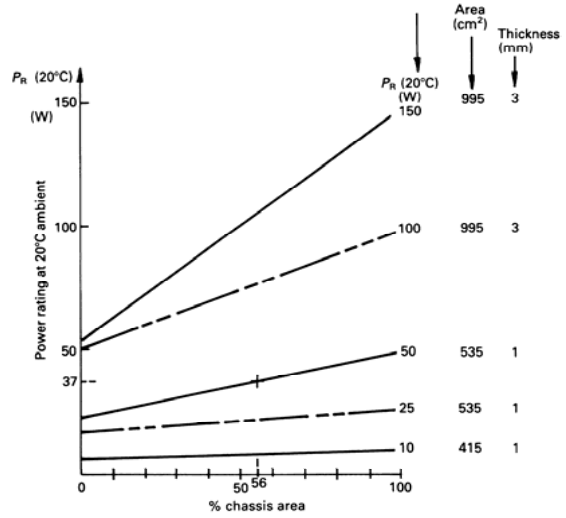


Figure 18.8. *Power dissipation of resistors mounted on a smaller heat sink than specified, right.*

18.4.1 Resistors with heatsinking

Aluminium clad resistors suitable for heatsink mounting, as shown in figure 18.1c, are derated with any decrease in the heatsink area from that at which the element is rated. Figure 18.8 shows the derating necessary for a range of heatsink-mounted resistors. For

a given heatsink area, further derating is necessary as the ambient temperature increases. Figure 18.6a, curve 4, describes the ambient temperature related power derating of the aluminium-clad resistors on the rated heatsink, characterised in figure 18.8. Figure 18.6a, curve 4, can be used to derate these resistors when operating in an ambient other than 20°C, with the rated heatsink area shown in figure 18.8. The same percentage derating is applicable to a heatsink area smaller than the nominal area.

Example 18.2: ***Derating of a resistor with a heatsink***

What power can be dissipated by an aluminium-clad, wire-wound resistor, rated nominally at 50 W, in an ambient of 120°C with a heatsink reduced to 300 cm^2 and 1 mm thick?

Solution

The heatsink area has been reduced to 56 per cent, from 535 to 300 cm^2, hence from figure 18.8 the power rating below 70°C is reduced to 37.5 W.
From figure 18.6a, curve 4, at 120°C ambient, derating to 75 per cent of the relevant power rating is necessary. That is, 75 per cent of 37.5 W, 28.1 W, can be dissipated at an ambient of 120°C and with a heatsink area of 300 cm^2.

♣

18.4.2 Short time or overloading ratings

Resistors with power ratings greater than a watt are designed to handle short-term overloads, either continuously for minutes, or repetitively in short bursts of a few seconds. Figure 18.9 can be used to determine allowable short-duration, repetitive pulses. It can be seen that high, short-duration power pulses of a few seconds can be handled if the repetition rate is low. As the pulse duration increases, the overload capability reduces rapidly, with minimal overload allowable with power pulses over a few minutes in duration.
For power pulses of less than 100 ms, the power is absorbed by the thermal capacity of the resistive element and little heat is lost to the surroundings. The temperature rise ΔT of the resistive element in this adiabatic condition is given by (equation 5.2)

$$\Delta T = \frac{W}{mc} \quad \text{(K)} \tag{18.6}$$

where c is the specific heat capacity of the resistive element (J/kg/K)
W is the energy in the pulse of time t_p, (J)
m is the mass of the resistive element (kg).

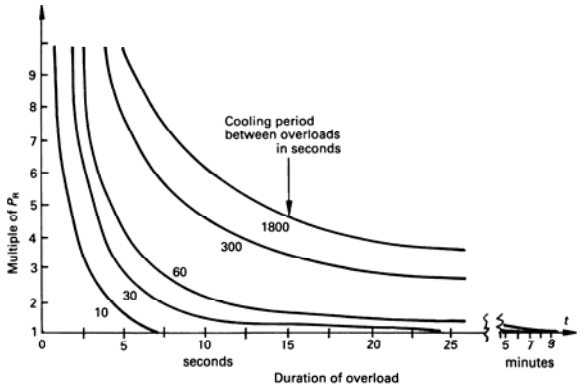


Figure 18.9. *Permissible short time overload ratings for heavy-duty tape wound power resistors.*

Example 18.3: ***Non-repetitive pulse rating***

A 100 A rms, sine pulse with a period of 50 ms is conducted by a wire-wound resistor, constructed of 1 mm^2 cross-section *Ni-Cr* alloy (Nichrome).
Calculate the temperature rise. Assume for *Ni-Cr*

resistivity	$\rho = 1 \times 10^{-6}\ \Omega$ m
specific heat	$c = 500$ J/kg/K
density	$\gamma = 8000$ kg/m^3

Solution

The mass m of the element of length ℓ and area A is given by

$$m = \gamma \ell A \qquad \text{(kg)}$$

Resistance R of the wire is given by

$$R = \rho \frac{\ell}{A} \qquad (\Omega)$$

The pulse energy is given by

$$W = \int_o^{t_p} i^2 R\, dt = \int_o^{50\text{ms}} \left(\sqrt{2} \times 100 \sin(\omega t)\right)^2 R\, dt$$
$$= 500R \qquad \text{(J)}$$

Substitution for R yields

$$W = 500 \times \rho \frac{\ell}{A} \qquad \text{(J)}$$

The temperature rise ΔT from equation (18.6) is given by

$$\Delta T = \frac{W}{mc} = 500 \times \frac{\rho \ell}{A} \times \frac{1}{c} \times \frac{1}{\gamma \ell A}$$
$$= \frac{500\rho}{\gamma c A^2} = \frac{500 \times 1 \times 10^{-6}}{8000 \times 500 \times 1 \times 10^{-12}}$$
$$= 125\text{K}$$

♣

18.5 Repetitive pulsed power resistor behaviour

A resistor may be used in an application where the power pulse experienced at a repetition rate of kilohertz is well beyond its power rating, yet the average power dissipated may be within the rated power. The allowable square power pulse $\hat{P}$, of duration t_p and repetition time T, can be determined from figure 18.10a, which is typical for power film resistors, at a 70°C ambient. Within these bounds, any resistance change will be within the limits allowable at the continuous power rating. The pulse duration t_p, restricts the maximum allowable pulse voltage $\hat{V}$, impressed across a film resistor, as shown in figure 18.10b.

Example 18.4: ***Pulsed power resistor design***

A 1 kΩ-10 nF, *R-C* snubber is used across a MOSFET which applies 340 V dc across a load at a switching frequency of 250 Hz. Determine the power resistor requirements.

Solution

The average power dissipated in the resistor is:

$$\overline{P} = CV^2 f = (10 \times 10^{-9}) \times 340^2 \times 250 = 0.29\text{ W}$$

Figure 18.10 is applicable to a 2.5 W metal film resistor, when subjected to rectangular power pulses. The peak power $\hat{P}$ occurs at switching at the beginning of an *R-C* charging or discharging cycle.

$$\hat{P} = V_i^2 / R = (340\text{V})^2/1000\Omega = 116\text{ W}$$

where V_i, 340 V, is the maximum voltage experienced across the resistor. The 2.5W element has a power rating greater than the average to be dissipated, 0.29W. Assuming exponential pulses, then

$$t_p = ½\tau = ½CR = ½ \times 10 \times 10^{-9} \times 10^3 = 5\mu\text{s}$$

The average pulse repetition time, T, is 2 ms, therefore $T/t_p = 400$. From Figure 18.10, the peak allowable power is 150 W while the limiting voltage is 500 V. Both the experienced voltage, 340 V, and power, 116 W, are below the allowable limits. The proposed 2.5 W, 1 kΩ, metal thin film power resistor is suitable.
Furthermore from figure 18.6, curves 2, with an average power dissipation of 0.29 W, that is 11.6 per cent of P_R, the maximum allowable ambient temperature is 213°C, while the hot spot temperature is 40°C above ambient for an ambient below 70°C. In terms of average power dissipated, this resistive element is lightly stressed. On the other hand, the transient stress is relatively high.

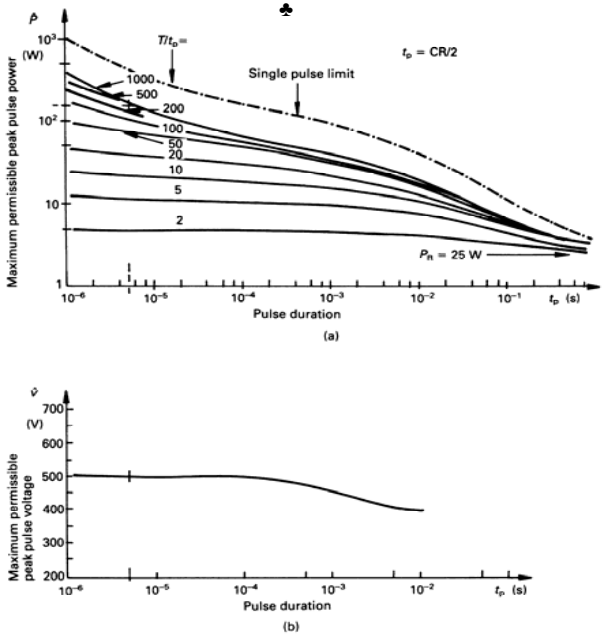


Figure 18.10. *Pulsed capabilities of a power metal film resistor, 2.5 W: (a) maximum permissible peak pulse power versus pulse duration and (b) maximum permissible peak pulse voltage versus pulse duration.*

18.5.1 Empirical pulse power

An empirical formula for the maximum pulse power may be given in the case of a metal film resistor. Typically, for a 1 W @ 70°C, 700 V rated, 60 K/W, metal film resistor

$$\hat{P} \leq \sqrt{\frac{15}{t_p}} \quad \text{(W)} \tag{18.7}$$

where 1 μs ≤ t_p ≤ 100 ms, such that the average dissipation is less than the rated dissipation.
Using t_p = 5 μs from example 18.2 in equation (18.7) indicates that this 1 W resistor is suitable for the application considered in example 18.4. In fact a ⅓W, 600 V rated resistor can fulfil the snubber function when using a quoted $\hat{P} = \sqrt{5/t_p}$.

18.6 Stability and endurance

The resistance stability of a resistor is dependent on power dissipation, ambient temperature, and resistance value. An endurance test gives the worst-case variation in resistance value or stability. It is the percentage resistance change at rated power and hot spot temperature after a specified time. An endurance specification is of the form:

> 1000 hours at recommended maximum dissipation P_R, which will limit the hot spot temperature to 375°C: ΔR better than 5 per cent of R

The time, percentage change in R, and temperature are varied with resistor type and size.
At power levels below rated dissipation, better stability than that for the endurance test is attainable, for the same duration. The stability period can be extended by the following empirical formula

$$\left|\frac{\Delta R}{R}\right|_t \approx X^{\log\frac{t}{t_1}} \times \left|\frac{\Delta R}{R}\right|_{t_1} \tag{18.8}$$

which is valid for $10^{-3} \leq t \leq 10^5$ hours. The base χ depends on the resistor type and is between 1.1 and 5.
Performance monograms as shown in figure 18.11 are provided to enable a given resistor to be used at dissipation levels which will result in the stability required for that application. The first quadrant in figure 18.11 satisfies the thermal equation (18.5), while the third quadrant satisfies equation (18.7), with χ = 3.17. The following example illustrates many of the features of the stability performance monogram of figure 18.11.

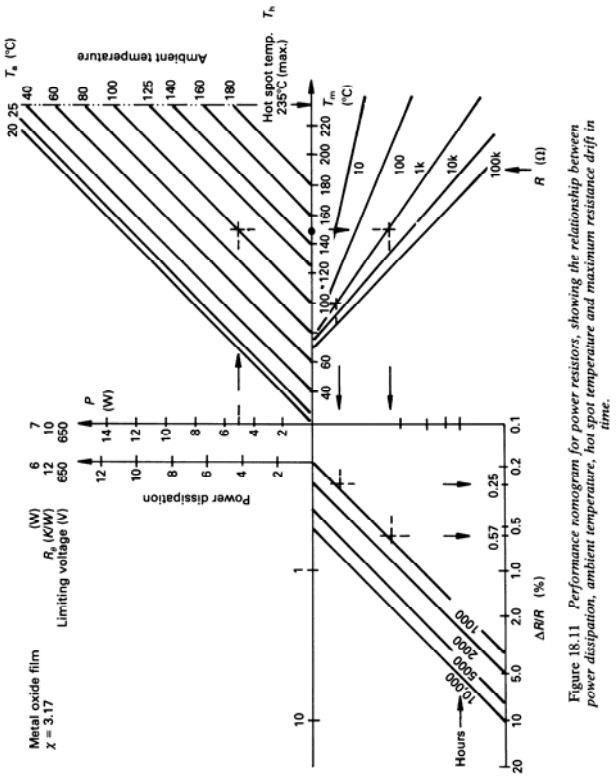


Figure 18.11 *Performance nomogram for power resistors, showing the relationship between power dissipation, ambient temperature, hot spot temperature and maximum resistance drift in time.*

Example 18.5: ***Power resistor stability***

A 1 kΩ, 7 W, power metal oxide film resistor dissipates 5 W. If the maximum ambient is 100°C, use the monograph in figure 18.11 to find

i. the stability at 100°C while in circuit for 1000 hours but in a standby mode, that is, $P = 0$ W
ii. the hot spot temperature when dissipating 5 W
iii. the maximum expected resistance drift after 10^3 and 10^5 hours.

Solution

i. The resistance change given from the monogram for $P = 0$W at a 100°C ambient is indicative of the shelf-life stability of the resistor when stored in an 100°C ambient.
The stability is determined by performing the following operations. Find the intersection of $P = 0$ and the diagonal for $T_a = 100$°C. Then project perpendicularly to the 1 kΩ diagonal. The intersection is projected horizontally to the 1000 hour diagonal. This intersection is projected perpendicularly to the stability axis.
For example, from projections on figure 18.11, after 1000 hours, in a 100°C ambient, a 0.25 per cent change is predicted. For the 1 kΩ resistor there is a 95 per cent probability that after 1000 hours the actual change will be less than 2.5 Ω.
ii. The 5 W load line is shown in figure 18.11. A hot spot temperature, T_m, of 150°C is predicted (100°C + 5 W × 10°C/W).
iii. With a 1 kΩ resistor after 1000 hours, a $\Delta R/R$ of 0.57 per cent is predicted, as shown on figure 18.11. There is a 95 per cent probability that the actual change will be less than 5.7 Ω.
The monogram does not show stability lines beyond 10,000 hours. Equation (18.8), with $\chi = 3.17$, can be used to predict stability at 100,000 hours

$$\left.\frac{\Delta R}{R}\right|_{10^5} \approx 3.17^{\log\frac{10^5}{10^3}} \times 0.57\% = 18.25\%$$

After 100,000 hours, it is 95 per cent probable that the actual resistance change of the 1 kΩ resistor will be less than 182.5 Ω.

18.7 Special function power resistors

Film and wire-wound resistors are available which have properties allowing them to perform the following functions

- fusing
- circuit breaking
- temperature sensing
- current sensing.

18.7.1 Fusible resistors

Resistors up to 2 W are available which fuse when subjected to an overload current. The resistive element fused is generally metal alloy film, although only wire-wound elements are suitable at low resistance levels. The power load and interruption time characteristic shown in figure 18.12a shows that rated power can be dissipated indefinitely, while as the power increases significantly above the rated dissipation, the interruption time decreases rapidly. Interruption generally means that the nominal resistance has increased at least 10 times. Irreversible resistance changes can be caused by overloads which raise the change in hot spot temperature beyond 150°C, for the elements illustrated by figure 18.12b. The nature of the resistive element makes it unsuitable for repetitive power pulse applications.
Typical fusible resistors are summarised in table 18.2.

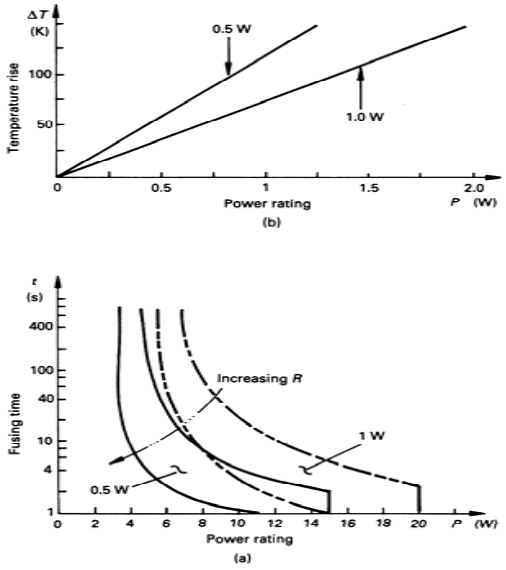


Figure 18.12. *Fusible resistor characteristics:*
(a) time to interruption (10 x R_R as a function of overload power and
(b) temperature rise above ambient as a function of power dissipated.

Table 18.2: Fusible resistor characteristics

parameter		condition	units	Metal alloy film	Wire wound
Power	P_R	@ 70°C	W	0.25 - 4.5	1 - 2
Resistance range	R		Ω	0.22 - 10k	0.1 - 1k
Tolerance			%	2	5
Temperature coefficient (resistance dependent)	α	x 10^{-6}	/K	± 500	-400 to + 1000
Stability		@ P_R T_a=70°C 1000 hours	%	2	10
Working voltage	V_m		V	$\sqrt{P_R R}$	$\sqrt{P_R R}$

18.7.2 Circuit breaker resistors

The construction of two types of wire-wound circuit breaker resistors is shown in figure 18.13. Under overload conditions the solder joint melts, producing an open circuit. After fusing, the solder joint can be resoldered with normal 60/40, Sn/Pb solder.
The joint melts at a specified temperature, and to ensure reliable operation the solder joint should not normally exceed 150°C. This allowable temperature rise is shown in figure 18.14a, while the circuit breaking time and load characteristics for both constructions are shown in figure 18.14b. This characteristic is similar to that of fusible resistors. A typical power range is 1 to 6 W at 70°C, with a resistance range of 75 mΩ to 82 kΩ and temperature coefficient of -80 to +500 × 10^{-6}/K depending on the resistance values. The maximum continuous rms working voltage tends to be limited by the power, P_R, according to $\sqrt{P_R R}$.

18.7.3 Temperature-sensing resistors

The temperature dependence of a resistive element can be exploited to measure temperature indirectly. Unlike normal resistors, temperature-sensing resistors require a large temperature coefficient to increase resistance variation with temperature.
Both metal film and wire-wound temperature sensing elements are available with a temperature coefficient of over +5000 × 10^{-6}/K with 1 per cent linearity over the typical operating range of -55°C to 175°C. The high temperature sensitivity gives a 57 per cent increase in resistance between 25°C and 125°C.

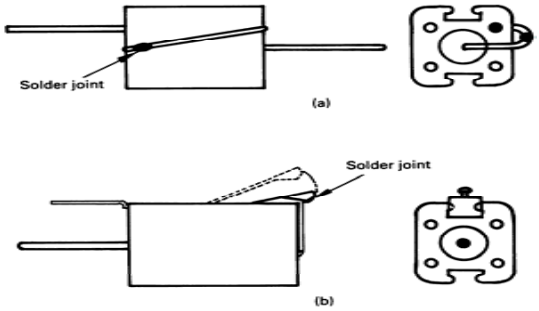


Figure 18.13. *Two circuit breaker resistors construction: (a) type 1 and (b) type 2.*

The low power elements, up to ¼W @ 70°C, tend to be metal oxide, with a typical resistance range at 25°C of 10 Ω to 10 kΩ. A conformal encapsulation is used to minimise thermal resistance, hence ensuring an extremely fast response. For example, a 1/20 W temperature sensing resistor can have a thermal time constant to a step temperature, in still air, of 3.7 s. This time constant increases to 31 s for a ¼ W rated resistor.

At powers commencing at 1 W, wire-wound elements are employed which utilise positive temperature coefficient alloy resistance wire. The nominal resistance range is lower than the film types; typically from 0.1 Ω to 300 Ω at 25°C. Response is slower than film types, and can be improved if oil immersed.

Glazed thick film temperature sensing resistors can be used to provide a negative temperature coefficient, -3000 × 10^{-6}/K at 25°C. Power is limited to ¼ W with a dissipation constant of up to 8.1 mW/K at 25°C in still air. Low thermal time constants of only 2.9 s are possible with 1/20 W elements. The allowable working voltage for all types is power limited.

18.7.4 Current-sense resistors

The resistive element consists of a flat metal band, with spot-welded terminals, and a ceramic encapsulation. The flat-band construction results in a non-inductive resistor of both high stability and overload capacity. Low current third and fourth terminal voltage sensing leads may be incorporated; alternatively a mΩ/cm correction factor for lead length is given.

Power ratings of up to 20 W at 70°C and 20 A maximum, with a resistance range of 10

mΩ to 10 Ω are available. At these low resistance levels, the maximum continuous working voltage is power limited. The resistance temperature coefficient is typical of a wire-wound resistor, 100 to 600 × 10^{-6}/K depending on the resistance level.

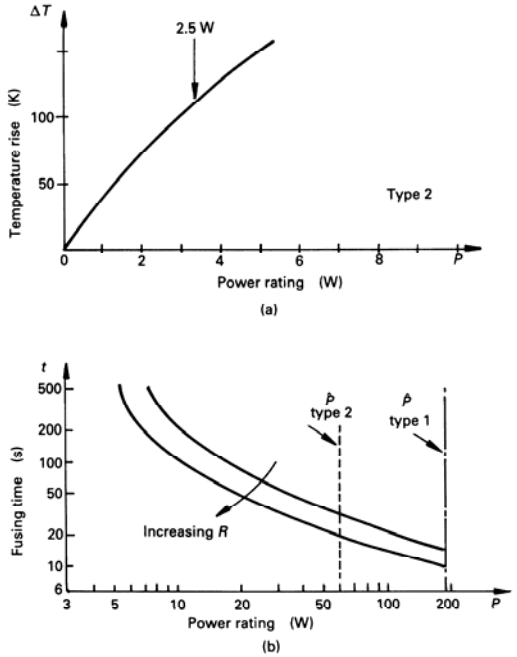


Figure 18.14. *Circuit breaker characteristics: (a) solder joint temperature rise versus power dissipated for resistor type 2 and (b) fusing times versus load for resistor types 1 and 2.*

Reading list

Philips, Book 3, Part 1c, Fixed Resistors, 1985.

Philips, Book 3, Part 1f, Varistors, Thermistors and Sensors, 1986.

Siemens, Components, 1986.

Siemens, NCT Thermistors, Data Book, 1986/87.

Problems

18.1. The resistance of a temperature dependent negative temperature coefficient resistor is given by

$$R(T) = Ae^{\frac{B}{T}}$$

where B = 3300 K and R = 10 Ω at 25°C. The resistive element has a thermal resistance to ambient of 45.5 K/W. Assume the maximum resistor temperature is 1000°C and absolute zero is -273°C.

(1) Calculate the temperature coefficient at 25°C.
[-0.037 or -3.7 per cent/K]

(2) When the non-linear resistor is dissipating power, what is the maximum attainable terminal voltage? At what temperature and current does this voltage occur at? Assume the ambient temperature is 25°C.
[58.3°C, 3.29 Ω, 0.73 W, 1.55 V, 0.47A]

(3) The non-linear resistance dependence on temperature can be 'linearised' by the parallel connection of a resistor. The resultant characteristic has an inflexion point, which is set at the mid-point of the required temperature operating range. Calculate the required parallel connected resistor if the mid-temperature point of operation is 58.3°C.
[2.2 Ω, 1 W]

(4) What series resistor must be added such that the maximum voltage condition occurs at 5 V across the series plus parallel combination?
[3.45 Ω, 6 W]

18.2. Derive a series of general formulae for the parts of problem 18.1.

$$\left[\alpha = -B/T^2; \hat{T} = \tfrac{1}{2}B\left(1 - \sqrt{1 - 4T_a/B}\right); R_p = R_{T_m}\left(\frac{B - 2T_m}{B + 2T_m}\right)\right]$$

18.3. Resistors coming off the production line are selected according to value and allocated to one of 12 bins for each decade.
Find the nominal centre value for each bin to give a range with equal ratios, and compare with the 'E12' series (1, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2, 10).
Find the maximum percentage difference between the nominal value and the E12 value.
Show that the 12-step series corresponds to a ±10 per cent tolerance for practical resistors.
[4.5 per cent between 3.16 and 3.3]

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